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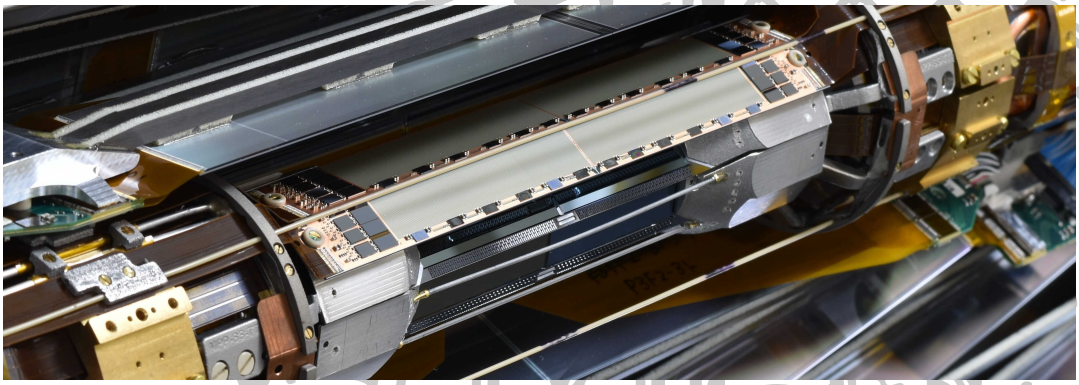

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Titelbild: Belle II Pixel Vertex Detector während der Hochzeit mit dem Silicon Vertex Detector im Oktober 2018 (Foto: Koji Hara)

Abstract

The Belle II particle physics experiment is located at the SuperKEKB e^+e^- collider in Japan. Its research focuses on the CP violation in B meson decays and addresses many open questions in electroweak interactions. The broad physics program also includes the search for new physics beyond the Standard Model of particle physics.

An essential component of the Belle II detector for the physics mentioned above, most importantly for analyses of CP violation, is the Pixel Vertex Detector (PXD). The PXD is the innermost tracking device, surrounding the beam pipe, and provides a precise measurement of the decay vertices of B mesons and other weakly decaying particles. The PXD consists of two layers of silicon semiconductor modules with new Depleted P-channel Field Effect Transistor (DEPFET) pixels, used for the first time in a high energy physics experiment. This technology allows for an exceptionally thin active detector design of only 75 µm, achieving 15 µm impact parameter resolution and greater than 99 % detection efficiency.

The PXD is an electronic device and must function properly as a subdetector of the larger Belle II electronic detector system. The first part of this thesis was the conduct of a test campaign to verify the electromagnetic compatibility (EMC) of the PXD module design. These were the first EMC measurements for a high energy physics pixel detector and also the first consideration of radiated noise from the beam pipe.

After the design and prototyping phase, the module production for the final detector was started. The second part of this thesis was the development of the entire chain of test procedures and a comprehensive quality management including quality assurance software for the characterization and optimization of all production modules. The performance of 75 PXD modules was evaluated, of which 72 % achieved the highest grading after optimization.

The third part of this thesis covers the assembly and commissioning of a first reduced version of the PXD at the Belle II experiment in Japan. Optimization of the module performance and operating software continued during operation. Following the occurrence of severe irradiation damage due to beam loss events, an automated

detection algorithm was developed. Possible damage mechanisms were investigated and additional protection measures were implemented.

The installed PXD successfully operated in the first physics data taking period of the Belle II experiment from 2019 to 2022. It reliably collected data of particular value for lifetime measurements and time-dependent CP violation analyses. During the shutdown period in 2022/23 the first PXD was replaced by PXD2, a complete successor, which will be the innermost tracking detector of Belle II for many years to come.

Zusammenfassung

Das Teilchenphysikexperiment Belle II befindet sich am SuperKEKB e^+e^- Beschleuniger in Japan. Sein Forschungsschwerpunkt liegt in der Untersuchung der CP Verletzung im Zerfall von B Mesonen. Darüber hinaus behandelt es viele offene Fragen zur elektroschwachen Wechselwirkung. Das breite Physikprogramm umfasst auch die Suche nach neuer Physik jenseits des Standardmodells der Teilchenphysik.

Eine wesentliche Komponente des Belle II Teilchendetektors für das genannte Physikprogramm, insbesondere für die Analysen zur CP Verletzung, ist der Pixel Vertex Detektor (PXD). Der PXD ist der innerste Detektor für die Spurrekonstruktion. Er umschließt das Strahlrohr und liefert präzise Messungen der Zerfallsvertices von B Mesonen und anderen schwach zerfallenden Teilchen. Der PXD besteht aus zwei Lagen von Silizium-Halbleitermodulen mit neuartigen deplitierten p-Kanal-Feldeffekttransistor (DEPFET) Pixeln, die zum ersten Mal in einem Experiment der Hochenergiephysik eingesetzt werden. Diese Technologie ermöglicht ein außergewöhnlich dünnes aktives Detektordesign von nur 75 µm, wobei eine intrinsische Positionsauflösung von 15 µm und eine Detektionseffizienz von über 99 % erreicht werden.

Der PXD ist ein elektronisches Gerät und muss als Teil des größeren elektronischen Detektorsystems Belle II funktionieren. Der erste Teil der vorliegenden Arbeit bestand in der Durchführung einer Messkampagne zur Überprüfung der elektromagnetischen Verträglichkeit (EMV) des PXD Moduldesigns. Dies waren die ersten EMV Messungen an einem Pixeldetektor der Hochenergiephysik und die erste Berücksichtigung von Störungen, die von einem Strahlrohr abgestrahlt werden.

Nach der Design- und Prototypenphase lief die Produktion der Module für den finalen Detektor an. Der zweite Teil dieser Arbeit bestand in der Entwicklung einer vollständigen Kette von Testverfahren und eines umfassenden Qualitätsmanagements einschließlich der Qualitätssicherungssoftware für die Charakterisierung und Optimierung aller produzierten Module. Die Leistung von 75 PXD Modulen wurde evaluiert, von denen nach der Optimierung 72 % die höchste Einstufung erreichten.

Der dritte Teil dieser Arbeit befasst sich mit dem Zusammenbau und der Inbetriebnahme einer ersten reduzierten Version des PXD am Belle II Experiment in Japan. Die Optimierung der Modulleistung und der Betriebssoftware wurde während des Be-

triebs fortgesetzt. Nach dem Auftreten gravierender Bestrahlungsschäden aufgrund von Strahlverlusten wurde ein automatischer Algorithmus zur Erkennung dieser Schäden entwickelt. Mögliche Schadensmechanismen wurden untersucht und zusätzliche Schutzmaßnahmen eingeführt.

Der installierte PXD konnte in der ersten Phase der Datennahme des Belle II Experiments von 2019 bis 2022 erfolgreich betrieben werden. Er nahm zuverlässig Daten auf, die für Lebensdauermessungen und Analysen zur zeitabhängigen CP Verletzung von besonderem Wert sind. Während der Abschaltung des Beschleunigers 2022/23 wurde der erste PXD durch PXD2 ersetzt, einen vollständigen Nachfolger, der für viele kommende Jahre der innerste Detektor für die Spurrekonstruktion des Belle II Experiments sein wird.

Contents

1. Introduction

> *Λεύκιππος δὲ καὶ ὁ ἑταῖρος αὐτοῦ Δημόκριτος στοιχεῖα μὲν τὸ πλῆρες καὶ τὸ κενὸν εἶναί φασι, [...] αἴτια δὲ τῶν ὄντων ταῦτα ὡς ὕλην.*
>
> *Leucippus and his pupil Democritus say the elements are the full and the empty, [...] these build, as matter, the causes of the being things.*
>
> — Aristoteles [1]

Particle physics ultimately addresses nothing less than the old, fundamental question of humanity about being and existence. By describing the structure of our universe, disclosing the laws it follows, and not least comprehend its genesis, we try to answer the question: *"How is our universe built?"*. In this attempt natural sciences refrain from the question about the meaning and leave this elaboration in the competences of other disciplines like philosophy and theology. The separation between description and interpretation of reality was one of the great achievements of the ancient Greek natural philosophers already almost 2 500 years ago. They raised empirical evidence and causality in the explanation of natural phenomena above traditional concepts, which required moody divine creatures, and thus succeeded in a demystification of the physical world.

Already at the early stage of our modern civilization, ancient Greek and ancient Indian natural philosophers were able to formulate a theory about the fundamental structure of our universe, which still pictures our current understanding surprisingly well. We have the written record about Leucippus and Democritus, who concluded only by the power of logical thinking and in debate with like-minded fellows that the unlimited universe (πᾶν ἄπειρόν) is composed by two components: matter, which they called the full (τὸ πλῆρες), and space, which they called the empty (τὸ κενὸν). They postulated that there must be a bottom of the scale, where the elementary constituents of matter are indivisible (ἄτομα). This idea immediately also demands the existence of an empty space, a void, which allows the particles to move and to rearrange; necessities to explain motion, genesis and transience. Remarkable is the fact, that nowadays the unification of the theory of matter (standard model of particle physics) and the theory of the space-time-continuum (general relativity) is still one of the big open questions of modern physics.

The ancient atomists assumed that the macroscopic properties of perceptible objects

are not defined by properties of the elementary building blocks of matter but rather emerge from the combination and arrangement of those. It was therefore not necessary to assume an unlimited number of different elementary particles to explain the apparent infinite number of different perceptible objects, just like "a tragedy and a comedy emerge from the same letters" [2] as Democritus phrased it.

After a long break of almost 2 000 years, these ideas were picked up again when the advancing knowledge about chemical processes started to shape our modern view on elements and atoms. At the beginning of the 19th century, the works of Lavoisier and Dalton culminated in the formulation of the law of multiple proportions, which quantitatively described the fixed ratios in chemical reactions. Another experimental hint to the existence of smallest particles was the observation of Brownian motion in 1827. Consequently, Boltzmann, Clausius and Maxwell were able to develop a kinetic theory of gases which explained the macroscopic properties of gases with the motion of small elastic particles. Subsequently, Mayer and Mendeleev succeeded in sorting the elements, which were known at that time, into the symmetric arrangement of a periodic table of the elements and at the same time predicting yet undiscovered elements.

At the beginning of the 20th century, the substructure of atoms was revealed when Rutherford observed in scattering experiments that the mass of an atom is not distributed equally over its volume but rather centered in a small heavy nucleus which is orbited by much lighter electrons. Just before these progresses, new insights about the structure of light were found by Planck who solved the problem of black-body radiation by postulating a quatization of energy. Building on this result, Einstein's explanation of the photoelectric effect finally paved the way to settle the argument if light was to be interpreted as wave or as particle: The wave-particle duality grants it both characteristics at the same time so that the actual appearance depends on the circumstances of observation.

Physicists like de Broglie, Bohr, and Sommerfeld further developed a quantum theory which was then mathematically formulated by Schrödinger and Heisenberg as quantum mechanics. The new theory described the motion of negatively charged electrons around positively charged protons in the nuclei of atoms by wave functions and delivered correct results for the observed discrete energy levels of these electrons. It also correctly required that a neutron is likewise an elementary particle and not just a bound state of an electron and a proton. This was confirmed in 1932 by Chadwick, who discovered the free neutron as "unusually" penetrating particle with about the same mass as the proton in scattering experiments.

At that time, the three most important elementary particles which account for the vast majority of known matter have been found: the electron, the proton and the neutron. All other particles we know today either exist only for a very short time (like muons,

pions, kaons, etc.), react immediately with matter (like positrons or antiprotons) or interact so weakly that they are very hard to detect (like neutrinos). These other particles may only make up for a small fraction of our current visible universe but they played an important role during its genesis and development. In fact, they grant us a view into the very first moments of the existence of our universe. Physicists first observed those new particles in cosmic rays and later also directly produced them in collision experiments to analyze their properties.

The increasing variety of new particles discovered during the 20th century was called the "particle zoo", before the formulation of the Standard Model of particle physics brought a new order into the observations. It turned out, yet again, that many of these particles can be described as being composed of still smaller constituents, the quarks. Today, the Standard Model of particle physics knows 17 fundamental types of particles. Whether we reached the end of the scale now, we do not know. In any case, according to Heisenberg the conclusions of another ancient Greek philosopher came true, "as the smallest units of matter are in fact not physical objects in the ordinary sense of the word; they are shapes, structures, or in terms of Platon, ideas, which can be unambiguously discussed only in the language of mathematics" [3].

The Standard Model of particle physics is the best description of nature on the microscopic scale that we have today. Its predictions are remarkably accurate and were confirmed by numerous sophisticated experiments throughout the last decades. To its large successes counts the prediction of particles which were not observed before, like the Higgs Boson, whose discovery finally completed the picture in 2012. Yet, it lacks the description of the fourth fundamental force, gravity, and it falls short to explain macroscopic, astronomic observations like dark matter and dark energy or the dominance of matter over antimatter [4]. By now, there is plenty of experimental evidence that there must be physics beyond the Standard Model. That is the reason why particle physicists continue to probe the predictions of the Standard Model in experiments on both the precision and the energy frontier.

The SuperKEKB e^+e^- collider in Japan is the most luminous particle accelerator in the world and provides an extremely high rate of collision events which are recorded by the Belle II detector system. The target instantaneous luminosity of $6 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ is about 30 times higher than for the predecessor machine KEKB. The target integrated luminosity is $50\,\mathrm{ab}^{-1}$ by the 2030s and will allow very precise measurements as well as searches for very rare decays. On this road, the SuperKEKB accelerator achieved a new luminosity record with $4.65 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ during its operation in 2022 and the integrated luminosity recorded so far by Belle II exceeded $426\,\mathrm{fb}^{-1}$. First physics results based on the new data such as lifetime measurements for D^0, D^+, Λ_c^+ and Ω_c^0 [5–7] as well as searches for dark matter candidates [8–10] are already available. Currently, the experiment has just restarted after its first long shutdown

period in 2022/23, during which improvements were made to both the machine and the detectors.

The central part of the Belle II detector system is the Pixel Vertex Detector (PXD), which is an entirely new design utilizing the DEpleted P-channel Field Effect Transistor (DEPFET) technology for the first time in a high energy particle physics experiment. The PXD consists of 40 modules cylindrically arranged in two layers around the collision point of the electron and positron bunches. The monolithic, all-silicon modules are highly integrated and contain three types of Application-Specific Integrated Circuits (ASICs) for matrix control, signal digitization, performance optimization and data processing. The active area of the pixel matrix is thinned down to only 75 µm to minimize multiple scatting of the traversing particles and thereby still provides very high detection efficiency and internal amplification of the analog signals. With a total number of 7.68 million pixels, its high resolution allows the PXD to narrow down the vertex of decayed particles to about 10 µm. It therefore plays a crucial role especially in lifetime measurements and time-dependent CP violation analyses.

Within the Belle II collaboration we are striving to record the physics events provided by the SuperKEKB accelerator as efficiently as possible. The accumulated data will be a valuable asset to probe physics within and beyond the Standard Model for many years to come, as every answered question, shifting the borders of knowledge, will open multiple new and even harder ones. A dilemma already known to Democritus who put it in these words:

> ἐτεῇ δέ οὐδὲν ἴδμεν· ἐν βυθῷ γὰρ ἡ ἀλήθεια.
>
> In fact, we know nothing; for the truth lies in the abyss.
>
> Diogenes Laërtios [11]

Still, our curiosity and desire to get to the bottom of things and answer the fundamental questions is unbroken. As every attempt to come to an conclusion is always limited to the amount of initial information, in this sense, particle physics contributes with its results also to the philosophical approaches to find the answers to the questions about being and existence. As Planck phased it: “Religion and natural science [...] mutually supplement and condition each other” [12]. According to Dürr, former director of the Heisenberg institute, quantum mechanics challenged the predetermination established by the earlier physics and brought back uncertainty and chance into the description of reality [13]. In fact, no other branch of science revolutionized our view of the universe so substantially and permanently like physics repeatedly did.

This thesis emerged from the work in the Belle II group at the Max Planck Institute for Physics (MPP) and within the PXD collaboration; it is structured as follows:

Chapter 2 provides a brief review of the discovery of CP violation and its role in the search for physics beyond the standard model leading to an overview of the physics program at Belle II.

Chapter 3 gives a description of the SuperKEKB accelerator facilities and the individual Belle II detector systems.

Chapter 4 provides a closer look at the central PXD including a description of the utilized DEPFET technology.

Chapter 5 illustrates the prerequisites in hardware and software for the operation of a PXD module in the laboratory.

Chapter 6 describes a measurement campaign regarding the electromagnetic compatibility (EMC) of a PXD module. After a general introduction to EMC, the test setup is described, followed by the discussion of emission and susceptibility measurements and their results.

Chapter 7 addresses the main production of the PXD modules and the concurrent quality assurance as well as the subsequent module characterization. The standardized testing procedure and the accumulated test results are presented.

Chapter 8 describes the gluing procedure of PXD modules to ladders and the PXD mounting process.

Chapter 9 provides the experiences from the commissioning and operation of the PXD at the Belle II experiment during Phase 3 covering the operator tasks, operation parameter optimization and detector damages in particular.

Chapter 10 ends with a conclusion and an outlook to the future PXD operation.

2. Physics at Belle II

> *Das Studium und allgemein das Streben nach Wahrheit und Schönheit ist ein Gebiet, auf dem wir das ganze Leben lang Kinder bleiben dürfen.*
>
> *Study and in general the pursuit of truth and beauty is a sphere of activity in which we are permitted to remain children all our lives.*
>
> — Albert Einstein [15]

The main focus of the Belle II physics program lies on studies of CP violation in the B meson system. The endeavor "Beauty physics" profits significantly from a so called B-factory, producing exclusively pairs of B mesons at the $Y(4S)$ resonance with very high rates. The electron-positron collider SuperKEKB provides the required luminosity for the Belle II experiment. The entangled neutral B meson pairs are especially favorable as the CP violation in the decays of the b quarks is relatively large and the entanglement allows time dependent analyses.

CP violation, as postulated by Sakharov, is a required and well established feature of the Standard Model of particle physics as explained below. However, the observed order of magnitude is too small to explain the matter-antimatter asymmetry in the universe [4]. Therefore, CP violation is still a lively field for the search for new physics. The rich physics program of Belle II challenges the Standard Model predictions and provides more beyond that, such as lifetime measurements, searches for new physics in rare decays, probing the dark sector, and physics of the τ leptons.

This chapter provides an overview of the discovery of CP violation and its contribution to the formulation of the Standard Model of particle physics (following mainly [16–18]). The current state of this successful theory and many still open questions motivate the physics program at Belle II, which is outlined at the end of this chapter.

2.1. History of CP violation

The symmetries of parity inversion (P) and charge conjugation (C) played a crucial role in the formulation of the Standard Model of particle physics. Both symmetries are intrinsically interwoven into the mathematical formulation of the theory, which describes our understanding of the smallest constituents of matter and their interactions with impressive precision. It came as a surprise that one of the fundamental forces, the weak force, violated, even maximally, these symmetries. The combined CP symmetry came to the rescue, but not for long, when it was discovered, that the CP symmetry is also violated in the weak interactions, although to a much lesser extent. Today, the violation of C, P, and CP symmetry in weak interactions is incorporated into the Standard Model and helps to address open questions such as the matter-antimatter asymmetry in the universe. However, while the CP violation has been precisely determined through various measurements, its strength is not sufficient to explain the cosmic matter-antimatter asymmetry [4] and thus remains still an open area of research.

2.1.1. Symmetries in particle physics

Symmetries are a fundamental concept in mathematics and physics. Knowledge of a system's symmetries allows deduction of its properties and behaviors, and utilizing them can be an extremely powerful tool to gain insights, even when the exact description of a system is unknown [16]. Additionally, symmetries are very closely related to conservation laws in physics, as formulated by the Noether theorem [19]. For example, rotational symmetry in classical physics is related to the conservation of angular momentum.

In particle physics, angular momentum is the combination of orbital and spin angular momentum, and it is conserved as well. Furthermore, particle physics involves "internal" symmetries, such as isospin and flavor. These symmetries share the same mathematical formulation as angular momentum but are not associated with macroscopic movement. In addition, there are also "discrete" symmetries:

- **Parity inversion** describes the transformation of a system into its "mirror image" by reflecting at the origin $\vec{x} = 0$. This is equivalent to the inversion of all spacial coordinates:
$$\hat{P} : (\vec{x}, t) \mapsto (-\vec{x}, t) \tag{2.1}$$
The postulate is that physics should not differentiate between directions. A mirrored universe should behave the same as our universe. Different physical quantities transform differently under parity inversion:

type	example	transformation
scalar	time, mass	$\hat{P}(s) = s$
pseudoscalar	helicity	$\hat{P}(p) = -p$
vector (polar vector)	momentum, force	$\hat{P}(\vec{v}) = -\vec{v}$
pseudovector (axial vector)	angular momentum, spin	$\hat{P}(\vec{a}) = \vec{a}$

- **Charge conjugation** inverts all charges and thus transforms particle p into its antiparticle $\bar{p}$.

$$\hat{C} : |p\rangle \mapsto |\bar{p}\rangle \tag{2.2}$$

  It is postulated that a universe made of antimatter would behave exactly like our universe. Only particles that are their own antiparticles are eigenstates of C, such as the photon and the π^0.

- **Time reversal** inverts the sequence of events. It reverts the direction of time. Time reversal transforms a process into its reverse process.

$$\hat{T} : (\vec{x}, t) \mapsto (\vec{x}, -t) \tag{2.3}$$

  The postulate is that for each reaction its reverse process should be equally possible, maybe not as probable but still possible.

Parity, charge conjugation and time symmetry are conserved in electromagnetic and strong interactions. It was assumed to also hold for weak interactions, like the radioactive β-decay. However, this assumption was questioned after the observation of new, "strange" particles in cosmic rays from 1947 on.

2.1.2. τ - θ puzzle

An increasing number of strange particles, which could until then only be observed in cosmic rays, was produced in the first modern particle accelerators from 1952 on. These particles did not fit into the existing picture. The fact, that they were produced rather fast (by the strong force), while they decayed significantly slower (by the weak force) made them appear very strange. Gell-Mann and Nishijima assigned them a new property, which they called "strangeness" and which was conserved in strong interaction but violated in weak interactions.

The two "strange" particles τ and θ stood out in particular. Both were measured to have the same mass and lifetime as well as the same spin. However, the θ^+ decayed into two pions and the τ^+ decayed into three pions. The internal parity of the pion was known to be (-1) and therefore the two final states had opposite parity.

$$\theta^+ \to \pi^+ + \pi^0 \qquad (P = (-1)^2 = +1) \tag{2.4}$$

$$\tau^+ \to \left\{ \begin{matrix} \pi^+ + \pi^0 + \pi^0 \\ \pi^+ + \pi^+ + \pi^- \end{matrix} \right\} \quad (P = (-1)^3 = -1) \tag{2.5}$$

Parity conservation stood against the interpretation of θ^+ and τ^+ as the same particle. The puzzle was in the question, why should two different particles share so many common properties [20].

In 1956, Lee and Yang tackled this puzzle by searching the literature about parity conservation. They found references for "parity conservation in strong and electromagnetic interactions to a high degree of accuracy, but that for the weak interactions [...] parity conservation is so far only an extrapolated hypothesis unsupported by experimental evidence" [21]. Lee and Yang discussed the possibility that parity could be violated in the weak interaction to propose a solution to the τ-θ puzzle, namely that both, τ and θ, are in fact one and the same particle (now called the K meson), and that parity is not conserved in its weak decays. At the same time, they proposed several experimental tests how parity conservation in the weak interaction could be tested experimentally. One of them was carried out by Wu [22] later that year.

The task was to set up an experiment that allowed to observe, if parity is indeed violated in weak interaction. A fitting choice was to look at a system containing a combination of spin (pseudo-vector), which does not change sign under parity, and momentum (vector), which does change sign. This requirement was fulfilled by the radioactive β-decay of cobalt 60. The cobalt nucleus was known to carry a spin component of $s_z = 5$, of which the emitted electron and neutrino carry each $s_z = \frac{1}{2}$ away. Due to conservation of angular momentum, all spin components point in the same direction.

	${}^{60}_{27}\mathrm{Co}$	$\longrightarrow$	${}^{60}_{28}\mathrm{Ni}$	$+$	e^-	$+$	$\bar{\nu}_e$	$+$ 2γ
components of s_z :	5	$\longrightarrow$	4	$+$	$\frac{1}{2}$	$+$	$\frac{1}{2}$	$+$ 0

However, assuming the much heavier nucleus stays at rest, the momenta of the electron and neutron point in opposite directions. If parity was conserved in the weak interaction, both emittance directions of the electrons (parallel and antiparallel to the spin) should be equally probable (compare fig. 2.1). The count rate of electrons would be the same measured in the direction of the spin polarization and against it.

The measurement revealed that the electrons were always preferably emitted against spin polarization and thus demonstrated that the parity inverted process is disfavored. "Conservation of parity is violated" [22] in the weak interaction. This result solved the puzzle, as it allowed to interpret τ^+ and θ^+ as the same particle, today known as K^+.

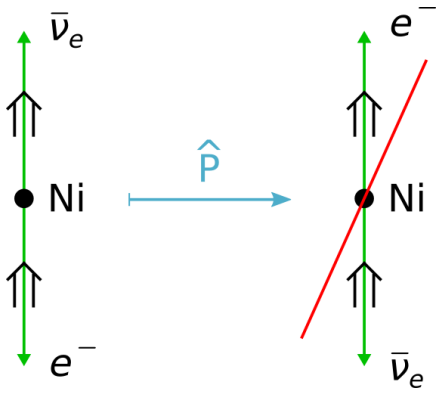


Figure 2.1.: Parity violation in beta decay. Parity inversion transforms the process in which an electron is emitted against the spin polarization into the process where it is emitted parallel to the spin polarization. The result of Wu's measurement showed that the latter process is disfavored by nature and therefore proved parity violation in the weak interaction.

These observations were confirmed by Garwin and colleagues in the same year in the decay of charged pions also reporting C violation [23]. The amount of P and C violation was not yet precisely determined, but it was clear that it was a large effect. Eventually, it was found that both are violated maximally in weak interactions giving rise to the consideration of the combined CP symmetry.

2.1.3. Combined CP symmetry

After the loss of P and C invariance in the weak interaction, the desire for symmetry in particle physics was satisfied again in 1957 by Landau who proposed the consideration of the combined CP symmetry [24]. Both symmetries are separately conserved in the electromagnetic and strong interaction and so is their combination. In the weak interaction, however, they are not conserved individually but their combination yields physically allowed processes again.

For this discussion the definition of helicity becomes helpful. The helicity h is the projection of the spin $\vec{s}$ onto the direction of linear momentum $\vec{p}$:

$$h = \frac{\vec{s} \cdot \vec{p}}{|\vec{s}| \cdot |\vec{p}|} \tag{2.6}$$

Spin is a pseudovector which does not change sign under parity inversion. However, momentum is a polar vector which does change sign. Helicity, therefore, incorporates the direction of the momentum vector and is a pseudoscalar changing sign under parity. Particles with positive helicity (spin and momentum in the same direction) are called right-handed, while particles with negative helicity (spin and momentum in opposite direction) are called left-handed. That makes helicity a good quantity to illustrate CP violation for example in the decay of charged pions: $\pi^- \to \mu^- + \bar{\nu}_\mu$ (see fig. 2.2).

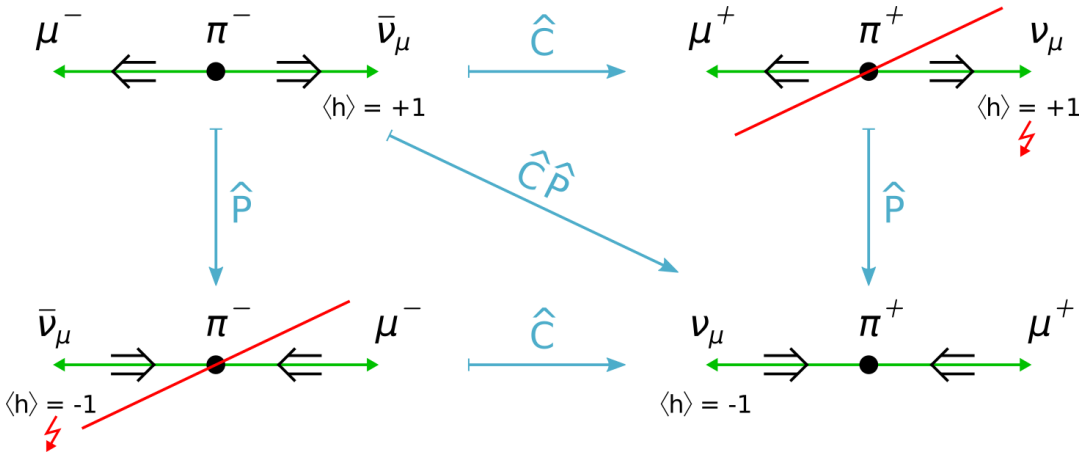


Figure 2.2.: Decay of charged pion under C, P and CP transformation. The pion in the center is in each case at rest. The green arrows indicate the direction of momentum of the decay particles, the black double arrows indicate the direction of their spin. The blue arrows indicate the corresponding symmetry conversion of the decay process.

In the observable decay of a charged pion, we consider the pion at rest so that the momentum of the emitted muon and neutrino point in opposite direction. As the pion has spin zero, the spins of the created fermions must be antiparallel. The process in the upper left results in a right-handed anti-neutrino and can be observed. The processes under C or P inversion, however, result in a right-handed neutrino or left-handed anti-neutrino, respectively, and can not be observed. When the initial process is transformed under the combined CP symmetry, we get a left-handed neutrino. This process can be observed again. The weak interaction couples only to left-handed fermions and right-handed anti-fermions[1].

[1] Note that the muon in the allowed processes has "wrong" helicity. The pion decay is therefore helicity-suppressed, which leads to a long lifetime of the pion. Due to the non-zero mass of the muon, its helicity is not exactly 1 and the process can take place. In fact, also the decay to an electron and neutrino is possible. Due to the lighter mass of the electron, more energy is available in the final state increasing the phase space which should result in a higher probablity for this decay mode. However, the lighter mass of the electron results in an even higher helicity suppression.

With his proposal of CP invariance Landau restored symmetry in the weak interaction. At the same time he already mentioned that this has consequences for other quantities, like the exclusion of an electric dipole moment for particles. After more than 60 years, this idea is still an ansatz to test CP invariance by measuring the upper limit for the electric dipole moment of e.g. the neutron [25].

The implications of CP invariance for the neutral kaon system were realized by Gell-Mann and Pais [26]. They noted that the neutral kaons K^0 and $\overline{K}^0$ can both decay to two pions. Using this channel, they can turn into each other and become their own antiparticle. This effect is called mixing:

$$K^0 \rightleftharpoons \pi^+ + \pi^- \rightleftharpoons \overline{K}^0 \tag{2.7}$$

However, neutral kaons K^0 and $\overline{K}^0$ are not CP eigenstates. CP conjugation transforms them into each other, including a minus sign as kaons are pseudoscalars and have negative parity:

$$\hat{C}\hat{P}\,|K^0\rangle = -\,|\overline{K}^0\rangle\,, \;\; \hat{C}\hat{P}\,|\overline{K}^0\rangle = -\,|K^0\rangle$$

Instead, the normalized CP eigenstates, which determine the decay mode into 2π or 3π, can be expressed as combinations of K^0 and $\overline{K}^0$. The neutral kaons must therefore be considered as a "particle mixture".

$$|K_1\rangle = \frac{1}{\sqrt{2}}(|K^0\rangle - |\overline{K}^0\rangle), \;\; |K_2\rangle = \frac{1}{\sqrt{2}}(|K^0\rangle + |\overline{K}^0\rangle) \tag{2.8}$$

with

$$\hat{C}\hat{P}\,|K_1\rangle = |K_1\rangle\,, \;\; \hat{C}\hat{P}\,|K_2\rangle = -\,|K_2\rangle \tag{2.9}$$

The final state with two pions has parity $P = +1$ and the final state with three pions has parity $P = -1$ so that

$$K_1 \to 2\pi, \;\; K_2 \to 3\pi \tag{2.10}$$

This results in two very distinct lifetimes as the rest mass of three pions is almost as large as the rest mass of a neutral kaon and therefore the phase space for the 3 pion decay is significantly smaller [16]:

$$\tau_1 = 8.95 \times 10^{-11}\,\mathrm{s}, \;\; \tau_2 = 5.11 \times 10^{-8}\,\mathrm{s} \tag{2.11}$$

Hence, K_1 and K_2 were also called K_S and K_L for "short" lived and "long" lived, respectively. This property played an important role in the discovery of CP violation.

2.1.4. CP violation in the neutral kaon system

The neutral kaon system with very distinct lifetimes of its CP eigenstates posed an ideal candidate to test, if the weak interaction strictly obeys CP symmetry. That is, if the short and long lived states are exact CP eigenstates:

$$K_S \stackrel{?}{=} K_1, \quad K_L \stackrel{?}{=} K_2 \tag{2.12}$$

In 1964, Cronin and Fitch addressed this question by producing a K^0 meson beam at the Brookhaven Alternating Gradient Synchrotron (AGS) [27]. The beam flight lengths of 17 m between production target and detector system accounted for 300 K_S decay lengths. Effectively, this resulted in a pure K_L beam as all K_S already decayed to two pions within the first meter after production. Only three pion decays were to be expected, if CP invariance holds in the weak interaction. However, Cronin and Fitch measured 45 two pion events out of 22 700 decays in total. This result showed that CP is violated in the weak interaction, although it is a very small effect. K_L is not an exact eigenstate of CP but contains a small admixture of K_1, and equivalent for K_S, with $|\epsilon| \sim 2 \times 10^{-3}$:

$$\begin{aligned} |K_L\rangle &= \frac{1}{\sqrt{1+|\epsilon|^2}} \left(|K_2\rangle + \epsilon\,|K_1\rangle\right) \\ |K_S\rangle &= \frac{1}{\sqrt{1+|\epsilon|^2}} \left(|K_1\rangle + \epsilon\,|K_2\rangle\right) \end{aligned} \tag{2.13}$$

This observation destroyed the hope for a perfect CP symmetry in nature, but is in fact required to explain the development of our universe.

2.1.5. Sakharov criteria

Our understanding of the origin of the universe suggests that the Big Bang produced matter and antimatter in equal amounts. Yet, all structures we observe in the universe today, are made out of matter. When antimatter shows up, it annihilates as soon as it encouters matter. The observable excess of matter over antimatter requires an asymmetry, that allowed matter to accumulate after the Big Bang while antimatter disappeared.

In 1967, Sakharov formulated three criteria, which had to be fulfilled, to explain the matter-antimatter asymmetry [28]:

- There must be a process that violates the conservation of baryon and lepton number. Otherwise, the ratio of matter and anitmatter would always be the same.

- The universe must have been out of thermal equilibrium at some point. Otherwise, all reactions were always balanced in both directions and no net change in baryon number would have occurred.

- There must be a difference in the reaction processes of matter and antimatter that favors matter over antimatter. This is exactly CP violation, which describes a different rate for reaction and CP conjugated reaction and thus leads to a net change in baryon number.

The observed CP violation in the neutral kaon system fitted well into this scheme. However, measurements of the baryon asymmetry in the universe and the CP violation in particle decays show that the effect is by far not large enough to explain the observations [4].

2.1.6. Towards the CKM matrix

The CP violation is described in the Standard Model of particle physics in the Cabibbo-Kobayashi-Maskawa (CKM) matrix [29]. The first step in its development was made by Cabibbo, who introduced a correction factor for the long lived "strange" particles in 1963 [30]. He introduced an angle θ_C describing the weak interaction with a suppression for strangeness-changing processes. This idea was very successful in describing many of the observed decay rates, but failed for the decay of a neutral kaon into a pair of muons $K^0 \to \mu^-\mu^+$, which should have occurred way more frequently than it was measured.

This shortcoming was overcome by Glashow, Iliopoulos and Maiani (GIM) in 1970 [31]. They introduced a fourth quark, which they called charm c. Its couplings were chosen to partly cancel the ones of the three already known quarks in the kaon decay and thus describing correctly the observed suppression (see fig. 2.3).

The "GIM mechanism" introduced weak interaction states of the quarks, which are composed of mass eigenstates:

$$d' = d\cos\theta_C + s\sin\theta_C, \quad s' = -d\sin\theta_C + s\cos\theta_C \tag{2.14}$$

or in matrix form with the Cabibbo angle θ_C as rotation:

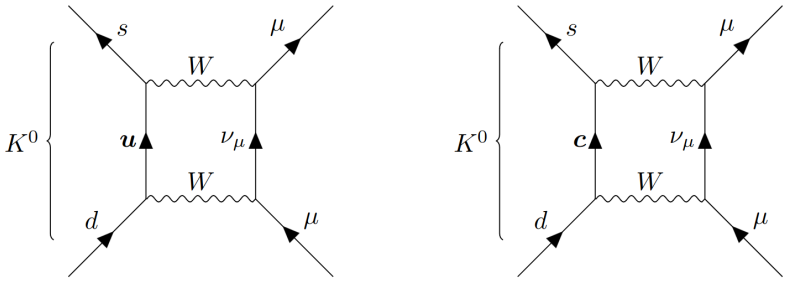


Figure 2.3.: The GIM mechanism in the $K^0 \to \mu^+ + \mu^-$ decay. GIM introduced the c quark with couplings that cause destructive interference between both amplitudes. Due to the higher mass of the c quark, a small excess remains explaining the small branching ratio.

$$\begin{pmatrix} d' \\ s' \end{pmatrix} = \begin{pmatrix} \cos\theta_C & \sin\theta_C \\ -\sin\theta_C & \cos\theta_C \end{pmatrix} \begin{pmatrix} d \\ s \end{pmatrix} \tag{2.15}$$

In order to introduce the by now established CP violation into this theory, Kobayashi and Maskawa found that it is necessary to introduce yet another quark family. In a 2×2 matrix there is only one physical parameter, the mixing angle θ_C. Only for a 3×3 matrix (or larger) at least one non-trivial phase remains irreducible [17]. In 1973, Kobayashi and Maskawa used this phase to incorporate CP violation into the Standard Model and predicted a third quark generation at the same time [29]. The discovery of the c quark in the J/ψ particle ($c\bar{c}$) in 1974 [32, 33] supported the quark model and verified the GIM mechanism. The third generation of elementary particles was first indicated in the lepton sector by the discovery of the tau (τ) lepton [34]. The bottom (b) quark followed soon in 1977 [35], while the much heavier top (t) quark took until 1995 to complete the third generation [36, 37].

The CKM matrix became a well established part of the Standard Model of particle physics and remains responsible for the description of CP violation in the quark sector. The elements V_{ij} of the unitary CKM matrix indicate the transition probability between the quarks i and j. Their amplitudes are described by three mixing angles θ_{12}, θ_{23}, and θ_{13} and one phase factor δ [16]:

$$\begin{aligned} V_{\text{CKM}} &= \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \\ &= \begin{pmatrix} c_{12}c_{13} & s_{12}c_{13} & s_{13}e^{-i\delta} \\ -s_{12}c_{23} - c_{12}s_{23}s_{13}e^{i\delta} & c_{12}c_{23} - s_{12}s_{23}s_{13}e^{i\delta} & s_{23}c_{13} \\ s_{12}s_{23} - c_{12}c_{23}s_{13}e^{i\delta} & -c_{12}s_{23} - s_{12}c_{23}s_{13}e^{i\delta} & c_{23}c_{13} \end{pmatrix} \end{aligned} \tag{2.16}$$

where c_{ij} stands for $\cos\theta_{ij}$ and s_{ij} for $\sin\theta_{ij}$. The four free parameters of the CKM matrix have to be determined experimentally.

The CKM matrix can also be expressed in the so called Wolfenstein parametrization [38] which visualizes the order of magnitude of the individual elements in terms of $\lambda = s_{12}$, $A\lambda^2 = s_{23}$, $A\lambda^3(\rho - i\eta) = s_{13}e^{-i\delta}$ and higher order terms:

$$V_{\mathrm{CKM}} = \begin{pmatrix} 1 - \frac{\lambda^2}{2} & \lambda & A\lambda^3(\rho - i\eta) \\ -\lambda & 1 - \frac{\lambda^2}{2} & A\lambda^2 \\ A\lambda^3(1 - \rho - i\eta) & -A\lambda^2 & 1 \end{pmatrix} + \mathcal{O}(\lambda^4) \tag{2.17}$$

The current values for the measured amplitudes of the matrix elements are [39]:

$$|V_{ij}| = \begin{pmatrix} 0.97373 \pm 0.00031 & 0.2243 \pm 0.0008 & 0.00382 \pm 0.00020 \\ 0.221 \pm 0.004 & 0.975 \pm 0.006 & 0.0408 \pm 0.0014 \\ 0.0086 \pm 0.0002 & 0.0415 \pm 0.0009 & 1.014 \pm 0.029 \end{pmatrix} \tag{2.18}$$

Figure 2.4 illustrates the quark transitions and their probabilities. The diagonal values of the CKM matrix are close to one, stating that the flavor transitions within the generations are the dominant ones. Note that each flavor change is accompanied by a change of the electric charge by one elementary unit. In the Standard Model there are no first-order flavor-changing neutral currents (FCNCs). Any observation of such a process would be a hint for physics beyond the Standard Model.

The unitarity condition

$$V_{CKM}V_{CKM}^{\dagger} = V_{CKM}^{\dagger}V_{CKM} = 1 \tag{2.19}$$

leads to nine independent equations. In particular, the product of different columns or rows of the CKM matrix need to vanish. The parametrization of the CKM matrix shows, that the largest manifestation of the CP violating phase lies in the transition of quarks between the first and third generation. This motivates the study of CP violation in the B meson system, which combines quarks of the third and first generation: B^0 $(\bar{b}d)$ and $\overline{B}^0$ $(b\bar{d})$.

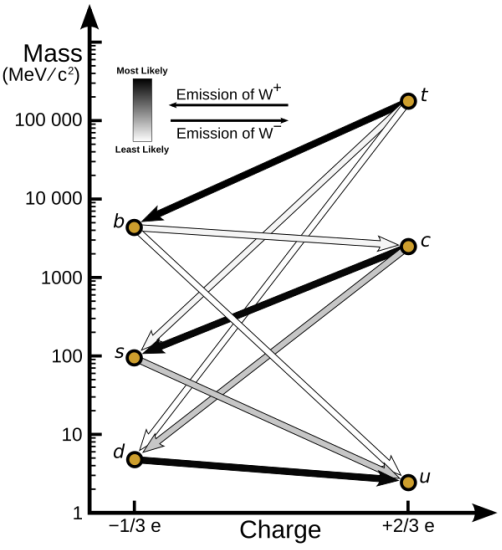


Figure 2.4.: CKM visualization [40]. The shade of the arrows indicates the transition probability.

For example, one equation from the unitary condition is obtained by multiplica-

tion of the first and third columns of the CKM matrix:

$$\begin{array}{lll} V_{ud}V_{ub}^{*}+ & V_{cd}V_{cb}^{*}+ & V_{td}V_{tb}^{*}=0 \\ \mathcal{O}(\lambda^3)+ & \mathcal{O}(\lambda^3)+ & \mathcal{O}(\lambda^3) \end{array} \tag{2.20}$$

This equation represents a "unitarity triangle" in the complex plane with similar side lengths. Several measurements are possible to determine lengths and angles, over-constraining the triangle, which allows to precisely determine the unitarity condition. The triangle needs to close and every deviation would point to physics beyond the Standard Model. A current fit of the CKM parameters from the equation above is shown in fig. 2.5. So far, all measurements are in agreement with the Standard Model predictions.

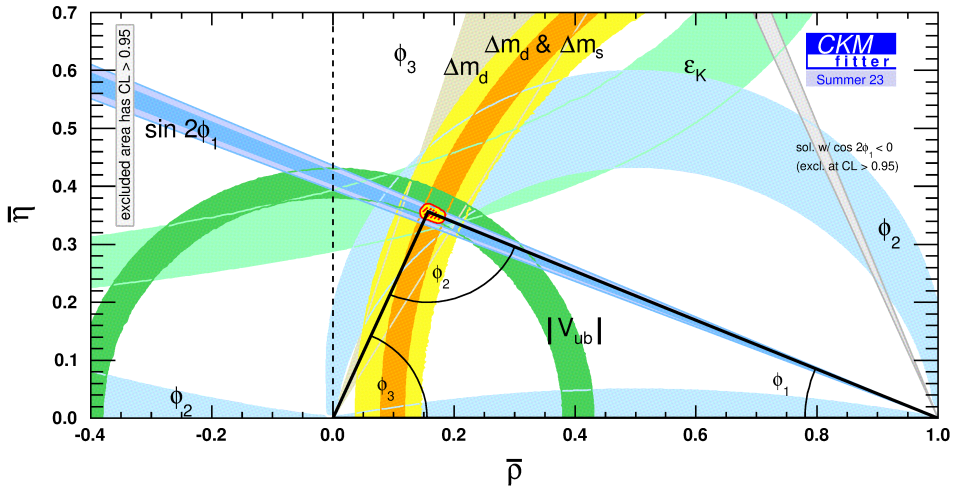


Figure 2.5.: CKM fitter [41]. Constraints on the unitarity triangle in the complex plain.

2.2. Standard Model of particle physics and open questions

The Standard Model of particle physics describes the known matter in form of elementary particles and their fundamental interactions through the strong, weak and electromagnetic force (yet excluding gravity). The current picture is shown in fig. 2.6.

The elementary particles are divided into twelve fermions with spin $\frac{1}{2}$ and five bosons with integer spin. The fermions consist of six quarks and six leptons, both occurring in three generations with increasing mass regimes. The up-type quarks (u, c, t) carry electrical charge $+\frac{2}{3}$, while the down-type quarks carry electrical charge $-\frac{1}{3}$, in units of the elementary charge e. In addition, the quarks also have a color charge (red,

green or blue) through which they couple to the gluon, the force carrier of the strong interaction. The electrically charged leptons (e, μ, τ) have no color charge as they do not interact strongly. The uncharged leptons (the neutrinos) are completely chargeless and interact only weakly.

The forces are transmitted by four kinds of gauge bosons with spin 1. The gluons are the carriers of the strong force and couple to the color charged quarks. There are in total eight differently colored gluons, which can also couple to each other. The photon is the exchange particle of the electromagnetic interaction and couples to all electrically charged particles, while itself does not carry any charge. The photon is its own antiparticle and does not couple to itself. The W and Z bosons are the force carriers of the weak interaction. All elementary fermions take part in the left-handed weak interaction. The Higgs boson is a scalar particle. It is responsible for the masses of the elementary particles. For each elementary particle there exists an antiparticle with the same mass and spin but all charges inverted.

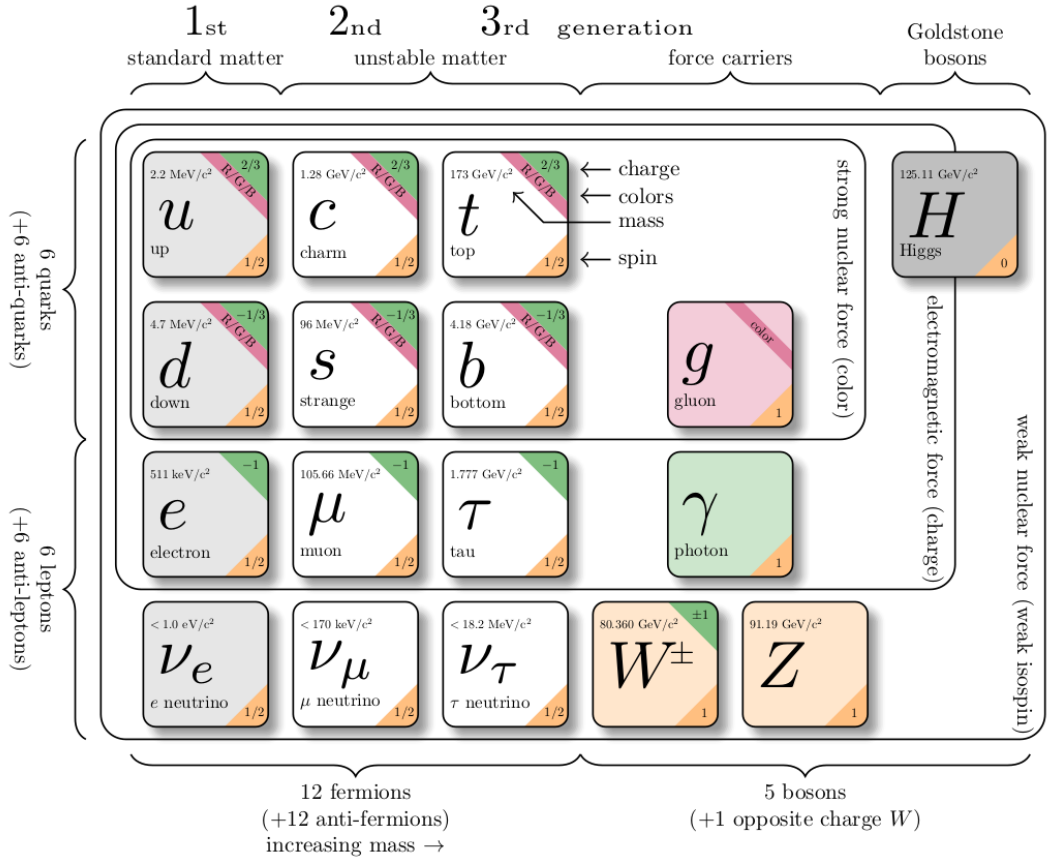


Figure 2.6.: Standard Model of elementary particles [42].

The Standard Model of particle physics succeeded in the unification of the weak and electromagnetic forces and is a well established theory confirmed by numerous experimental measurements. However, many questions within the standard model remain still unanswered. Why are there three generation of particles or are there maybe more? Why are there so many free parameters that have to be determined experimentally, like the masses of the elementary particles, the gauge couplings (the strengths of the fundamental froces) or the CP violating phase?

Beyond that, many open questions stem especially from observations in astrophysics and cosmology. The matter-anitmatter asymmetry and concepts like dark matter and dark energy cannot be explained by the Standard Model [4] and point to physics that goes beyond. These and many more questions are addressed by particle physics experiments around the world. One approach to find new physics is to push the energy frontier and the search for new particles at ever higher energies. This is the main strategy of e.g. the Large Hadron Collider (LHC) at CERN with energies up to 13 TeV. The other approach aims to push the intensity frontier and looks for small deviations in the Standard Model processes that could occur by the virtual contribution of new particles in higher order loop corrections. The latter is followed by B factories that collect huge data sets and therefore enable analyses with very high precision and the search for rare decays.

2.3. Physics program at Belle II

B factories are especially designed and constructed to produce a large amount of B mesons. They use electron and positron beams which are collided at a center of mass energy of 10.58 GeV. At that energy lives the $Y(4S)$ resonance in the e^+e^- spectrum, which is an excited state of the Y meson ($b\bar{b}$) that lies just above the threshold to produce a pair of free B mesons. The neutral B mesons are produced in an entangled state, which requires to determine the flavor of one of the B mesons (B_{signal}) at its decay by reconstructing the flavor of the other one (B_{tag}). The charged B mesons can be identified through the net charge of their decay products. These techniques are summarized under the term “flavor tagging” [17].

In order to assign the decay products correctly to the individual B mesons, their vertices have to be separated. This is achieved through an energy difference between the electron and positron beams. This boost gives the B mesons, which are almost at rest in the center of mass system, a momentum in the laboratory system and therefore translates a difference in the decay times into a measurable difference in the decay vertices (see fig. 2.7).

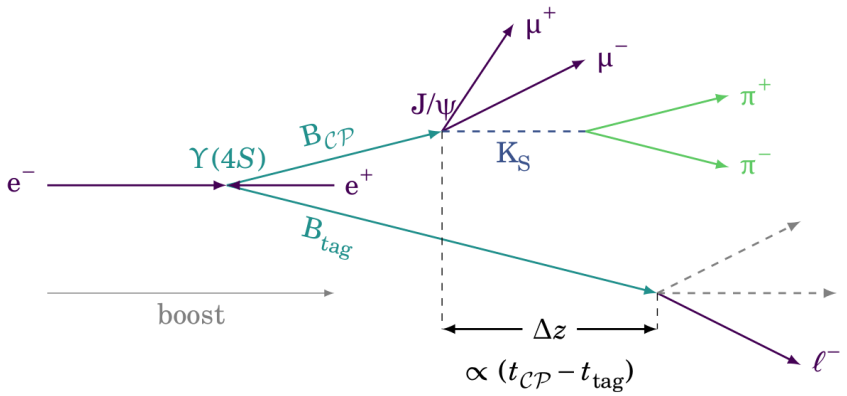


Figure 2.7.: Typical decay of the $Y(4S)$ resonance for measurement of time dependent CP violation [43].

In the 1990s and 2000s, two B factories were in operation, the PEP-II accelerator at SLAC and the KEKB accelerator at Tsukuba. The results of their respective detector collaborations, BaBar and Belle, confirmed, among many other achievements, the postulated CP violation in the B meson system and helped to measure the CKM parameters with unprecedented precision [44, 45]. The verification of their theory won Kobayashi and Maskawa the 2008 Nobel Price in Physics. The KEKB accelerator was upgraded to SuperKEKB and also the detector was upgraded to Belle II (see following chapter) providing the worldwide exclusive B factory today. Data taking has already started in 2019. Although not a B factory, the LHCb experiment [46] at CERN performs complementary measurements but works at different conditions as the collision particles are protons at much higher energies.

The Belle II physics program spans a wide variety of fields (see fig. 2.8). It is centered around the mentioned questions on B physics including CKM matrix elements, time dependent CP violation and rare decays. However, the collected data also allows to study e.g. the physics of the lighter charm quark. Lepton flavor universality violation can be tested in the decays of the tau leptons. Measurements at higher Y resonances, quantum chromodynamics (QCD) measurements and studies in the electroweak sector are further directions of the collaborative analysis effort of the Belle II experiment. In the dark sector, dark photons (A' and Z') and dark higgs h' hypotheses are tested and searches for axion-like particles (ALPs) are performed. Belle II has a world-leading potential to address all these cases [47].

During the first run period from 2019 to 2022, the recorded data set exceeded $426\,\mathrm{fb}^{-1}$, which is about as large as BaBar's data set. About $365\,\mathrm{fb}^{-1}$ were recorded at the Y(4S) resonance. This amounts to a number of $(387.1 \pm 5.6) \times 10^6$ B meson pairs [49].

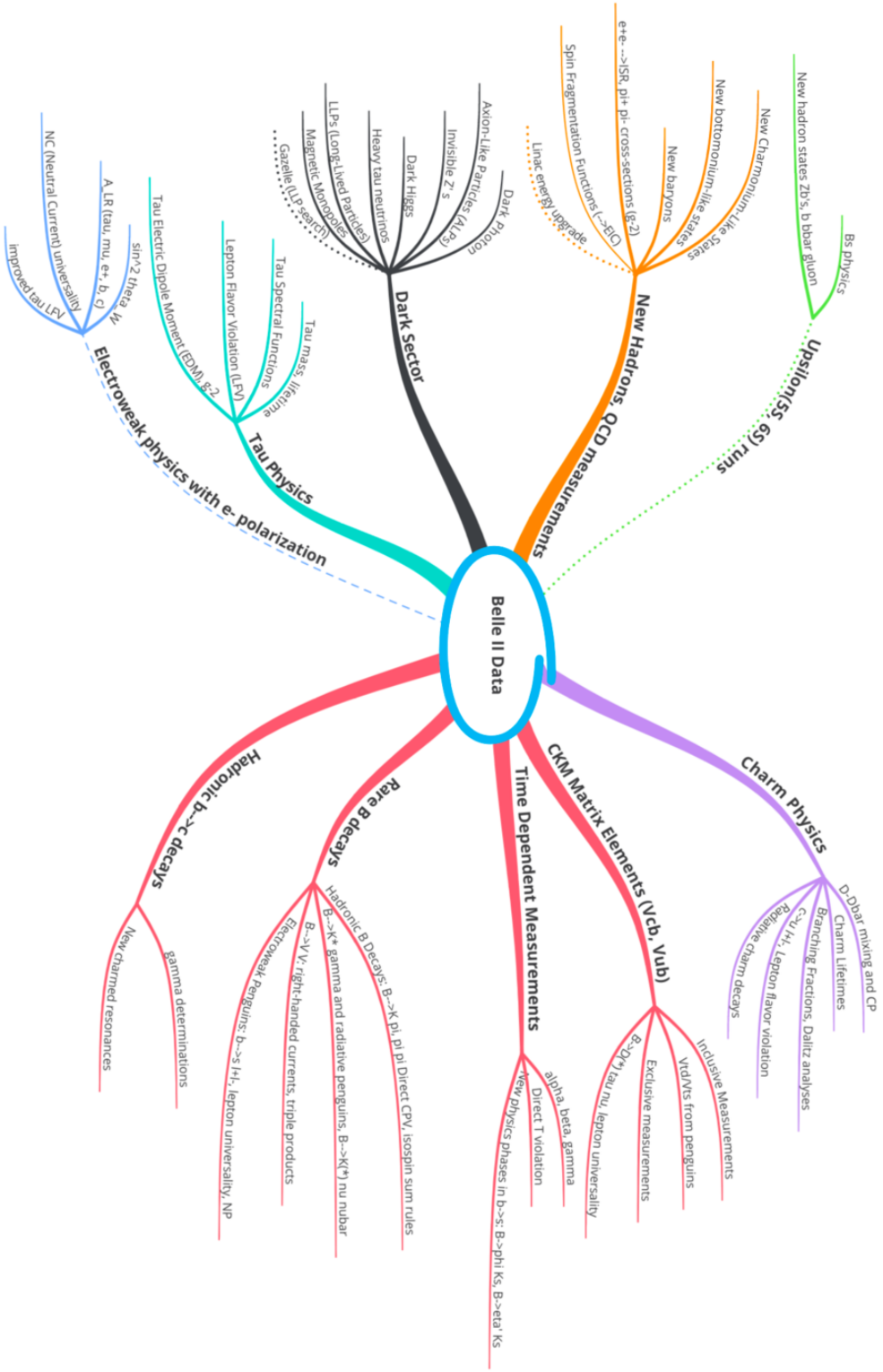
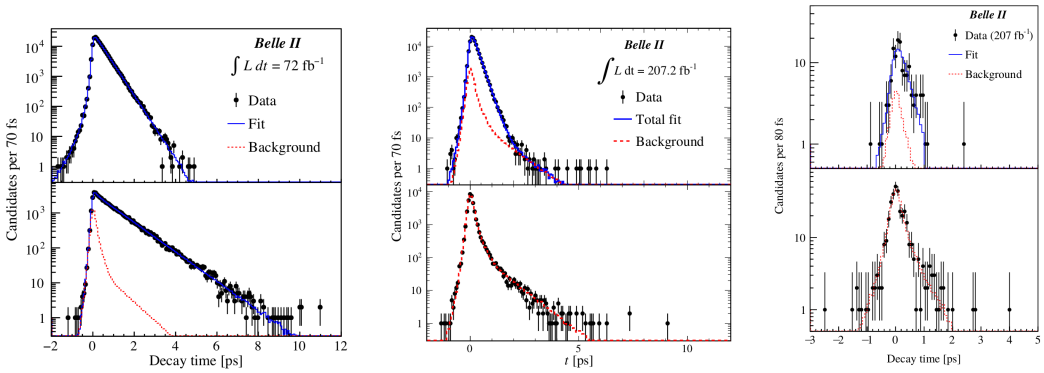


Figure 2.8.: Illustration of Belle II physics program [48].

In particular, time-dependent CP analyses and lifetime measurements benefit from the high resolution of the PXD, which has already allowed first results on lifetimes of e.g. D mesons and Λ_c^+ and Ω_c^0 baryons [5–7] (see fig. 2.9).

- $\tau(D^0) = 410.5 \pm 1.1\,(\text{stat}) \pm 0.8\,(\text{syst})$ fs
  $\tau(D^+) = 1030.4 \pm 4.7\,(\text{stat}) \pm 3.1\,(\text{syst})$ fs
- $\tau(\Lambda_c^+) = 203.20 \pm 0.89\,(\text{stat}) \pm 0.77\,(\text{syst})$ fs
- $\tau(\Omega_c^0) = 243 \pm 48\,(\text{stat}) \pm 11\,(\text{syst})$ fs



(a) D^0 and D^+ **(b)** Λ_c^+ **(c)** Ω_c^0

Figure 2.9.: Lifetime measurements at Belle II. Decay-time distributions of: (a) $D^0 \to K^-\pi^+$ (top) and $D^+ \to K^-\pi^+\pi^+$ (bottom) candidates in their respective signal regions with fit projections overlaid [5]. (b) $\Lambda_c^+ \to pK^-\pi^+$ events in the signal region (top) and sidebands (bottom) with fit projections overlaid [6]. (c) $\Omega_c^0 \to \Omega^-\pi^+$ candidates populating the signal region (top) and the sideband (bottom) with fit projections overlaid [7].

The Ω_c^0 lifetime measurement independently confirmed the LHCb results [50] which also found that the Ω_c^0 is not the shortest lived baryon among the four singly charmed baryons that decay weakly. Instead the observed lifetime hierarchy is $\tau(\Xi_c^0) < \tau(\Lambda_c^+) < \tau(\Omega_c^0) < \tau(\Xi_c^+)$. This result shows that a deeper understanding of the underlying principles is still required.

The new PXD significantly contributed to these measurements, which require carefully controlled systematics and a very high resolution. In fact, the new vertex detector offers two times the decay time resolution of Belle and BaBar although it has to operate under even more demanding conditions. A reduced boost of the beam energies reduces the separation of primary decay vertices and the higher event rates and background conditions increase the occupancy. The nonetheless increased performance is only possible through the high granularity of the new PXD featuring two layers of thinned silicon pixel modules (see chapter 4).

3. SuperKEKB and Belle II

The SuperKEKB accelerator at the KEK in Tsukuba, Japan, is the B-factory for the Belle II detector. The main goals of the SuperKEKB accelerator are to reach an instantaneous luminosity of $6 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and a target integrated luminosity collected by the Belle II detector of $50\,\mathrm{ab}^{-1}$ by the 2030s. A new peak luminosity record of $4.65 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ (more than twice the one of KEKB) was reached during the first run period from 2019 to 2022[1].

SuperKEKB and Belle II are substantial upgrades of their predecessors and aim for a tremendous increase in the available physics data sample. The most important components of both systems are described in this chapter as well as the strategies to achieve the set targets in luminosity and to efficiently record the data.

3.1. SuperKEKB

SuperKEKB is an asymmetric-energy electron-positron collider. It operates mainly at a center of mass energy of 10.58 GeV (about 7 GeV for the electrons and 4 GeV for the positrons) corresponding to the $Y(4S)$ resonance, while the energies are tuneable up to a center of mass energy of about 12 GeV. The boost transforms the life time difference Δt of B mesons into a separation of their decay vertices Δz of about 125 µm [51]. SuperKEKB is an upgrade of the KEKB accelerator and continues the history of Japan's first electron-positron collider TRISTAN [52, 53]. The Transposable Ring Intersecting Storage Accelerator in Nippon (TRISTAN) was proposed in 1973, at a time when only the three lightest quarks were known, and was built from 1981 to 1986 in the north of Tsukuba city on the KEK ground site. After construction, the symmetric electron-positron collider reached the design collision energy of over 60 GeV, but it turned out to be not high enough for the production of the at that time still missing top quark. It took until 1995, when the required center of mass energy of almost 2 TeV was finally reached at the TEVATRON in $p\bar{p}$ collisions [36, 37].

[1] The SuperKEKB collider reached an even higher peak luminosity of $4.71 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ during machine studies, but the Belle II detectors were switched off for protection during these runs and no data was recorded.

In the 1990s, the tunnel of the TRISTAN experiment was reused to install the beam lines of the B-factory KEKB maximally utilizing the existing infrastructure, but with reduced energies to fit the $Y(4S)$ resonance. The asymmetric-energy e^+e^- collider operated from 1998 to 2010 to study CP violation in B meson decays. The associated Belle detector collected more than $1\,\mathrm{ab}^{-1}$ of collision data and the results of the collaboration finally confirmed the CKM theory leading to the award of the Nobel Prize in physics in 2008 to Kobayashi and Maskawa.

The accelerator was upgraded to the SuperKEKB collider from 2010 to 2018 for a major luminosity upgrade which allows an extension of the physics program and to address open questions with a larger data sample and therefore higher precision. The aim is the collection of a data set 50 times as large as the predecessor by a significant increase of the instant luminosity by a factor of about 30 with respect to the KEKB machine. An aerial view of the KEK site with a drawing of the accelerator structure overlaid is shown in fig. 3.1.

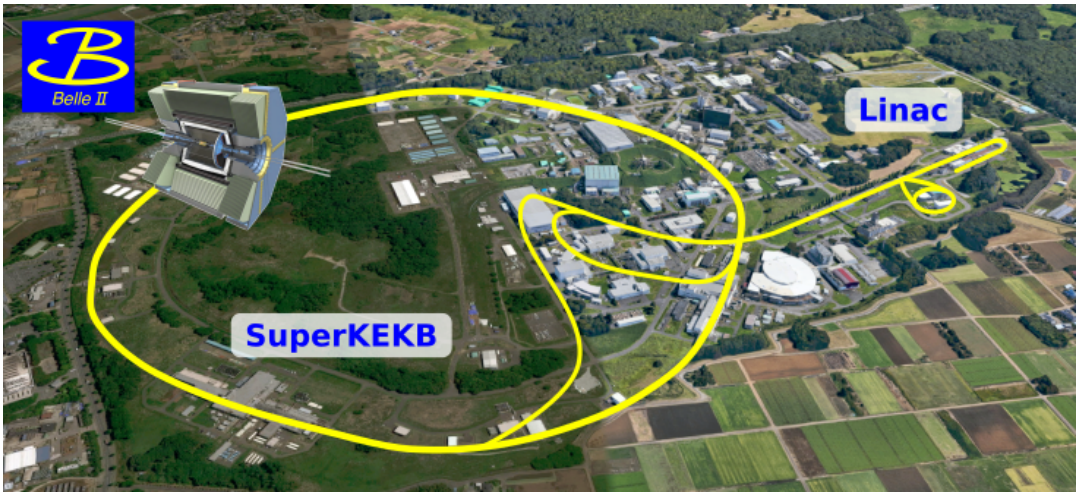


Figure 3.1.: Schematic drawing of the SuperKEKB accelerator on top of a Google Earth view from the KEK facilities.

A larger luminosity allows to collect collision data faster as it is a measure for the number of collisions per unit cross section and time. For an electron-positron collider the luminosity can be written as [54]:

$$\mathcal{L} = \frac{N_{e^+} N_{e^-} f_c}{4\pi\sigma_x\sigma_y} R_L \tag{3.1}$$

where N stands for the number of positrons/electrons in a bunch, f_c for the bunch collision frequency, $\sigma_{x/y}$ for the horizontal and vertical bunch sizes at the collision point, and R_L is a correction factor due to the crossing angle and the hourglass effect. The increase of luminosity is reached through a significant reduction of the

transverse beam sizes (factor of 20) and an increase in beam currents (factor of 1.5). The beam size reduction becomes possible through the implementation of the so called "nano-beam" scheme discussed below at the description of the interaction region.

The main components of the SuperKEKB collider are the linear accelerator (linac), a new damping ring for the positron bunches, the Low Energy Ring (LER) for the positron beam and the High Energy Ring (HER) for the electron beam, and the interaction region with the Belle II detector (see fig. 3.2).

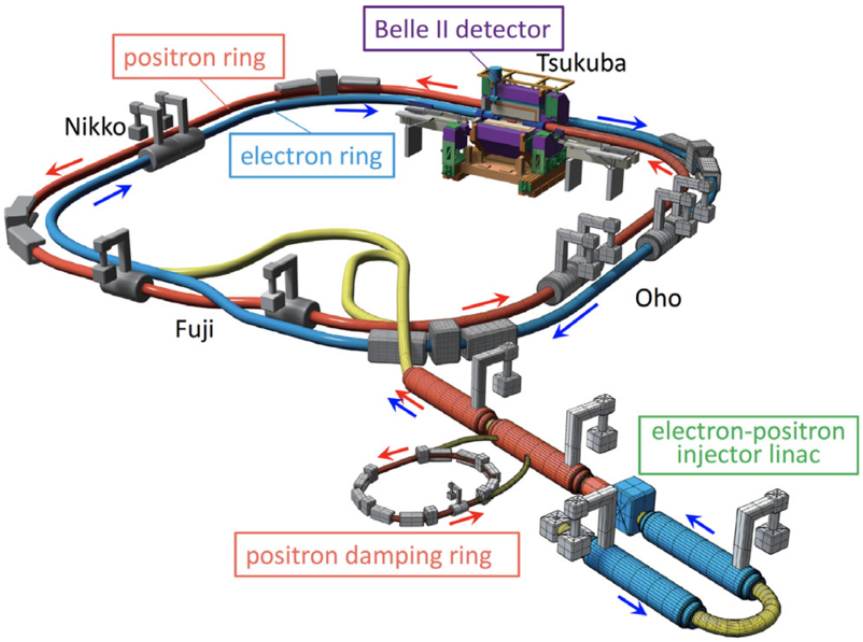


Figure 3.2.: SuperKEKB electron-positron collider [55]. The main components are linac, positron damping ring, LER and HER storage rings, and the interaction region with the Belle II detector.

The linac has a length of 600 m and consists of 60 accelerator units, which are installed with a very high alignment precision (300 µm on the entire length [55]) to achieve the beam emittance requirements for the nano-beam scheme (see eq. (3.3)). An Ytterbium-doped yttrium aluminum garnet (Yb:YAG) laser creates the electron bunches through photo effect at the beginning of the linac. For the production of the positron bunches, the electron bunches are deflected after the first acceleration stages to hit a tungsten target. The resulting high energetic photons from bremsstrahlung convert to electrons and positrons through pair creation at a secondary thin target. The positrons are separated magnetically and fed into the positron damping ring. At an energy of 1.1 GeV the emittance of the positron bunches is reduced by synchroton cooling. Afterwards, they are transferred back to the linac.

Finally, the linac accelerates electron and positron bunches to 7 GeV and 4 GeV, respectively, and injects them into their corresponding storage rings. A continuous injection scheme with a rate of 50 Hz is achieved with high bunch charges (about 4 nC per bunch [54]) to maintain the high currents of the main rings with short beam life times of only several minutes. In parallel, the two rings of the Photon Factory are also supplied by the same linac.

The storage rings of SuperKEKB have a circumference of 3 km. The LER keeps the positron bunches at an energy of 4 GeV and aims for a design value of 3.6 A of beam current, while the HER keeps the electron bunches at an energy of 7 GeV and aims for 2.6 A of beam current. The bunch revolution time in the storage rings is 10 µs. Both rings will store up to 2500 bunches each. This results in a bunch crossing frequency of 250 MHz, while the physics event rate is expected to be about 20 kHz at full luminosity [56]. This expectation is based on the cross sections for quark or lepton pair creation from electron-positron collisions in the order of 1 nb [57] and the rate from several QED monitoring reactions, such as Bhabha scattering.

In preparation for the high luminosity operation, also several parts of the storage rings were upgraded (see fig. 3.3). New beam pipes with antechambers and additional titanium nitride (TiN) coating were installed to mitigate the electron cloud effect and to reduce the synchrotron radiation power density at the beam pipe walls. New collimators for the new antechamber beam pipes were developed and installed. The power supplies for the cavities were almost doubled to meet the higher demand. A new technique was developed to recover degraded cavities. The beam diagnostics were extensively upgraded [55].

Figure 3.3.: Beam lines north west of Tsukuba Hall facing the detector. The LER (left) containing the positron beam and the HER (right) containing the electron beam cross at the Interaction Point in the center of the Belle II detector which is visible in the back.

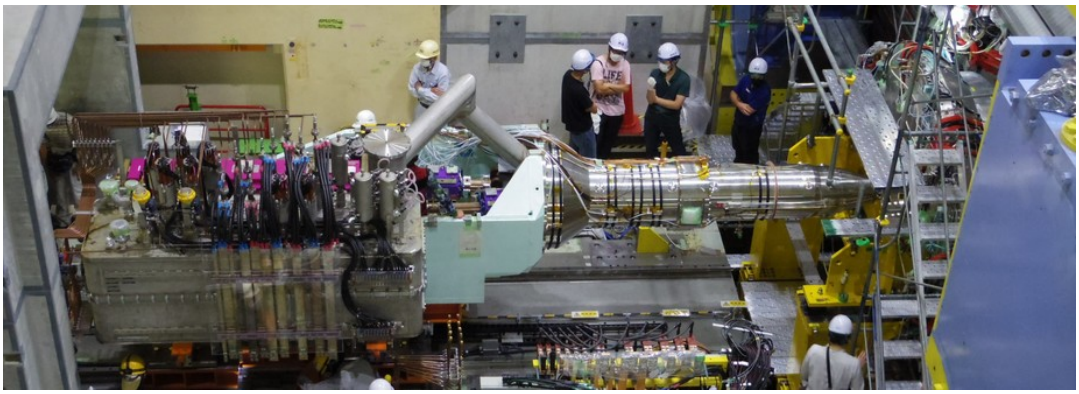


Figure 3.4.: Right QCS (forward) during extraction in 2022 [58].

3.1.1. Interaction region

The most substantial upgrades for the luminosity increase are found at the interaction region. In the "Tsukuba Hall", the otherwise separated beam pipes are joined into a single beam pipe with only 20 mm inner diameter. The final focusing superconducting magnet system QCS squeezes the vertical bunch sizes down to extremely low values of about 50 nm at the Interaction Point (IP) where the bunches collide. After the IP, the beams are separated into their own storage rings and complete another turn before they collide again. The Belle II detector encloses the IP to detect and measure the collision products.

3.1.1.1. Final focusing magnet system

The QCS[2] system consists of two cryostats (left and right) containing in total 55 superconducting magnets [60]. Both cryostats reach close to the IP and thus far into the detector volume when inserted to their final position (see figs. 3.4 and 3.5 for their extracted position). The QCS system was completely new designed and constructed for the nano-beam operation at SuperKEKB.

[2]The naming convention originates from the final focusing magnets scheme used at TRISTAN [59]. Initially two pairs of normal iron-core quadrupole magnets (Quadrupole Couple), QC1 and QC2, were used for the so called low-beta optics. The mini-beta optics extension included a further pair of superconducting quadrupole magnets QCS. The QCS of SuperKEKB combines QC1 and QC2 into one superconducting magnet system.

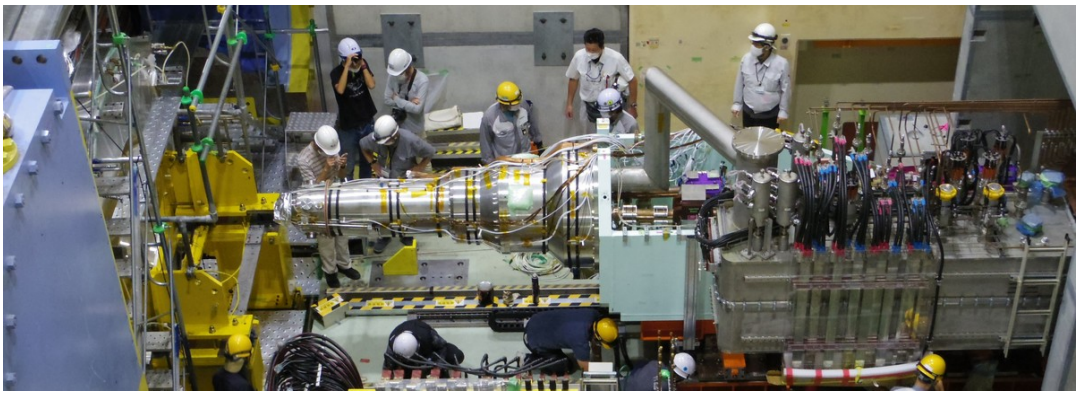


Figure 3.5.: Left QCS (backward) during extraction in 2022 [58].

3.1.1.2. Nano-beam scheme

The main increase in luminosity for SuperKEKB compared to KEKB is achieved through the implementation of the so called nano-beam scheme (see fig. 3.6). Besides eq. (3.1), the luminosity dependency can also be expressed in correlation to beam operation factors of the collider as [61]:

$$\mathcal{L} \propto \frac{N\xi_y}{\beta_y^*} \qquad \text{with} \qquad \xi_y \propto \frac{N\beta_y}{\sigma_x\sigma_y\sqrt{1+\phi_{Piw}^2}} \tag{3.2}$$

where ξ_y is the vertical beam-beam parameter, β_y^* is the vertical beta function at the IP and ϕ_{Piw} the Piwinski angle:

$$\phi_{Piw} \approx \frac{\sigma_z}{\sigma_x}\,\phi_x \qquad \text{and} \qquad \sigma_{x,y} = \sqrt{\beta_{x,y}\,\epsilon_{x,y}} \tag{3.3}$$

with the crossing angle ϕ_x and the emittance ϵ.

A luminosity increase is therefore achieved through an increase of particles per bunch, i.e. the beam currents, an increase of the beam-beam parameter ξ_y and the reduction of the vertical beta function β_y^* [62]. These goals are hard to reach in conventional head-on collision as very short bunches are hard to realize and bunch lengths $\sigma_z > \beta_y^*$ result in beam-beam blowups through the "hourglass effect" and in problematic betatron oscillations [63]. Therefore, nano-beams are only possible through the simultaneous application of the crab waist scheme [61]. A large Piwinski angle decreases the overlapping area at the IP and introduces a horizontal separation which reduces unwanted particle interactions outside of the IP [64]. In addition, vertical betatron resonances are strongly suppressed by the compensation of nonlinear terms [65], allowing a significant ξ_y increase.

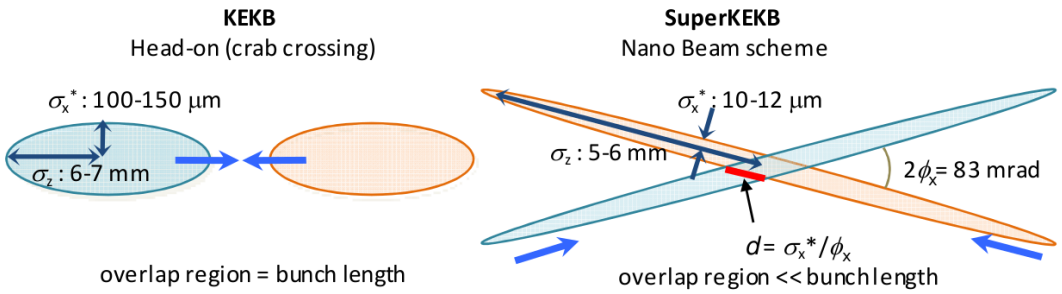


Figure 3.6.: Beam collision schemes of KEKB and SuperKEKB [66]. Left: The initial collision design of the KEKB collider used a head-on collision of the bunches. Right: The nano-beam scheme requires a large Piwinski angle and thus incorporates also a large crossing angle ϕ_x.

A further change compared to KEKB is the reduction of the boost factor $\beta\gamma$. The asymmetry of the beam energies is reduced from 8 GeV electrons and 3.5 GeV positrons to 7 GeV electrons and 4 GeV positrons, effectively reducing $\beta\gamma$ from 0.42 to 0.28. This helps to reduce the emittance growth from intra-beam scattering (Touschek effect [67]) and to improve the limited lifetime of the positron beam [68]. Also the emittance of the electron beam is reduced as well as the synchrotron radiation power, which is of larger concern because of the larger currents [55, 68]. However, the reduced boost results in a smaller separation of decay vertices, which poses a higher challenge for the vertex detector (details in chapter 4).

The design machine parameters for SuperKEKB and the comparison to the already achieved values are given in table 3.1. In 2022, SuperKEKB reached beam currents above 1 A, beta functions of 1 mm and beam-beam parameters of about half the design value for the LER and a quarter of the design value for the HER. A new world record in peak instant luminosity was achieved with a value of $4.65 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. For a further increase challenges have to be overcome such as further beta squeezing, reduction of beam–beam blowup, and increasing beam currents while simultaneously suppressing detector beam backgrounds [64].

3.1.1.3. Beam pipe

The interface between the SuperKEKB collider and the Belle II detector at the IP is the beam pipe. It is a hollow cylinder made of beryllium with a double wall for paraffin cooling. Beryllium is chosen for its transparency to particles, high specific stiffness, and compatibility with ultra-high vacuum [70]. The inner wall at a radius of 10 mm is 0.6 mm thin and has a coating of 10 µm gold on the inside to reduce the

Table 3.1.: SuperKEKB machine parameters - goals / achievements [55, 68, 69].

		LER	**HER**	Unit
Beam energy	E	4.000	7.007	GeV
Circumference	C	3016.315		m
Crossing angle	$2\phi_x$	83		mrad
Horizontal emittance	ϵ_x	3.2 / 4.0	4.6 / 4.6	nm
Beam current	I	3600 / 1321	2600 / 1099	mA
Number of bunches	n_b	2500 / 2249		
Particles per bunch	N	9.04 / 3.69	6.53 / 3.07	10^{10}
Bunch current	I_b	1.44 / 0.59	1.04 / 0.49	mA
Horizontal beam size	σ_x^*	10.1 / 17.9	10.7 / 16.6	µm
Vertical beam size	σ_y^*	48 / 215	62 / 215	nm
Betatron tunes	v_x	44.53 / 44.53	45.53 / 45.53	
Betatron tunes	v_y	44.57 / 46.59	43.57 / 43.57	
Beta function at IP	β_x^*	32 / 80	25 / 60	mm
Beta function at IP	β_y^*	270 / 1000	300 / 1000	µm
Piwinski angle	ϕ_{Piw}	24.6 / 10.7	19.3 / 12.7	rad
Beam-beam parameter	ξ_y	0.088 / 0.041	0.081 / 0.028	
Luminosity	L	6×10^{35} / 4.65×10^{34}		$\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Integrated luminosity	L_{int}	50 / 0.426		ab^{-1}

intensity of soft photons from synchrotron radiation. The gap between the inner and outer wall is 1.0 mm wide and filled with paraffin ($H_{10}C_{22}$) as coolant to dissipate the energy input from mirror currents on the inner surface, higher order mode heating and particle interactions [71]. The outer wall has a thickness of 0.4 mm defining the outer radius of the beam pipe at 12 mm. The inner layer of the PXD is installed at a radius of 14 mm leaving a gap of only about 2 mm (see fig. 3.7).

The beam pipe at the interaction region was replaced with an entirely new one during the long shutdown in 2022/2023. An additional gold coating of 10 µm was added on the outside of the inner pipe outside of the acceptance window to absorb scattered soft x-rays. In addition, the straight section of the beam pipe was shortened by 1 cm on forward side and by 0.5 cm on backward side to mitigate the effect of scattered x-rays hitting the PXD during beam injection. The radiation length at the IP acceptance area on perpendicular incident is estimated as 0.7 X_0 [72].

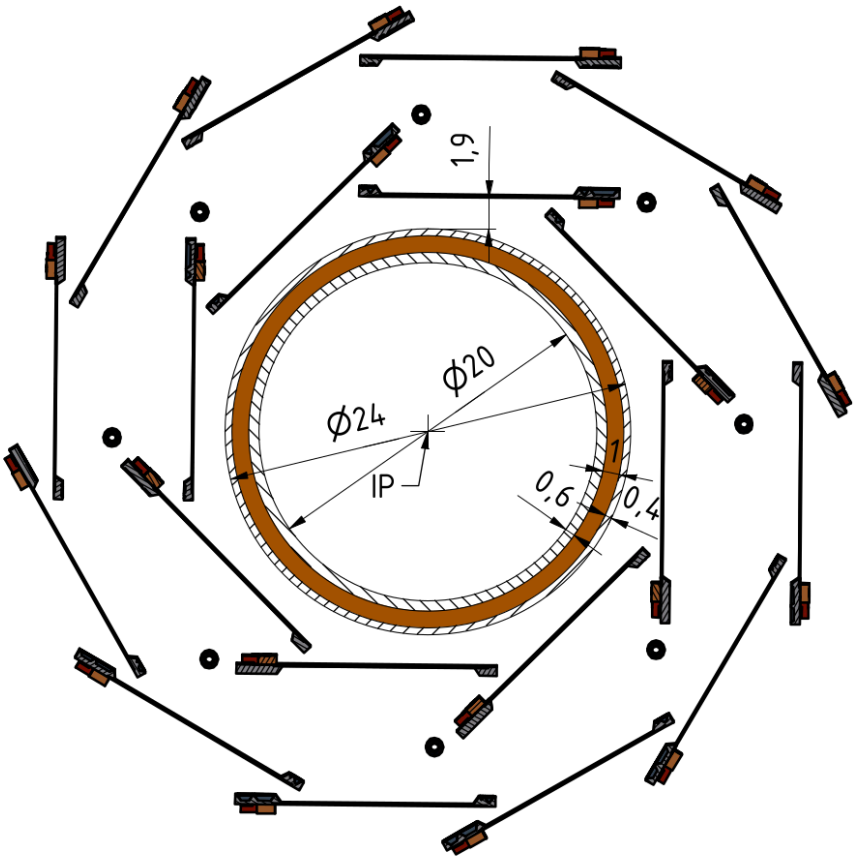


Figure 3.7.: Profile of beam pipe and PXD at the IP [73]. Values in mm.

3.2. Belle II

In order to study the physical processes of interest, a specialized particle detector is required to precisely record and measure the properties of the produced particles. In addition, high event and background rates, requirements on radiation hardness, and the necessity to avoid multiple scattering pose special challenges to the detector design. The Belle II detector system [72] performs these tasks for the SuperKEKB collider. It is located in the Tsukuba Hall on the KEK site. The detector geometry around the IP accounts for the asymmetric beam energies and covers a more shallow angle in the forward direction (17° to 150°). Mechanical reasons, especially the QCS, which reaches far into the detector volume, but also compulsory space for services and cables, limit the achievable coverage.

The Belle II detector consists of several subdetectors, which serve special purposes, like particle identification, energy and momentum measurement, and precise tracking close to the particle origin. Within the detector system, the subdetectors are arranged cylindrically around the beam pipe at the IP (see fig. 3.8). In this section, the seven main subdetectors are briefly presented in their current state.

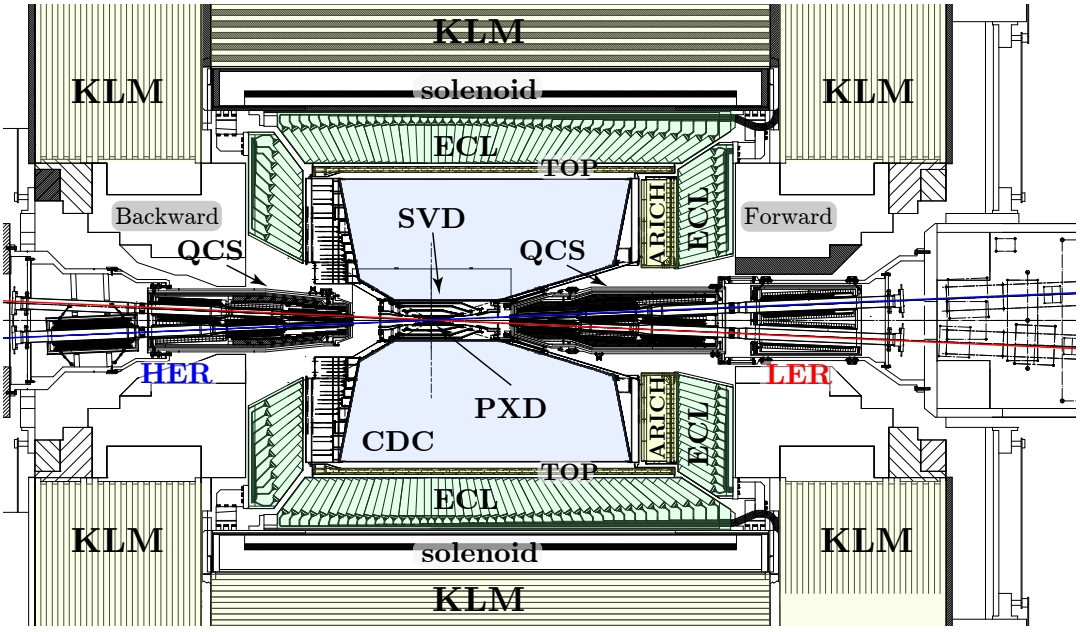


Figure 3.8.: Interaction region with the surrounding Belle II detector [51]. The technical drawing demonstrates the arrangement of the subdetectors in a view from above.

The detector volume is divided into three parts, which are referred to as the barrel region, the forward endcaps and backward endcaps. The spacial coordinates are defined by the z-axis along the beam pipe in forward direction, the y-axis pointing upwards and the x-axis pointing radially outward from the accelerator ring. The origin is located at the IP (x, y, z=0).

The task of detector development, construction and operation as well as the data analysis is covered by the Belle II collaboration. It aims to accumulate a data sample of $50\,\mathrm{ab}^{-1}$ to address the various topics of its physics program [47]. As of the beginning of 2024, the Belle II collaboration consists of over 1170 physicists and engineers from 123 institutions distributed across 28 countries [74] (see fig. 3.9).

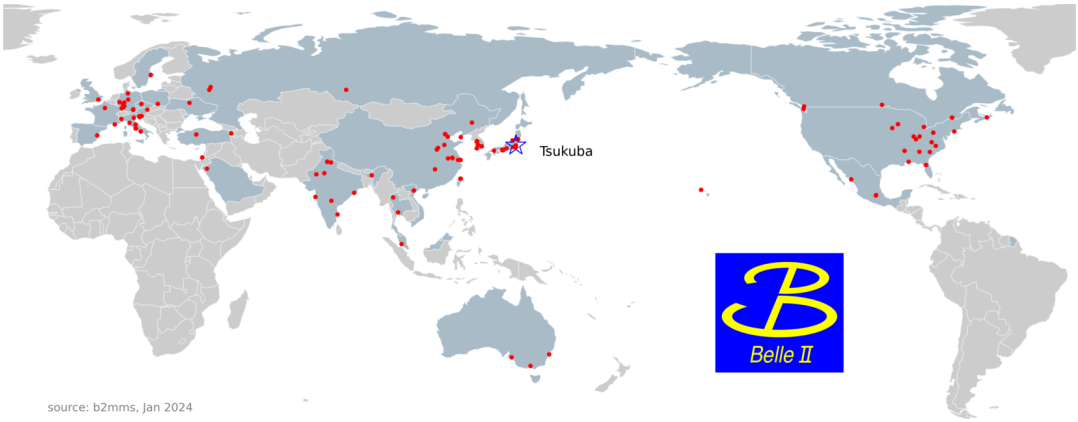


Figure 3.9.: Map of the international member institutes of Belle II.

The Belle II detector is an upgrade of the preceding Belle detector [75]. Several parts are reused, like detector components in the outer barrel part, the scintillator crystals of the calorimeter and the solenoid. The other detector parts, mainly the tracking and particle identification detectors, as well as the readout system of all subdetectors, were replaced by newly developed systems. The detector was upgraded from 2010 until spring 2019, when physics data taking started.

Figure 3.10 provides a look into the Tsukuba Hall down onto the Belle II detector. The entire detector, including the adjacent Electronic Hut (E-Hut), can be moved out of the interaction region for work on the detector systems. The E-Hut houses the required electronics for operation, readout and monitoring of the subdetectors on two floors. Further services are installed on top of the E-Hut and on “top of Belle”. After the completion of detector work, the entire system is moved into the beam line position again. Then both sides of the QCS are inserted and the beam pipes are connected to close the accelerator rings. The end yokes, which contain the KLM endcaps, are closed and a concrete shield is placed at both sides of the detector to protect against radiation in the experimental hall.

The Belle II control room is also located in the Tsukuba Hall. It provides operation and monitoring terminals for the local control room shifters and the local subdetector experts, who operate the detector systems during data taking and maintenance days.

3.2.1. KLM

The K_L^0 and muon detector (KLM) is the outermost and therefore largest subdetector of Belle II. It detects long-lived neutral kaons, which permeate the other subdetectors unnoticed. Muons leave traces in the inner tracking detectors, like e.g. electrons. However, electrons are stopped in the ECL where they create showers, while muons reach the KLM and eventually escape the detector volume. The KLM is divided into a barrel region, a forward and a backward endcap. It is constructed as a stack of alternating sensor and iron layers, the latter serving also as flux return for the solenoid.

Traversing K_L^0 create hadronic showers in the iron plates, which are detected in the sensor layers. There are 15 sensor layers in the barrel region, 14 in the forward endcap, and 12 in the backward endcap. Resistive plate chambers (RPCs) [77] from Belle are reused in the outer barrel region. To cope with the higher hit rates of SuperKEKB, the RPCs in the inner two barrel layers and in the endcaps are replaced by new scintillator strips with wavelength shifting (WLS) fibers and silicon photomultiplier (SiPM) readout [78]. The width of a strip is 40 mm. In total, there are about 38 000 readout channels, of which half are for the new scintillators and half for the reused RPCs [79].

3.2.2. Solenoid

Inside of the KLM, a superconducting solenoid provides a magnetic field of 1.5 T aligned with the z-axis. The curvature of charged particles crossing the magnetic field is used to infer their charge and momenta.

3.2.3. ECL

Inside the solenoid structure lies the electromagnetic calorimeter (ECL) [72]. Like the KLM, it is divided into a barrel region and a forward and a backward endcap. The ECL detects photons from neutral decay particles of the B mesons (like π^0) with a high resolution. It reuses the 8736 thallium-doped cesium iodide (CsI(Tl)) scintillation

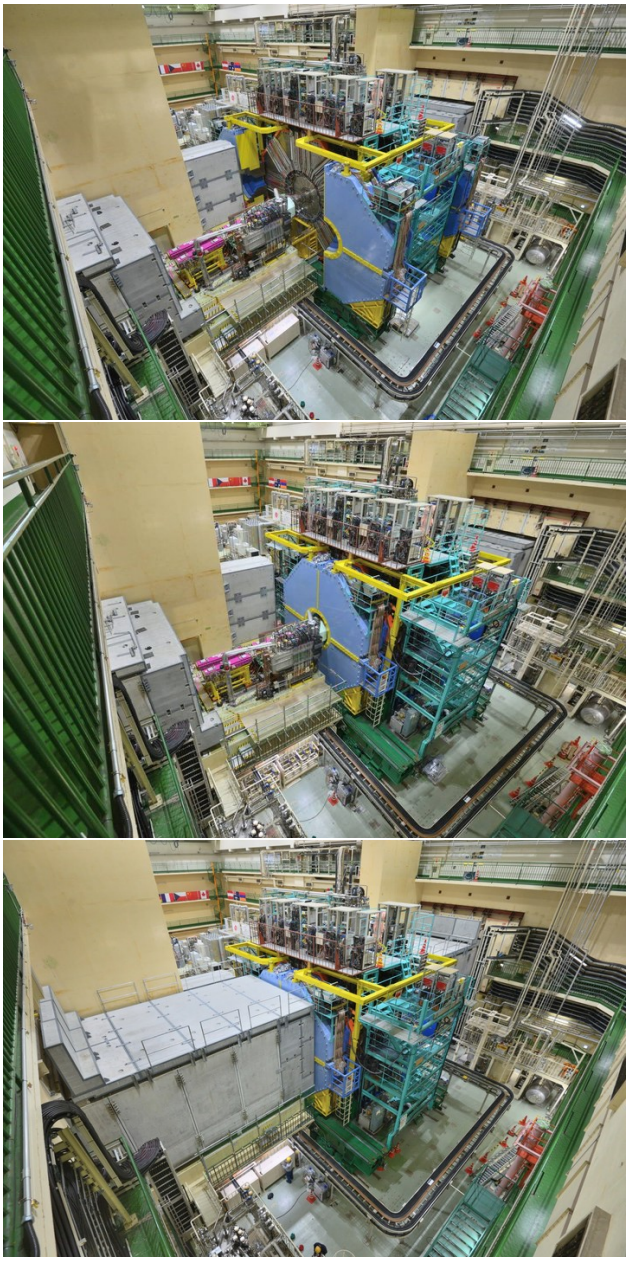


Figure 3.10.: Closing of the end yokes and the concrete shielding around the Belle II detector and the beam pipe [76]. Multiple racks for electronics and further service structures are installed on top of Belle. Top: End yokes open. Middle: End yokes closed. Bottom: Concrete shield closed.

crystals from Belle with a cross section of 6 x 6 cm^2 and a length of 30 cm [80]. They are arranged pointing towards the IP. The tasks of the ECL include detection of neutral particles, determination of photon energies, particle identification (by pulse shape discrimination based on particle specific energy deposition) and providing input signals for the trigger system. In addition, the ECL uses Bahbah scattering to measure the luminosity online as well as offline. The readout system was completely reworked for the upgrade.

3.2.4. ARICH

The Aerogel Ring-Imaging Cherenkov detector (ARICH) [81] is a newly developed part of the particle identification system of Belle II. It is installed in forward direction, in front of the ECL forward endcap. ARICH can separate pions from kaons up to a momentum of 4 GeV/c. Cherenkov photons emitted by charged particles in the two-layer silica aerogel radiator are detected by 420 Hybrid Avalanche Photo Detectors (HAPDs). Through the measurement of the emission angle and by taking also the momentum measurement of the tracking system into account, it is possible to determine the mass of the particles.

3.2.5. TOP

The time of propagation (TOP) detector [82] is the second particle identification device. It consists of 16 modules in the barrel region arranged cylindrically around the tracking detectors. The sensor material are 2 cm thick silica bars with a length of about 2.5 m. Particles crossing the bars emit Cherenkov photons, which are reflected inside the bar until they reach the readout photomultipliers on the backward side of the detector. The propagation time of the emitted photons depends on the Cherenkov angle. In combination with the measurement of the time until the particle reaches the detector (time of flight), this allows a reliable discrimination between kaons and pions. In total, TOP has 8192 photomultiplier channels and uses the dedicated IRSX ASIC for sampling and data handling.

3.2.6. CDC

The Central Drift Chamber (CDC) [72] is a gas-filled wire chamber inside the particle identification detectors TOP and ARICH. It consists of a total number of 42 240 aluminum field wires with a thickness of 126 µm and 14 336 gold-plated tungsten sense wires with a thickness of 30 µm. The wires are arranged in 9 super layers with

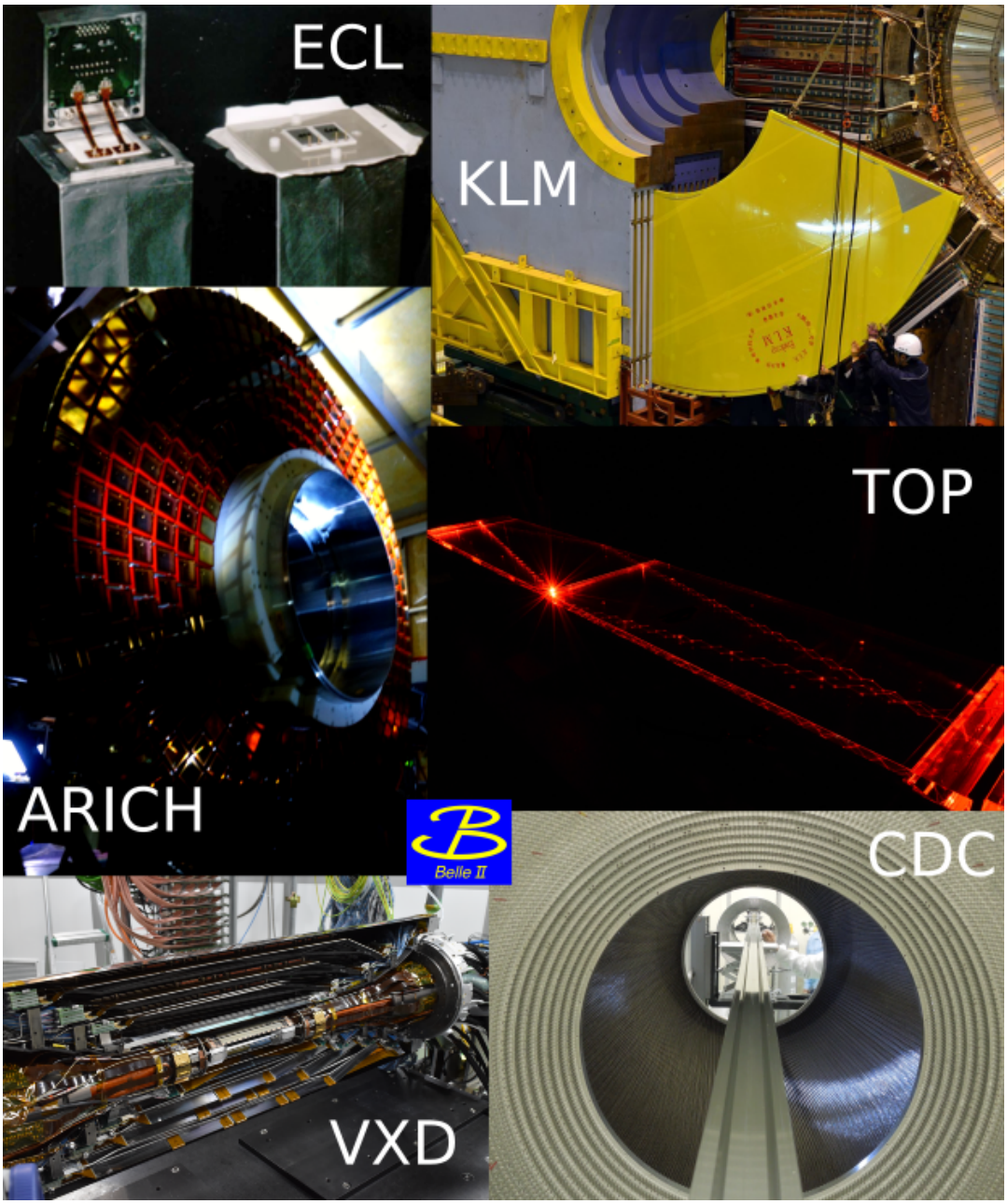


Figure 3.11.: Collage of Belle II subdetectors. The seven subdetectors of the Belle II detector are from outside to inside: KLM (new forward endcap module) [83], ECL (photomultipliers on scintillator crystal) [84], ARICH (matrix of aerogel blocks) [85], TOP (red laser light in quartz bar) [86], CDC (look inside the wire chamber) [87], and VXD (i.e. marriage of SVD and PXD) [88].

alternating axial orientation (parallel to the z-axis) and stereo orientation with an angle of a few mrad. The sense wires are biased with a high voltage of about 2 kV relative to the field wires, which creates a drift potential. The detector volume is filled with a gas mixture of helium and ethane (50:50). Charged particles crossing the detector volume ionize gas molecules and the free electrons drift to the sense wires. The high bias voltage leads to an avalanche ionization and the resulting currents are measured at the sense wires with an FPGA-based readout system at a 1 ns time resolution. By taking also the drift times into account, the CDC reaches a spatial resolution of 120 µm.

The CDC covers three important tasks. It allows to reconstruct the tracks of charged particles and through the curvature of their trajectories the measurement of their momenta. It also provides particle identification information by the measurement of energy loss in the gas mixture. This is especially important for low momentum particles which do not reach the outer particle identification system. Finally, it is the sole input for the track trigger as the readout of the vertex detector is not fast enough for this task.

3.2.7. VXD: SVD and PXD

In order to increase the spatial resolution close to the IP, a transition to silicon semiconductor detectors is made. At the core of Belle II lies the Vertex Detector (VXD), which is a combination of the four-layer Silicon Vertex Detector (SVD) [89] and the two-layer Pixel Vertex Detector (PXD).

The SVD is an upgrade of the vertex detector used at Belle. It consists of double-sided silicon strip detector (DSSD) modules with p and n strips on opposite sides of an about 300 µm thick n-type silicon bulk. A traversing ionizing particle creates electron-hole pairs in the bulk, which are separated by the applied biasing. The charge carriers arrive at the closest strip and the signal can be measured. The strip orientation is almost perpendicular between p and n strips, so that the signal of one strip on each side determines the crossing point of the ionizing particle.

Taking the two innermost layers of the PXD into account, the four layers of the SVD are counted as 3, 4, 5 and 6. They are installed at radii of 38 mm, 80 mm, 104 mm and 135 mm around the IP. Layers 4, 5 and 6 have a slanted orientation of the modules in forward direction to improve acceptance and precision for forward boosted particles. The SVD has in total 223 744 channels which are read out by so-called APV25 chips. These provide a short pulse shaping time of 50 ns, pipeline readout for dead time-free operation and high radiation tolerance [80].

The innermost subdetector is the PXD. It is an entirely new development required for the high particle density close to the IP. The luminosity increase of SuperKEKB results in a higher event rate, increased background levels and at the same time a reduction of vertex separation for the B mesons due to the reduced boost. The small diameter of the beam pipe allows the innermost detector layer to sit closer to the IP, which further increases the density of crossing particles. This makes the implementation of a pixel detector inevitable. The increase in particle density towards the center of the Belle II detector is mirrored by the increase of readout channel density of the subdetectors (see fig. 3.12). The details of the PXD are presented in the next chapter.

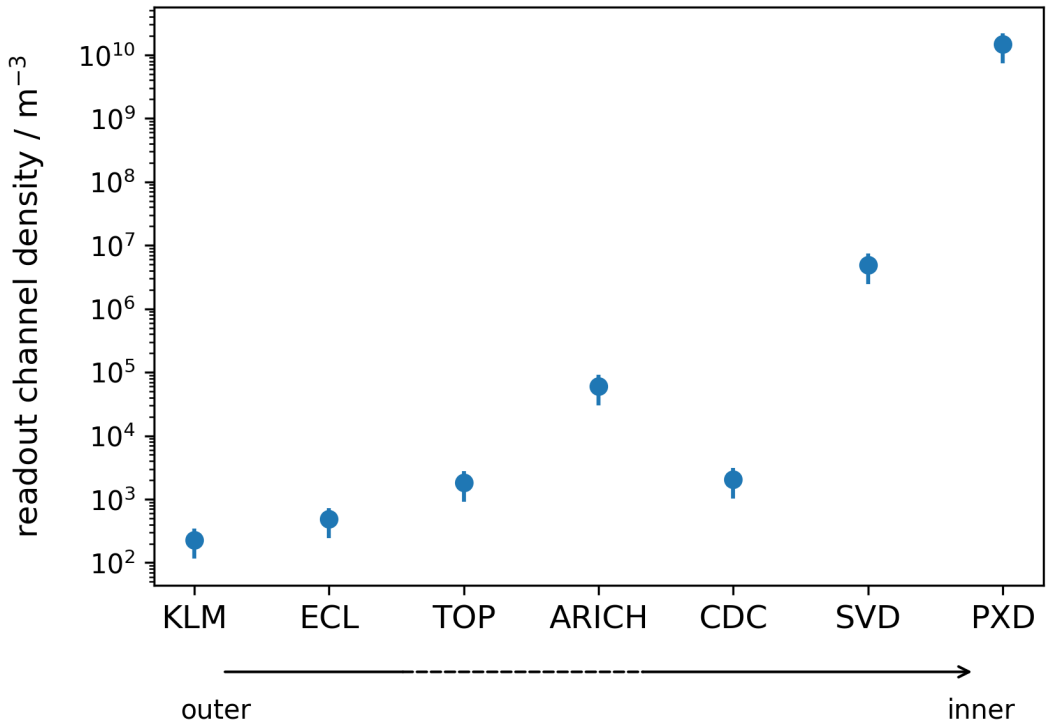


Figure 3.12.: Readout channel density of Belle II subdetectors. The readout channel density grows exponentially from outside to inside just as the density of crossing particles emerging from the IP. The volume of the detectors was roughly estimated from the technical drawing of the Belle II detector.

4. Pixel Vertex Detector

The significant luminosity increase of SuperKEKB is mainly achieved by the implementation of the nano-beam scheme and the increase of the beam currents. Both measures lead to an increase of the collision and background rates and thus lead to higher particle densities in the detector. This is particularly relevant for the innermost subdetector, where this effect is amplified by the smaller radius of the first detector layer. At the same time, the reduced boost factor leads to a smaller separation of the decay vertices.

In summary, the main requirements for the inner vertex detector are a high vertex resolution, a high granularity (reducing occupancy) and a high radiation tolerance, along with a low material budget (reducing multiple scattering), low power consumption (no need for bulky cooling structures in the acceptance region), and not least a high detection efficiency. The new PXD (see fig. 4.1) meets these criteria and achieves an impact parameter resolution of about 15 µm with a material budget of only 0.2 % of the radiation length per layer [72].

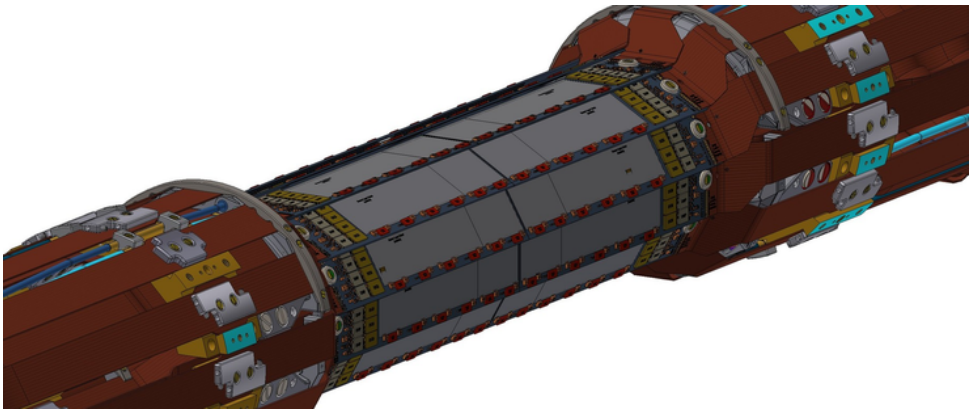


Figure 4.1.: Pixel Vertex Detector for the Belle II experiment [73]. The PXD consists of 40 modules arranged in two layers that enclose the beam pipe at the IP. Data and power lines are carried out of the inner detector volume by flat cables (brown color). Support and cooling structures as well as readout ASICs and cables are placed outside the acceptance region.

An overview of the main design features of the PXD is presented in this chapter, followed by a description of the DEPFET technology, the module concept with inte-

grated electronics and the services required to operate the PXD. The first version of the PXD installed at Belle II had a reduced configuration with an incomplete second layer (see chapter 8 for details).

The PXD is a silicon pixel detector for precise vertex measurements at the Belle II experiment. It consists of 40 monolithic silicon modules that are arranged cylindrically in two layers around the beam pipe at the IP. The radii of 14 mm and 22 mm place the detector as close as possible to the IP to optimize the tracking capability. The windmill structure of the overlapping modules ensures a full coverage of the azimuthal angle ϕ (around the beam pipe). Each pair of modules along the beam pipe is glued together at the short side to form self-supporting ladders spanning a distance of about 9 cm for the inner layer and about 12 cm for the outer layer with active detector material. These dimensions match the required acceptance of $17° < \theta < 150°$ in the polar angle. The total length of the silicon part of the PXD is 17 cm. Power, control and data lines are routed to the innermost detector volume by flexible multi-layer polyimide printed circuit boards (called Kapton cables) with a length of about 50 cm.

The PXD uses the DEpleted P-channel Field Effect Transistor (DEPFET) technology. The active DEPFET pixels amplify the signal from an ionizing particle by converting the stored signal charge into a measurable current. The pixel size for the PXD varies from 50 µm × 55 µm to 50 µm × 85 µm with a thickness of only 75 µm. The readout time for a DEPFET pixel is approximately 100 ns. The PXD provides a total number of 7 680 000 DEPFET pixels. For steering and readout of DEPFET pixels Application-Specific Integrated Circuits (ASICs) are required which are placed on the PXD modules as front-end electronics. By parallelizing, a readout frequency of 50 kHz is achieved for the entire PXD detector, which corresponds to an integration time of 20 µs.

4.1. DEPFET technology

The DEPFET technology was first proposed by Kemmer and Lutz in 1987 [90, 91] and experimentally confirmed three years later [92]. The starting point is a standard Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) on a high resistivity n-doped silicon bulk. The key feature is an additional internal gate below the external MOSFET gate that collects electrons generated in the silicon bulk. The stored charge modulates the conductivity of the MOSFET. This concept combines signal detection and amplification in one step. The characteristics of the DEPFET pixels are highly dependent on the design and layout and can be optimized for the specific task. Several designs have been developed, resulting in three devices that are currently part of

particle physics and astrophysics experiments[1] [93]. This section describes the basic concepts of the DEPFET technology and provides an overview of the PXD pixel design. Then the wafer processing steps for the fabrication of DEPFET modules for the PXD are presented.

4.1.1. Operating principle of DEPFET pixels

Following a p-type MOSFET structure, a DEPFET pixel has a p-doped **source** implant, an isolated **external gate** contact and a p-doped **drain** implant on the top surface. A negative voltage at the external gate causes a conductive **p-channel** to form below the external gate. By pushing the electrons away, the channel gets populated with holes that provide a conductive connection between source and drain. The key feature for DEPFET pixels is an additional deep n-implant below the external gate. Together with the depletion of the silicon bulk, it forms a potential minimum for electrons. Charge collected in this **internal gate** introduces mirror charge into the p-channel. These additional charge carriers increase the conductivity of the channel. The change in current can be measured to detect a passing ionizing particle. A three-dimensional layout sketch and the equivalent circuit are shown in fig. 4.2.

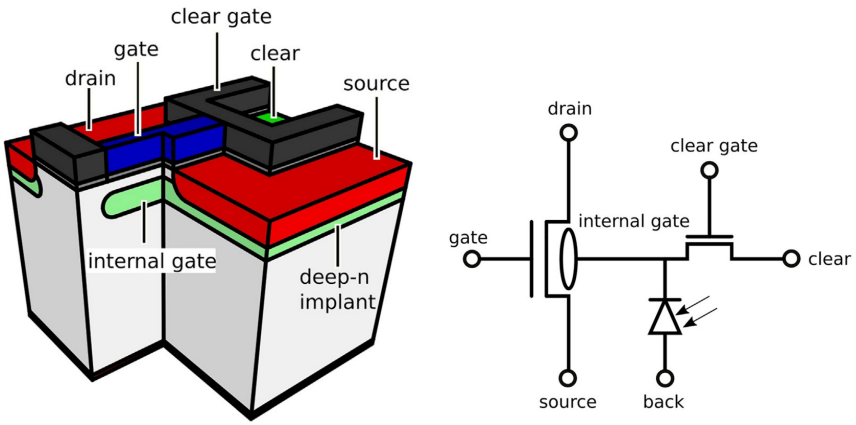


Figure 4.2.: DEPFET pixel [93]. Left: The 3D sketch of a DEPFET pixel shows the transistor structures on the top surface with additional deep implantations and the silicon bulk as sensitive detector volume below (not to scale). Right: The equivalent circuit of the DEPFET places the individual structures in relation to each other. The signal detection is based on the modulation of the current through the MOSFET by the charge stored in the internal gate, which can be discharged again by the clear structures.

[1] PXD for Belle II, Mercury Imaging X-ray Spectrometer (MIXS) aboard the BepiColombo Spacecraft and Advanced Telescope for High ENergy Astrophysics (ATHENA)

The drain current I_{drain} depends primarily on the external gate voltage. The transistor needs to be activated by a sufficiently low gate voltage (about $-2\,\mathrm{V}$ for unirradiated pixels). The voltage difference between source and drain causes a current through the p-channel, which can be assumed to be the sum of a **pedestal current** I_{ped}, which represents the case of an empty internal gate, and a **signal current** I_{sig}, which is caused by the charge stored in the internal gate.

$$I_{drain} = I_{ped} + I_{sig} \tag{4.1}$$

The signal current I_{sig} is proportional to the signal charge Q_{sig} stored in the internal gate. The gain g_q describes the conversion of the signal charge into the current. It can be described as the change in drain current per number of signal electrons.

$$I_{sig} = g_q Q_{sig} \qquad \text{with} \qquad g_q = \frac{\Delta I_{drain}}{N_{e,sig}} \tag{4.2}$$

The value of g_q depends on several factors, such as the geometry of the p-channel, and can be expressed as [94]:

$$g_q = fk\sqrt{\frac{2\mu I_{drain}}{WL^3 C_{ox}}} \tag{4.3}$$

where f and k are a parasitic influence and a voltage coupling correction factor, μ is the mobility of holes in the p-channel, W and L are the width and length of the p-channel and C_{ox} is the capacitance of the gate oxide [94]. The DEPFET pixels for PXD achieve a g_q factor of about $750\,\mathrm{pA/e}$ [72] corresponding to a current rise of about $4.5\,\mu\mathrm{A}$ for a minimum ionizing particle, as expected from the particle collisions at the IP.

To separate the electron-hole pairs that are created by ionizing particles traversing the silicon bulk, a depletion voltage (hv) of about $-70\,\mathrm{V}$ is applied to the p^+ backside contact via a punch-through mechanism [95]. The silicon bulk is fully depleted, resulting in a potential distribution that causes the holes to drift to the backside contact, where they are drained. The electrons, on the other hand, drift to the internal gate, where they are collected (see fig. 4.3).

A clear mechanism is implemented to remove the stored signal electrons and those from other sources, such as thermal excitation or leakage currents. The clear contact allows a positive voltage (about $19\,\mathrm{V}$) to be applied to remove the electrons from the internal gate. The capacitively coupled clear-gate assists in forming the connection between the internal gate and the clear contact, thereby enhancing the clearing process. A deep p-well below the clear implant ensures that the internal gate

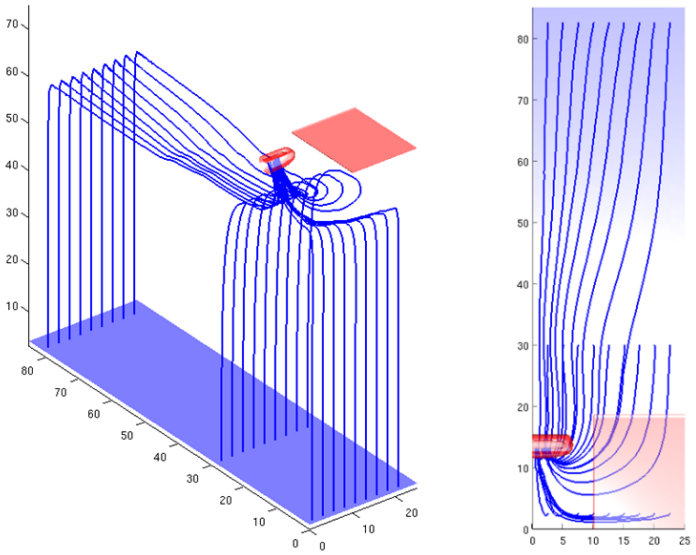


Figure 4.3.: Electron drift trajectories for the charge collection process in a DEPFET pixel [51]. The generated electrons first drift upwards and then sideways to the internal gate.

remains the most attractive potential for signal electrons during charge collection mode.

Readout and signal detection for the PXD follows the following scheme. During the **charge collection** phase, the external gate is off and only static voltages are applied to guide any electrons that may occur to the internal gate. The pixel consumes almost no power during this phase. The *charge collection time* or *integration time* for the PXD is 20 µs due to the matrix and module layout described below.

The pixel is read out in the **sampling** phase by activating the external gate. The pedestal value of a pixel is determined by repeated measurements of the drain current for an empty internal gate. The mean value of these measurements is stored in the readout electronics. The signal current of an actual measurement can be determined by subtracting the previously recorded pedestal value from the present drain current.

After sampling, the internal gate is **cleared** by applying the clear voltage to the clear contact. A conductive channel forms between the internal gate and the clear contact, and the stored charges are pulled out of the internal gate. Sampling and clearing together take about 100 ns. Then the pixel is sensitive again and starts with the next charge collection phase.

The DEPFET technology combines several advantages. A key features is the internal signal amplification combined with very low noise at room temperature, which results in an excellent signal-to-noise ratio (SNR) of 30 to 40 [96]. Furthermore, the small thickness and the low power consumption allow a detector design with a very small material budget [97]. The concept of charge storage in the internal gate and the non-destructive readout opens the possibility for readout methods that further reduce the noise. However, these are not used for the PXD and are not part of this discussion.

For the PXD the DEPFET pixels are arranged in a fourfold pattern to create a base unit that can be stitched together to form large pixel matrices (see fig. 4.4). The small thickness of the active DEPFET sensors, however, requires a frame-like support structure for the thin pixel matrix. A new processing technique has been developed [98] to achieve a self-supporting all-silicon structure without the need for additional bulky support structures in the acceptance region. This is illustrated in the wafer production description below.

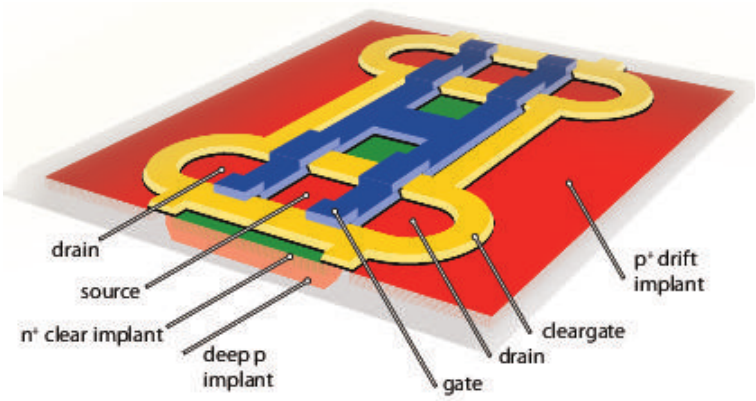


Figure 4.4.: DEPFET pixel layout for PXD module matrix. [99]. The base unit is a fourfold design of DEPFET pixels in form of two double cells. Each pixel has its own drain implant. The double cells share a common source implant. The unit of four pixels share gate, clear and clear-gate structures. An extended pixel matrix is achieved by repeating the base unit in two dimensions. The result is a column and row structure such as for a matrix.

4.1.2. Wafer processing

A new customized thinning technology for ultra-thin fully depleted sensors with electrically active backside has been developed at the Max Planck Halbleiterlabor (HLL) [98]. Direct wafer bonding in combination with deep anisotropic etching allows DEPFET pixel thicknesses down to 50 µm [100]. A thicker sensor, and thus more material, results in more deposited charge and therefore a higher signal, which improves

the signal-to-noise ratio. On the downside, more material also increases multiple scattering, deflecting charged particles and distorting the vertex reconstruction. In addition, the distribution of the generated charge also increases laterally in a thicker sensor. This initially blurs the information about the crossing point, but can eventually lead to charge sharing between pixels and improved resolution. For the PXD modules an optimal thickness of 75 µm was found in simulations [101].

The production process of the ultra-thin sensors is based on wafer bonding, thinning and etching as shown in fig. 4.5. First, the backside p^+ implantation of the top wafer is applied. Then the top wafer and the handle wafer are oxidized and directly bonded together by high temperature annealing. The backside implants and the silicon oxide are now buried in between the two wafers. The next step is the thinning of the top wafer to the desired thickness by grinding and polishing. The resulting wafer stack can be treated as a conventional wafer during the subsequent implantation of the DEPFET pixels, polysilicon and metal structures on the top wafer. After passivation of the top layer, the bottom handle wafer is selectively etched away. The silicon oxide on the back side of the top wafer stops the etching process. This results in the desired thickness of 75 µm for the active pixel region and a stable support frame with the thickness of the handle wafer (450 µm) plus the top wafer (in total 525 µm)[2]. To further reduce the material budget in the acceptance region, additional cavities are etched into the support frame along the balcony to form a support grid. At the far end of the module, three grooves are etched into the support frame, to accommodate ceramic stiffeners that strengthen the gluing joint between two modules.

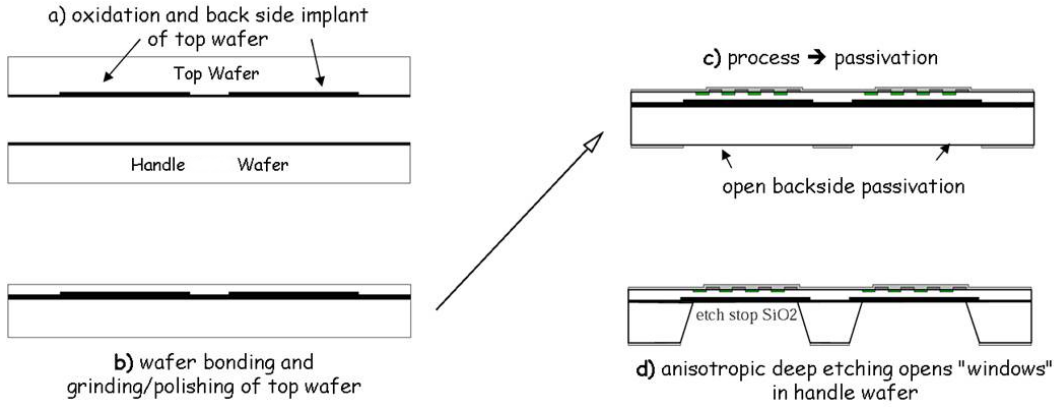


Figure 4.5.: Thinning technology for PXD wafers at the MPI Semiconductor Lab of the MPG [100]. The individual processing steps are explained in the text.

The PXD modules are produced on standard 150 mm silicon wafers ("6-inch wafers"). The wafer layout accommodates all four different module geometries and reflects the

[2]In the later production of modules for the successor detector PXD2 a thinner handle wafer was used resulting in a total thickness of 450 µm.

higher demand for outer modules (see fig. 4.6): Each wafer contains two outer forward (OF) modules and two outer backward (OB) modules, as well as one inner forward (IF) module and one inner backward (IB) module.

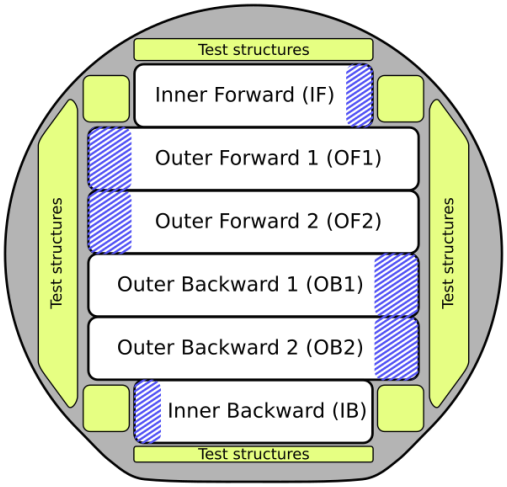


Figure 4.6.: PXD wafer layout. Around the six modules and their fan-out (striped blue) further test structures like small DEPFET matrices are placed to make use of the remaining space.

The PXD wafer production process is divided into three phases, including 19 lithography steps and several inspection steps in between. Phase I involves the implantation of the DEPFET structures on the thinned top wafer. Two layers of polysilicon are added to form the contacts for e.g. external gate and clear gate. In phase II, the first and second aluminum layers are added to form the circuit interconnections within the module. A first benzocyclobutene polymer (BCB) passivation layer is applied. Phase III adds the third and final metal layer. This time, copper is used to create the solder bump pads for the ASIC and surface-mount device (SMD) assembly. Finally, the applied structures are passivated with a second BCB layer and the sensitive area is thinned by etching the handle wafer. A sketch of the resulting wafer structure is shown in fig. 4.7. After the final production step, the bare modules are still part of the wafer (see fig. 4.8). To obtain individual modules, they are cut out with a water-guided laser.

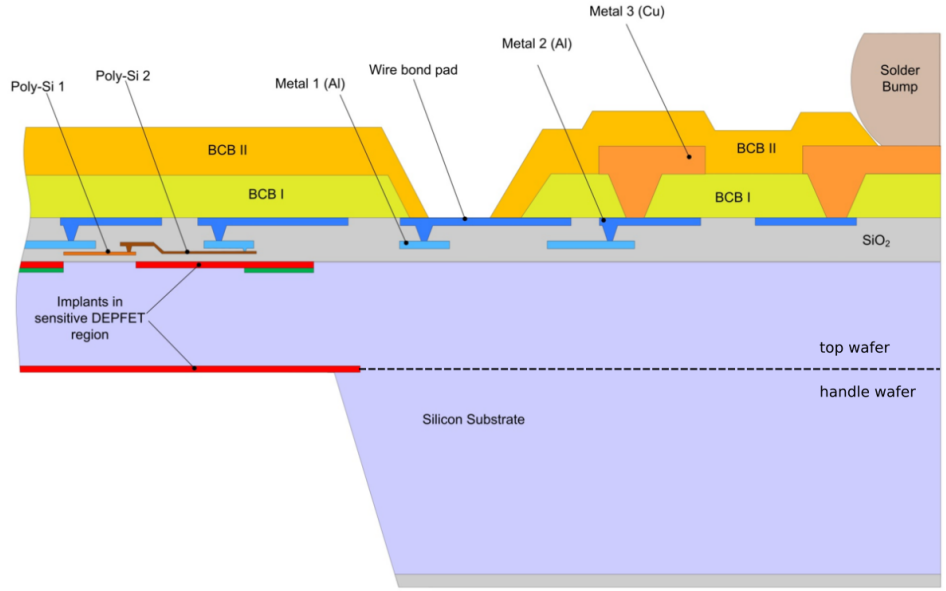


Figure 4.7.: Structure of PXD9 wafer technology [102]. The DEPFET implants are integrated in the top wafer. The module circuit is applied on top, comprising two polysilicon layers (e.g. gate contacts), two aluminium layers (e.g. gate and drain lines and wire bond pads) and one copper layer (e.g. ASIC bump bond pads). Several dielectric layers of silicon dioxide (SO_2) are used to isolate the metal layers and to obtain the required circuit stack. Two layers of BCB passivation protect the processed structures. Backside implants are applied before wafer bonding and later exposed again by etching after finishing the top side.

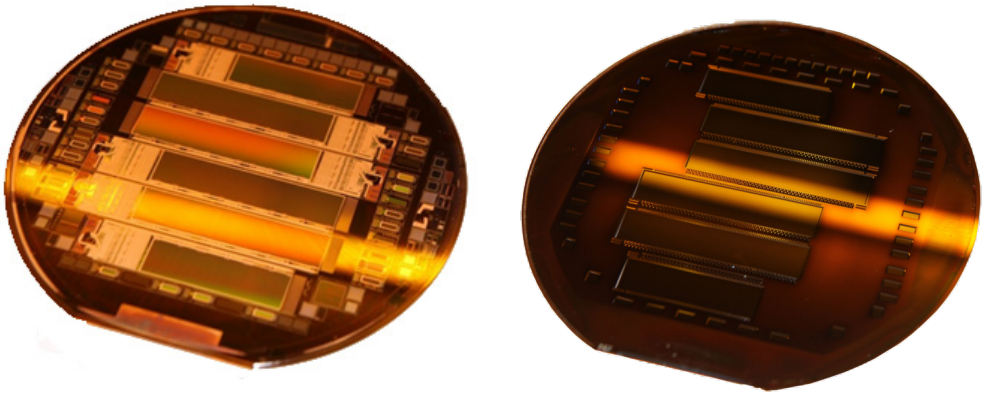


Figure 4.8.: PXD wafer before cutting [103]. Left: On the top side of the wafer the two smaller inner modules and the four larger outer modules can be identified with their matrices and corresponding circuits on the balcony and on the end-of-stave. Right: On the back side only the contours of the thinned regions are visible: the large sensitive areas of the modules and the small areas of the test matrices around the modules.

4.2. Module layout

A PXD module consists of a large single-die silicon base. The sensitive area is a 75 µm thin DEPFET pixel matrix. The matrix is held by a thicker[3] support frame with a 2.3 mm wide balcony along one of the long sides and a 23 mm long end-of-stave (EOS) (see fig. 4.9). Balcony and EOS provide landing pads for the required control and readout ASICs, passive electronic components and for the Kapton cable attachment. The connection lines between the components are routed on the silicon modules in three metal layers during wafer processing. The self-supporting modules need no additional support structures. After assembly of all components (see section 7.2), a module is the smallest unit of the PXD that can be operated on its own (see chapter 5). Functional tests and optimization of operation variables (see section 7.4) are performed on module level.

The matrix is a geometrical arrangement of 250 × 768 DEPFET pixels, 192 000 pixels per module in total. The width of all pixels is 50 µm, the length, however, varies depending on the position of the pixel within the matrix and between inner and outer modules. In the inner layer, the pixels in the 256 rows farthest away from the EOS are 55 µm long, the pixels in the remaining 512 rows are 60 µm long. For the outer layer, the lengths of the pixels are 70 µm and 85 µm, respectively. The shorter pixels are closer to the IP, counteracting the effect of a more perpendicular incident angle that results in less charge sharing and therefore lower resolution.

The readout scheme of the DEPFET matrix follows a fourfold "rolling shutter" mode. Four consecutive geometrical rows are read out at once. One gate (clear) line output of a Switcher is always connected to the corresponding gate (clear) contacts of four geometrical DEPFET rows. These four rows are electrically treated as one unit, which is therefore called *electrical row* or simply *gate line*. As result, always 1 000 pixels are active and read out at the same time and four *drain lines* (or *electrical columns*) for each geometrical pixel column are required. When the readout and clearing process for one electrical row is completed, the next electrical row (again four geometrical rows) is switched on. This pattern continues throughout the entire matrix and starts over again when the end of the matrix is reached. In total, the matrix is controlled by 192 gate lines (and clear lines) and the DEPFET currents are delivered through 1 000 drain lines. The readout of one electrical row takes about 100 ns resulting in a readout time of 20 µs for the entire matrix or a readout frequency of 50 kHz.

The difference between the geometrical arrangement of the pixels and their electrical connections results in different *mappings* of the recorded data, which have to be

[3] The support frame has a thickness of 525 µm or 450 µm depending on the thickness of the handle wafer used during production (see section 4.1.2).

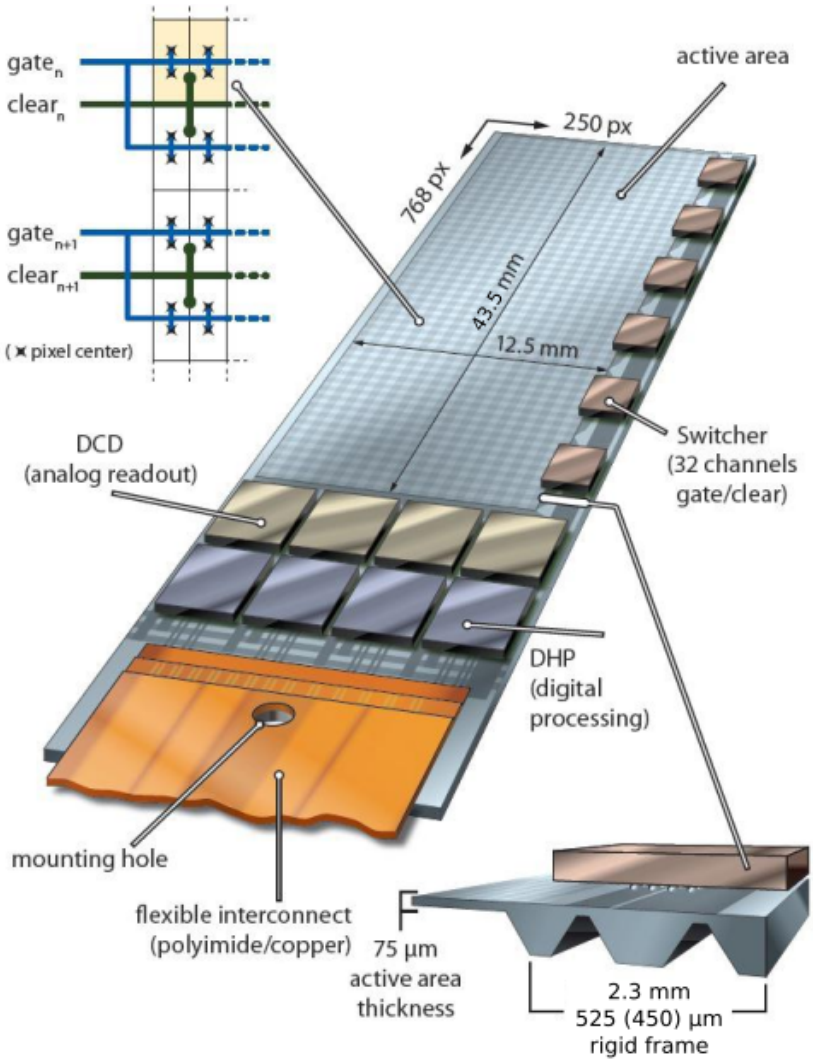


Figure 4.9.: PXD module sketch [104]. The PXD module consists of a large DEPFET pixel matrix which is surrounded by the required electronics. The support frame around the matrix provides mechanical stability for assembly and handling. A balcony provides space for the ASICs that control the gate and clear lines. Grooves in the rigid frame minimize the material budget in the acceptance region (lower right). The readout ASICs are placed on the EOS next to a single mounting hole and the connections to the Kapton cable. The fourfold connection of gate and clear lines to the geometrical pixel rows is illustrated in the upper left.

considered during data analysis. The geometrical representation (250 × 768 pixels) represents the physical geometry of the matrix, while the electrical mapping (192 gates × 1000 drains) helps to visualize issues in the matrix, such as broken drains or "dead" gates (see later in chapter 7 and chapter 9).

The PXD modules are glued together on the short side to form ladders (see chapter 8), which requires four different module layouts: IF, IB, OF and OB ((see fig. 4.10)). The layouts differ in the lengths of the pixels and therefore in the lengths of the matrices (inner vs. outer), but also the mechanical configuration differs in the placement of the balcony (forward vs. backward) with influence on the configuration chain (see below).

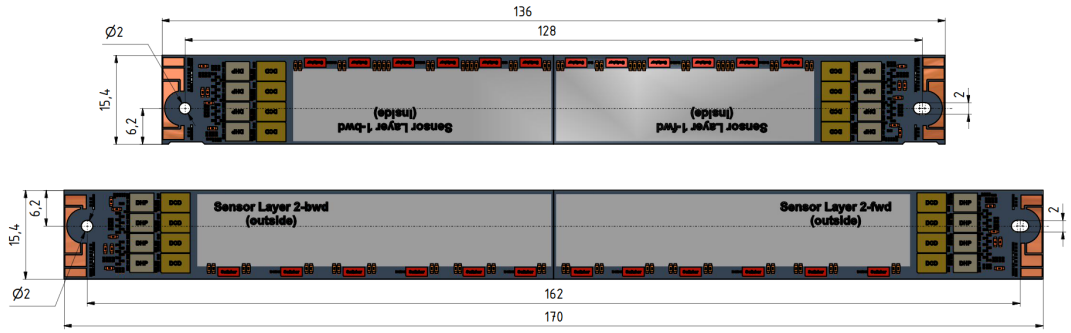


Figure 4.10.: PXD ladders [105]. A forward and a backward module of the same layer form a ladder, which spans the entire acceptance region between the mounting points without further support structures.

4.3. Front-end electronics

Three types of ASICs are bump-bonded to the PXD modules for the control and readout of the DEPFET pixels. The ASIC types and their main purposes are briefly discussed in this section. The details of their functionalities and the corresponding optimization strategies are presented in section 7.4.

4.3.1. Switcher

The Switchers are placed on the balcony to control the gate and clear voltages for the DEPFET pixels. They control the readout and clearing process through a voltage swing between gate-on/gate-off potential and clear-on/clear-off potential on the corresponding lines. One Switcher has 32 drivers for gate and clear lines each, thus,

can control 32 electrical rows (128 geometrical rows). Six Switchers per module are required to operate the entire matrix. The Switchers are designed to be arranged in a daisy-chain. The control signals are shifted through the chain realizing the rolling-shutter readout mode. The sequence of control signals (*Switcher sequence*) can be adjusted to optimize the readout process [51].

4.3.2. Drain Current Digitizer

The Drain Current Digitizers (DCDs) are connected to the drain lines reaching the EOS. They sample the currents from the DEPFET pixels and convert the analog signal into a digital reading. One DCD has 256 inputs, each providing an 8-bit Analog-to-Digital Converter (ADC) with a dynamic range of up to 31 µA depending on the gain settings. The output is a value of 0 to 255 in arbitrary Analog-to-Digital Unit (ADU). Only 250 inputs per DCD are connected to the matrix drain lines, while the remaining 6 inputs stay unconnected at a floating potential. Four DCDs per module are required to cover the 1 000 drain lines of the matrix. The DCDs provide current sources and sinks to shift the input signal into the dynamic range. An Analog Common Mode Correction (ACMC) and a *2-bit offest* correction on pixel basis is available to compress the spread of the pixel currents.

4.3.3. Data Handling Processor

A Data Handling Processor (DHP) is placed behind each DCD on the EOS. The combination of DCD and DHP is also called *ASIC pair*. The DHP receives the reading of each pixel from the DCD, provides a Digital Common Mode Correction (DCMC) and performs a data reduction by zero-suppression. For this purpose, a pedestal map is stored in a memory of the DHP and subtracted from the readings. The result is compared against an adjustable threshold. Only values above the threshold a further processed. Each DHP provides a high-speed data link to the back-end electronics and sends the data upon receipt of a trigger signal. Also full frames (without zero-suppression) can be transmitted, though with limited frequency due to the available bandwidth. The values for the *2-bit offset* compression are stored in a memory and transmitted to the DCD synchronously to the data sampling. The DHPs provide the on-module control signals for the other ASICs, such as the fast DCD clock and synchronization signals. The *Switcher sequence* is stored in a configurable memory and transmitted to the Switcher daisy-chain by the DHP closest to the Switchers.

Further specification about the three ASIC types are listed in table 4.1.

Table 4.1.: ASIC specifications.

ASIC	**DHP**	**DCD**	**Switcher**
Technology	TSMC 65 nm	UMC 180 nm	AMS 180 nm
Size	3280×4200 µm^2	3240×5100 µm^2	1470×3627 µm^2
Thickness	350 µm	350 µm	300 µm
Pins	296	431	96
Supply voltage	1.2 V	1.8 V	1.8 V

The slow control system uses the Joint Test Action Group (JTAG) protocol to read and write the configuration shift registers of the ASICs. The modular design of the ASICs allow to configure the number of ASICs in the JTAG chain. The JTAG implementation allows the usage of boundary-scan tests of the on-module connections for quality assurance during production [106].

4.4. Data acquisition system

The standard data acquisition (DAQ) system of the PXD is called Data Handling Hub (DHH) [107]. It consists of Field Programmable Gate Array (FPGA) based modules which are connected to a custom made Advanced Telecommunications Computing Architecture (ATCA) carrier board. One Data Handling Engine (DHE) per PXD module receives the high-speed data link, which uses the Aurora link protocol. Five DHEs are connected to one Data Handling Concentrator (DHC), which combines the forwarded data to create events. The DHC sends the data to the ONline SElection Node (ONSEN) as the next step in the Belle II DAQ chain [56, 108, 109]. The data of the subdetectors is then merged and analyzed by the Belle II Analysis Software Framework (basf2) on the event builders. The DHH sends a copy of the data also to the PXD LocalDAQ (see section 5.3.2), which is used for monitoring.

The DHH receives the trigger and clock signals from the Belle II trigger and time distribution system (B2TT). They are forwared by the Data Handling Integrator (DHI) which covers the communication to the modules. Besides the clock and trigger signals, it also sends the slow control signals (JTAG configuration signals) to the attached PXD modules. Five DHEs, one DHC and one DHI build a complete DHH system (see fig. 4.11). For the entire PXD, eight DHH systems are required. On the other side, for a test setup with just one PXD module, a single DHE is sufficient. A special firmware is available, which enables the DHE to generate the control signals and to send the data directly to the LocalDAQ.

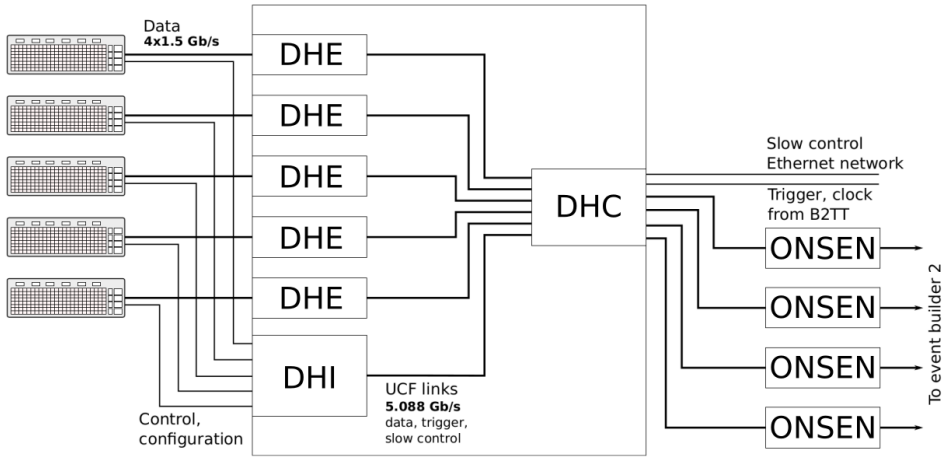


Figure 4.11.: DHH system [110].

Important frequencies on the back-end and front-end electronics are:

- The global reference clock (GCK) has a frequency of 76.33 MHz and is provided by the Belle II experiment. This is the main digital clock for the DHPs.
- The DCD clock results from the multiplication of the GCK with a factor 4 (about 305 MHz).
- The high-speed data links reach a transmission rate of 1.5 Gbps (factor 20).
- The frame frequency, which can be calculated as:

  $$\text{GCK} \times 4\,(\text{DCD clock}) \div 32\,(\text{DCD clock cycles per gate}) \div 192\,(\text{gates}) \approx 49.7\,\text{kHz}$$

  This corresponds to about 20 µs integration time and two turns of the particle bunches in the SuperKEKB accelerator rings.
- The maximal trigger frequency for the Belle II detector DAQ is 30 kHz.

4.5. Services

The **DockBoxes** are the interface between the highly integrated module cables (PatchPanel cables) with a length of less than 2 m and the outer cables for the long distance of about 15 m to the back-end electronics in the E-Hut or on top of Belle. The DockBox PCB accepts the Infiniband, Glenair and Ethernet connectors from the PatchPanel

cable and transfers them to optical data links, two rigid power cables and a Camera-link cable for the slow control and trigger lines (see fig. 4.12). The DockBoxes are required only in the experiment due to space limitations in Belle II detector volume. A simpler structure is used in the single PXD module setups in the laboratory (see chapter 5).

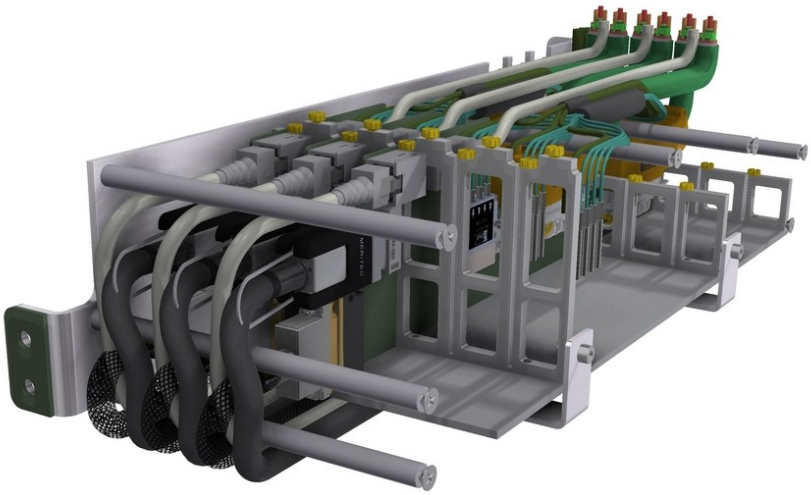


Figure 4.12.: DockBox with partially installed DockBox PCBs and cables [105]. The DockBoxes are installed within the Belle II detector volume strictly limiting the available space. Each DockBox houses five PCBs and therefore serves for five PXD modules.

A **multichannel Power Supply for PXD** [111] provides 23 voltages and two ground potentials (see table 4.2), which are required for the module operation. Each PXD module is powered by one PXD Power Supply. The PXD Power Supplies feature low noise, voltage sensing and settable current limits. The power up and power down sequences are programmed as state machines with intermediate safety checks. A overvoltage protection (OVP) board is installed, which monitors voltage limits and controls also dependencies between voltages. An emergency off is triggered for values out of the specified ranges.

Both, gate-on and clear gate, are divided into three domains along the DEPFET matrix. This allows to individually adjust the voltages to the three regions which might receive varying radiation doses.

The VXD is cooled by the 2-phase CO_2 cooling system **IBBelle**. It uses the phase transition of the coolant to efficiently remove the heat from the detector. The 3D printed metal Support and Cooling Blocks (SCBs) are the mounting structures for the PXD ladders outside of the acceptance region. The liquid CO_2 reaches the SCB

Table 4.2.: PXD supply voltages

dgnd	digital ground
adng	analog ground
sw-sub	Switcher substrate
sw-dvdd	Switcher digital supply
sw-refin	Switcher reference input
dcd-amplow	DCD current sink
dcd-avdd	DCD analog supply
dcd-dvdd	DCD digital supply
dcd-refin	DCD reference input
dhp-core	DHP core supply
dhp-io	DHP input output supply
clear-on	Switcher clear-on supply
clear-off	Switcher clear-off supply
gate-on1	Switcher gate-on supply first domain
gate-on2	Switcher gate-on supply second domain
gate-on3	Switcher gate-on supply third domain
gate-off	Switcher gate-off supply
bulk	DEPFET bulk
source	DEPFET source
ccg1	DEPFET capacitive coupled clear gate first domain
ccg2	DEPFET capacitive coupled clear gate second domain
ccg3	DEPFET capacitive coupled clear gate third domain
hv	DEPFET high voltage aka. back plane
drift	DEPFET drift (adjusts drift fields for electrons)
guard	DEPFET guard (prevents electrons from entering from outside)

through tubes, evaporates in the channels inside the SCB and leaves again as gas in direction back to the cooling plant (see fig. 4.13). IBBelle is able to hold an operation point at about $-30\,°C$ while efficiently cooling the about 9 W per PXD module and the additional heat load from the SVD.

A **forced N_2 flow** is guided in between the two PXD layers by openings in the SCBs. In addition, carbon tubes span between the forward and backward SCBs and direct the cooled N_2 flow on the positions of the Switcher ASICs. A dry volume for the inner detectors is maintained to avoid condensation on the detectors.

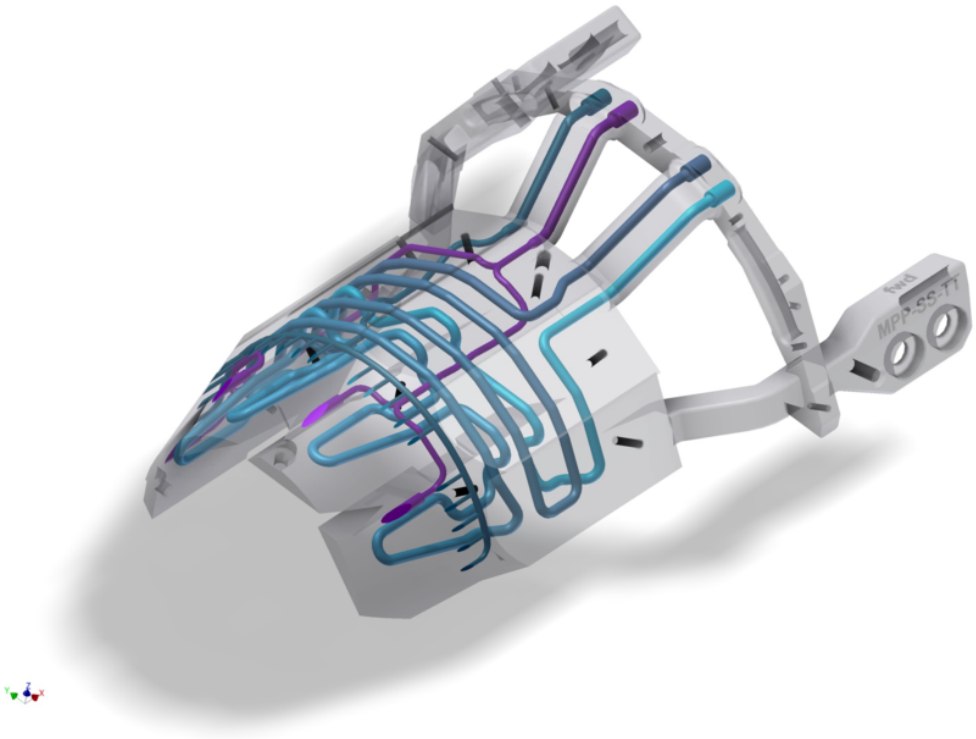


Figure 4.13.: Support and cooling block [105]. The liquid CO_2 enters the SCB (light blue) and is guided in serpentines through the massive metal block. The CO_2 absorbs the heat generated from the electronics on the modules and evaporates. The gaseous CO_2 leaves the SCB again (dark blue). Cooled N_2 is blown in between the PXD layers (dark green). Carbon tubes are attached to outlets in the SCB (magenta) and guide the flow onto the Switcher positions.

5. Standalone PXD Module Operation

During the design of system components for the PXD as innermost subdetector of Belle II, specific requirements for each component had to be fulfilled as described in the previous chapter. The focus had to be placed on the final installation and on the integration into the framework of the experiment. However, various reasons required the possibility of a standalone operation of individual modules, e.g. testing of prototype modules [51], beam tests [112, 113], irradiation campaigns [96], development of optimization algorithms and characterization of individual modules during the main production.

This chapter describes the hardware and software which is required for a laboratory setup to operate a single PXD module. Almost all system components were still under development during the course of this thesis, therefore, the following description mainly reflects the state during the characterization of main production modules (see chapter 7). Some hardware components are dedicated equipment for laboratory setups, which were created as more simple versions of final components which had still to be designed, e.g. Power Breakout Board instead of the Dock Box PCB, or the Data and Power Patch Panel instead of the final Patch Panel Cable. Equally, some software components fulfill dedicated requirements for a standalone module operation, e.g. the LocalDAQ for data readout or the Utility IOC for configuration tasks and DHP temperature readout.

5.1. Setup concept

The minimum setup configuration covers the three major domains for PXD operation: power supply, slow control and data acquisition. Each domain requires dedicated hardware and software. The ratio between PXD module and PXD Power Supply is always one-to-one. Instead of a complete DHH system, the module setup uses a reduced version consisting of only one DHE with a dedicated firmware. The software for slow control, data acquisition and data analysis runs on a dedicated PC. Figure 5.1 illustrates the required hardware components for a module setup and the interconnections between them.

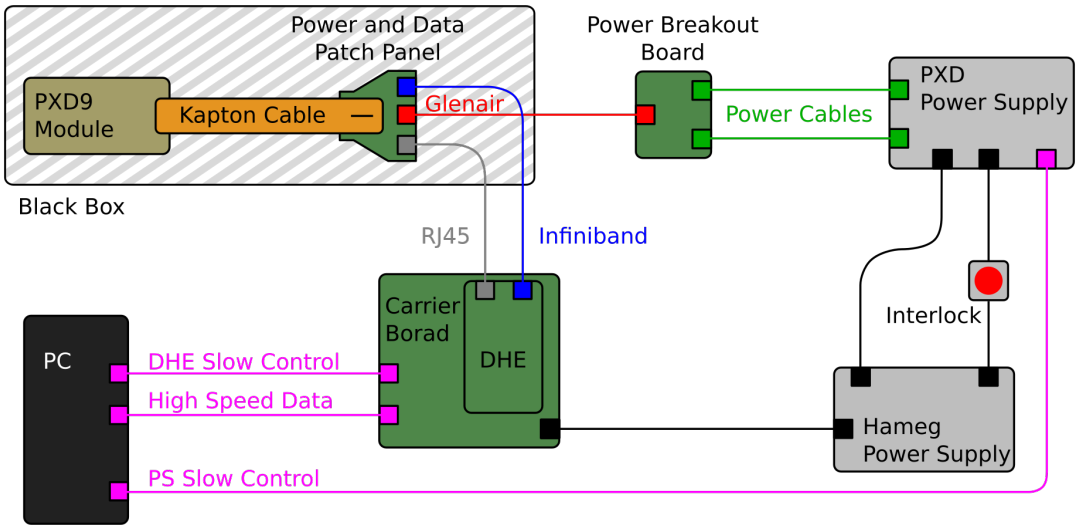


Figure 5.1.: Sketch of laboratory setup for PXD module operation. The PXD module is placed in a Black Box to shield the light sensitive sensor from ambient light. Power, slow control and data transmission lines are split at the Power and Data Patch Panel. A commercial bench power supply (e.g. HAMEG HMP4040) is used to power all system components.

5.2. Hardware

All hardware components (except PC and bench power supply) are custom made items tailored for their specific application in the laboratories. For some components several iterations and optimizations were necessary and different versions exist at different testing locations throughout the collaboration. The described hardware components were used in the testing laboratory at the MPP in Munich.

A picture of a PXD module setup with installed module is shown in fig. 5.2. Support structures allow a safe handling and mounting of the module. A cooling block with integrated tubes for vacuum suction ensures proper thermal contact and heat dissipation. Adjustable mounting plates with long holes are required to fit all dimensions of the four different module geometries and Kapton cable lengths, e.g. inner forward, inner backward, outer forward and outer backward. At the Data and Power Patch Panel the transmission lines for the three domains are separated and connected via individual cables to the PXD Power Supply and DHE. A raspberry computer controls a linear translation stage which is used to place a radioactive source above the sensitive area of the module. The remaining hardware, like power supplies and readout electronics, is placed outside the Black Box.

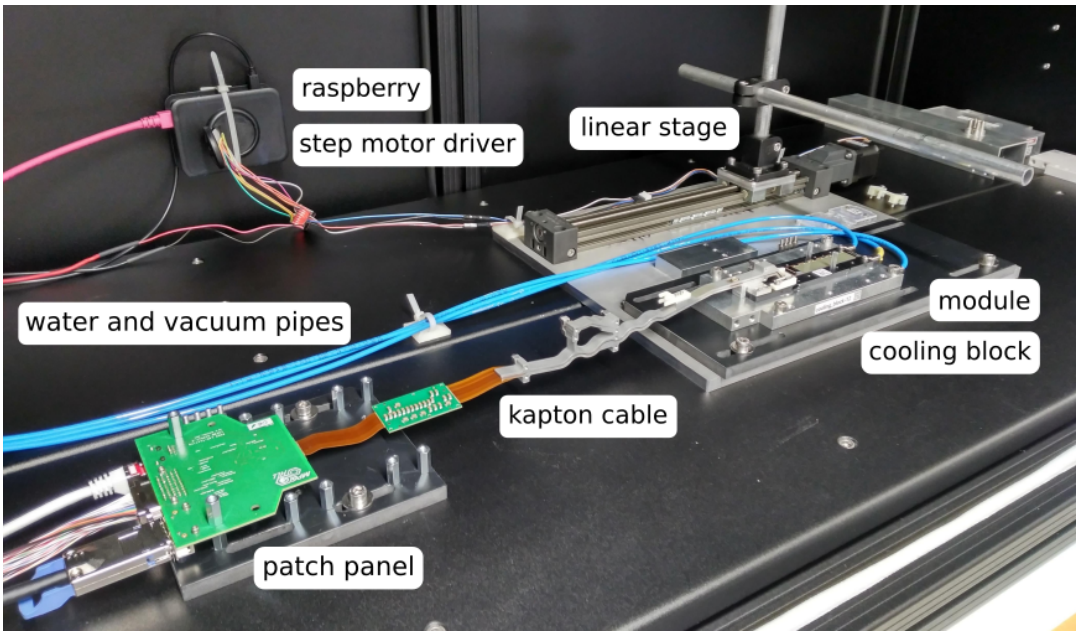


Figure 5.2.: PXD module setup during main production testing. The module is mounted onto a cooling block inside a Black Box. A linear translation stage is installed next to the module to move a radioactive source over the sensitive matrix. The step motor of the stage is controlled via a raspberry computer.

5.2.1. Module support

The base for each laboratory module setup is a Black Box (see fig. 5.3). It provides the required space for all setup components. Mounting threads in the ground plate in combination with adjustable mounting plates are used to securely install all setup components. With closed front doors the module inside is shielded from ambient light and a stable background for measurements is achieved. Cables are guided through shielded openings at both sides. The larger components (e.g. long power cables, power supplies and readout electronics) are placed on top of the Black Box or attached to its sides.

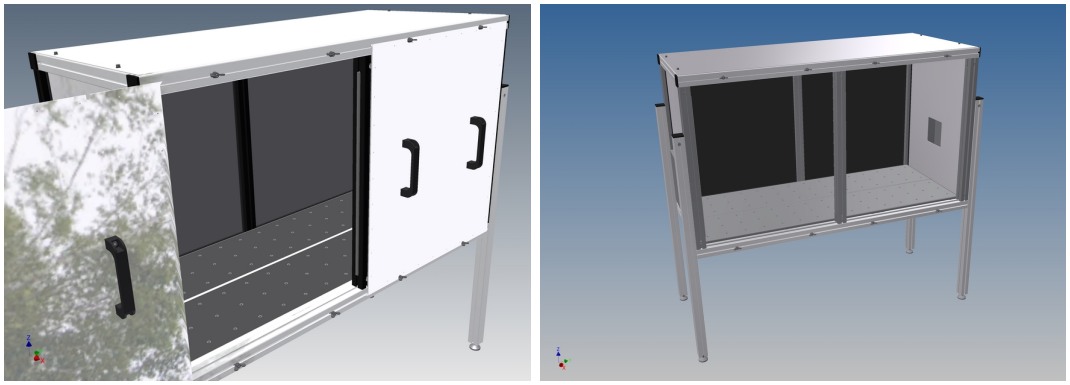


Figure 5.3.: Black Box for a PXD module setup. Approximate dimensions: 1.5 m wide, 0.7 m deep, 2.0 m high.

Each manufactured PXD module is equipped with a module support set (see fig. 5.4). Its primary purpose is to achieve a save transport and storage of modules by protecting each part of the module from external influences. The module transport jig in combination with the module transport cover and the Kapton cover build the outer shell. The module itself lies on the module base jig and is fixed by a module clamp. In addition, a Kapton jig is mounted onto the base jig and holds the Kapton Cable at the correct angle and position. It also follows the bending of the Kapton Cable which already reflects the final geometry after installation in the Belle II experiment[1].

The PXD modules are always placed on the base jig with their mounted components (i.e. ASICs, passives and Kapton Cable) facing upwards. In the final detector geometry, however, inner modules are facing the beam pipe while outer modules are facing the first layer of the adjacent SVD. This results in different bending directions of the Kapton Cable relative to the base jig. While outer modules can be mounted on a flat ground plane and the Kapton Cable sticks upwards, for inner modules the

[1] Only the last bend is added to shorten the overall length during storage.

Kapton Cable has to be lowered below the module plane. Therefore, the module base jig features a cut out at the end of the Kapton Cable. In addition, a support set for inner modules with spacers is required. They lift the module over the installation plane and give the Kapton Cable enough space.

When the module is handled for installation into a testing setup, first the transport cover and the Kapton cover are removed. Next, the module base jig together with the Kapton jig is lifted from the transport jig. The module itself is never touched! An additional inner module cover protects the fragile silicon module. The inner module cover features also little springs which hold the module down[2]. It is only removed while the module is installed in a test setup and the DEPFET matrix has to be exposed to a radioactive source.

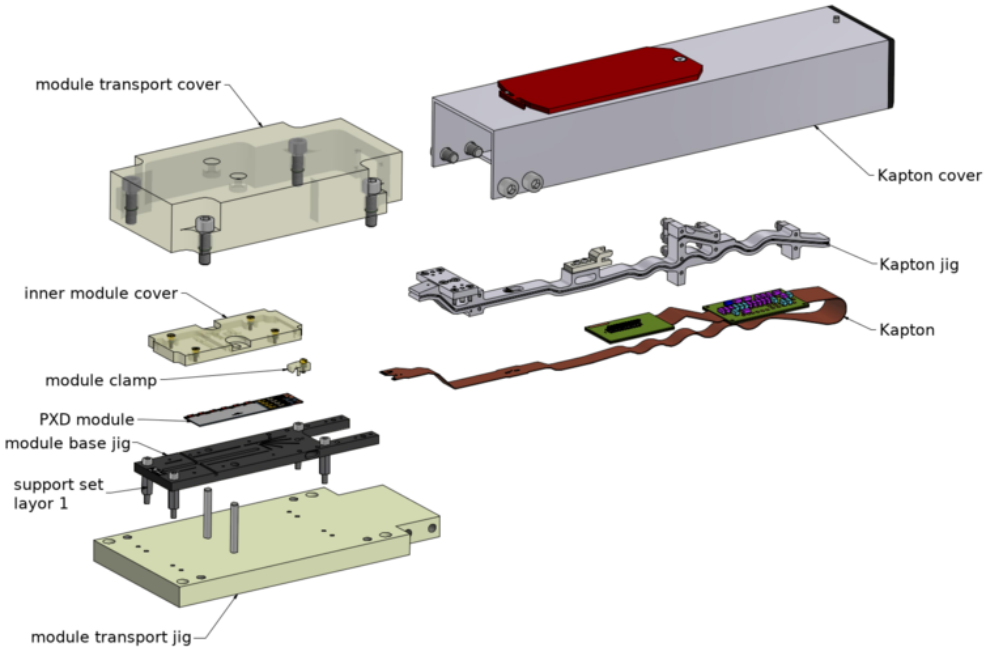


Figure 5.4.: Hardware components of PXD module support set.

According to the four different PXD module designs and four different Kapton Cable geometries, there are also four different versions of the Data and Power Patch Panel. It is a special development for laboratory setups. In combination with the Glenair, Infiniband and Ethernet cables it fulfils the task of a Patch Panel Cable from the final design. A dedicated mounting plate takes care of a proper stress relief. No torque is transmitted to the joint between Kapton Cable and module (see again fig. 5.2).

[2]These springs are just for mechanical stability. They are not strong enough to ensure a proper thermal contact during operation.

5.2.2. Cooling and vacuum

The power consumption of a PXD module is about 9 W [51, 114]. The very thin module (75 µm sensitive area to 525 µm silicon support frame) has a low heat capacity and heats up quickly. It has to be cooled during operation to avoid damages from overheating, like electro-migration in the electronics or loosening of solder joints.

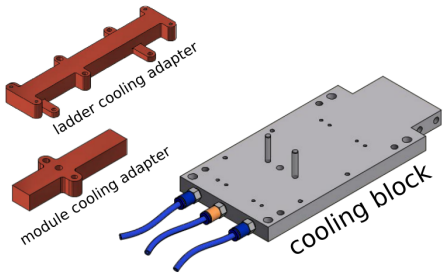
In the laboratory setups instead of two phase CO_2 cooling a water cooling system is used. It operates at higher temperatures but is sufficient for the module setups in terms of heat dissipation and has less requirements in terms of isolation and pressure safety. One refrigerated circulator (fig. 5.5a) is used to provide cooling for the three module test setups at the MPP laboratory. The setups are connected in parallel and the lines to the individual setups can be opened and closed by valves.

In each module setup a cooling block (fig. 5.5b) closes the cooling circuit with inlet and outlet connection. It also features a connection for vacuum suction. Two alignment pins on the cooling block and guiding holes in the module base jig ensure a proper positioning of the setup components (fig. 5.5c). For the inner modules or ladders cooling adapters are required which fill the gap between cooling block and base jig.

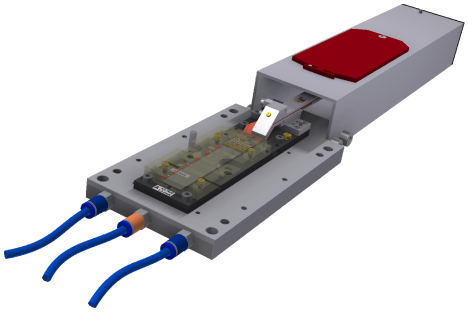
The water temperature of the cooling circuit is set to about 14 °C. Although the temperatures are way above the freezing point, it is still required to ensure suitable environmental conditions around cooled surfaces to avoid condensation. Especially during the warmer summer months the dew point rises and wetting can cause severe damage to the modules. Crystalline soldering flux remaining from the flip chip and SMT soldering processes disperses in condensed humidity and corrodes the surfaces. Entirely separated bond wires were observed due to this effect. Monitoring of air temperature and air humidity is therefore obligatory.

A good thermal contact between all components is mandatory for sufficient heat dissipation. Special attention has to be payed to the contact between module and base jig. Tension in the Kapton Cable can lift the module from the base jig and a small air gap isolates the module thermally (see fig. 5.6). This results in a raise of about 50 °C within few seconds during the operation of a module in PEAK state (see fig. 5.7). Temperatures above 100 °C at the solder joint between module and Kapton Cable are high enough to soften the solder. In combination with stress from the bent Kapton Cable this can result in a shift between module and Kapton Cable. The flexible wire bonds can follow this shift to some degree but this can result in a modified arch geometry which prohibits the integration of this module into the final

(a) JULABO refrigerated circulator.



(b) Cooling block and adapters for inner layer.



(c) PXD module installed on cooling block.

Figure 5.5.: Cooling circuit equipment for laboratory module setup.

PXD detector assembly. Ultimately, the solder joint can open completely which also destroys the wire bond connections. Both scenarios were observed during module operation. It is absolutely necessary to prevent an overheating of modules during operation.

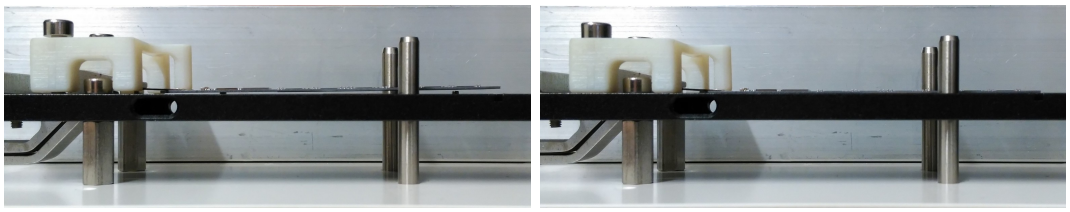


Figure 5.6.: Example for bad contact between module and base jig. Left: The tension at the joint between Kapton Cable and module forces the module to float over the base jig. Right: In this example a tightened module clamp is sufficient to press the module down. During the operation in the setup the vacuum suction provides additional force downwards over the entire module length.

To achieve a proper thermal contact between module and base jig in the module setups two measures are taken. First, a 3D printed clamp mounted on the base jig presses the module down. The finger of the clamp touches the module at the EOS above the mounting hole. At the EOS the majority of the power consumption arises. Second, a vacuum suction connected to the cooling block and transmitted through the cooling adapter and module base jig extends the downward force along the entire length of the module. Often the combination of both is required for a proper thermal contact.

After two modules were glued to a ladder, the ladder is placed on a ladder base jig and fixed to it with two screws like the final fixation to the SCB. Therefore, clamp and vacuum suction are not applied for the operation of a ladder in the test setups. Nevertheless, each installation has to be checked for a proper thermal contact before the power up of a module or ladder.

5.2.3. Power supply

As primary power source for a module setup a programmable four channel **bench power supply** (e.g. HAMEG HMP4040) is used. It is connected via a USB cable to the control PC. It can be switched remotely (required for setups with limited access like beam tests) and its outputs can be integrated into automated programs. Four channels are enough to power all setup components. The required settings for each channel are listed in table 5.1. The **PXD Power Supply** requires two inputs: the primary supply at 24 V and an emergency shutdown input, which enables the operation as long as a potential above 3 V is applied. The DHE requires a 5.5 V

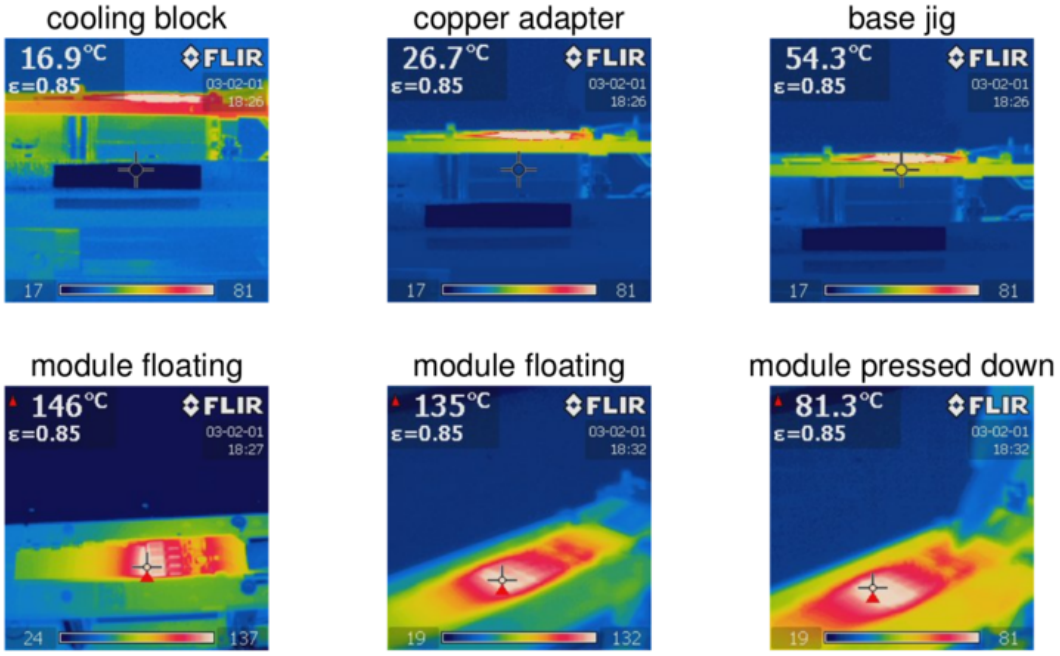


Figure 5.7.: Impact of proper thermal contact between module and base jig on the module temperatures. The thermal images of a module setup with an inner module demonstrate the temperatures of the individual components. The cooling block has a temperature of 17 °C, the cooling adapter is about 10 °C warmer. The base jig has a temperature of almost 55 °C. Without proper thermal contact between module and base jig the DCDs as largest consumers on the module reach temperatures up to 146 °C. When the module is pressed down onto the base jig the maximal temperature is lowered to about 81 °C.

supply and a high current during power on. Hence, the corresponding current limit should be set to the maximum value. The PXD Power Supply as well as the DHE card have to be cooled by air ventilation. The fans are connected to the remaining channel.

Table 5.1.: Bench power supply settings for PXD module setup

channel purpose	voltage	current limit	exp. current	power
PXD Power Supply	24.0 V	6.5 A	2.6 A	62 W
PXD PS emergency input	5.0 V	0.2 A	0.01 A	0.05 W
DHE Carrier Card	5.5 V	10.0 A	1.8 A	10 W
fans	15.0 V	1.0 A	0.1 A	1.5 W

The PXD Power Supply is connected to the control PC with an Ethernet cable for slow control. The 25 required supply lines for the PXD module operation and corresponding sense lines are transmitted from the PXD Power Supply outputs via a pair of about 15 m long custom made power cables. The bench power supply, the PXD Power Supply and the majority of the power cables are stored on top of the Black Box (see fig. 5.8). From there the power cables are guided down towards the side of the Black Box and connected to a Power Breakout Board. This passive Printed Circuit Board (PCB) replaces the power domain part of a Dock Box PCB from the final design. It converts the two bulky power cables into one Glenair cable, which is guided through the shielded opening at the side of the Black Box and bridges the last about 2 m to the Data and Power Patch Panel inside.

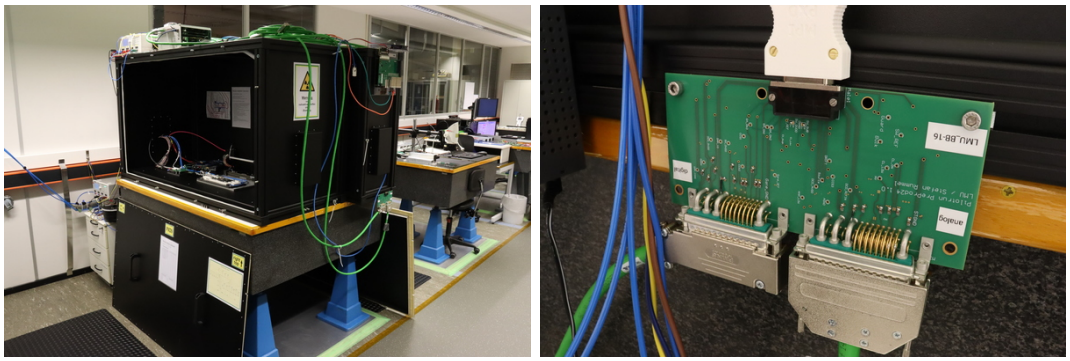


Figure 5.8.: Power supply for laboratory module setup. A programmable four channel bench power, the PXD Power Supply and the majority of the power cables are stored on top of the Black Box. The Power Breakout Board transfers the lines of the two power cables into one Glenair cable.

In order to verify the correct cabling of the power lines before a module is plugged to the services, it is necessary to check each line with a voltmeter. This should be done as close to the module as possible, usually at the Patch Panel where contacts

are still accessible. Although this can in principle be done with a Data and Power Patch Panel, it is very tricky to contact all nets as some are only available at the solder pins of the Glenair connector and have no label on the PCB. The necessity for this check applies for newly built and untested laboratory setups as well as for the final commissioning of the PXD at Belle II. In the latter case the amount of 40 modules, the complicated cable routing and the long distance between PXD Power Supply rack on top of Belle II and the detector in the center make this task especially challenging.

To optimize this process a Power Lines Test Board was designed (see fig. 5.9). It offers a female Glenair connector to provide the same connection to the power services like the Data and Power Patch Panel. All nets are then routed to labeled test pads, which can be contacted comfortably with a standard voltmeter probe. To provide the correct reference for the measurements three 4 mm banana plugs for dgnd, agnd and source are available as well.

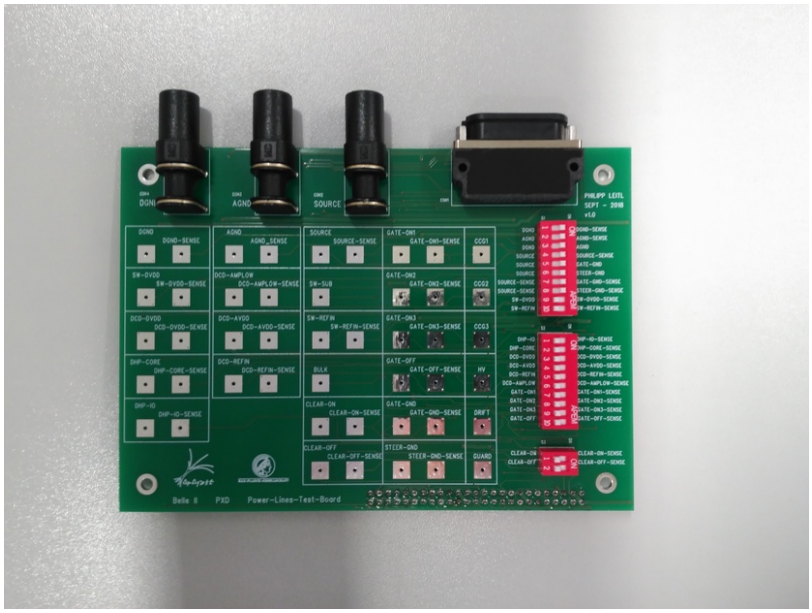


Figure 5.9.: Power Lines Test Board. At the upper right side the Glenair cable has to be connected. The three banana connectors provide the reference voltages for the different domains: dgnd, agnd and source. The test pads feature a large contact area and are clearly labeled simplifying the task of voltage verification. The DIP switches on the right side can be used to close or open the connections between force and sense lines.

On the Patch Panel and on the module some nets are connected to each other, like the sense lines with the corresponding force lines. To mimic this behavior DIP switches are placed on the Power Lines Test Board making it possible to close or open those connections as required.

In addition, all lines are routed to a pin header on the bottom side of the Power Lines Test Board. This could be used as interface for a further board (still to be developed) which serves as dummy load instead of a real module. Power resistors of appropriate size have to be used for this purpose.

5.2.4. Slow control and data acquisition

For the reduced requirements of a laboratory module setup a single DHE card can replace the overhead of a complete DHH system. A dedicated firmware is required as well as custom made support electronics called VME Carrier Card (see fig. 5.10). A custom-made mechanical support allows the convenient attachment of the VME Carrier Card to the side of the Black Box including a holding structure for the required cooling fan.

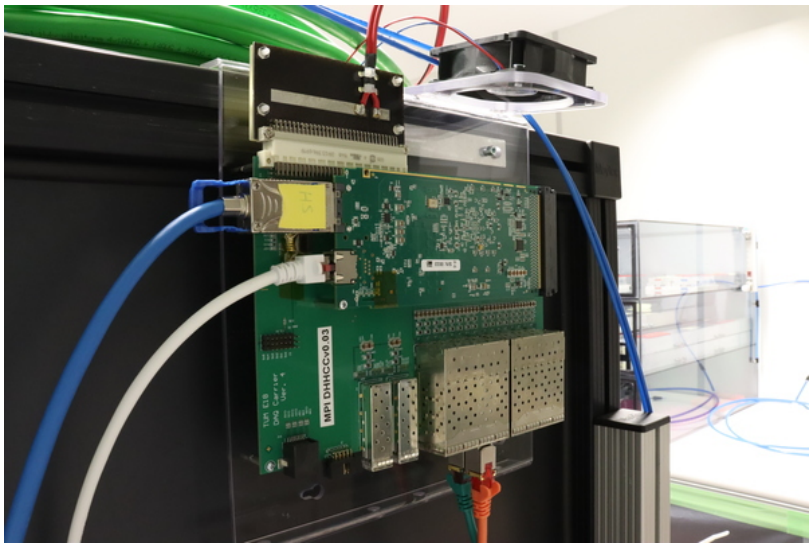


Figure 5.10.: DHE on VME Carrier Card attached to the Black Box.

The Infiniband cable carrying the high speed data transmission lines and the Ethernet cable for the slow control signals are guided through the shielded opening in the side of the Black Box towards the Data and Power Patch Panel. In the final detector design the Infiniband cable connects the module with the Dock Box PCB where the copper lines are converted to optical fibers. The remaining module control lines from the Infiniband cable are combined with the lines from the Ethernet cable into one Camera Link Cable. Optical fibers and Camera Link Cable are guided to the DHH rack and connected to the back plane. Hence, the Infiniband and Ethernet inputs of the DHEs are not used. In terms of data transmission the laboratory module setup covers only the copper line connections between module and Dock Box PCB.

Two Ethernet cables connect the outputs of the VME Carrier Card with the control PC: again separated between data and slow control. The software for slow control, data acquisition and data analysis runs on a computer with Scientific Linux as operation system.

5.2.5. Linear translation stage

For characterization and optimization procedures a radioactive source is used in the laboratory setups. These radioactive sources are typically small, i.e. few millimeter in diameter. In order to illuminate the entire matrix of a PXD module with about $560\,\mathrm{mm}^2$ for an inner module and about $768\,\mathrm{mm}^2$ for an outer module the source would have to be installed at a large distance from the module. This would lower the efficiency due to less coverage of the irradiation spot and the matrix. Consequently, a higher activity of the source would be required to achieve an acceptable measurement duration. This can be avoided when the source is dynamically moved over the entire sensitive area.

A linear translation stage is installed next to the module support in the Black Box (see again fig. 5.2). It features a holding structure for a radioactive source which can be moved along the long axis of a module. The step motor of the linear translation stage is controlled by a step motor driver electronic attached to a raspberry computer. A dedicated EPICS IOC runs on the raspberry computer which is accessible via the setup network and can be remotely steered from the setup control computer. In this way the movement of the linear stage is integrated into the automated measurement routines (see fig. 5.11).

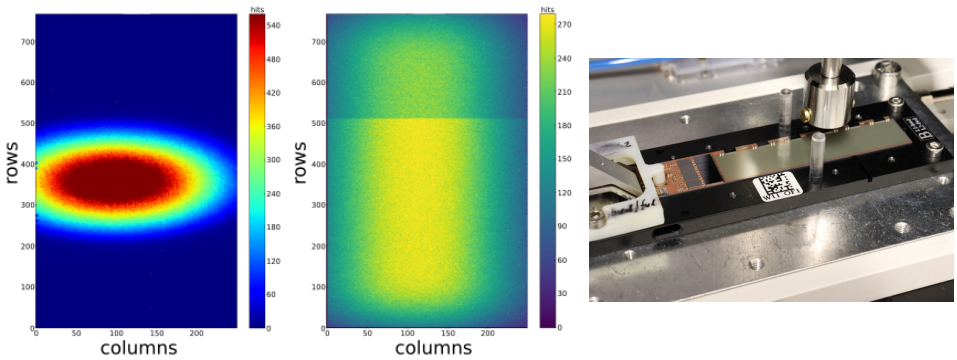


Figure 5.11.: Comparison of hit distribution across the sensitive matrix between a static mounted source and a dynamic linear stage. With the linear stage the entire matrix can be illuminated with high coverage efficiency. Local effects become visible like the smaller pixel pitch in the upper third of the matrix.

5.3. Software

The software used to operate a module setup is in large parts congruent with the one used for the final installation of the PXD at Belle II. In fact, many developments started and were tested on module setups and had to be extended to the full size application later. Modular and object oriented programming is used to reach a flexible and scalable software stack. The slow control relies on EPICS, an advanced and proven control solution from the experimental physics community. The local data acquisition software was developed especially for the PXD at the University of Bonn. The software framework utilizing the recorded data for calibration, optimization and analysis of module performance emerged from a collaborative effort between the member institutes of the PXD collaboration.

5.3.1. Slow control - EPICS system

Experimental Physics and Industrial Control System (EPICS) is a free and open source project providing software tools and components for distributed control systems [115, 116]. Its collaborative development started in the early 1990s and encompasses more than 50 large science institutes today. It is used at particle accelerators, telescopes and other large scientific facilities and by several companies.

EPICS uses a client-server architecture. Input/Output Controllers (IOCs) manage the interface to the hardware, like sensors and actuators, and provide as servers information about the system via Process Variables (PVs). These PVs are records in the Distributed Run Time Database accessible for clients in the network through the Channel Access or the newer pvAccess protocol. Clients can query the state of the IOC or attached hardware through the *get* command (get the current value of the requested PV). They can also change PV value with the *put* command or demand a notification on change through the *monitor* command. A list of typical client applications includes Operator Interfaces, Alarm Managers, Archivers, Sequencers and Application Programs. All components can be distributed over an unlimited number of workstations in the network enabling the control of large scale systems with thousands of IOCs and millions of PVs.

A typical EPICS configuration of a PXD module setup is shown in fig. 5.12. Most of the components are running on the operator computer of the corresponding setup installation. The IOC for the linear stage is running on the attached raspberry computer. For the archiving task a dedicated computer is installed hosting an instance of the EPICS Archiver Appliance [117]. A single instance is sufficient to serve all module setups connected to the network.

While all PVs are accessible within the LAN of the laboratory as intended for an distributed control system, filters are applied on the workstations of the individual setups so that only the PVs of the corresponding module setup are visible to the operator. This prevents unintended changes to other setups.

Generally, it is important to keep in mind that EPICS is a *slow* control system. Changes to PVs can not be applied without delay to hardware and vice versa changes at the hardware can not be reflected in the PV values instantaneously. Programmers have to take this into consideration during the development of applications which access and change PV values frequently.

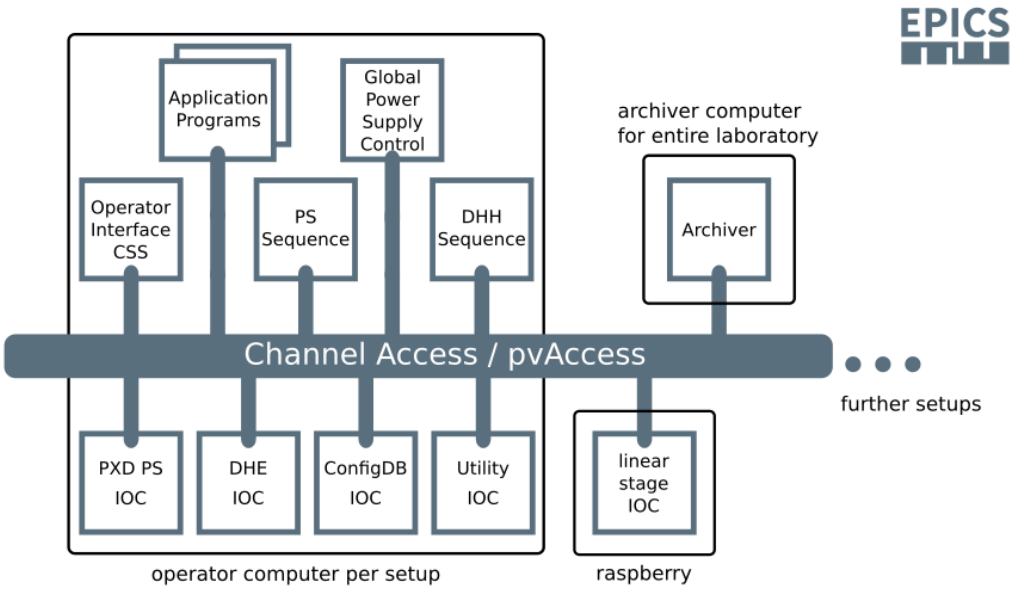


Figure 5.12.: EPICS structure of a PXD module setup. For the reduced module setup most of the EPICS components are gathered on the operator computer while for larger installations dedicated IOC servers are used. Only the archiver task is outsourced to a separate computer serving for all module setups in the same network. Furthermore, the hardware controller for the linear stage is steered by a raspberry computer installed next to the linear stage.

Each module setup requires three IOCs which are connected to the corresponding hardware components:

- The **PXD Power Supply IOC** provides the interface to the PXD Power Supply and all PVs for its operation. PVs for the applied and for the sensed voltages are available as well as measured currents of each Power Supply channel. When a client wants to set a PV value for voltages or for current limits, these requested values are checked against internal safety limits and only applied after valida-

tion. The internal OVP reports its status and communicates which channel was out of bounds, when an OVP event happened.

- The **DHE IOC** is the interface to the PXD module. It provides PVs for the state of the DHE hardware and its configuration but also PVs for the configuration of the ASICs on the PXD module itself. The communication between the IOC and the DHE is realized via the UDP-based IPBus protocol [107]. The commands for the ASIC configuration are translated on the DHE to JTAG commands which then act on the internal registers of the ASICs.

- The **linear stage IOC** controls the step motor driver connected to the outputs of the raspberry computer. The table of the linear stage is moved by setting a position value. The start and end point as well as a safe standby position have to be calibrated manually before the start of a scan over the module's matrix.

There are several more IOCs which provide additional PVs and act on PVs of the already described IOCs. However, they are not directly connected to a hardware component and therefore are called "soft" IOCs:

- The **ConfigDB IOC** connects to the PostgreSQL Configuration Database [118] which stores all required PV values for an entire setup configuration in individual commits. The commits are linked to a particular PXD module by its unique module name. After calibration and optimization, updated PV values are stored in a new commit. The ConfigDB IOC provides the commitid PV and loads all stored PV values from the Configuration Database when the corresponding commitid is set. The other IOCs retrieve the module specific PV values from the ConfigDB IOC.

- The **Power Supply Sequence** is a sequencer IOC and contains the knowledge on how to power on a PXD module. It automates the numerous steps of applying current limits and ramping voltages for turning on and off. This procedure is programmed as state machine with precisely defined states and transitions between them. As this process also requires the configuration of the ASICs on the PXD module, handshakes between the Power Supply Sequence and the DHH Sequence are implemented.

- The **DHH Sequence** is the corresponding sequencer IOC and state machine for the configuration of the DHE and ASICs. It prepares the DHE before powering the module and writes and verifies (where possible) the configuration of the ASICs at the correct point during power up. Only after successful configuration it reports back to the Power Supply Sequence which is waiting for this handshake before continuing its sequence. This is illustrated with the following example: When the DCDs are supplied with power after they were turned off,

their internal registers are in an undefined state. Their analog parts will not be switched off correctly, which can lead to potentially harmful high currents. Hence, the current limit for not yet configured DCDs must be low[3]. Only after the DCDs have been configured correctly the Power Supply Sequence is allowed to continue increasing the current limits.

- The **Global Power Supply Control** combines the states of the two previous IOCs (Power Supply Sequence and DHH Sequence) in order to get to an overall state of the corresponding module. Requests by the operator to change the module state, like powering on or off, are addressed to the Global Power Supply Control which triggers the required operations in the other IOCs. For the final installation of the PXD with 40 modules only one instance of the Global Power Supply Control is foreseen taking care of the state of the entire PXD.

- The **Utility IOC** covers dedicated configuration tasks like reconfiguration of individual ASICs. This is frequently required during optimization of PXD modules, e.g. during the characterization of new modules or during maintenance days at Belle II. In addition, the Utility IOC performs an automated temperature readout of the internal DHP temperature sensors. This procedure requires an extensive usage of JTAG commands and the Utility IOC takes also care of blocking new user commands until the previous command finished. Alarm limits for the DHP temperatures are set and an emergency shutdown is triggered for the corresponding module when the temperatures were above the threshold for three consecutive readings. This important safety feature is integrated in the DHI firmware for the final installation.

Control System Studio (CS-Studio) is used as graphical user interface (GUI) for the operator [119]. Customized Operator Interfaces (OPIs) (or BOBs for the newer implementation called **Phoebus**) were created using different available widgets like buttons, switches and LEDs to visualize the system's state and to interact with the system. A variety of OPIs are available on different levels of complexity intended to give a combined overview to the non-expert shifter and the full control over all PVs to the experienced operator further down the OPI hierarchy. After a long development it became finally possible to comfortably turn on a PXD module or even the entire PXD by pushing only one button.

[3] In fact, it must be as low as for only one DCD. At first all four DCDs share the current to equal parts, but after the first configuration the configured DCD will correctly switch off its analog part and draw significant less current. The now available current will be distributed among the other three DCDs and same after the next configuration until three DCDs are configured and draw only very few current. The entire current limit, which was at first set for four DCDs, is now available for only one which might get damaged.

Application Programs written in the Python programming language allow for an automated control of PXD modules. These programs act on the PVs to bring the system into a desired state and analyse the systems response, e.g. ASIC configurations are systematically changed to find the optimal operation parameters. Most of these programs also use data from the module's matrix as input. The LocalDAQ and the software framework for these programs is described in more detail below.

The **Archiver** is a very important component for every control system. It allows to constantly monitor a very large number of PVs and track their evolution over time enabling the analysis of changes and the investigation of unexpected events in retrospect. CS-Studio / Phoebus provides a Data Browser tool for the operator which displays the time development of PV values. In addition, a dedicated Archive Viewer is available as web application [120]. For custom analysis the archived data can also be accessed via a web interface providing the data in machine readable JSON format or directly through the stored data files on disk. For the unpacking and decompression a dedicated program is required [121], which is added to the software framework as submodule.

5.3.2. Local data acquisition

The DAQ scheme for the entire Belle II experiment is a highly integrated system with a common trigger logic for all subdetectors including the merging of their data streams. For standalone PXD installations like the module setups a lighter LocalDAQ version was developed in Bonn [112]. The LocalDAQ software runs on the setup computer and receives the PXD raw data directly from the DHE as UDP packages over an Ethernet cable. The data is then processed and typically stored on disk for later analysis, but live data can also be provided for real time analysis and online monitoring. Due to a missing trigger system in the module setups, the DHE also generates the trigger signal for data readout[4].

The LocalDAQ is a standalone software and not part of the laboratory framework itself, but it is an indispensable requirement as it records the data for each analysis. All analysis tools in the framework are built on its data structure. The pyDepfetReader software reads the stored raw data files from disk and provides the data as numpy arrays for the Python analysis scripts. For online monitoring at the Belle II experiment the LocalDAQ runs on a dedicated server and receives a fraction of the current raw data stream. The LocalDAQ is also used for the module calibration tasks and optimization routines between the runs and during maintenance days.

[4]The DHE features also an input for external trigger signals for special applications like test beams.

5.3.3. PXD laboratory software framework

The PXD laboratory software framework (lab_framework) contains the already mentioned application programs. It is a structured set of Python scripts which automatize several different tasks. The main aspects are the calibration and optimization of PXD modules as well as online data quality monitoring. To interact with the hardware the PyEpics library [122] is used, which grants access to the PVs provided by the IOCs. The PXD laboratory software framework is used extensively during the characterization and qualification of main production modules and at all installations of PXD modules including the final detector setup in Belle II.

The most important components of the software framework are "configurations", "libraries", "calibrations" and "run control":

- **Configurations:** For module setups there is a *start-epics* script which automatically configures and starts the required IOCs. The necessary information about hardware and software versions as well as network IPs and ports is stored in a `host-<hostname>.ini` file and has to be adjusted by the operator. Also the scripts of the application programs require configuration. The `master.setup.<hostname>.ini` file stores mandatory information about the specific installation. The used PXD Power Supplies and DHEs are specified with their PV prefixes so that the Python scripts automatically attach to the right PVs. It must be stated if a DHC or DHI is used an if external triggers are provided. Also a base path for the storage of the recorded data and analyses is required. These settings have to be specified manually by the operator but only during the initial setup and can stay unchanged as long as the installation stays unchanged.

  In addition, there is a configuration script which tells the EPICS archiver which PVs have to be archived and also allows to retrieve archived data for analysis.

- **Libraries:** For frequent tasks libraries provide routines which are called from the individual scripts. There are currently more than 50 library files, each for its particular purpose. Table 5.2 gives a short list with the most frequently used library files and their applications as overview.

  The classes of the abstraction layer leverage the full potential of Python's object oriented approach. The hierarchical structure mimics the hardware installation: *Setup* $\rightarrow$ *DHCs* $\rightarrow$ *Devices* (e.g. PXD modules). The module setups use a dummy DHC instance to comply to this scheme. Each instance has all required attributes assigned and for frequently used operations corresponding functions are available taking care of the complex details. This concept eases the devel-

opment and maintenance of applications for the PXD modules.

- **Calibrations:** In order to find the best operation parameters for individual modules automatized calibration and optimization scripts are used. According to the PXD specific coding guidelines all calibrations scripts follow the following scheme: *Measurement* → *Analysis* → *Update*

  The paradigm behind this structure is the possibility to separate these steps in time and space. The measurement data and all information about the system required for an analysis have to be stored together. The analysis can then be started subsequently or postponed to a later point in time. It is also possible to perform the analysis on a different computer (provided the installation of the software stack). Both are requirements for a long term accessibility of the recorded data.

  Specific configurations for the individual measurements and analyses are provided in the `measurement.ini` and `analysis.ini` configuration files, respectively. Elog entries are automatically created and uploaded for each measurement and analysis as documentation [96]. For the final installation of 40 PXD modules and the operation by non-expert shifters a user friendly CS-Studio interface was created which controls the Calibration IOC [again 96]. It takes care of the individual steps and can be easily steered by clicking buttons in the corresponding OPI. It also gives feedback about the current status of a calibration and its results. The focus was placed on the pedestal taking, which is the most frequent calibration also required in between of data taking runs at Belle II. However, the Calibration IOC calls the scripts from the laboratory framework which makes it expandable to all measurements.

  A detailed description of the most important calibrations which were also used during the characterization of main production modules is given later in section 7.4.2.

- **Run control:** All applications which support the operator in terms of task automation and quality monitoring are collected under the term "run control". The already mentioned Utility IOC and Calibration IOC are two examples. Another important application is the Online Monitor [112]. It receives a portion of the current PXD data via the LocalDAQ in parallel to the ongoing data taking. The Online Monitor then provides a set of histograms and a hitmap plot in its own OPI as fast feedback to the operator.

Table 5.2.: Examples for most frequently used library files

lib file	description	used by
daq.py	recording of data	measurement scripts
file_utils.py	reading data from file	analysis scripts
mapping.py	conversion between mappings	analysis and upload scripts
plots.py	plotting of data	analysis scripts
elog.py	automated creation of Elog entries	measurement and analysis scripts
abstraction_layer_utils.py dhh.py devices.py asics.py	abstraction layer classes	where applicable
config_utils.py	reading/writing configuration files	measurement and analysis scripts

All setup components described in this chapter, in terms of hardware and software, are prerequisites for the successful operation of PXD setups ranging from single module laboratory installations up to the final integration of the PXD into the Belle II experiment. Their design, production and development was not a straightforward path and requirements often changed. Several years of collaborative effort and constant growth in the operational experience finally led to a working infrastructure for the operation of PXD modules. The operational capability was demonstrated not only at several beam and irradiation tests but also during the EMC measurement campaign (chapter 6). For these measurements the PXD setups had to be transported, rebuilt and operated under time constraints in unfamiliar environments. The performance of the system was also proven during the characterization of the main production modules (chapter 7) and finally - after ladder gluing and assembly (chapter 8) - by the successful commissioning of the PXD at Belle II (chapter 9).

6. Electromagnetic Compatibility of the PXD

The PXD and even subsets of the PXD down to an individual module can be operated as fully functional, standalone device. However, the successful deployment of the PXD requires a parallel operation of 40 modules integrated together with multiple other subdetectors to jointly constitute a united data acquisition system designed to precisely measure the properties of single crossing particles with very high sensitivity. While each electronic device emits electromagnetic disturbances, itself is susceptible to such disturbances at the same time. A stable and reliable cooperation depends on the electromagnetic compatibility (EMC) of all involved components [123].

The development towards ever larger and more complicated detector systems with faster switching frequencies (up to GHz) and lower supply voltages (below 3 V) makes an appropriate consideration of EMC inevitable. Although industrial standards do not apply to scientific devices like particle detectors, they contain good advice and important guidelines. Consequently, we followed a dedicated EMC plan for the PXD [124] including also emission and susceptibility tests which we performed in the controlled environment of the Instituto Tecnológico de Aragón (ITAINNOVA) in Zaragoza, Spain.

The PXD module we used for the tests provided an adequate performance to deliver significant results. We recorded the emission spectrum and analyzed the data link stability as well as the system's response to external disturbances, where we put the focus on disturbances transmitted through the power lines and on those radiated from the beam pipe. From the derived transfer functions we conclude that the highest susceptibility for conducted noise lies between 8 MHz and 20 MHz. For radiated noise the transfer function forms a plateau up to higher frequencies, but below 40 MHz the susceptibility is significantly lower than for conducted noise. Compared to the EMC standard CISPR 32 the PXD emissions keep the limits for industrial equipment over almost the entire frequency range. Its robustness is high enough to cope with emissions from such equipment. In summary, the PXD module showed an overall good EMC performance which promised an unobstructed operation at the Belle II experiment.

6.1. Basics about electromagnetic compatibility

For the successful operation of each electronic device its electromagnetic compatibility with respect to its environmental electromagnetic conditions plays a crucial role. It must be ensured that the device can still fulfill its foreseen purpose under the influence of external noise and it must not disturb other devices in its surroundings. Industrial standards issued by public authorities specify the guidelines to be followed during hardware development and testing. Those standards do not apply to custom-made electronic devices for research, but with a growing number of subdetectors combined to a large data acquisition system EMC requirements gained increasingly in importance also for High Energy Physics (HEP) experiments. The requirements and instructions of the industrial standards provide a valuable guideline for the development of particle detector systems as well.

Since the foundation of the European Union (EU) the European Parliament pushed the harmonization of national standards forward and released several Directives relating to EMC. The EU Directives are following the approach to omit all technical content but refer to standards developed by the European Standardisation Organisations (ESOs) for technical details [125]. The standards define the testing procedure and set the limits to be kept [126].

The effective European Directive on EMC defines two essential requirements [126, 127]:

- *Emission Requirement*: Equipment shall be designed and manufactured in a way to ensure that the electromagnetic disturbance generated allows radio and telecommunication equipment and other equipment to operate as intended;

- *Immunity Requirement*: Equipment shall be designed and manufactured with an inherent level of immunity to the electromagnetic disturbance to be expected in its intended use which allows it to operate without unacceptable degradation.

The basic model of electromagnetic interference (EMI) is usually visualized by three states where the **Coupling** is the connection between emitted and received noise:

$$Interference\ Emitter \longrightarrow Coupling \longrightarrow Interference\ Receiver$$

In this concept the emitter is the source of the EMI and the receiver is the sink or also called victim. The coupling methods can be divided into several possible categories as shown in fig. 6.1.

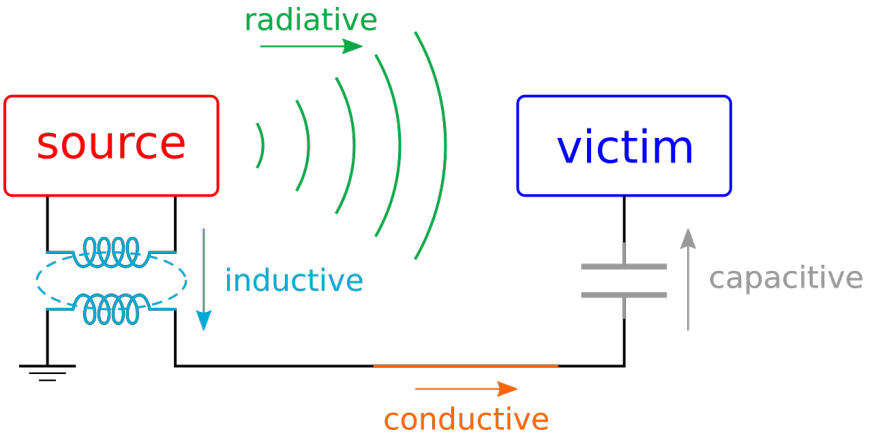


Figure 6.1.: EMC coupling mechanisms. This sketch illustrates the four possible paths for an electromagnetic interference from source (emitter) to victim (receiver): radiative, capacitive, inductive and conductive.

Radiative Coupling is characterized by the transmission of energy through electromagnetic radiation. Source and victim are typically separated by a large distance, greater than one wavelength. They can be depicted as radiating and receiving radio antennas.

Capacitive Coupling can be thought of as additional capacitance between otherwise separated but adjacent circuits. A change in the quasi static electric field transmits a voltage change from one circuit to the other.

Accordingly, **Inductive Coupling** can be thought of as additional inductance between otherwise separated but adjacent circuits. A change in the quasi static magnetic field transmits a current change from one circuit to the other.

Conductive Coupling occurs when a common impedance is shared between circuits. This may be formed by a mutual transmission line, mutual reference conductors or by a common ground, like a metal enclosure. If more than one conductive path is present, this kind of coupling can be divided into a **common-mode**, where the noise appears in phase on the impedances, and into a **differential-mode**, where the noise appears out of phase.

Mitigation strategies and methods against EMI are broadly discussed in the technical literature, e.g. [128–132]. The basic measures are quieting the sources of interference, inhibiting coupling paths and hardening the potential victims by proper grounding and shielding. However, as noise sources are usually not in ones field of responsibility or simply not accessible, the understanding of the coupling mechanisms of noise into the own device as well as the detailed knowledge about its susceptibility is most important.

In addition, it has to be ensured that other devices nearby are not disturbed by high emitted noise levels. Therefore, in the study of the EMC properties of an electronic device three categories are of major interest:

Emission, **Coupling** and **Susceptibility**

It is often stated that the costs for mitigation measures against high noise emission or susceptibility can be significantly cheaper when the EMC of the device is already considered during its design. Solutions for a finished design are often expensive or may not exist [126]. The importance of EMC considerations already during the design phase is also emphasized by its explicit mention in the corresponding EU Directive.

6.2. EMC of HEP particle detectors

As stated above, custom-made devices developed for HEP applications are not subject to the EU Directive about EMC. These regulations apply only to such equipment which is made available on the market for distribution and end consumers. It is even explicitly stated that this Directive "shall not apply to: custom built evaluation kits destined for professionals to be used solely at research and development facilities for such purposes" [127].

Nevertheless, the existence of those regulations is of course well justified as they are designed to guarantee a save and problem-free operation of different electronic devices close together or even of their combination into a larger system. The joint effort by the Belle II collaboration as well as by other HEP collaborations is exactly aiming to achieve this task in combining different subdetectors to an even more complex system where all parts have to cooperate and may not disturb each other [133].

The technological progress in electronics applies also for the development of HEP particle detectors and the same difficulties are faced. Higher switching frequencies for faster readout and processing lead to a higher noise emission, whereas lower operation voltages increase the susceptibility. In HEP applications EMI occurs for example as noise currents flowing through the cabels for power distribution and auxiliary equipment and in turn couples to the sensitive areas and reduces the signal-to-noise ratio [134]. Consequently, EMC becomes increasingly important in this field. For the largest HEP particle detectors, ATLAS and CMS, their respective collaborations performed measurements of the system's immunity against conducted and radiated

emissions present in the experimental area, as well as measurements of the electromagnetic emissions of the installations themselves [135].

One of the most recent EMC measurements for HEP particle detectors were performed in 2016 on the CMS silicon tracker detector and the SVD for Belle II [both in 134]. Both detectors are silicon micro-strip detectors and were characterized at the ITAINNOVA in Zaragoza, Spain. Their performance and EMC properties were evaluated and compared. Coupling mechanisms could be identified and countermeasures were proposed.

In addition to those measurements, a generic EMC plan to address the integration of HEP detectors in general was developed by Arteche and Rivetta [136]. An EMC plan should contain these four basic steps:

- power supply distribution block diagram per subdetector
- grounding scheme
- emission tests
- immunity tests

The PXD Power Supply design and configuration including block diagram is described in detail in [111]. The grounding of the PXD is one of the interfaces to the other Belle II subdetectors and was therefore addressed already in the Belle II Technical Design Report [71]. A detailed grounding and shielding scheme as shown in fig. 6.2 was developed by Arteche in cooperation with PXD experts and the implementation concerning the actual installation components is given in fig. 6.3. Iglesias et al. performed emission tests for the PXD Power Supply including the power distribution cables and an early PXD prototype module (electrical multi-chip module (EMCM)) in dedicated studies [137–139]. Together with colleagues from ITAINNOVA and further PXD experts we conducted the remaining emission and immunity tests for a PXD9 prototype module as discussed below.

Where usually PCBs are used to build up the circuits of electronic devices the DEPFET pixel sensors and its electric connections to the control and readout ASICs are placed on top of a monolithic silicon structure. Therefore, and to keep the material budget as low a possible to minimize multiple scattering, standardized EMI mitigation procedures like additional ground planes can not be used. In addition, the geometrical constrains made the circuit design already challenging so that a close look on the EMC properties is important to ensure a successful integration into the Belle II detector. Already during the functional test phase of prototypes, for example, internal

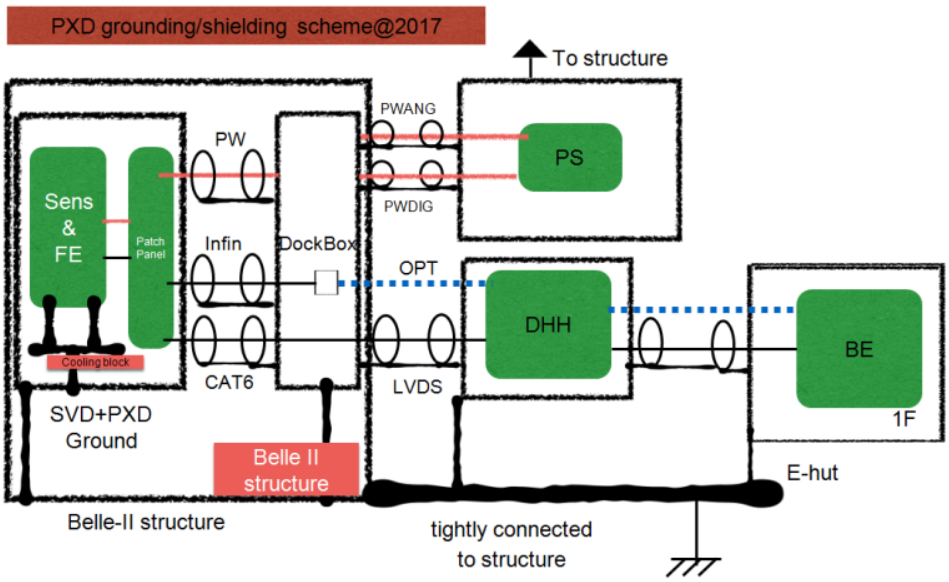


Figure 6.2.: PXD grounding and shielding scheme [138]. All cables are shielded to ensure signal integrity and reduce disturbing influences from outside. However, to avoid unwanted ground loops the shields are open at the connection on the module side.

interference of high speed data transmission lines between the DCD and DHP ASICs was observed [140]. Crosstalk between the lines resulted in specific bit error patterns, which were observed in the readout data. This was successfully cured by increasing the spacing between the lines in a next iteration of the layout and shows the importance of design verification and proper consideration of EMC already during early stages of the development process.

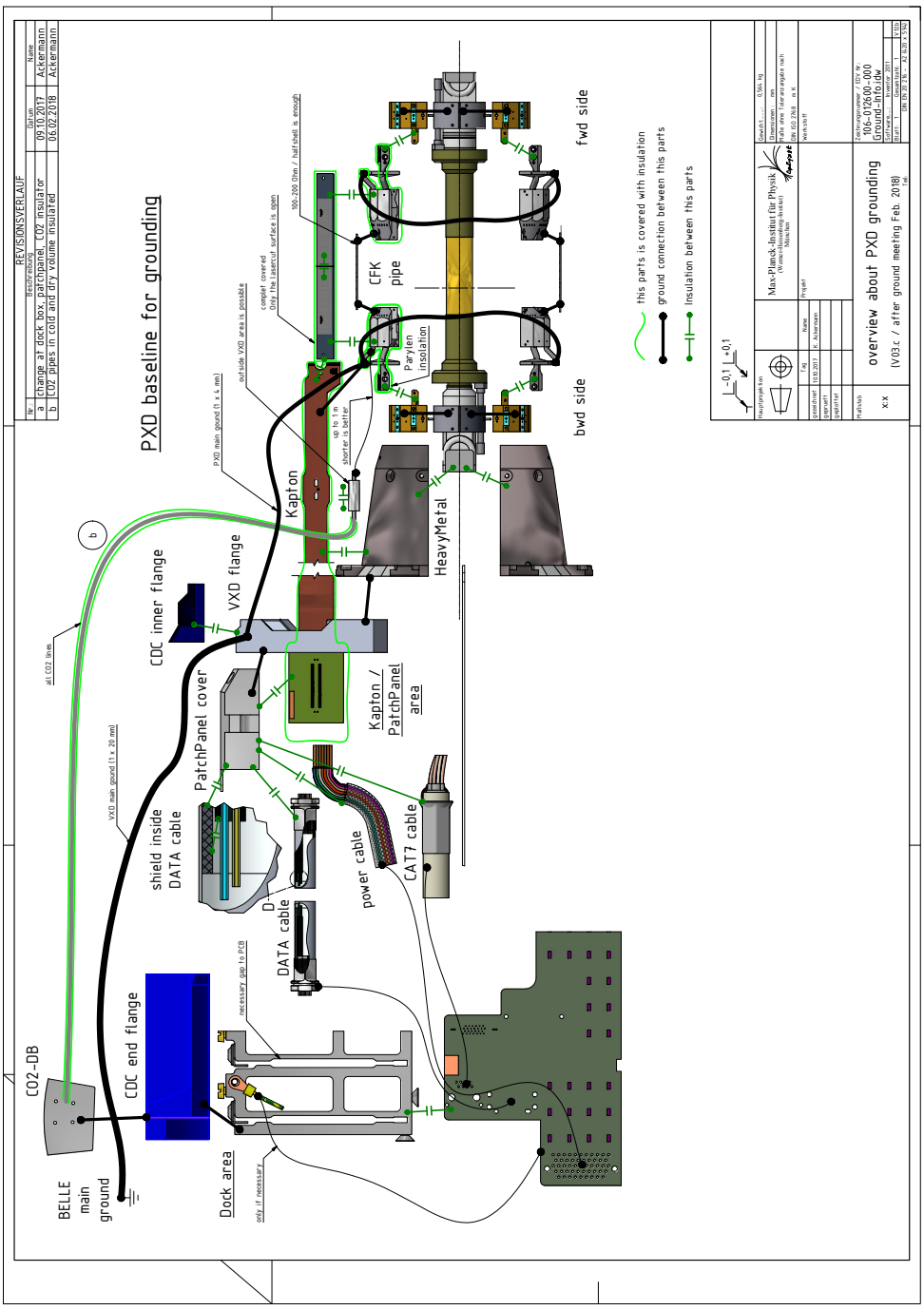


Figure 6.3.: PXD grounding and shielding implementation [141]. During the installation of the PXD2 a small adjustment was implemented. The SCB was connected to the brass piece and instead the brass piece was isolated from the beam pipe [142].

6.3. EMC measurement campaign of a PXD module

To complete the EMC plan for the PXD the recommended emission and susceptibility measurements were performed in the semi-anechoic[1] chamber of the ITAINNOVA technology center in Zaragoza, Spain. This chamber provided the required environment, as for the measurement of radiated emission it is necessary to shield the high levels of base noise, as those are often well above the emission levels [126]. Similarly, when the impact of a specific frequency and amplitude on the system should be studied, it is important to shield all other noises to ensure that the reaction of the system is solely caused by the deliberately introduced interfering signal. A picture of the installed test setup is shown in fig. 6.4.

The goal for this measurement campaign was to record the emission spectrum of a PXD module and to characterize its performance under external electromagnetic perturbation to figure out if there are specifically weak points. This knowledge is important for each installation of a PXD system, from the test setups in the laboratories to the installations for beam tests in unfamiliar environments and, not least, for the commissioning and operation of the full PXD system into the Belle II detector.

There are several different immunity tests defined by the standard, e.g. a radiated, radio-frequency, electromagnetic field immunity test or an immunity test to voltage dips, short interruptions and voltage variations [126]. For the PXD module the focus was placed on disturbances on the power lines and the susceptibility to radiated noise from the very close beam pipe. Those tests were the first EMC measurements which have been performed for a HEP particle detector based on the DEPFET technology [143].

6.3.1. Test setup description

The test system was set up as close as possible to the final detector configuration. A schematic drawing of all setup components is shown in fig. 6.5. Although almost all components were later on further optimized for the final integration into the Belle II detector, there was no major change in the system which would result in a significant impact on the EMC properties. Therefore, the results are applicable also for the final installation of the PXD detector.

[1] In contrast to full anechoic chambers, semi-anechoic chambers have a solid floor to support the devices under test and their auxiliary equipment and serve as work surface. Nevertheless, the floor is shielded against electromagnetic radiation from outside as well.

Figure 6.4.: Setup of the EMC measurement campaign of the PXD subdetector inside of the semi-anechoic chamber at ITAINNOVA. The PXD module including the electronics under test were placed on top of a table with a solid copper plane connected to the electrical ground (metallic chamber floor). The auxiliary equipment (power supplies and readout electronics) was placed on the floor next to the table and connected to the PC for control and data analysis.

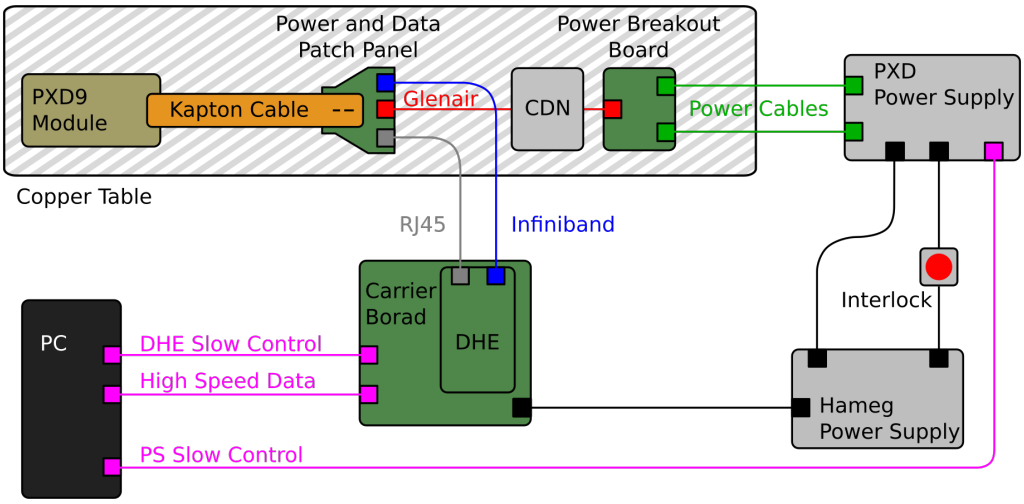


Figure 6.5.: Schematic drawing of the PXD test setup for the EMC measurements. In contrast to the installations of test setups in the laboratory, the module was not placed into a black box but on top of a copper table which served as electrical ground. In addition, a Coupling Decoupling Network (CDN) was integrated to the power cables.

The PXD module W30_OB2 served as Device Under Test (DUT) (see fig. 6.6 for a picture of the module). It was part of the pilot production run with the so called PXD9 layout. The thickness of the sensitive area was 300 µm instead of 75 µm used for the final design. The ASIC versions were the next to final ones with DHPT 1.0, DCDBv4 pipeline and SwitcherB18v1.

The connection of the Kapton Cable to the Power and Data Patch Panel was still realized in an interim scheme with two connectors instead of a single one. As usual for a laboratory setup, individual cables were used for the high speed and slow control signals as well as for the power lines: Infiniband, RJ45/Ethernet and Glenair, respectively. Different from the final design, where at the Dock Box the power and data lines are transferred from the inner cables to the cables outside of the detector volume and where the data lines are switched to optical transmission, here only the power lines were transferred by the Power Breakout Board to the final, 15 m long power cables. The data lines, instead, were connected directly by copper lines from the Patch Panel to the DHE.

In order to have a well defined ground, the module and the described equipment were placed onto a copper plane on a table as suggested by EN 61000 [144]. The remaining parts of the setup rested on the floor which was electrically connected to the copper plane and served as large grounding plane as well. The data and slow control lines were directly connected to the DHE via an Infiniband cable and an RJ45 Ethernet cable, respectively. Instead of the nominal clock frequency of 76.33 MHz we

set the system clock GCK provided by the DHE to 62.5 MHz in order to improve the link stability and data taking reliability. This is considered in the discussion of the results. While the hardware of the PXD Power Supply and the DHE was already in the final state, their firmware versions were, and are still, developed further. A four channel primary power supply (HAMEG HMP4040) powered the supplementary PXD equipment. We installed a dedicated PC to run the software for module operation and data acquisition as well as for data analysis.

We used a bulk current injection probe connected to a radio frequency (RF) signal generator with adjustable amplitude as external noise source. The injected noise current was measured using an inductive current clamp and a spectrum analyzer.

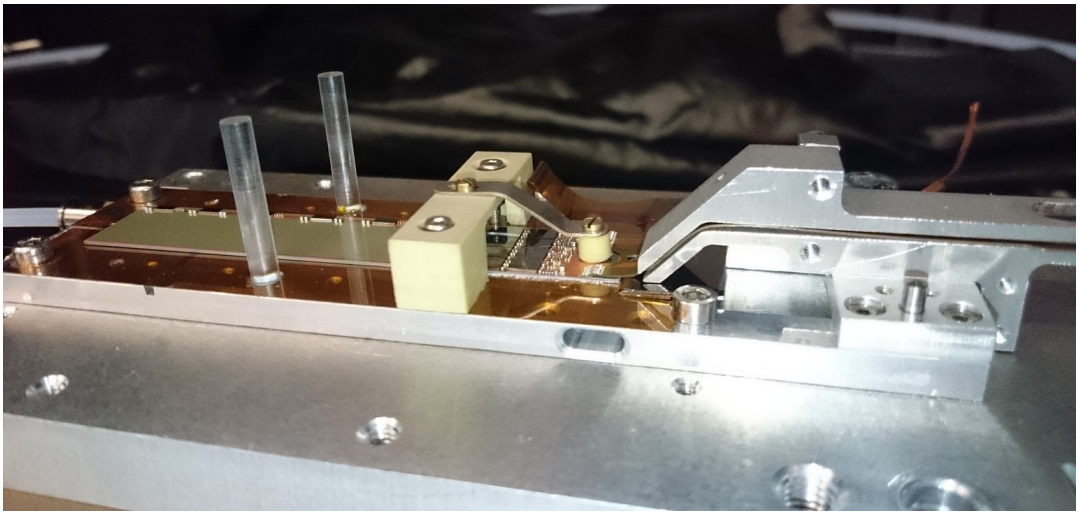


Figure 6.6.: Device Under Test for the PXD EMC measurements: W30_OB2. The bare module is shown without the protective cover on top. It is pressed down to the supporting aluminum block by a metal spring attached to a 3D printed bridge across the module. A layer of Kapton tape was placed between the module and the not coated supporting block as electrical isolation.

The test setup was different from the usual laboratory setup as described in chapter 5 in two aspects. It was not possible to bring a large black box to the testing facility which is typically used to darken the light-sensitive modules. Instead, we used dark synthetic fabric and a cardboard box to shield the ambient light and ensure a sufficiently stable background. The second difference was the Coupling Decoupling Network (CDN), which was integrated in the power lines at the Glenair power cable. Its purpose was to separate the DUT from the PXD Power Supply so that external noise was filtered and any disturbance signal coupled to the power lines on the module side could not propagate to the Power Supply side. Hence, making it possible to observe the reaction of the DUT independently.

A sketch of the CDN circuit is illustrated in fig. 6.7. The individual wires of the Glenair cable were opened in the middle of the cable and connected to a breadboard with a dedicated RLC circuit[2] for each connected line to decouple the module from the Power Supply. The breadboard was mounted in a metal box which shielded the circuit and served as good ground connection at the same time. Not all 51 wires of the Glenair cable were attached to the CDN box. We put the focus on the supply voltages of the ASICs and the presumably most sensitive operation voltages of the DEPFET matrix. Across all four Power Supply domains 14 lines were chosen beforehand and equipped with the shown decoupling circuit. The other lines simply bypassed the CDN box. The lines connected to the CDN box were:

dgnd	agnd	source
dhp-core	dcd-avdd	gate-on1
dhp-io	dcd-refin	ccg1
dcd-dvdd	dcd-amplow	drift
sw-dvdd		hv

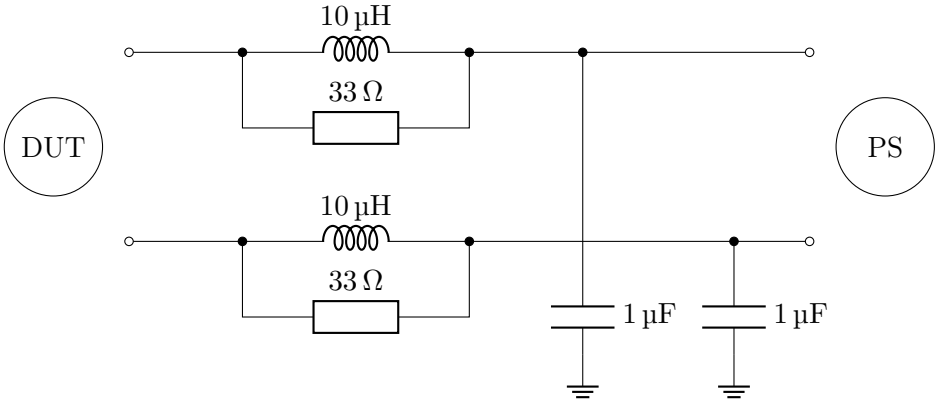


Figure 6.7.: Schematic sketch of the Coupling Decoupling Network (CDN). Two exemplary lines are drawn as an illustration. All of the 14 connected lines were handled in the same way.

Only at the end of the measurement campaign it was realized that the specifications of the components of the CDN were not chosen sufficiently for the lines carrying the most current, especially dcd-avdd and agnd. As result, for most of the measurements the largest power consumers on the module, the DCDs, were not biased correctly, as the nominal voltage for dcd-avdd was not reached. The issue was resolved and several measurements were repeated with the nominal biasing and the characteristic shape of the response curve stayed the same. This will be demonstrated in detail below in section 6.5.2.3. Therefore, it is justified to state that the results were not affected by the insufficient power supply to the analog lines dcd-avdd and agnd.

[2] An RLC circuit consists of a resistor (R), an inductor (L) and a capacitor (C).

6.3.2. Test setup performance

For the measurement of the EMC characteristics of a particle detector the behavior of each readout channel of the Front-End Electronics (FEE) should be analyzed individually. In the case of the PXD the FEE is composed of the electrical circuit on the module including all ASICs and the DEPFET pixels of the matrix. Each individual pixel represents one readout channel. In principle, a single PXD module provides 192 000 pixels but due to a variety of possible circumstances, like opens or shorts in the matrix and pixels out of the dynamic range, a certain fraction of them might not be suitable for operation. For the final detector production values above 99 % working pixels were aimed for and also achieved (see section 7.5). For the pilot production module W30_OB2, however, this value was lower for the following reasons.

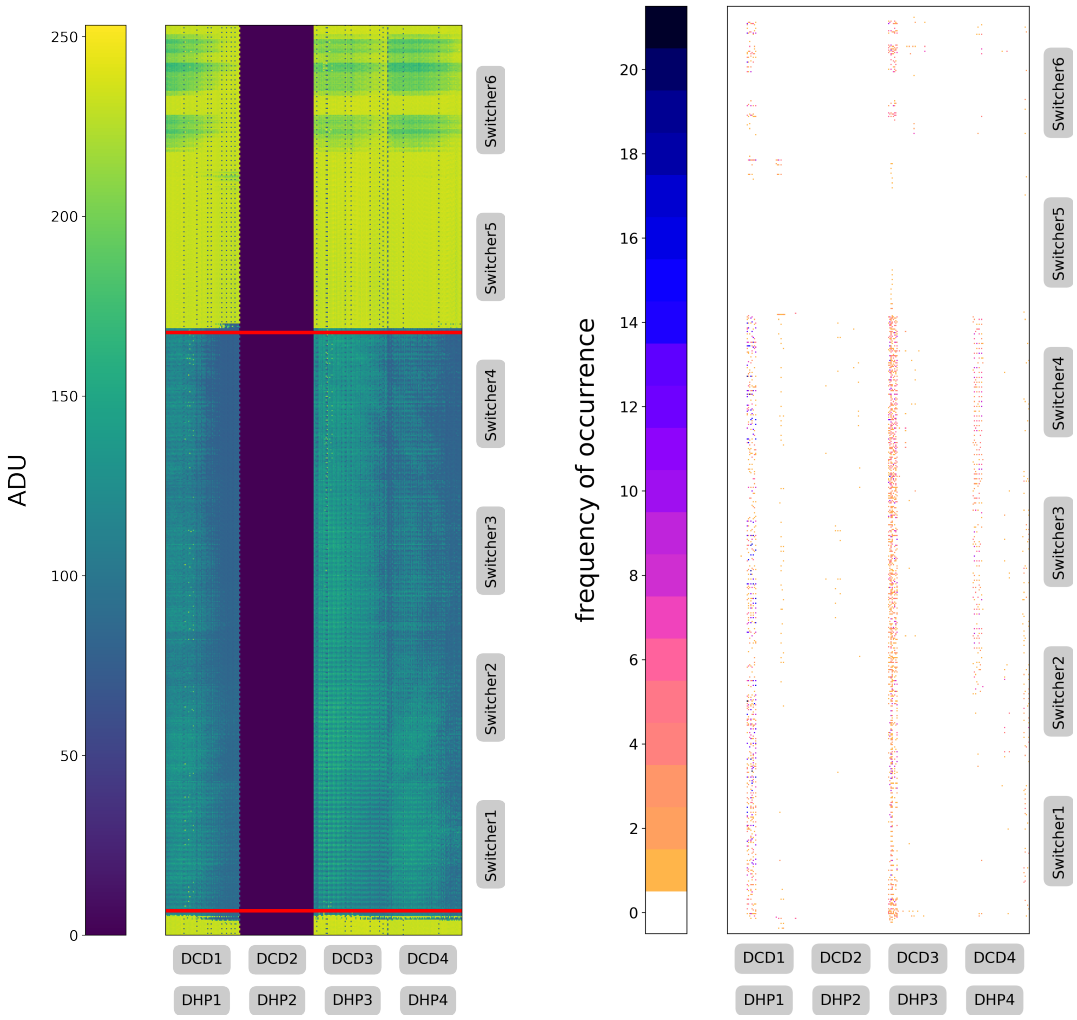
The connection between the Kapton Cable and the Power and Data Patch Panel was established with two individual connectors, one for the data lines and one for the power lines. This configuration was a result of the progressing development of the auxiliary PXD equipment. Different teams of colleagues developed the data [107] and power [111] regimes and initially separated Patch Panels were provided. The first step of merging them to a single PCB kept the configuration with two individual connectors. Only in a further iteration those were combined to a single connector as it turned out that the reliability of the connection with two individual connectors was too low[3]. Therefore, during the EMC measurements the present configuration resulted in one of the four data links of the module being not stable enough for reliable data transmission. It was not possible to establish the high speed link of DHP2 and to readout data from this fourth of the matrix.

In addition, one of the three gate-on regimes on the module, gate-on3, did not work properly and the corresponding region controlled by Switcher5 and Switcher6 delivered too high ADU values exceeding the dynamic range of the DCDs. This third of the matrix was also not available for the EMC study.

Both issues are clearly visible in fig. 6.8a which shows the matrix response at the beginning of the measurement campaign. The mean ADU value for each pixel of the matrix (calculated from 1 000 pedestal frames) is displayed in geometrical orientation as present on the matrix. All pixel values for DHP2 are set to 0 ADU as default value for missing data.

In the shown pedestal plot a sudden jump to higher values at the transition between Switcher4 and Switcher5 stands out. More current flows to the DCDs which sig-

[3]The tolerances of soldering the connectors were higher than the tolerances for the contact pins resulting in stress on the pins and loss of connections.



(a) Mean ADU values over 1 000 pedestal frames for the entire matrix.

(b) Map of noisy pixels over all calibration runs without noise injection.

Figure 6.8.: Performance status of the sensitive matrix of the DUT at the beginning of the measurements. (a) The not working data link of DHP2 and the region affected by the gate-on3 supply line can be easily distinguished from the properly working areas. The red lines indicate the cut made for data analysis. (b) All noisy pixels detected over all performed calibration runs during the measurement campaign are indicated with their frequency of occurrence. They accumulate in the left parts of each DCD.

nificantly exceeds the dynamic range. As the readout of the matrix continuously performs the rolling-shutter mode readout and immediately starts over from the beginning when it reaches the end, also the very first gates are affected. The ADCs are still saturated and need about 0.6 µs to relax down to the nominal working point. The affected regions are cut from the data for analysis. In particular, gates 5 - 127 were used (indicated by the red lines in fig. 6.8a) for DHP1, DHP3 and DHP4 corresponding to drains 0 - 255 and 512 - 1023. This includes also the six not connected ADCs per DCD. Removing those as well, a total number of 92 250 physical pixels remains.

In addition, a number of broken drain lines lower the amount of active pixels. Those not responding pixels can also be seen in the pedestal plot. They are best visible in the bright regions of Switcher5 and Switcher6 where these non working pixels stay at low ADU values. In the electrical mapping they appear as straight lines representing the disconnected drain lines. Out of the total 750 drains for the three DCDs, we identified 20 drains to be disconnected and removed them from the analyzed channels as well. In the end still 90 870 working pixels remain for the analysis.

However, in addition to the working pixels it is possible to take advantage of those channels, which were intentionally not connected or unintentionally disconnected from the matrix, and use them as reference to analyze effects in the electronic part independently from effects in the matrix.

Besides these global cuts on the pixel selection also the individual performance of each pixel was taken into account regularly during the measurements by monitoring the intrinsic noise. Calibration runs were taken at the same operational parameters as during the measurements but without external noise injection. Each time the pixel noise was calculated from 1 000 pedestal frames and a mask was created containing all pixels with a noise value of 15 ADU or above. In addition, a complete drain line was masked when it contained more than 8 noisy pixels. Masked pixels and drains were ignored for all following measurements until the next calibration run aka. mask run was performed and the calculations for masking were repeated. Figure 6.8b) shows the distribution of all noisy pixels determined in this way. The color indicates the frequency of occurrence of each pixel in all of the 30 mask runs taken during the complete EMC measurement campaign. The plot reveals an accumulation of noisy pixels in the left part of each DCD where DCD3 is affected the most. At least a major part of this effect can be attributed to the insufficient powering of the DCDs due to the CDN configuration as shown later in section 6.5.2.8. There are no noisy pixels shown for DCD2 as no data could be taken for this region.

A detailed analysis of the distribution of noisy pixels within the DEPFET matrix of the studied PXD module and their development over time during the measurement campaign can be found in appendix A. There, also the influence of the CDN on the

power supply of the module and an adjustment of the CDN during the measurement campaign is described in detail. In section 6.5.2.3 it will be shown that this issue had no effect on the susceptibility analysis of the PXD module.

6.4. Electromagnetic emission

Iglesias [139] measured and analyzed the electromagnetic emissions of the individual PXD system components and described the results in detail in his thesis. He investigated the PXD Power Supply and the power cables individually as well as a system with an early PXD prototype module (EMCM) and a system with a PXD9 module. The measurements for the PXD9 system were performed during the EMC measurement campaign in Zaragoza with the setup described above.

The analysis shows that the conducted noise of the PXD Power Supply can be considered to be low and close to ambient noise levels. Nevertheless, a filter was proposed [139, p. 72]. Equally, the radiated electromagnetic field emissions are very low in all operation modes (see fig. 6.9). The PXD Power Supply benefits in this respect from its metal enclosure which acts as shield, although not all sides are entirely covered as openings are left for air cooling.

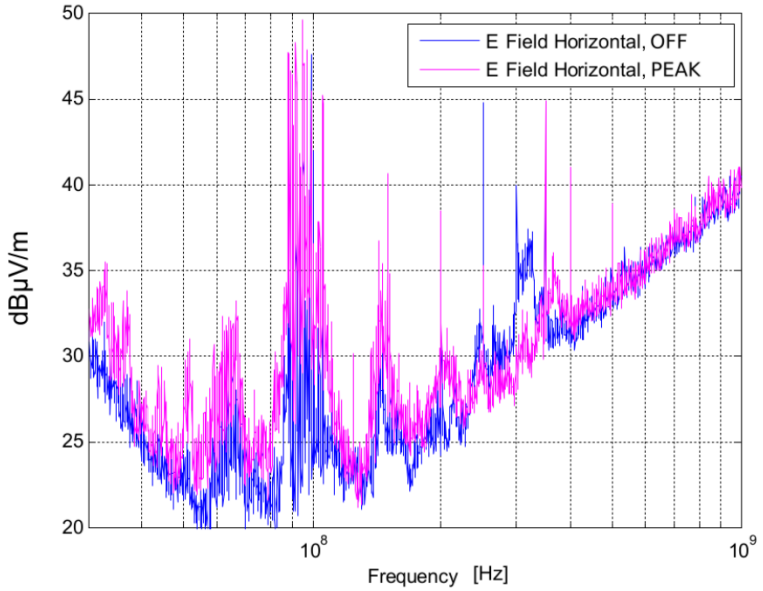


Figure 6.9.: Radiated electromagnetic field emission of the PXD Power Supply measured in horizontal polarization [139]. Comparison between system states OFF (Power Supply on but outputs not yet activated) and PEAK (with dummy load).

Concerning the measurement of the FEE, the results for EMCM and PXD9 module are comparable. The predominant mode of conducted noise propagation is in both cases the common-mode and the highest emissions occur when the modules are completely powered and in data taking mode (PEAK) [139].

The overlay of the emission measurements of the PXD Power Supply and the PXD9 module (see fig. 6.10) shows that the emissions of the FEE are predominant below 1 MHz and above 10 MHz whereas in specific areas between these values the emissions of the PXD Power Supply are predominant. Most of the conducted noise is emitted in the range of 9 kHz to 1 MHz and 10 MHz to 50 MHz. The limits of the EU standard CISPR 32 for industrial multimedia equipment [145] are not kept over the entire frequency range. However, we do not expect a severe impact on other subdetectors as the exceedances of the PXD9 measurement are not severe. Furthermore, it is possible to identify important operation frequencies of the PXD module and explain distinct peaks in the recorded emission spectrum. The frame rate at 40.69 kHz and the gate rate at 7.81 MHz including their respective harmonics shape dominant structures of the spectrum. For operation at the nominal GCK clock, these frequencies would be shifted to 49.69 kHz for the frame rate and to 9.54 MHz for the gate rate.

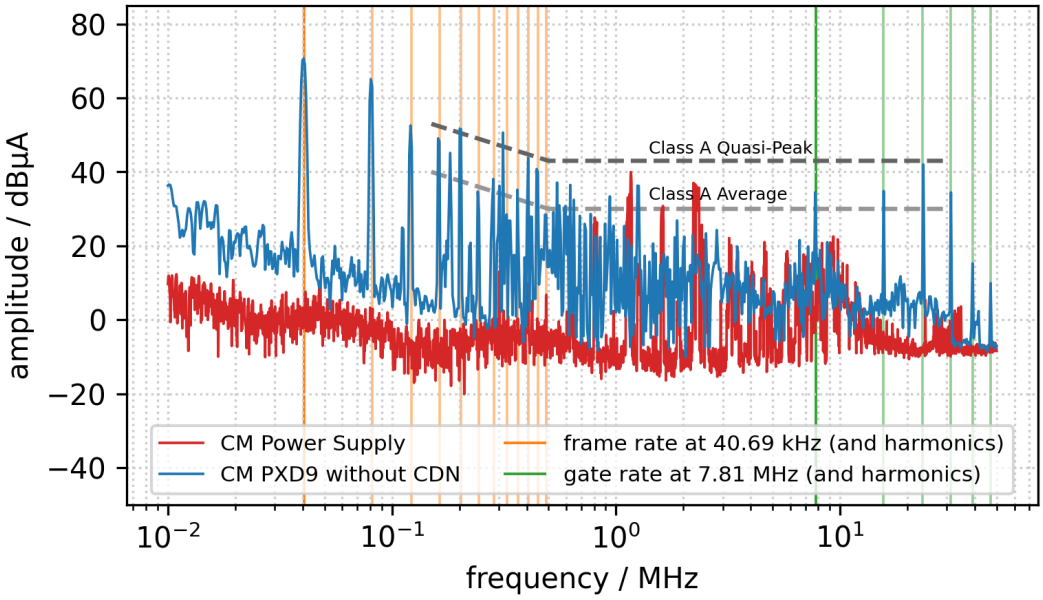


Figure 6.10.: Conducted common-mode emission of PXD Power Supply and PXD9 module. The most significant spikes in the recorded PXD9 emission spectrum correspond with the frequency values of the frame rate and the gate rate and their harmonics. The emission requirements from the CISPR 32 EU standard are shown for comparison.

Additionally, peaks at about 183 kHz and at about 313 kHz with respective harmonics can be found in the spectrum of the PXD9 module[4]. However, their origin could not be assigned unambiguously. They do not occur in the Power Supply spectrum and might originate from the DHE whose emission was not recorded individually.

With the recorded spectra we documented the frequencies where the PXD system has the highest electromagnetic emissions and their magnitude. It is now possible to compare these values to the susceptibility of other subdetectors and to judge if existing noise in a system can be attributed to the PXD.

[4]The peak at 313 kHz is also present in the EMCM emission spectrum.

6.5. Electromagnetic susceptibility

To conclude the EMC plan for the PXD a variety of immunity measurements were performed. In a first step the high speed data link stability was tested under the influence of external noise. Further on, the system's susceptibility to external perturbation was analyzed by recording pedestal data and calculating the resulting noise for different frequencies and amplitudes of the perturbing signal.

As proposed by Arteche et al. [146] we used a frequency generator and a current probe to inject a perturbing sine-wave signal through the input power cables while a second current probe was used to monitor the injected current. The setup was prepared so that it was possible to pick specific power lines for noise injection in order to differentiate between common-mode and differential-mode noise and to investigate even single lines (see fig. 6.11). In addition, the beam pipe was imitated to simulate radiated noise emitted from perturbation currents on the outer surface of the beam pipe.

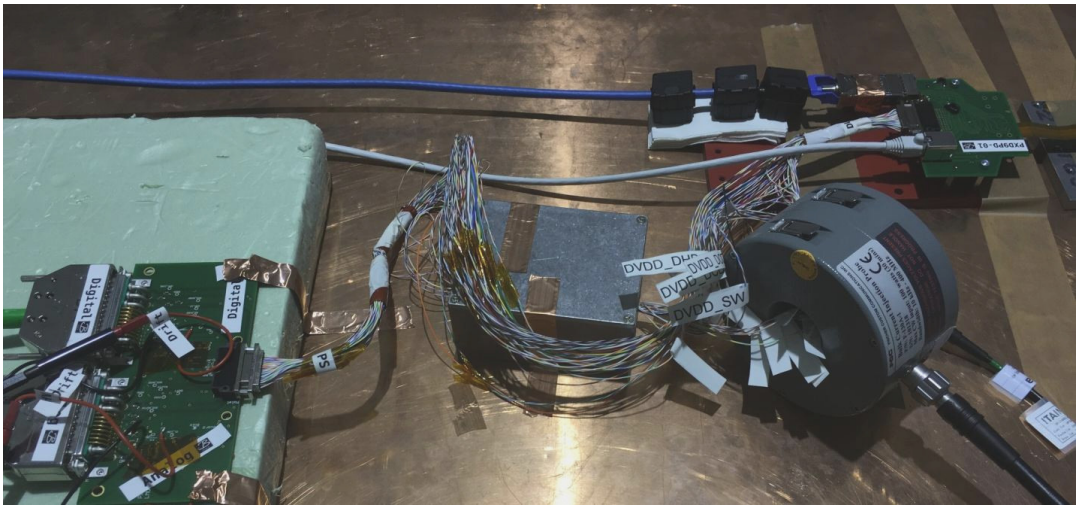


Figure 6.11.: Noise injection into the power distribution lines with an bulk current injection probe [139]. The Glenair cable connects all power distribution lines from the Power Breakout Board (left) to the Patch Panel (right) via 51 wires. While the cable is shielded under normal operation, we opened the shielding to access the individual wires for systematic noise injection. The current probes (front right) are installed on the module side of the CDN box (center).

On basis of the recorded measurements transfer functions were created for the different types of noise coupling which quantitatively describe the susceptibility of the PXD to specific noise frequencies. Out of all evaluated power distribution lines the gate-on line is the most vulnerable. The PXD is less susceptible to radiated noise,

whereas it is most vulnerable to conducted noise in the frequency range between 5 MHz and 50 MHz. The maximum of the susceptibility lies between 8 MHz and 20 MHz. Subsequently, we calculated a maximal allowed perturbation current for the PXD to keep the contribution of external noise below 25 % of the intrinsic noise. Overall, the results demonstrate a good robustness of the tested PXD module against external perturbation. We expected an unobstructed operation of the PXD which was finally confirmed by the successful operation of the PXD during Phase 3 of the Belle II experiment.

6.5.1. Stable data link operation

A stable data link operation is essential for the successful operation of the PXD. Occasional link drops during the characterization measurements in the laboratories may be cured with a simple link reset and a repetition of the affected scan. A lost link during physics data taking, however, results in an irretrievable data loss and deterioration of data taking efficiency leading to less recorded luminosity. As the link stability was a critical issue for almost all prototype modules, which often required to reduce the system clock frequency to 62.5 MHz instead of the nominal 76.33 MHz, the data transmission system from the DHPs to the back end electronics was constantly optimized. In the final implementation the data links take only the rather short distance of about 2.5 m to the Dock Boxes on copper lines where they are transferred to optical fibers for the remaining distance of about 15 m between the Dock Boxes and the DHHs on top of Belle. The tested configuration matches the remaining copper connection between module and Dock Box, but with reduced system clock frequency.

We started the link stability measurement by injecting noise into the dcd-avdd and dcd-amplow lines. For each frequency, we increased the amplitude of the perturbation signal until the first of the three working data links was lost or the maximal injection current was reached. We repeated the measurement after the adjustment of the CDN. In this configuration the dcd-avdd line effectively bypassed the CDN, so we injected the noise only into the dcd-amplow line. However, the characteristic shape of the curve stays the same (see fig. 6.12).

The data links are most stable below a noise frequency of 1 MHz, for some frequencies below this value none of the links dropped even at the maximal available amplitude. For increasing frequencies up to 40 MHz the stability decreases. A local maximum occurs at around 0.8 MHz to 1.0 MHz. The data links are most vulnerable in the range between 30 MHz and 100 MHz and especially at 250 MHz. In both measurements, data link 4 is the weakest although the results are more evenly distributed over the three links for the configuration with nominal voltages supplied.

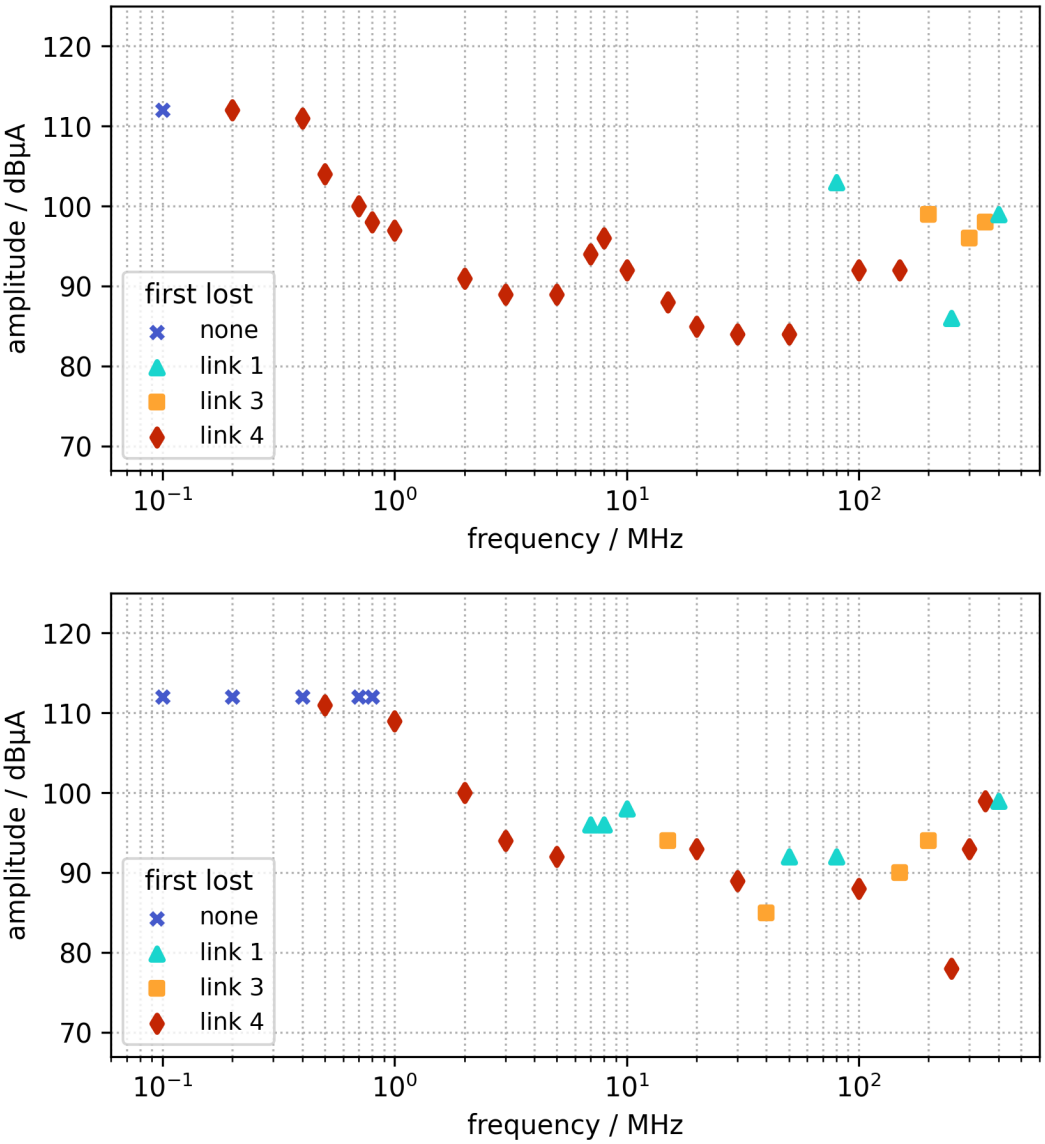


Figure 6.12.: Noise susceptibility of stable data link operation. The amplitudes of the injected noise when the first of the three working data links was lost are plotted against the tested frequencies. Color and shape of the markers indicate which link was lost first. The dark blue cross is used when no link was lost even at the highest available noise amplitude. Compared to the initial situation where the power distribution was affected by the CDN (top) the link stability increased with nominal voltages supplied (bottom) mostly in the lower and middle frequency range up to 50 MHz.

6.5.2. Effect of coupled noise on pedestal data

In order to receive normalized response functions for the tested module the impact of external noise on pedestal data was analyzed. Therefore, we injected the noise signals through different sets of power distribution lines and in addition tested against radiated noise from a beam pipe dummy. Transfer functions describing the system's susceptibility to external perturbation were calculated from pedestal data recorded for various noise configurations at different frequencies and amplitudes.

The PXD module reacted most vulnerable to noise injected into the gate-on1 line. While the module's response is larger for common-mode noise compared to differential-mode noise, the differences between lines are significantly higher. The susceptibility to radiated noise below about 40 MHz is more than a magnitude lower compared to conducted noise coupled to the power distribution lines. For frequencies below 100 MHz the contribution from the DEPFET matrix' response to noise is significantly higher than the one from the readout electronics. The noise distribution within the channels changes with frequency and for different noise configurations. No particularly sensitive region was found.

6.5.2.1. Measurement method

Following the approach of Arteche et al. [134] a noise signal was injected in form of a sine wave at different frequencies and amplitudes which perturbs the FEE by adding a noise component to the intrinsic noise component of the FEE. For conducted noise injection we chose different combinations of power distribution lines (see fig. 6.11) to test for particularly vulnerable lines and differences between common-mode and differential-mode noise. For radiated noise injection the beam pipe was imitated using a thick wire installed directly above the module cover. The noise currents were injected into this wire and the impact of the radiated noise was recorded. Calibration data without noise injection was taken regularly to determine the system's intrinsic noise. Each measurement consisted of 1 000 pedestal frames recorded consecutively.

Data from "virtual" pixels was used to differentiate between the noise response of the DEPFET matrix (including Switchers) and the readout system of DCDs and DHPs. There are six ADCs in each DCD which are not connected to any drain line. The broken drain lines identified on the tested module have effectively the same result as their lines are open already before the first pixel[5]. No current from the matrix

[5] On other modules also partially broken drain lines were observed. When the open appeared

is flowing into the ADC but the digitization process is carried out in parallel with the other ADCs. Therefore, values independent from the influence of the matrix are available.

6.5.2.2. Transfer function

The definition of the transfer function follows after Arteche et al. [134, 139, 143, 147]. For this PXD study the noise of each channel is defined as standard deviation of the channel's pedestal values over all recorded frames. From the calibration runs without noise injection the intrinsic noise is calculated as baseline for all coming measurements until a new calibration run was taken. A discussion about different contributions to intrinsic noise for transistors and readout electronics in general and for DEPFETs in particular can be found at [51, 148–150]. The most important contributions are thermal noise, 1/f noise and shot noise. We assume that the intrinsic noise and the contribution of the external perturbation are uncorrelated and therefore add up in a quadratic way [134]. Hence, the external part of the noise N_{ext}, which is solely caused by the artificial perturbation from outside, is given by:

$$N_{ext} = \sqrt{N^2_{measured} - N^2_{intrinsic}} \tag{6.1}$$

For each configuration of selected power distribution lines and noise frequency f the response of the module was monitored. The perturbing current $I_p(f)$ was increased until either the additional noise was clearly visible in online data, the maximal injection amplitude of the frequency generator was reached, or the link stability limited the data taking. Therefore, we have to set the calculated external noise component $N_{ext}(f)$ into relation to the applied noise currents to reach a normalized system response called transfer function $TF(f)$.

$$TF(f) = \frac{N_{ext}(f)}{I_p(f)} \tag{6.2}$$

A transfer function was calculated for each pixel and each injection scheme. After the cuts described in section 6.3.2 a maximal number of 90 870 working pixels remained, but due to additional cuts for several hundred noisy pixels the numbers

somewhere in between two gates in the DEPFET matrix, the part closer to the DCD can still be read out. The broken drains on the tested module were all entirely disconnected from the matrix.

are typically a bit lower. The curves of the transfer functions describe the susceptibility of the individual data channel over the measured frequency range (see fig. 6.13).

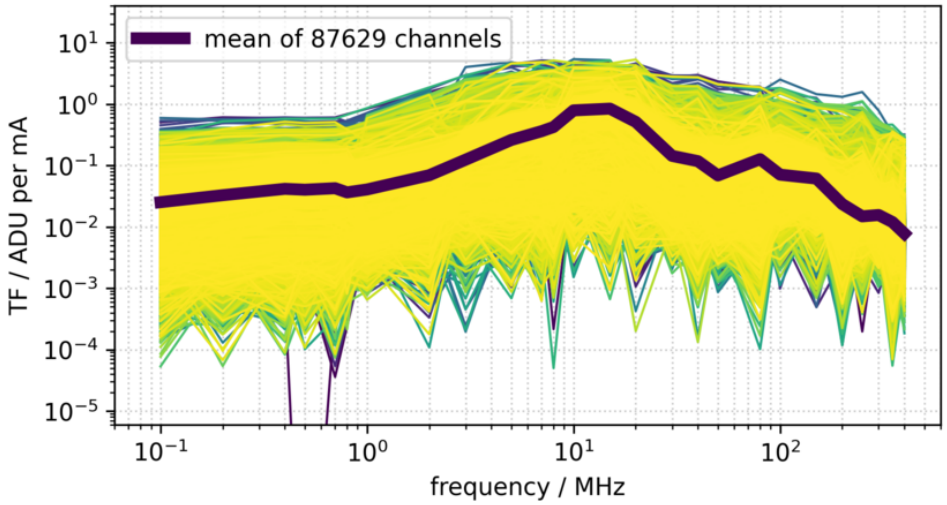


Figure 6.13.: Transfer functions of all working pixels for conducted common-mode noise injected into the analog supply domain. The noise was injected into agnd, dcd-avdd, source and dcd-refin lines. The 87 629 individual curves are color-coded sequentially with the last curves plotted on top with the lightest color. The mean of all lines is shown as dark thick line on top.

6.5.2.3. Data quality

The recorded pedestal data was prepared by focusing on the parts of the matrix with the best performance. The gate-on3 region was cut away due to values out of the dynamic rage of the DCDs and the region of ASIC pair 2 was omitted as the data link was not working (details in section 6.3.2). The remaining parts of the working matrix are associated with the ASIC pairs 1, 3 and 4 and, therefore, referenced as regions 1, 3 and 4. Occasional data link drops of one or more links during the recording of 1 000 pedestal frames resulted in pedestal values of 0 for the entire region in affected frames (see figs. 6.14 and 6.15). The data of each region was filtered for partially empty frames to receive a correct mean and noise value from only valid data frames.

Also the effect of the improper components in the CDN, which resulted in an insufficient power supply of the DCDs (details in appendix A), was analyzed. The issue was spotted only at the end of the measurement campaign after the majority of the data was already recorded. After the CDN was changed to restore the nominal

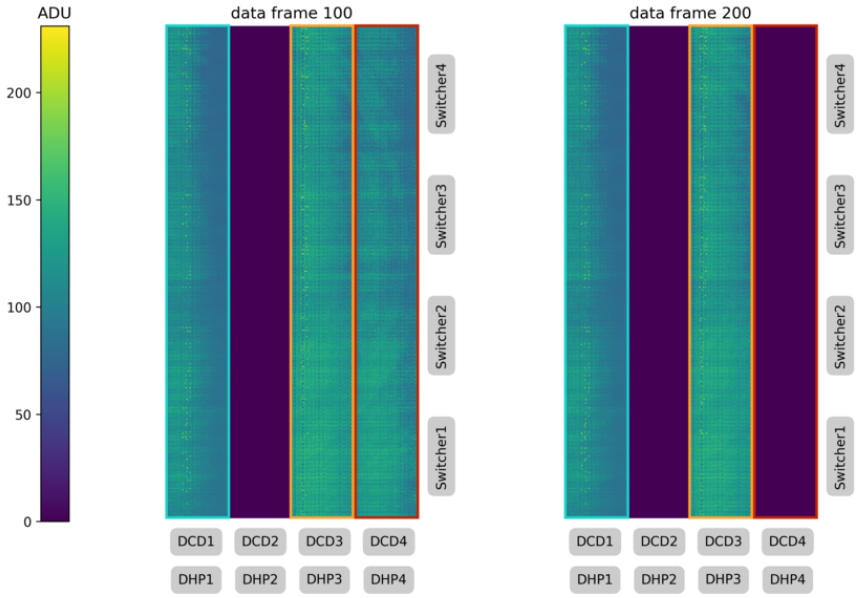


Figure 6.14.: Comparison of two data frames from the same run with link drop during data taking. Only the previously defined region with good performance is shown. Data frame 100 shows data from all three working ASIC pairs, whereas the fourth column in data frame 200 is empty due to the lost data link on the fourth DHP. The three regions of the matrix associated to the ASIC pairs are highlighted by the colored frames.

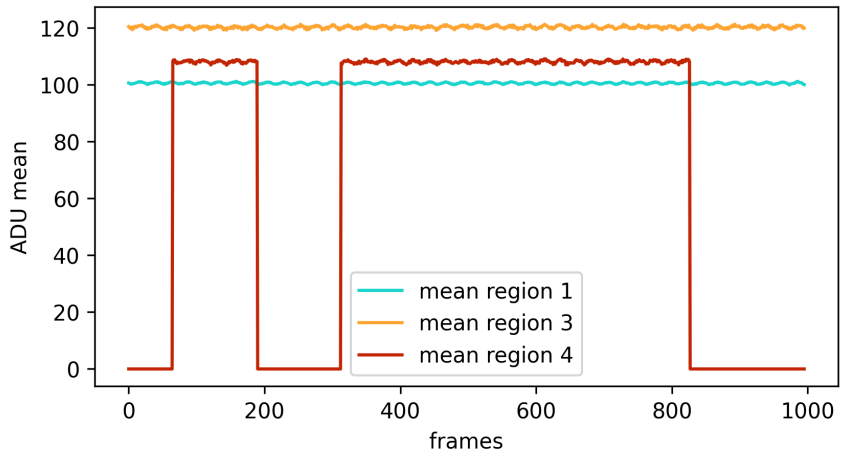


Figure 6.15.: Course of calculated mean per frame during a run with dropping data link. The breakdown is confined to the region associated with the lost data link. The graph illustrates one example measurement. It is possible that the connection was reestablished and lost again several times during data taking.

power supply to the DCDs one entire measurement was repeated and for several other measurements three reference points each.

The comparison of the measurement for conducted common-mode noise injected into the digital power domain, which was repeated for all frequencies, shows a good agreement of the calculated mean curves of all transfer functions (see fig. 6.16). With the restored nominal power supply the spread of the individual transfer functions per pixel is significantly lower for frequencies below 40 MHz; the channels behave more homogeneously under nominal supply. Also the variations between the three regions are reduced for frequency below 10 MHz (see fig. 6.17). Before the change the lowest disturbance was always seen in region 1, the highest in region 4. This corresponds to a large number of undersupplied pixels in region 1 which yielded lower ADU values and a weakened response to noise compared to the other working pixels as described below in the analysis of noise distribution (see section 6.5.2.8). However, the characteristic shape and also the absolute values of the mean curves over all channels are comparable. The results are not affected by the insufficient dimensioning of the CDN components and the insufficient power supply of the DCDs during data taking.

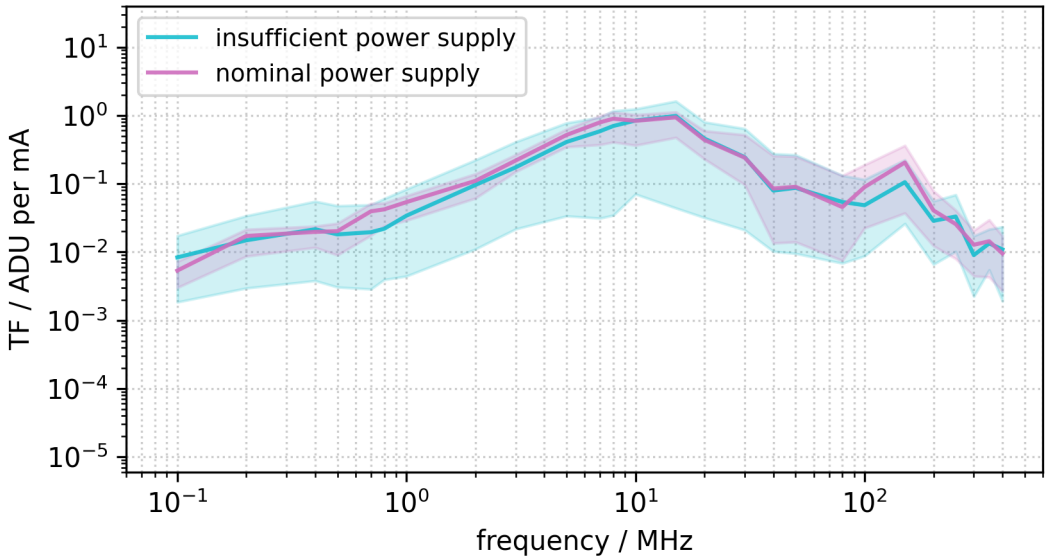


Figure 6.16.: Comparison of calculated transfer functions before and after the change in the CDN for the same measurement settings. The noise was injected into dgnd, dcd-dvdd, dhp-core, dhp-io and sw-dvdd lines. After the change in the CDN this measurement was repeated with otherwise same settings. The 5-to-95-percentile-band around the mean curve reduces largely for frequencies below 40 MHz. The calculated mean curves show good agreement between the two measurements.

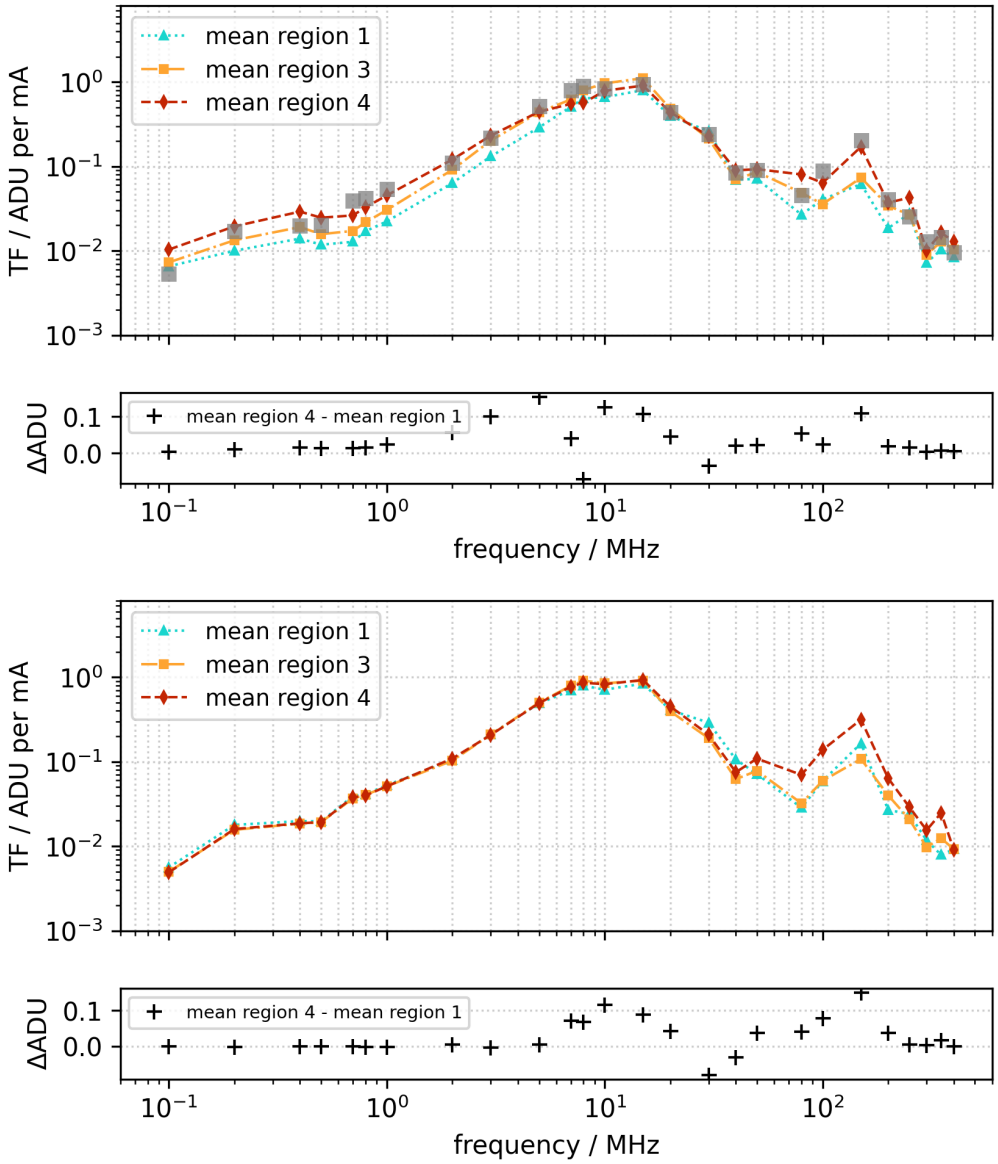


Figure 6.17.: Comparison of transfer functions of the three matrix regions before and after the change in the CDN for otherwise same measurement parameters. The noise was injected into the dgnd, dcd-dvdd, dhp-core, dhp-io and sw-dvdd lines. Before the change (top) there is a spread between the regions below about 10 MHz which is no longer present after the modification (bottom). The gray squares in the plot of the first measurement indicate the mean over all channels from the repeated measurement as references.

6.5.2.4. Conducted noise on power distribution lines

The results of the individual measurements are visualized as boxplots which show in addition to the mean and median values of the transfer functions for each measured frequency also the data distribution of the almost 90 000 analyzed channels. The size of the boxes indicates the interquartile range from the 25th percentile to the 75th percentile. The length of the whiskers is set to contain 98 % of the channels; only the upper and lower 1 % outliers each are drawn as gray circles above and below, respectively. If reference measurements after the adjustment of the CDN with the nominal power supply for the DCDs are available, the former data point is replaced with the result from the later reference measurement. The resulting plots of all recorded measurements are collected in appendix B for a complete documentation. Here, the focus will be placed on two examples and the general results.

The measurement with noise injected into all nets connected to the CDN might be closest to the system's reaction to noise which appears on all power distribution lines in the same way (see fig. 6.18). The susceptibility to noise frequencies below 1 MHz stays almost constant on a relatively low level, before it reaches a minimum at 2 MHz followed by a steep rise to the maximal susceptibility at 10 MHz. With increasing frequencies the values decrease again. A local maximum occurs at 100 MHz. The values are down to the previous minimum value again at the highest measured frequency of 400 MHz. For frequencies above 20 MHz the size of the boxes increases which means the spread between the channels increases. This applies for all measurements but is especially visible for the measurement with nominal power supply where the channels reacted in general more homogeneously (see figs. 6.16 and B.3).

For the measurement of conducted noise injected into the gate-on1 line the resulting values are over the entire frequency range higher than for any other measurement (see fig. 6.19). The spread for low frequencies below 0.5 MHz is increased. The minimum lies already at 1 MHz, the maximum between 10 MHz and 20 MHz. The shape of the curve is similar to the previously discussed measurement. However, the local maximum is less prominent and shifted to a higher frequency of 150 MHz. For the reference points at 1 MHz and 10 MHz the interquartile range is significantly lower and also the whiskers are significantly shorter compared to the points recorded with insufficient power supply. This effect is not visible for the third reference point at 100 MHz which confirms the observation of a higher spread between the channels for higher frequencies.

The course of the retrieved transfer function depends primarily on the selection of power distribution lines on which the noise occurs. Furthermore, it is possible to draw some conclusions from the combined results of all investigated configurations of conducted noise injection (see fig. 6.20). The PXD module reacts most vulner-

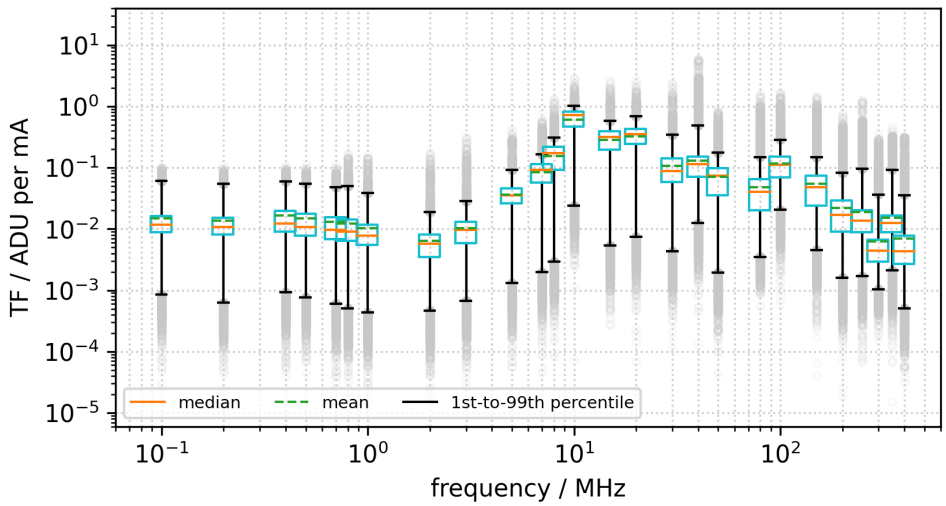


Figure 6.18.: Transfer function for conducted common-mode noise injected into all lines connected to the CDN. A total number of 88 635 channels entered in this analysis. The noise was injected into dgnd, dhp-core, dhp-io, dcd-dvdd, sw-dvdd, agnd, dcd-avdd, dcd-refin, dcd-amplow, source, gate-on1, ccg1, drift and hv lines.

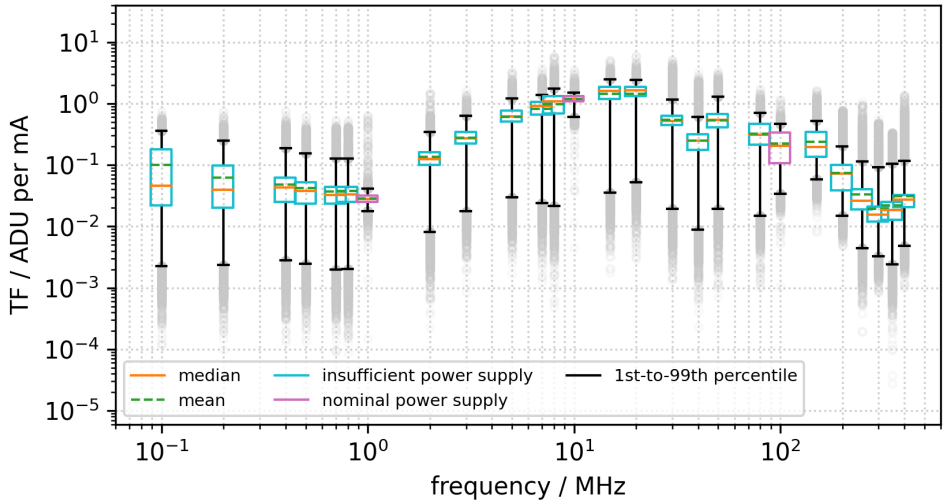


Figure 6.19.: Transfer function for conducted differential-mode noise injected into the gate-on1 line. A total number of 88 060 channels entered in this analysis. While most data points where recorded during insufficient power supply conditions for the DCDs (cyan), three data points were replaced with values from the reference measurement taken with nominal power supply (magenta).

able to conducted noise on the gate-on1 line. The maximum of the susceptibility throughout the measurements lies between 8 MHz and 20 MHz. Some measurements show a second local maximum but of varying degree and varying frequencies between 100 MHz and 250 MHz. The local minimum at 2 MHz for the measurement of all lines connected to the CDN is an exceptional behavior not observed for the other configurations. Only the dcd-amplow line shows comparably low values for noise frequencies between 1 MHz and 7 MHz.

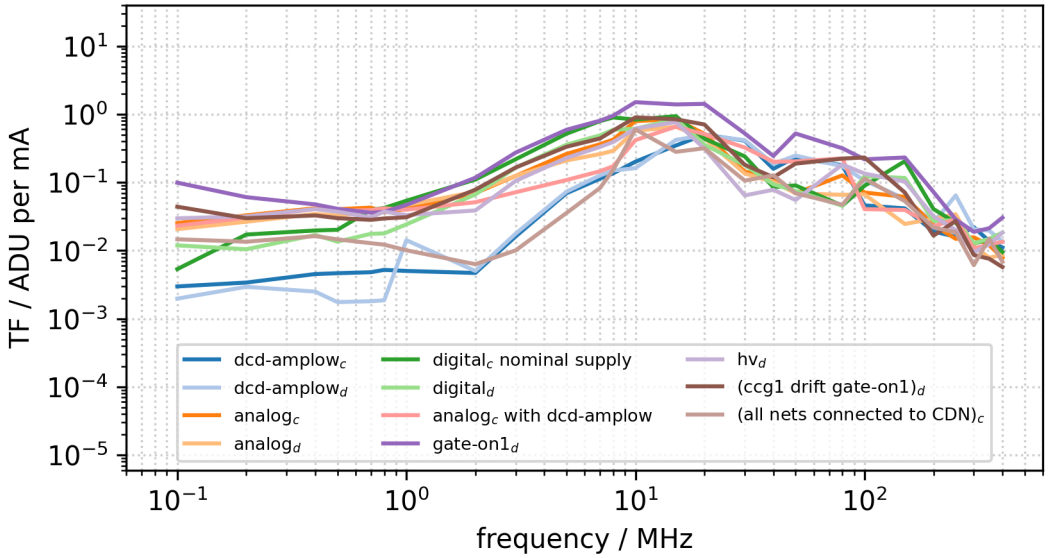


Figure 6.20.: Combined result of all analyzed transfer functions for conducted noise injection. Only the calculated mean curve for each measurement is plotted. The highest susceptibility throughout the measurements occurs between 8 MHz and 20 MHz. All transfer functions for conducted noise injection show mostly a similar shape. For individual plots see appendix B.

6.5.2.5. Common-mode vs. differential-mode noise

If there is more than one path for conducted noise in a system a distinction is made between common-mode, where the noise appears in phase on the conductors, which means in the same direction, and differential-mode, where the noise appears out of phase, which means in opposite directions. For the PXD setup we assumed that the main return path of injected conducted noise will be the corresponding ground line of the affected domain. Hence, we speak of common-mode noise when the noise was injected also into the corresponding ground line, which effectively forced the noise current on all lines of this domain in the same direction. When we took the ground line out of the RF injection probe and allowed the return current through the ground

line in opposite direction, we speak of differential-mode noise.

We measured three configurations where once the noise was injected as common-mode and once as differential-mode noise; the dcd-amplow line, the analog domain (dcd-avdd, dcd-refin and source) and the digital domain (dhp-core, dhp-io, dcd-dvdd and sw-dvdd). For the latter two the common-mode is significantly the predominant mode especially at the most critical frequencies. However, the variation between the measured configurations exceeds the differences in the modes (see fig. 6.21). It can be concluded that the mode of the conducted noise is less important for the system's response than the specific line it occurs on.

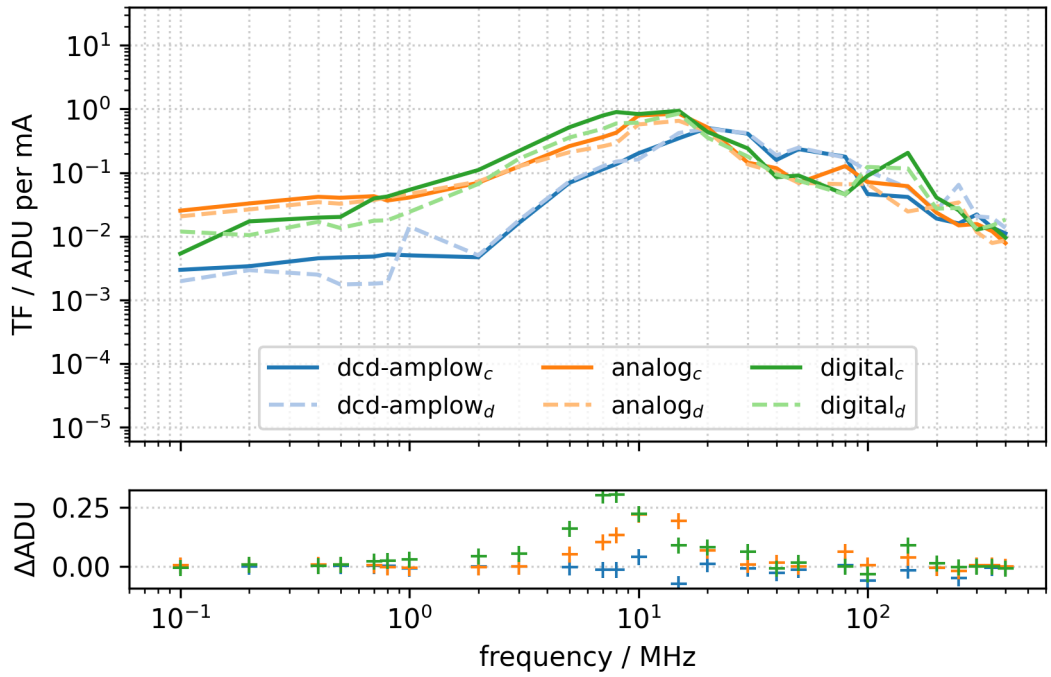


Figure 6.21.: Comparison between common-mode and differential-mode noise. For all three configurations the perturbing signal was injected once also into the corresponding ground line (common-mode denoted by the subscript letter c) and once this line was excluded (differential-mode denoted by the subscript letter d). The difference between common-mode and differential-mode for each configuration is shown in the lower plot. For an individual plot for each of the measurements see appendix B.

6.5.2.6. Beam pipe radiated noise

As innermost vertex detector the PXD is installed in close proximity to the beam pipe. The distance between the outer wall of the beam pipe and the inner layer of the PXD is only 2 mm. While the beam pipe acts as Faraday shield and confines the electromagnetic fields of the beams, the beam pipe itself is grounded to the accelerator structure and may have a connection to auxiliary electronics like power converters of vacuum pumps, cryostats, magnets, collimators, etc. Through this connection noise currents can occur on the outer surface of the beam pipe and may affect the PXD through radiative coupling. Therefore, we considered the beam pipe as a significant source for induced noise and also measured the susceptibility of the PXD to radiated noise in a setup with a simplified beam pipe geometry [143].

The actual beam pipe at the interaction point of SuperKEKB is a hollow cylinder with an outer radius of 12 mm made of beryllium as described in detail in section 3.1.1. The electromagnetic noise radiated from the beam pipe was simulated with a simplified geometry by placing a thick wire above the plastic protection cover of the test module (see fig. 6.22). The distance between module and wire was about 20 mm. Due to the fragility of the module and mechanical constraints we did not take the risk to measure with a smaller distance which would have required to remove the protection cover. The wire was connected at both ends to the copper table. The noise signal was produced by a frequency generator and injected through a bulk current injection probe. The resulting current was measured with a second current probe. We followed the same procedure as for the measurement of the conducted noise injection described above to collect pedestal data and to calculate a transfer function for radiated noise.

The impact of radiated noise is significantly lower compared to most conducted noise measurements up to a frequency of 40 MHz (see fig. 6.23). For higher frequencies the transfer function for radiated noise stays on a rather constant level whereas the curves for conduced noise decline. Consequently, for 400 MHz the system is slightly more vulnerable to radiated noise than to conducted noise, but still on a low level.

In addition, different orientations between radiating cable and module were tested. With very thorough shielding with copper foil it was possible to prevent any disturbance of the PXD module. By removing the shielding step by step the Kapton Cable was identified as the region most prone to radiated noise when the emitting cable was installed parallel to the Kapton Cable. The effect was largely reduced when the cable was installed by the side of the module sparing the Kapton Cable, as well as when the emitting cable was placed perpendicular across the module or the Kapton Cable [143].

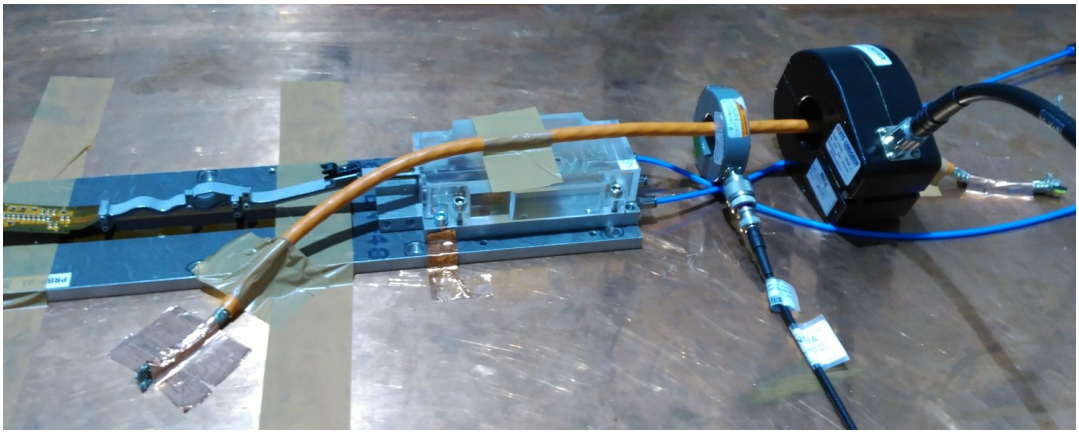


Figure 6.22.: Configuration of the beam pipe setup for radiated noise measurement. The beam pipe was simulated by a thick wire installed above the module's protection cover in parallel to the long side of the module. The distance between wire and module was about 20 mm. The noise signal was injected with a bulk current injection probe and the resulting current measured with a second current probe.

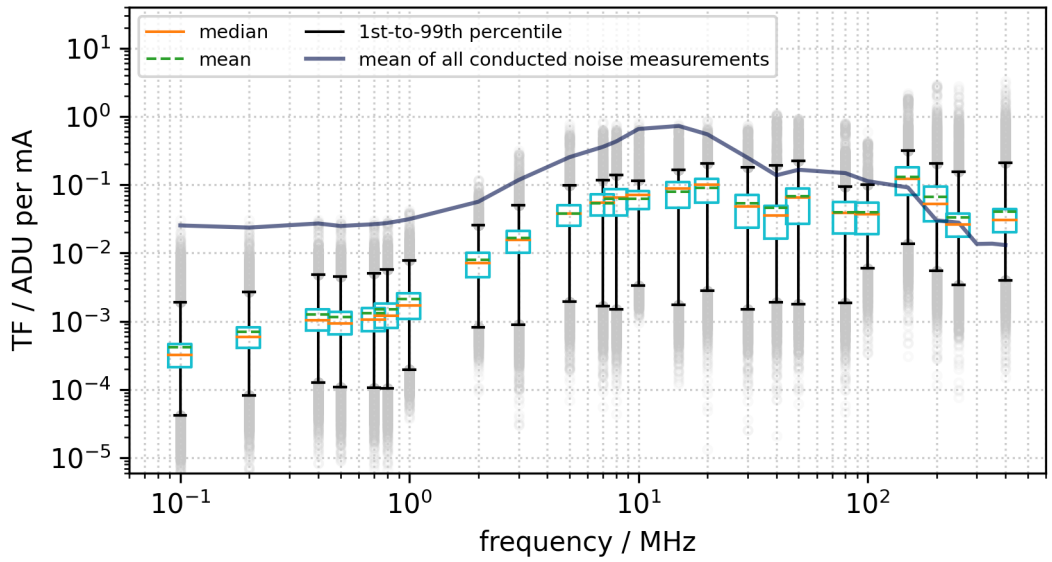


Figure 6.23.: Transfer function for radiated noise emitted by a beam pipe dummy installed directly above the module cover. The beam pipe dummy was oriented parallel to the long side of the module (see fig. 6.22). For comparison also the mean of all transfer functions for conducted noise injections is shown.

6.5.2.7. Readout electronics vs. DEPFET matrix

The ADCs not connected to the DEPFET matrix were used to analyze the effects of electromagnetic interference on the readout electronics separately from the effects on the matrix. Each DCD has six ADCs which are not connected to any drain line from the matrix due to geometrical reasons. In addition, due to the analysis of the module performance during the measurement campaign several drain lines could be identified which did not deliver input current from any pixel[6] to the ADCs and can therefore be assumed to be disconnected as well (see section 6.3.2). The digitization process is still performed in all ADCs in parallel and therefore data of "virtual" pixels became available, which can be considered as mostly independent from the combination of DEPFET matrix and Switcher ASICs.

The six not connected ADCs on each of the three analyzed DCDs in combination with the 123 gates used for data analysis result in a total number of 2 214 "virtual" pixels, i.e. 2 214 pedestal values in each data frame for analysis of the electronics. Due to the 20 broken drain lines another 2 460 "virtual" pixels are available. Each of those "virtual" pixels was analyzed in the same way as the working pixels by calculating transfer functions on the basis of the recorded noise for the different frequencies of the injected noise signal.

Both classes of "virtual" pixels are in good agreement verifying the assumption that the broken drains are indeed entirely disconnected (see fig. 6.24). For conducted noise injection the mean curve of all "virtual" pixels stays one order of magnitude below the mean curve of all working pixels up to a frequency of 100 MHz. For higher frequencies the distance decreases, yet the curve of the working pixels stays always above the one of the "virtual" pixels as the response from the working pixels include both, the noise from the readout electronics and from the matrix. For radiated noise the situation is comparable but again with overall lower values.

It can be concluded that for noise frequencies below 100 MHz the susceptibility of the PXD module to EMI is dominated by the response of the matrix system, including DEPFET pixels and Switcher ASICs. For higher frequencies the contribution of the readout ASICs becomes more significant. The additional part from the matrix system (represented by the area in between the curves) gradually disappears until almost the entire module response is driven by the response of the readout ASICs.

[6] In other PXD modules also partially broken drain lines were observed, where the open apparently occurred within the matrix between two gates. Those drains discussed here showed no signal from any pixel.

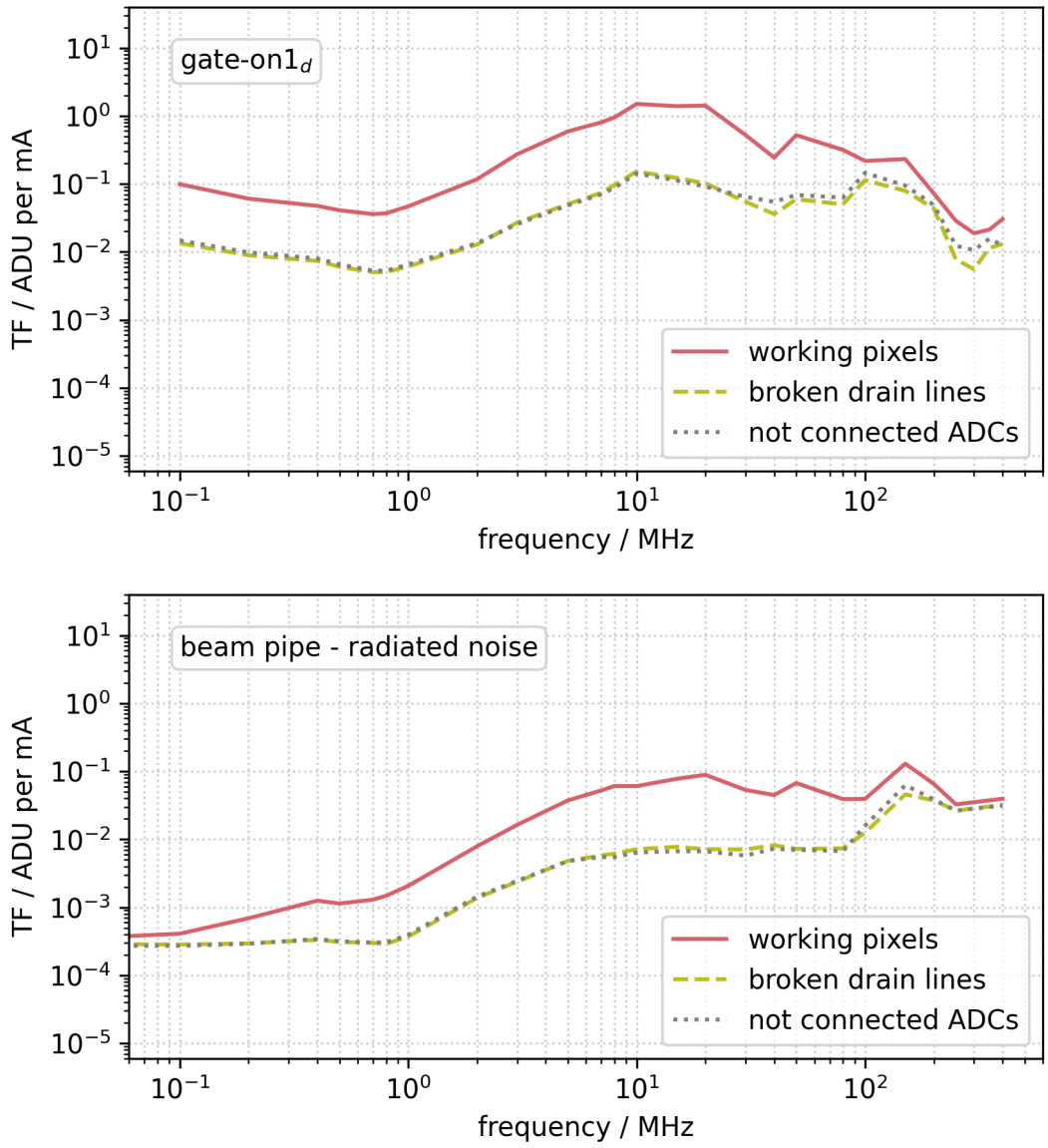


Figure 6.24.: Susceptibility comparison between readout electronics and DEPFET matrix. The results for conducted noise injection into gate-on1 line (top) and beam pipe radiated noise injection (bottom) are comparable. For frequencies below 100 MHz the noise contribution is dominated by the response of the matrix system, including DEPFET pixels and Switcher ASICs.

6.5.2.8. Noise distribution

Different parts of the same electronic device can react differently to EMI as the individual implementation of each subdomain determines its natural frequency and susceptibility. Therefore, also geometrical dependencies of the noise response within the recorded DEPFET channels were analyzed. The noise distribution varies for different frequencies of injected noise (see fig. 6.25) due to impedance variations between each channel. However, within the analyzed data we could not identify a conspicuous part or region of the matrix with significantly increased susceptibility.

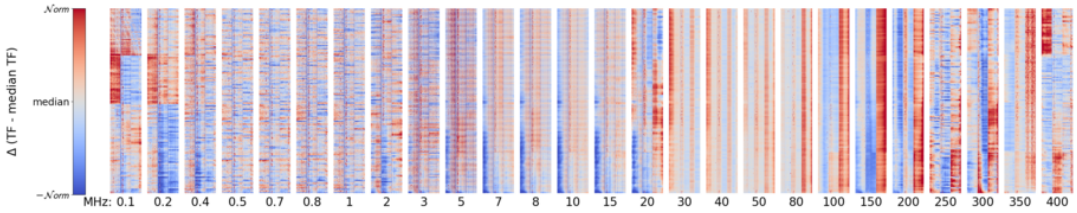


Figure 6.25.: Noise distribution within the DEPFET matrix over all measured frequencies for common-mode noise injected into the digital power domain. A noise distribution map for each measured frequency is shown. To set the individual noise distribution maps into relation the following normalization was used. For each frequency the median value of the transfer functions over all pixels is calculated and subtracted from these values. Deviations to higher noise values are shown in red and lower noise values in blue. $\mathcal{N}orm$ is the maximum of the absolute values of the 5th and 95th percentile of the transfer function values reduced by the median for each frequency.

Nevertheless, two special questions appeared and their analysis will be discussed in particular. For the first one, the measurement with noise injection solely into the gate-on1 line was analyzed. The expected confined reaction of the individual subdomain is only visible for frequencies below 8 MHz. For higher frequencies the response is homogeneous across the entire matrix. The second case concerns a left to right dependency within the ASIC pair columns, which is observed throughout all measurements with insufficient power supply of the DCDs due to the CDN issue. After the change in the CDN and with nominal power supplied the observed dependency disappeared.

Gate-on1 measurement: Each power line of a PXD module is in a sense universal to this module as the single line supplies all the corresponding loads. There are for example six Switcher ASICs on each module but only one sw-dvdd line providing the digital power for all of them. The only exceptions are the gate-on and clear-gate lines. For those the DEPFET matrix is divided into three sections along the gates, 64 gates each, corresponding to two Switcher ASICs each (see also section 4.2). For one of the measurements we injected the noise only into the gate-on1 line, which supports the lower third of the DEPFET matrix of the tested W30_OB2 module,

i.e. Switcher1 and Switcher2, corresponding to about half of the analyzed pixels in this study. Indeed it was possible to provoke a noise response of this subdomain different from the response of the neighboring domain. This regional dependency was expected and demonstrates that the noise response of a gate-on subdomain can be in fact considered separated and the injected noise may stay restricted to this subdomain. However, this effect is only visible for frequencies below 0.8 MHz. For higher frequencies the noise couples also into the other domains and the response of the entire matrix becomes independent from the subdomain to which the noise is injected to (see figs. 6.26 and 6.27). This effect also explains the larger spread between the pixels in the transfer function of the gate-on1 measurement for lower frequencies as described above (see fig. 6.19).

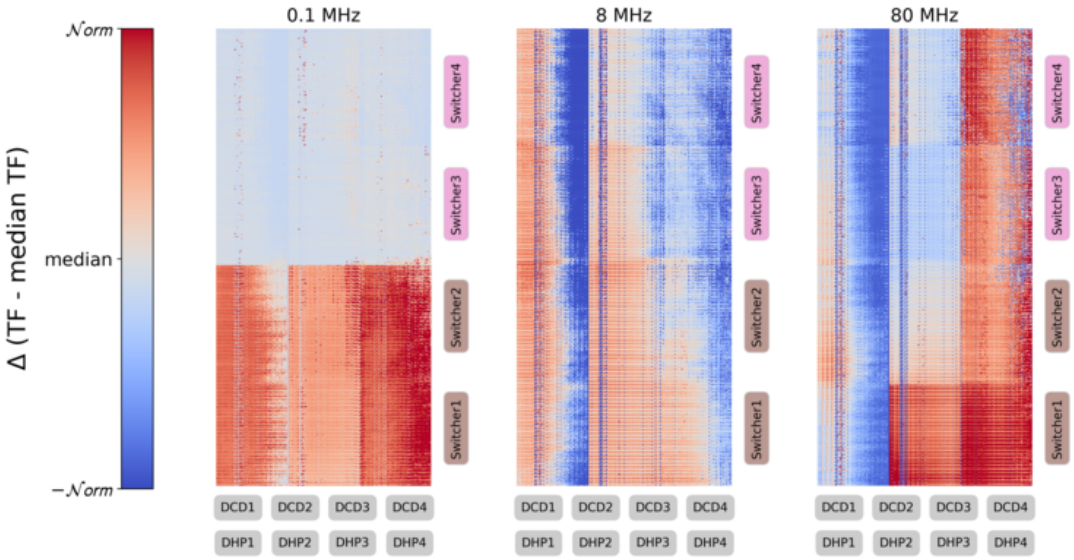


Figure 6.26.: Comparison of the noise distribution across the DEPFET matrix between three different frequencies for noise injection into the gate-on1 line. The two different gate-on regions are indicated by the different colors of the Switcher ASIC pair corresponding to region 1 (brown) and region 2 (pink). Left: At the lowest frequency measured of 0.1 MHz a higher noise response of the gate-on1 region and the transition between the regions is clearly visible. Middle (right): At 8 MHz (80 MHz) the mean response values of the two gate-on regions differ for about the same order of magnitude (see fig. 6.27), however, the distribution is not aligned with the transition between the gate-on regions.

Left to right dependency: To filter the data for empty frames due to lost links during data taking, the matrix was divided into three regions corresponding to the three ASIC pairs as described in section 6.5.2.3. As mentioned there, the mean of region 1 showed always the lowest susceptibility as long as the initial configuration of the CDN prevented the nominal supply of the DCDs (see fig. 6.17). This correlates with a large number of pixels in region 1 which did not only yield lower ADU values compared to the other pixels in the same region (see fig. 6.8a) but also showed a

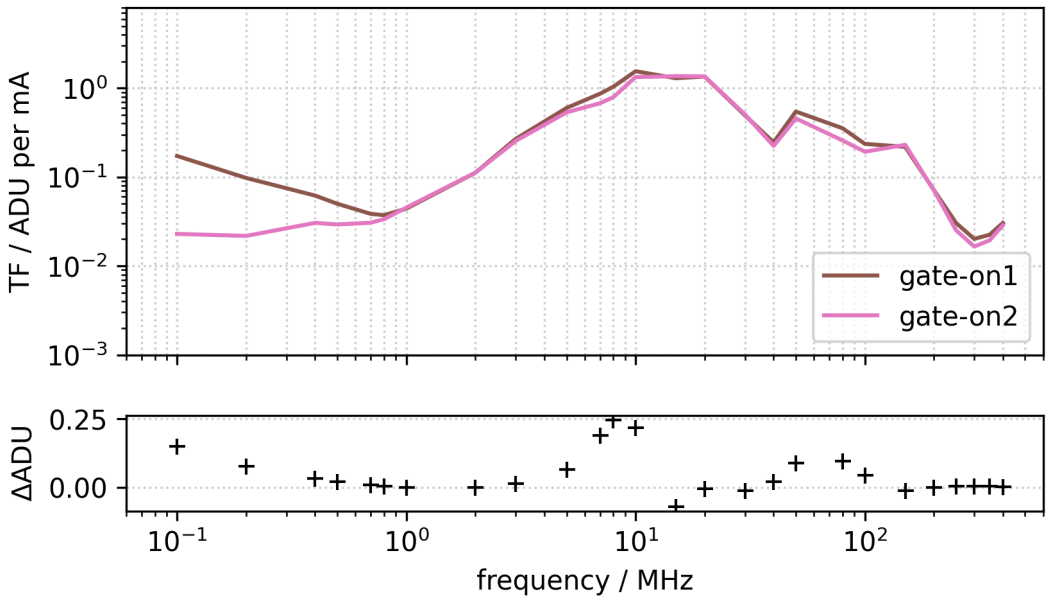


Figure 6.27.: Comparison of transfer functions over all measured frequencies between the regions of gate-on1 and gate-on2 for noise injection into the gate-on1 line. The mean curves of the corresponding regions are plotted for comparison. For frequencies below 0.8 MHz the gate-on1 region is more affected by the external perturbation. At about 8 MHz and about 80 MHz the absolute difference between the mean values of the two gate-on regions in ΔADU is of comparable size. However, the noise distribution in the matrix is not aligned with the transition between the two gate-on regions (see fig. 6.26).

weakened response to noise visible in fig. 6.26 (middle and right: dark blue). This effect vanished after the change in the CDN. One measurement was repeated for all frequencies with the nominal voltages supplied: the common-mode noise injection into the digital supply domain. For this measurement the system's response can be compared for all frequencies. To do so, the geometrical representation of the transfer functions is used which illustrates the location of the pixel on the matrix. Data link 2, which was not working, is omitted in the plots. The highest susceptibility of the system can be clearly identified for frequencies between 7 MHz and 15 MHz in both measurements (see fig. 6.28). The dark vertical line representing the pixels with the lower response is no longer visible for the measurement with the nominal voltages supplied. Hence, the observed effect can be attributed to the improper CDN configuration and a cause in the matrix can be excluded.

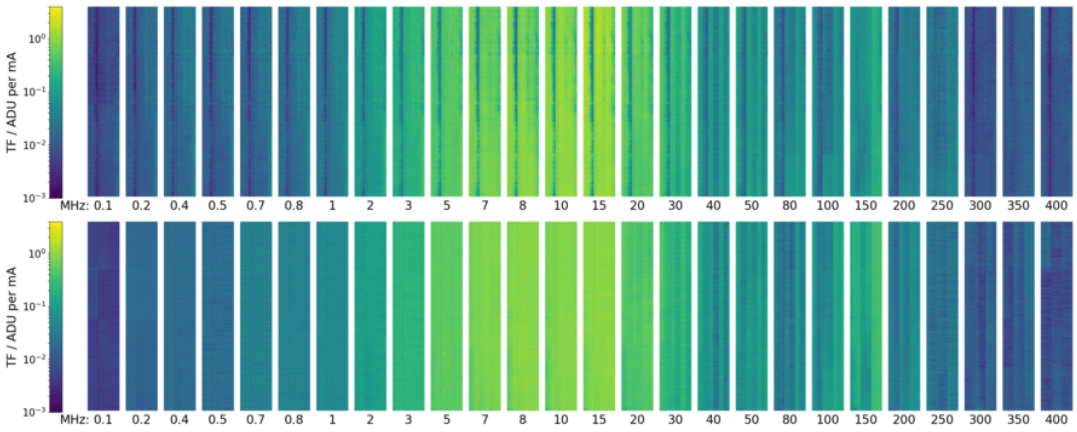


Figure 6.28.: Geometrical representation of the transfer functions for common-mode noise injected into the digital power domain. Top: The first measurement was taken with insufficient power supply for the DCDs. Bottom: The entire measurement was repeated after the change in the CDN with nominal power supplied. Both measurements show the same result for the highest susceptibility of the module between frequencies of 7 MHz and 15 MHz, but there are no longer pixels with reduced response in the repeated measurement. The matrix performance is more homogeneous.

Although the origin for this effect could be identified, there is no explanation of the specific mechanism behind it. As the power supply of the analog part of the DCDs is the decisive factor, the power distribution to the ASICs on the module was studied, but the results are not entirely conclusive. The DCDs require five supply lines for power: dgnd, dcd-dvdd, dcd-amplow, dcd-avdd and agnd. Broad lines on the module ensure that a sufficiently high current flow is possible. The supply lines are routed below the DCDs to connect to the power pins of the ASICs as well as to transfer the lines to the neighboring DCD (see fig. 6.30). Due to the limited space on the module, the broad distribution lines are also routed below the analog part of the DCDs.

For both measurements the mean of the transfer functions was calculated for each drain line, which corresponds to one of the DCD pins, and the results were plotted in the same geometrical orientation as the pins on the module (see fig. 6.29). In the pin map of DCD1 approximately the right third of the pins show a reduced response to noise matching the routing of the analog supply lines which were affected by the improper CDN components. However, this effect is clearly reduced for DCD4 and does not appear for DCD3. The distribution of currents and power consumption within one module, especially for situations with undersupply, may explain the differences in the ASICs but is not known. The causal relation is therefore not evident. A similar pattern was described by Müller in the study of the DCD current sink [51, p. 308]. At least the results show an improved and homogeneous performance of the module when the nominal power was supplied. The positions of the not connected ADCs and of the broken drain lines are visible as well as the reduction of noisy drains.

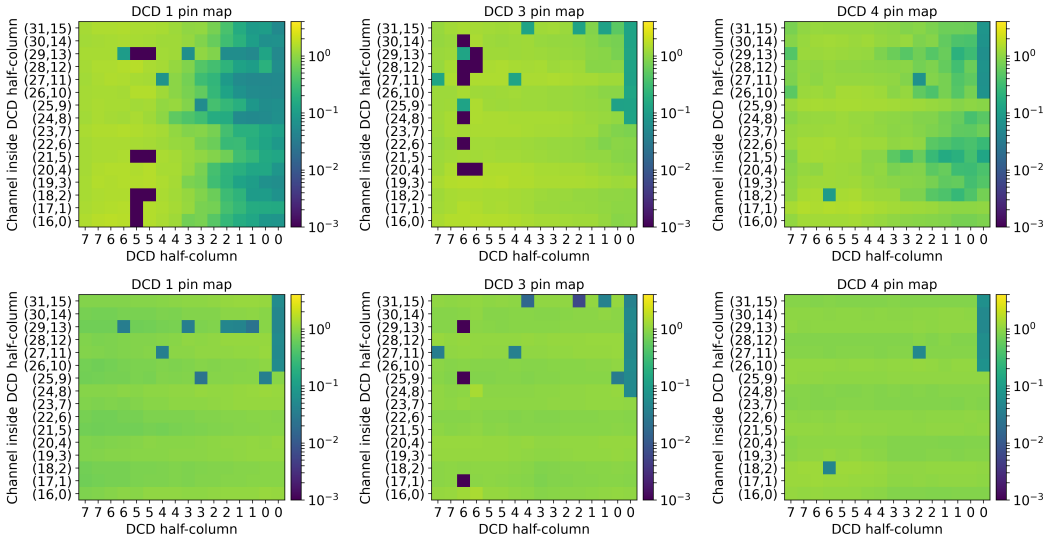


Figure 6.29.: DCD pin map representation of transfer function values for noise injection into the gate-on1 line at 10 MHz. Top: The largest number of ADCs which were affected by the improper power supply are accumulated on the right side of DCD1. Bottom: With nominal power supplied the response is much more homogeneous. The upper six pins in the rightmost column of each DCD are the six ADCs which are not connected to the matrix. The other ADCs with similar response represent the broken drain lines. The number of masked drains (very dark) is largely reduced for nominal power supply conditions.

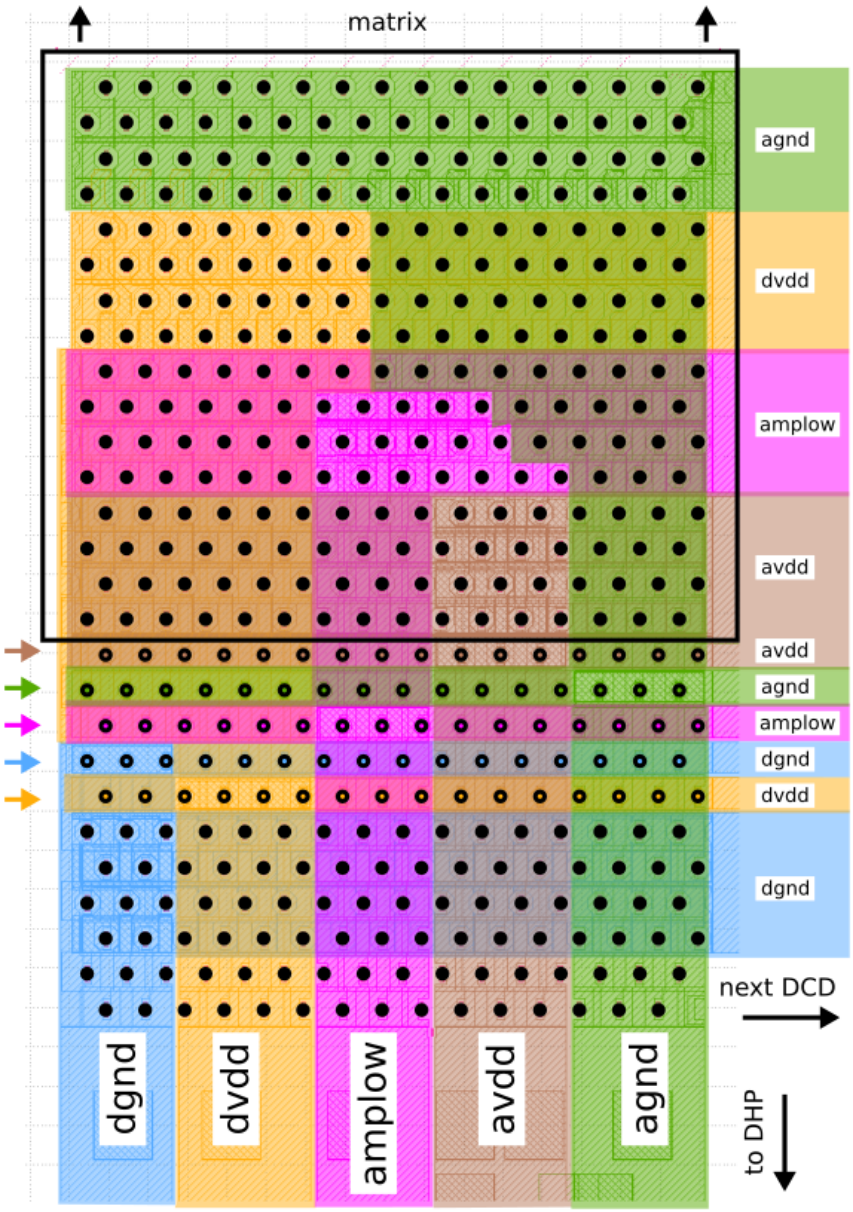


Figure 6.30.: DCD pin map layout with supply lines. The lower solid black pins are used for digital communication. There is one entire row of pins dedicated for the connection to each of the five supply lines (indicated by the colored arrows). In order to provide a sufficient current flow the power lines are implemented as broad lines and routed below the ASICs. The upper pins are connected to the 250 drain lines coming from the matrix (indicated by the black frame). The analog supply lines are below the right and upper part of the matrix pins.

6.5.2.9. Maximal allowed perturbation current

On basis of the obtained transfer functions we are able to determine the maximum of a perturbing noise current so that the induced noise in the data stays below 25 % of the intrinsic module noise. This procedure is demonstrated for three of the measurements: conducted common-mode noise injection into the digital domain, conducted differential-mode noise injection into the gate-on1 line and radiated noise injection emitted from the beam pipe dummy. The previous results demonstrated that the PXD module reacted most susceptible during the gate-on1 measurement across all tested frequencies. Therefore, this measurement poses an upper bound on the acceptable perturbation currents and hence provides the most stringent limits.

The baseline for this considerations is the intrinsic noise of the module without any external noise contribution. During the entire measurement campaign, 30 reference measurements were taken with no noise injection and 1000 pedestal frames each. Only the well performing pixels were selected which also entered in the analysis of the transfer functions and the noise per pixel was calculated for each reference measurement as standard deviation of the pedestal values. Subsequently, a normal distribution was fitted to the resulting noise histogram per reference measurement and all resulting mean values were collected in a further histogram (see fig. 6.31).

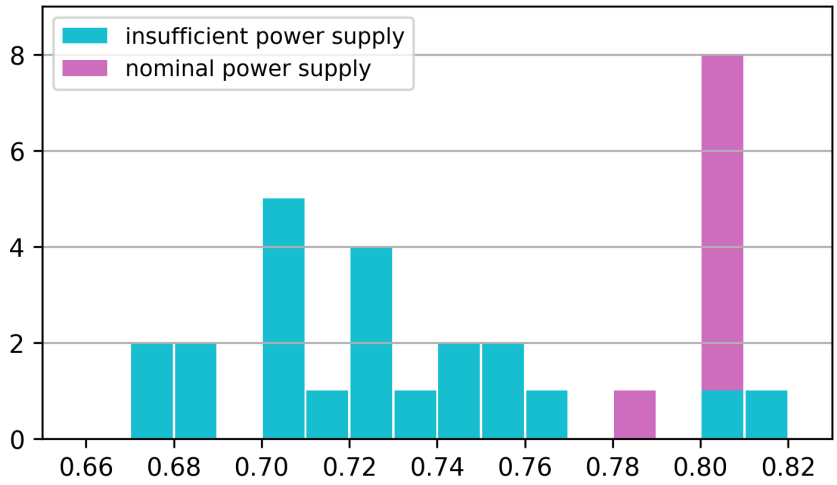


Figure 6.31.: Distribution of fitted mean values for noise in pedestal data for all reference measurements during the measurement campaign. Only the well performing part of the matrix is taken into account. Compared to the state before, the noise values are a bit higher and more stable at around 0.8 ADU after the change in the CDN.

The mean over all reference measurements is about 0.75 ADU. However, separated again into before and after the change in the CDN a better estimate for the intrin-

sic noise $N_{intrinsic}$ of the module under nominal conditions is about 0.8 ADU (also found by Schreeck [96, p. 93]). Additional 25 % from external perturbation sources would result in a noise value of about 1.0 ADU. In combination with typical signal values between 20 ADU to 30 ADU for comparable configurations [151] this yields a SNR between 20 to 30 which is still very acceptable for the operation of a PXD module.

The previously retrieved transfer functions describe the externally introduced noise per perturbation current. Therefore, the maximal allowed perturbation current $I_{p,max}$ is calculated by dividing the chosen noise threshold through the measured values of the transfer functions.

$$I_{p,max}(f)\ [\mu\mathrm{A}] = \frac{0.25 \cdot N_{intrinsic} \cdot 1000\ \frac{\mu\mathrm{A}}{\mathrm{mA}}}{TF(f)} \tag{6.3}$$

The resulting limits on the perturbing noise currents are in the range of 100 µA for conducted noise on the power distribution lines at the most critical frequencies around 8 MHz to 20 MHz and in the range of 2 mA for noise currents on the beam pipe with frequencies above 10 MHz (see fig. 6.32).

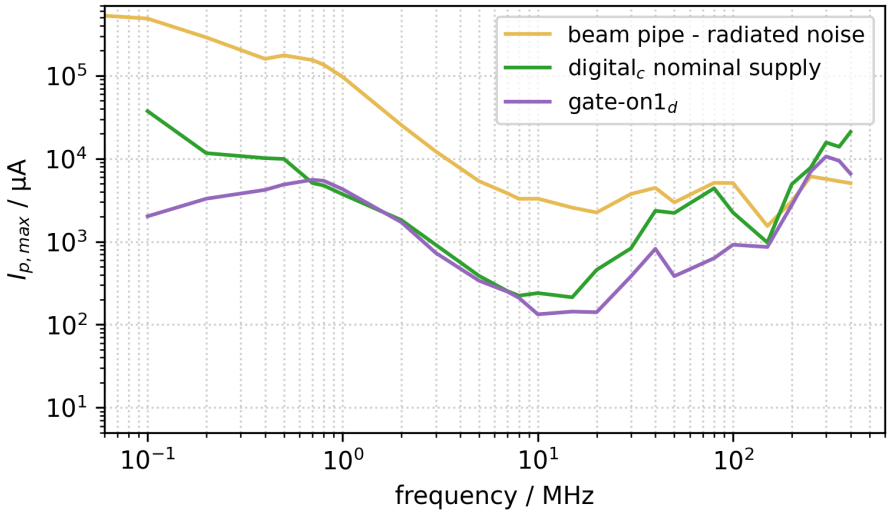


Figure 6.32.: Maximal allowed perturbation current to limit the externally induced noise to 25 % of the intrinsic noise depending on frequency and injection mode.

To compare the results to emission limits of the EU standard CISPR 32 for multimedia equipment [145] as already described in section 6.4, the maximal allowed current values are converted into amplitudes [152].

$$amplitude(f)\ [\mathrm{dB\,\mu A}] = 20 \cdot log_{10}(I_{p,max}(f)) \tag{6.4}$$

Electronic devices complying to the defined emission limits of CISPR 32 have no large impact on the operational performance of the PXD (see fig. 6.33). The PXD is save against commercial multimedia devices of Class B. As for the higher limits for industrial multimedia devices (Class A) the maximum of the PXD susceptibility between 10 MHz and 20 MHz is on a level with the upper emission limit. However, the displayed curves are mean values over all analyzed pixels, so some pixels will have larger noise as the defined threshold value. Nevertheless, these results demonstrate a good EMC performance of the tested PXD module confirming the present design.

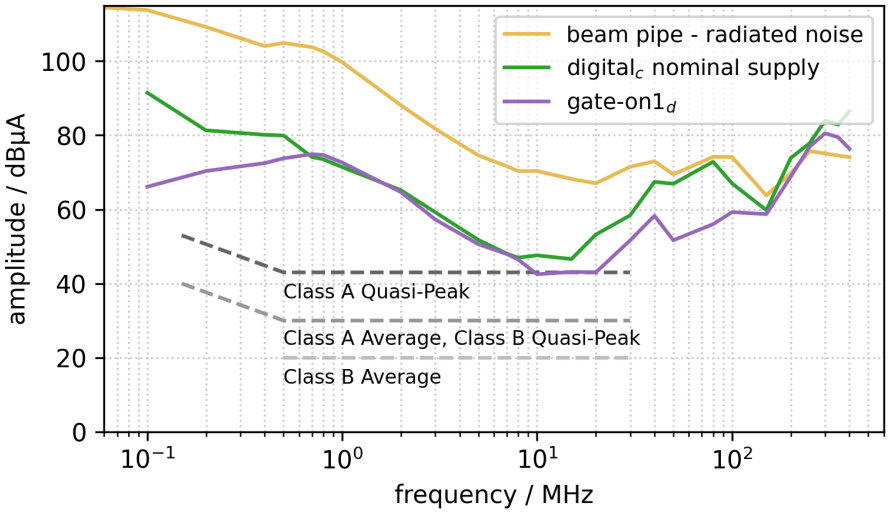


Figure 6.33.: Comparison of measured PXD module susceptibility to emission limits defined by EU standard CISPR 32 for industrial multimedia devices.

6.6. Discussion of results

With the extensive measurement campaign at ITAINNOVA we completed the dedicated EMC plan for the PXD and documented its electromagnetic emissions and susceptibility. The characterization of the entire system including PXD Power Supply, PXD module and readout chain confirmed the present design in terms of EMC. No critical vulnerability was found and the results are even close to industrial specifications as defined by European standards. For a detailed interpretation of the results the transfer functions are set into relation to the system frequencies present on the PXD module. Some direct correlations hint to the affected parts of the module's electronics. For instance, the data links are most vulnerable at the clock frequencies (system clock GCK and DCD clock) and the maximum of the susceptibility for conducted noise injection occurs at the gate rate.

6.6.1. Overview of PXD operation frequencies

All frequencies on the PXD module depend on the GCK provided to the module by the back end electronics. In the Belle II experiment the DHH system retrieves the timing from the B2TT as a 127.21 MHz clock synchronized to the beam revolution cycle in the accelerator. From this signal the DHC generates the GCK as 76.33 MHz clock which is then distributed to the DHEs, DHIs and further down to the PXD modules [107].

In the standalone laboratory setups the DHE generates the GCK itself and can also provide slower clock frequencies than the nominal 76.33 MHz. To increase the link stability of the data transmission and to stabilize data taking during the measurement campaign we reduced the GCK to 62.50 MHz, roughly a factor of 1.22 times slower. On the module the DHPs use a Phase Locked Loop (PLL) to multiply this clock by a factor of four to generate a fast clock for the DCDs. The ADC digitization process in the DCDs, which corresponds to the gate readout rate, takes eight system clock cycles. However, the actual current is sampled within one clock cycle of the DCD clock. The frame rate equals to the gate rate divided by the number of 192 gates.

In addition to these continuous processes the iterative clear pulse of up to 20 V (referenced to source) is a considerable part of the readout process. For the reduced system frequency the clear pulse has a length of about 32 ns during which the voltage is driven by the Switcher output and an additional settle time resulting in a pulse shape of about 50 ns [51, p. 200]. Consequently, a pulsed signal of about 20 MHz is generated with a pulse repetition frequency equal to the gate frequency. An overview of the

resulting nominal and reduced frequencies is given in table 6.1.

Table 6.1.: Operation frequencies of the PXD system

	nominal	reduced
PXD system clock GCK	76.33 MHz	62.50 MHz
DCD clock	305.32 MHz	250.00 MHz
ADC digitization / gate rate	9.54 MHz	7.81 MHz
frame rate	49.69 kHz	40.69 kHz
clear pulses	∼24 MHz	∼20 MHz

6.6.2. Relation to emission and susceptibility

By studying the EMC properties of the PXD the conducted noise emission spectra of a PXD Power Supply, an EMCM prototype and a PXD module were documented and classified as low enough to not have a significant impact on individual components of the system or on any other subdetector of Belle II. The emissions of the FEE (see fig. 6.10) were found to be predominant except for a few frequencies between 1 MHz and 10 MHz where the emissions of the Power Supply are predominant. Two PXD system frequencies and their respective harmonics occur in the recorded emission spectrum: the frame rate at 40.69 kHz and the gate rate at 7.81 MHz. Further spikes at about 183 kHz, 313 kHz could not be directly assigned to system frequencies.

The data links are most vulnerable to conducted noise injection for a broad range around the clock frequency between 30 MHz and 100 MHz (see fig. 6.12). In addition, they are especially unstable for noise injection at the DCD clock frequency of 250 MHz. Consequently, it can be stated that these clock frequencies are particularly important for the data link stability.

The response of the PXD system to external noise was characterized by calculating transfer functions for the different injection configurations. The susceptibility was analyzed and the most critical frequencies as well as the most vulnerable power line were determined. The PXD system is most susceptible to conducted noise between 8 MHz and 20 MHz, which corresponds to the gate rate and the frequency of the clear pulses both correlated to the digitization process of the DEPFET currents. An additional hot spot at higher frequencies between 100 MHz and 250 MHz varied also in extent between the different configurations and can therefore not be assessed reliably. The most vulnerable power line is the gate-on line across all measured frequencies. This can be explained as the gate-on potential directly influences the drain current of the DEPFETs.

6.6.3. Summary of additional results

Two out of the three configurations which could be compared directly showed a larger response of the PXD module to common-mode noise compared to differential-mode noise (see section 6.5.2.5). However, the variations between the transfer functions of the different power lines are significantly larger. The system's response depends rather on the line the noise occurs on than on the noise injection mode.

Radiated noise from the beam pipe simulated by a dummy cable had a significantly reduced effect compared to the conducted noise injection for frequencies below about 40 MHz (see section 6.5.2.6). For higher frequencies the results are comparable. The most vulnerable part of the FEE system to radiated noise is the Kapton Cable, especially when the emitting cable was oriented in parallel to the long side of the module. This is actually the case for the installation of the PXD at the SuperKEKB accelerator, where the Kapton Cable is approximately parallel to the beam pipe. However, it is shielded by the "heavy metal" absorber (see section 3.1.1).

The matrix system of DEPFET pixels and Switcher ASICs dominates the noise response characteristic for frequencies below 100 MHz (see section 6.5.2.7). For higher frequencies the response of the readout electronics to external noise becomes the dominant factor.

The noise distribution within the matrix varies with the noise frequency due a different impedance of each channel (see section 6.5.2.8). However, no especially susceptible part or region of the matrix was found. It was demonstrated that noise injected into the gate-on1 line stays confined to its domain for frequencies below 8 MHz and couples to the entire system for higher frequencies. For low frequencies down to 100 kHz the susceptibility increases in contrast to the other measured configurations. A further increase of the susceptibility at still lower frequencies closer to the frame rate of about 50 kHz (or 40 kHz at slower GCK) is expected.

To limit the externally introduced noise to 25 % of the intrinsic noise level a maximal perturbation current in the gate-on1 line of about 100 µA at the highest susceptibility (between 10 MHz and 20 MHz) is still tolerable (see section 6.5.2.9). For noise currents on the beam pipe the limit is at about 2 mA for frequencies above 10 MHz.

The tested setup deviated from the final integration of the detector in a few aspects:

- Only the next to final version of the ASICs and Patch Panels were used;

- Just a fraction of the pixel matrix was operational and used for the analysis;
- Due to wrong components in the CDN the DCDs were not sufficiently powered during the majority of the data taking.

Nevertheless, the impact of these issues on the retrieved results is low and the same affirmative characteristics are assumed for the final version of the PXD. These results allowed to foresee an unhindered operation of the PXD with regard to EMC and to proceed with the integration of the detector into Belle II at KEK.

6.6.4. Further resilience improvement

In addition, the situation is improved by the ability of both readout ASICs to compensate noise online during data taking. While the DCD is capable to perform an analog common mode correction before signal conversion, the DHP features a digital common mode correction before hit detection (see section 7.4.2.7 item 2). Both methods were not prepared for testing during the measurement campaign, but the algorithm for the digital part (DHP) was implemented in software and applied to the offline data. The results indicate an overall positive and very promising effect in noise reduction especially at the most critical frequencies where the transfer function values are decreased by one order of magnitude (see example in fig. 6.34).

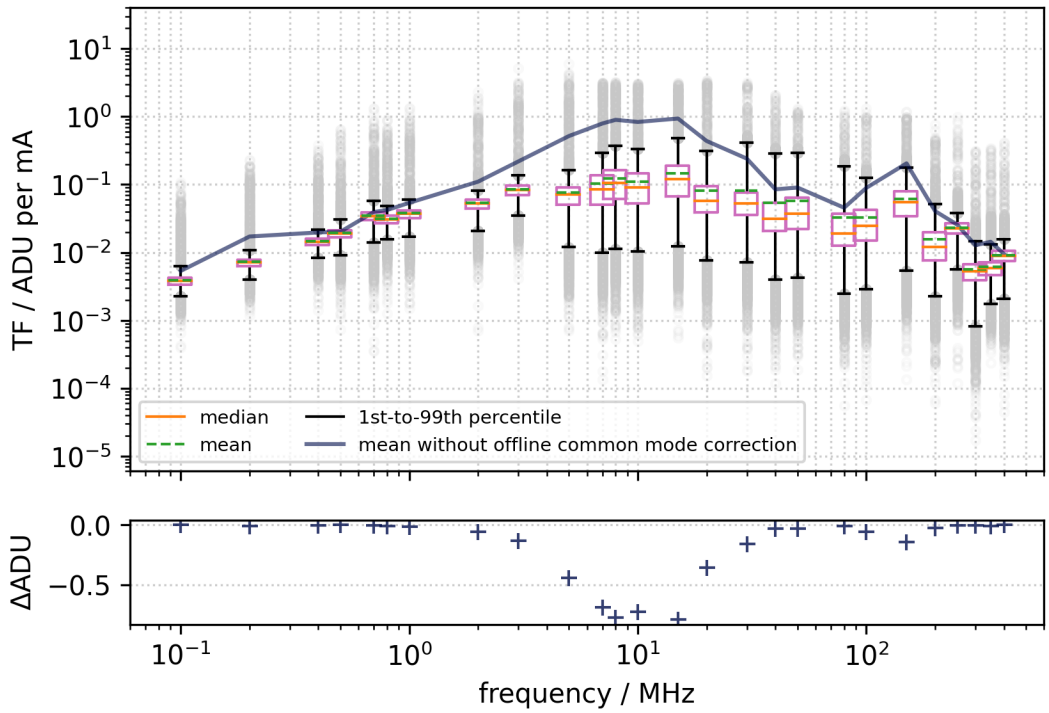


Figure 6.34.: Effect of offline digital common mode correction on susceptibility to external noise injection. The mean values of the actual measurement are plotted as dark line for reference. The response of all pixels was processed by the offline common mode correction and the resulting values entered as box plot. The data from the measurement after the change in the CDN was used. The noise was injected into dgnd, dcd-dvdd, dhp-core, dhp-io and sw-dvdd lines.

6.6.5. Experience from operation at KEK

The assumption of an unhindered operation of the PXD in terms of EMC was finally confirmed by the successful data taking during Phase 3 of the Belle II experiment. This is shown by the following two evaluations in particular.

First, the observed noise levels of the modules after installation were comparable to the ones found during testing in the laboratories (at around 0.8 ADU as shown in fig. 6.35). However, due to the suffered radiation damage during the operation at the accelerator the system parameters like gate-on and clear-gate voltages had to be adjusted and also the pedestal distributions changed. Both issues are not related to EMC but led to an increase in noise for the PXD modules (see again fig. 6.35).

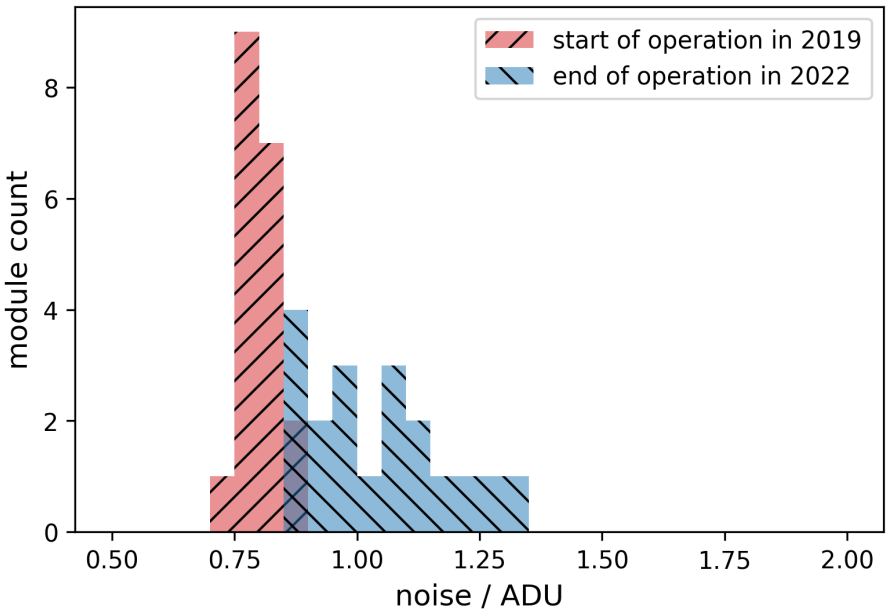


Figure 6.35.: Distribution of noise values in pedestal data for all 19 PXD modules. The initial state after installation at KEK is comparable to the situation in the laboratory with values around 0.8 ADU. After about three years of operation at the SuperKEKB accelerator the radiation damages and consequently changed operational parameters resulted in a broader distribution and overall higher values between 0.86 ADU and 1.34 ADU.

Second, a dedicated study of the influence, which the SVD as closest subdetector to the PXD might have, found no detectable effect on the noise values. The study was performed after the end of run 2022b (no beams present) by taking pedestal data in three different PXD configurations and for four different operational states of the SVD. In the standard configuration for the PXD the ACMC and the offsets are turned on. Both were sequentially turned off, first the ACMC then the offsets. Analogously,

the SVD was sequentially turned off from its standard state during physics data taking:

- SVD HV in PEAK and taking data (DAQ high rate test at this point)
- SVD HV in PEAK but not taking data
- SVD HV in STANDBY (only LV on)
- SVD with PS in IDLE (LV and HV off)

This constellation resulted in twelve different configurations and 1000 pedestal frames were taken for each of them[7]. To calculate the noise per module, at first only those pixels of each module were selected which were well within the dynamic range (between 20 ADU and 230 ADU) in the measurement with the highest noise expected: SVD fully powered and taking data combined with PXD ACMC off and offsets off. This was necessary as the pedestal values of pixels outside the dynamic range will be stuck either at high or low and would enter with artificially low noise values. Only the resulting selection of pixels was used for the further analysis. For each of those pixels the noise was again calculated as standard deviation over all recorded pedestal frames. All retrieved noise values entered in a noise histogram per module. The noise distributions are usually fitted by a Gauss function, which works quite well for measurements with ACMC enabled, although an indication of a fat tail towards higher values can already be noticed. For the measurements with ACMC turned off the distributions broaden and the fat tail becomes more pronounced. Therefore, not only Gauss but also Landau and Langau functions were fitted and the best fit was used to determine the most probable value (MPV) as noise value for this module (see fig. 6.36). It is noted that there was no physical motivation for the selection of these fit functions, still they can describe the shape and especially the MPV of the distributions quite well.

In addition to the significant reduction in the width of noise distributions on individual modules the ACMC is also able to reduce the overall noise per module by about 20 % for the conditions present after about three years of operation (see fig. 6.37). Those values still guaranteed a good data taking performance of the PXD. During the long shutdown in 2022 and 2023 the PXD will be replaced with a fully equipped version and thereby also the initial conditions of unirradiated modules will be restored. In view of a higher luminosity and simultaneously increased irradiation after the shutdown, further improvements in the beam stability, resulting in less instantaneous radiation damage, and improvements in the module optimization will be required to ensure a constantly good performance for several years of data taking.

[7] Except one configuration, where the applied system settings were overwritten unnoticed by an automatic configuration software actually searching for configuration changes by single event upsets (SEUs).

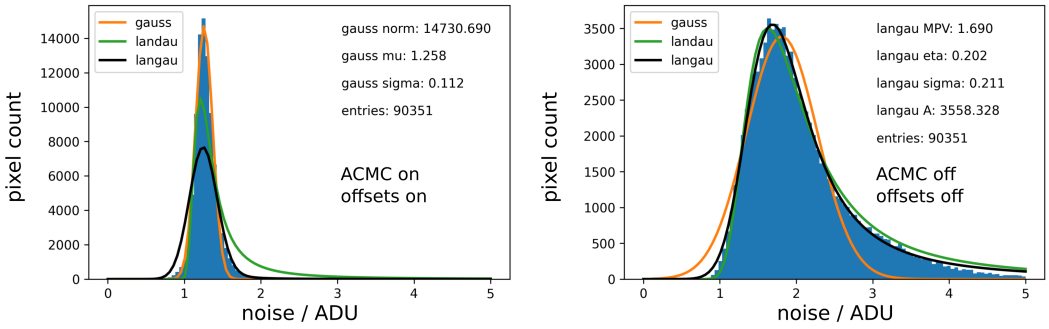


Figure 6.36.: Finding the best fit for different noise distributions of module H1011. While for configurations with enabled ACMC the best fit was always reached by a Gauss function, Landau and Langau functions often showed better agreement with data for disabled ACMC. Here, two examples from the module H1011 are shown: ACMC on and offsets on (left), ACMC off and offsets off (right). Due to a broad raw pedestal distribution only about half of the pixels entered in the analysis, which were all within the dynamic range. For both plots the same selection of pixels was analyzed. In the right plot the vertical axis is zoomed to show the differences between the fitted curves.

Finally, the cumulated results of all PXD modules for the different configurations show that the PXD is not affected by the operation of the SVD throughout all tested states (see again fig. 6.37). While the measured noise increases with disabling ACMC and offsets of the PXD (along the horizontal axis), there is no significant change in the noise distributions visible for the changes in SVD powering and operational states (along the vertical axis). In terms of EMC the PXD copes very well in the neighborhood of the SVD and being the heart of the Belle II tracking detector.

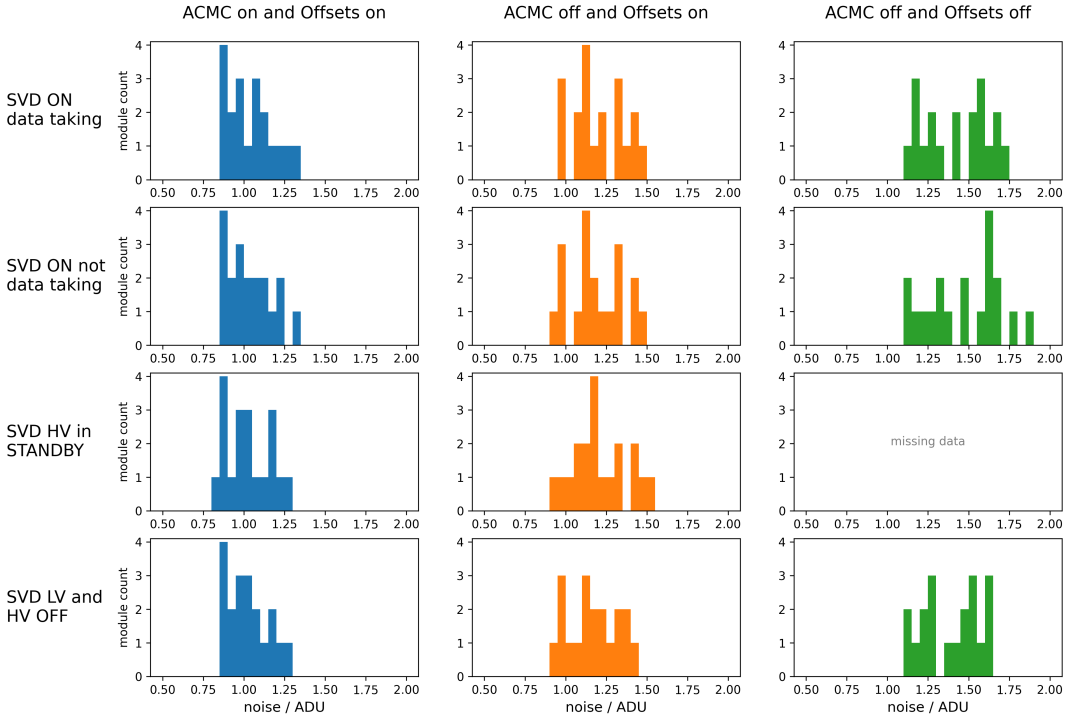


Figure 6.37.: Influence of PXD configuration and SVD operational states on noise in pedestal data. After three years of operation at the SuperKEKB accelerator the offsets and ACMC are still able to reduce the noise per module to an acceptable value of about 1 ADU. Independent from the PXD configuration the SVD operational state has no impact on the noise values.

Acknowledgment for EMC campaign

I want to sincerely thank all participants of the EMC measurement campaign who made this detailed study possible. Due to great preparation and very concentrated work we smoothly collected a lot of valuable data within two weeks during the hot summer of Aragon. Main credit goes to the team of ITAINNOVA, Fernando Arteche, Ivan Echeverria and Mateo Iglesias, for providing the perfect environment and equipment as well as contributing with large expertise. Many thanks also to Christian Koffmane for the help in preparing the CDN box and for the invaluable remote support during the entire campaign.

This Project has received funding from Ministerio de Economia (Spain) under grant agreement FPA2014-55295-C3-3R (CMSRUN2) and FPA2017-85155-C4-3R (CMSRUN2B), from Advanced European Infrastructures for Detectors at Accelerators (AIDA2020) under grant agreement H2020-INFRAIA-654168 and from MoU between ITAINNOVA and Max Planck Institute for Physics.

The Spanish broadcast RTVE reported briefly about this measurement campaign on TV, available on YouTube: https://www.youtube.com/watch?v=K-fUQMNNRnE.

Figure 6.38.: Participants of the EMC measurement campaign at the ITAINNOVA. From left to right: Fernando Arteche, Hans-Günther Moser, Felix Müller, Ivan Echeverria, Philipp Leitl, Mateo Iglesias, Christian Koffmane (missing in the picture).

7. Main Production Module Characterization

After the conclusion of the design phase and several iterations based on prototype measurements [51, 112, 153] the production mode of the PXD modules proceeded to the main production. The goal was to produce and characterize enough high quality modules in order to pick the 40 best performing ones to build a complete PXD.

This chapter gives an overview of the different production steps and describes the quality assurance and quality control measures applied. The characterization procedure of the final modules in the laboratories and the results of the individual optimizations will be presented for 62 completely tested PXD modules. Observed issues encountered during the process will be illustrated, like inefficient gates, a pre-irradiation effect, and disconnected drain lines.

While the initial goal to select the 40 best performing modules was achieved, chapter 8 provides the explanation why mechanical difficulties during the assembly prevented a successful construction of an entire PXD with two complete layers on the first attempt.

7.1. From prototype to production modules

The PXD system consists of several distinct components, namely the monolithic silicon module with the active DEPFET matrix, three different ASIC types, cables and connections, read-out electronics and power supply as well as slow control, data acquisition and optimization software. Each component was designed and developed by different groups within the collaboration. After initial standalone tests the components were combined to first prototypes in order to test the integration. The next pages give a short overview of the most important development stages. One task of this thesis was the commissioning of the final modules after all components came together, to operate the modules and to find optimized operation values for each individual module of the final production batches.

A fully equipped **Hybrid5** module (see fig. 7.1) includes one ASIC of each type (DHP, DCD and Switcher) and a small DEPFET matrix (32 × 64 pixel) on a PCB. The ASICs are mounted on bump bond adapters, which are glued to the PCB, and connected with bond wires. Also the matrix is glued to the PCB, which features a hole underneath the sensitive area for backside illumination and reduced material budget during beam tests. Jumpers can be used to configure the path of the JTAG chain or to connect external configuration tools. The data and power lines are connected with commercial cables, no custom Kapton cable is required yet. This approach of reduced complexity provides comfortable access to low level signals. The traces and the headers can be easily contacted with the tip of a probe and the signals can be measured with an oscilloscope. The Hybrid5 setup was used, among other things, for system integration tests, laser measurements, energy calibration measurements and software development [51, 112].

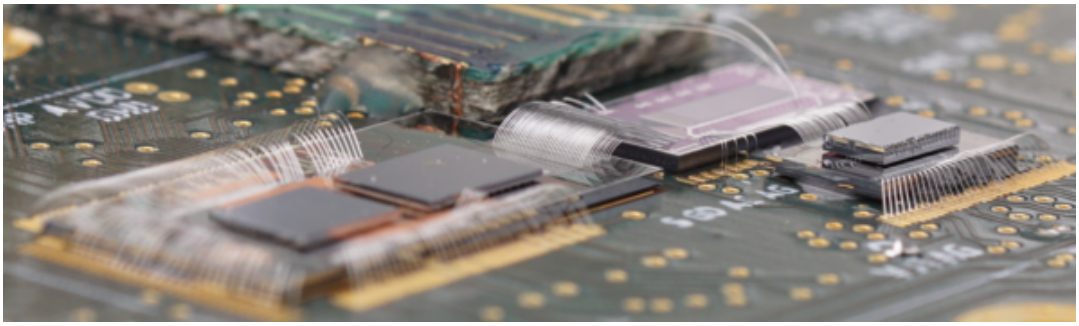


Figure 7.1.: Hybrid5 [112]. One pair of DCD and DHP (left) is connected to the drain lines of the small DEPFET matrix (middle). Next to the matrix a Switcher (right) is connected to the gate lines. Bond wires bridge the transitions between the bump bond adapters and the PCB.

The **electrical multi-chip module (EMCM)** (see fig. 7.2) is the first full size system integration with the final number of ASICs and corresponding SMD components. The all-silicon module has the final geometry of a PXD module and serves as support and in addition provides the metal circuit connections between the ASICs and the connection interface to the Kapton cable. There is no full size DEPFET matrix on the EMCM, but a small DEPFET matrix can be attached with a wire bond adapter. Its purpose includes verification of the circuit design, measurement of signal integrity and power distribution, confirmation of the three metal layer technology and tests of the data link stability between DHPs and DHE over the Kapton cable [51].

The **PXD9** module version (see fig. 7.3) is the final system configuration of the full size all-silicon module. It features four DCD-DHP ASIC pairs on the end-of-stave, six Switcher ASICs on the balcony along the matrix, and a large scale DEPFET matrix with 192 000 pixels embedded in a 75 µm thin silicon substrate. The production

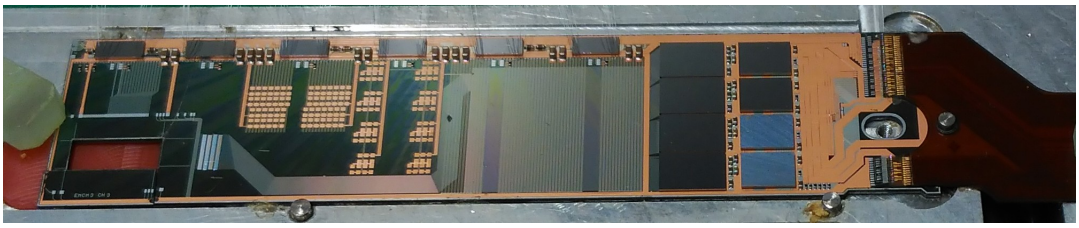


Figure 7.2.: EMCM: W17_3. This EMCM is populated with the final number of ASICs (6 Switchers, 4 DCDs and 4 DHPs). The Kapton cable (right) is soldered to the EOS and further traces are connected with bond wires. A small DEPFET matrix can be mounted at the far end (lower left).

started with a pilot run batch. Testing of the these first module resulted in further iterations with minor modifications and optimizations, like increased spacing between transmission lines to mitigate cross talk, and increased trace width of the Switcher clear supply to compensate the voltage drop along the line [51]. However, the good performance of the pilot run modules confirmed the layout design and the production technology.

In summary, the prototype testing contributed to the successive understanding of the interplay between individual components, demonstrated possibilities for further improvements and could therefore contribute valuable insights towards the optimization of the entire system.

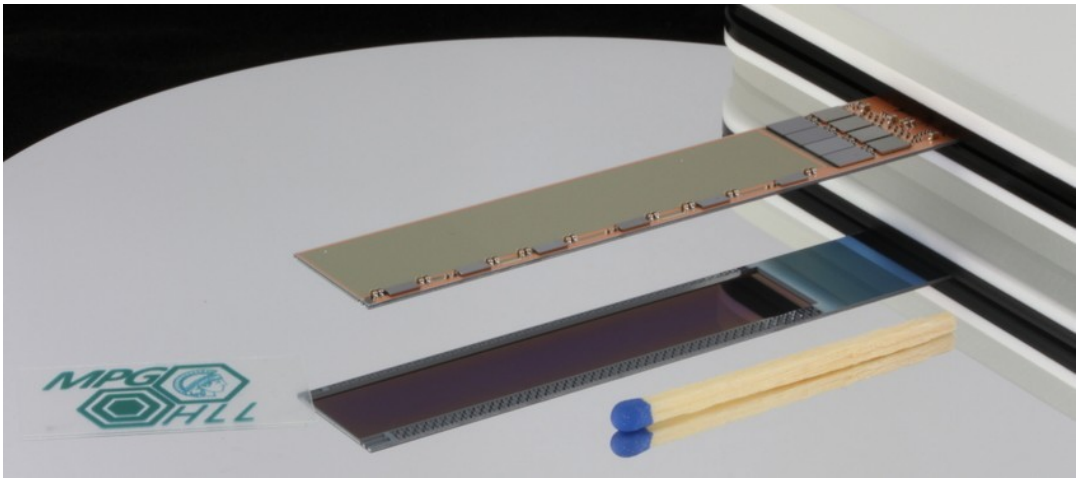


Figure 7.3.: PXD9 pilot run module W30_OF1 [154]. All components are mounted on the top while the thinning is applied from the bottom (visible in the mirrored image).

7.2. Production processes

A short overview of the most important production processes of the PXD modules including their associated quality assurance measures is presented on the next pages. These are the wafer level testing during the wafer processing, ASIC tests after external production, ASIC and SMD assembly, probe card test of the fully equipped modules as well as the Kapton attachment.

Although these processes were not in the field of responsibility of the author[1], it provides an introduction to the topic and sets the context for the further quality assurance measures during the module characterization phase which fell under the responsibility of the author and is presented in the next section.

7.2.1. Wafer level testing

The three phases during the wafer processing for the PXD modules were already described in section 4.1.2. Here, complementary information about the wafer level testing is given. After phase II (both aluminium layers and first passivation layer) the first interconnection tests are carried out. Each module is processed on the wafer with an extension on the far end, the so-called "fan-out" (indicated with blue color in fig. 4.6 and image in fig. 7.4). This allows testing of the matrix circuit and the DEPFET structures still on wafer level. The test pads are contacted with a needle card. Through four long contacts on both sides the source, all-clear, all-gate and all-clear gate potentials are applied. By contacting also the test pad for each drain line, shorts and opens can be found. In addition, I-V curves of the DEPFET pixels are measured for individual characterization [155]. As the wafer is still intact, a repair of certain faults using wafer processing technologies is still possible.

At the end of phase III, after the application of the last metal layer (copper), an extended interconnection test of all metal lines on the modules is carried out with a flying needle prober. Again, faults can still be repaired using wafer level technologies. After the final passivation the modules are cut out with a laser, which also separates the fan-out testing structure from the modules.

[1] except for the development of the Boundary-Scan routine applied during the probe card testing, which is described in a former work [106]

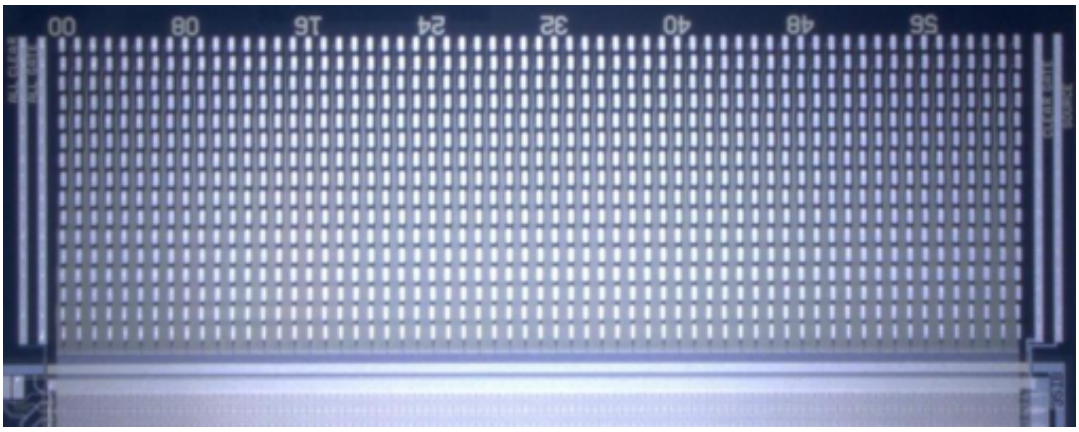


Figure 7.4.: Module fan-out [156]. The long contacts on the sides are (from left): all-clear, all-gate, all-clear gate and source. Each of the 1000 drain lines per module is connected to one of the small pads in the center. The entire fan-out is later cut from the module.

7.2.2. ASIC assembly

The first step for the bare silicon modules is the assembly of the control and readout ASICs. After the production, they were cut and delivered as dices. Subsequently, the responsible groups tested the basic functionality of individual ASICs with needle card setups, reporting yields of 98 % for DHPs, 99 % for DCDs, and 97.5 % for Switchers [153, 157, 158], before they sent them to the HLL for the assembly process.

The contact interface of all ASICs is realized as ball grid array to achieve a form factor as dense as possible. Hence, the flip chip technique is used to mount the ASICs to the module. Solder bumps are applied to the pads on top of the ASICs after wafer processing (see fig. 7.5).

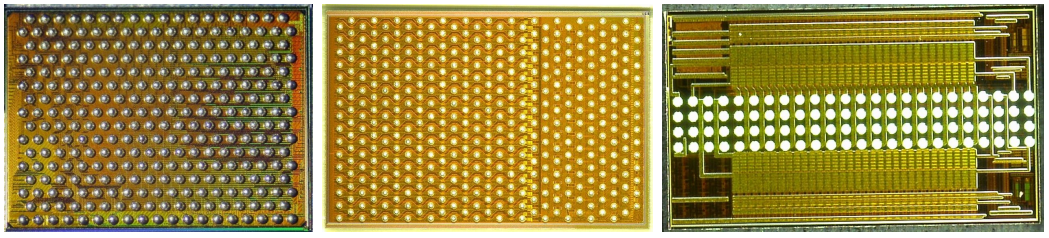


Figure 7.5.: ASIC footprints (from left): DHP, DCD, Switcher (not to scale).

The ASICs are then flipped around and placed on top of their corresponding landing pads on the module circuit. Through a reflow process at about 240 °C the solder gets liquefied, performs a self-alignment between the solder pads and establishes the

electrical connection (see fig. 7.6). This process was carried out by the Fraunhofer Institute for Reliability and Microintegration IZM in Berlin for the fist PXD modules and later adopted by the HLL. The quality of the ASIC assembly was checked by x-ray inspection of each assembled module. Initially, metal covers were used to minimize the irradiation dose of the DEPFET matrix. However, incomplete coverage resulted in a shifted pedestal value of the irradiated pixels and broadened the pedestal distribution (see section 7.5.2). The covers were removed for later inspections.

The assembly of the Switcher ASICs was especially challenging. These ASICs were produced on a multiproject wafer and already shipped as cut dices before placement of solder bumps was possible. "Bumping" of individual dices was not feasible, so the Switchers were re-assembled to a "wafer" by gluing them onto a glass wafer [159]. Through this technique, solder balls could be added to the Switchers.

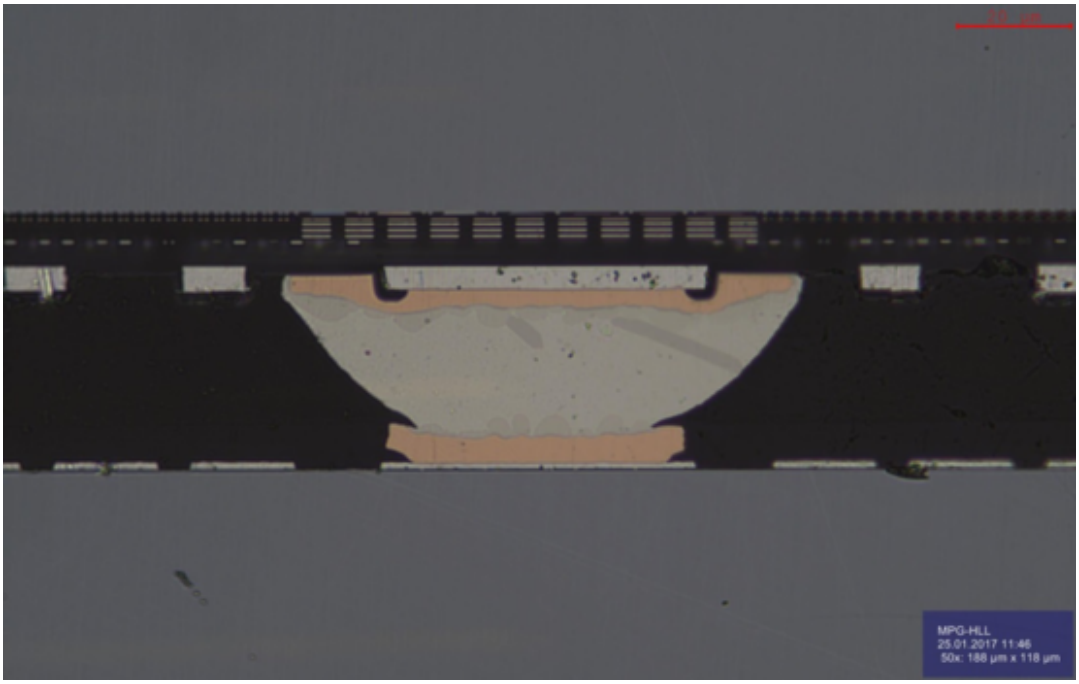


Figure 7.6.: Switcher bump cross section [159].

7.2.3. SMD assembly

After the assembly of the ASICs, the required passive components (i.e. termination resistors and decoupling capacitors) are mounted. A pick-and-place machine auto-

matically puts them at the correct spot (see fig. 7.7). Then the modules undergo a further reflow process at about 200 °C. This process was carried out at the HLL for all PXD modules. It was qualified with sheer tests where the capacitors with a form factor of 0201 withstood a lateral force of 3.5 N to 4.7 N [160]. After each SMD assembly the quality of the individual solder process was inspected visually by the technician.

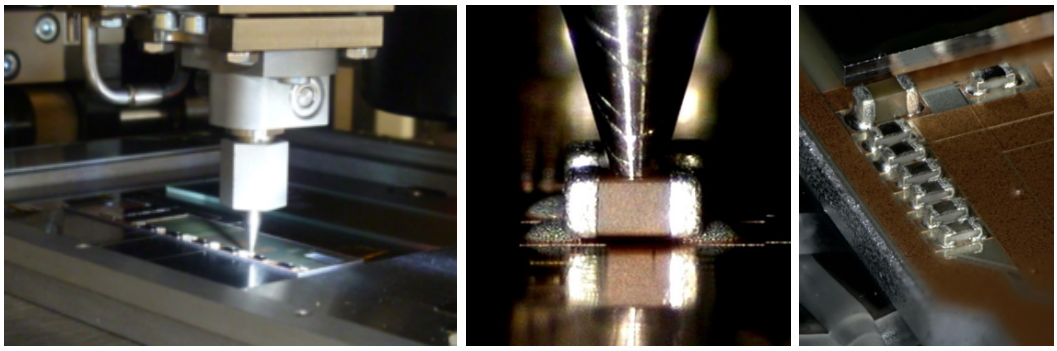


Figure 7.7.: SMD assembly with pick-and-place machine at the HLL [160].

7.2.4. Probe card testing

After the placement of all active and passive components, the modules are electrically functional. Now the first functional tests of the entire system are possible. A needle card setup is required to contact all lines at the bond pads and solder pads at the EOS (see fig. 7.8). The wire bond pads should be touched only in the corners to leave the largest part of the pads intact for the later wire bonding [161].

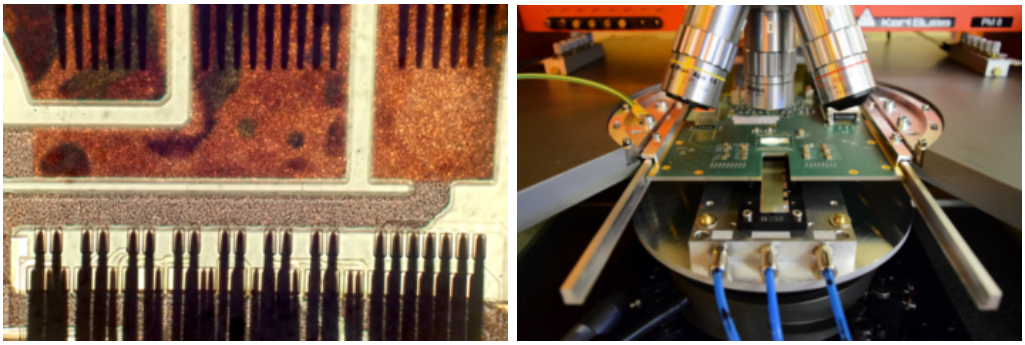


Figure 7.8.: Needle card setup at the HLL [162]. Left: The two rows of the lower needles contact the wire bond pads, while the upper row of needles contact the larger solder pads. Right: The PXD module is placed on a cooling block below the needle card. The position of the needles and the touchdown is monitored through a microscope.

Performed testes on the needle card setup include: power consumption of the digital part, test of the JTAG communication and a boundary-scan test [106], data transmission through the high speed links, power consumption of the analog part and the matrix, and taking a full pedestal map. Depending on the stability of the needle contact not all tests could be performed for all modules. Still, already the first, more probable to achieve tests have proven very helpful in detecting severe component failures. All production modules were tested with this protocol before going on to the Kapton attachment [162]. Out of 66 modules, 8 modules were found to have a faulty ASIC and 5 of them could be repaired.

After a module passed the probe card testing, it is safely stored in a protective transportation set and prepared for shipment to the MPP, where the final production step, the Kapton attachment, takes place.

7.2.5. Kapton attachment

The Kapton cable is the connection of the PXD module to the outer world. Depending on the module geometry, it is 0.43 m to 0.47 m long. As the available space in the experimental setup is very limited, it is only about 350 µm thick in order to guide all power and data lines out of the inner most part of the Belle II detector. The additional decoupling capacitors on the Kapton cable are located at a specific position where enough space is available. Already before the attachment, the Kapton cables are pre-bent in the MPP electronics workshop with dedicated jigs at 120 °C for 4 hours, so that the initially straight Kaptons adopt the shape required for the detector geometry in the experiment.

Four pads on the bottom side of the Kapton are then soldered to the four large copper pads of the module to connect the lines carrying the most current (i.e. dgnd, agnd, dcd-avdd and dcd-amplow). A tin-bismuth solder (Bi58/Sn42) with a melting point at 138 °C is screen printed onto the Kapton pads (see fig. 7.9 left). The Kapton is then aligned to the module pads and pressed down by a dedicated fixation weight. After vapor phase reflow soldering with a temperature profile maximum at about 160 °C, the distribution of the solder is controlled through x-ray inspection (see fig. 7.9 right).

Finally, the two rows of aluminium wire bond pads on the module are connected to the stepped rows of gold plated wire bond pads on the Kapton cable [163]. In total, 80 aluminium wires (AlSi1%[2]) are bonded wedge-to-wedge in two overlapping rows of arches (see figs. 7.10 and 7.11). The diameter of the bond wires is 30 µm.

[2] 99% aluminum and 1% silicon

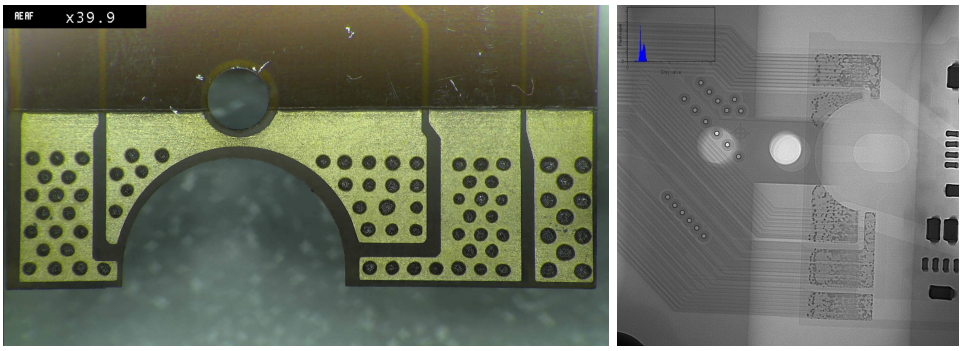


Figure 7.9.: Kapton soldering [163]. Left: Screen printed solder paste on Kapton pads. Right: X-ray image of solder joint. The entire pads are wetted and no excess or other cause for a short is visible.

Depending on the expected current, one to six wire bonds are used per line/bond pad.

The entire Kapton attachment process follows a detailed instruction manual to guarantee a traceable and reproducible procedure for each module. All images shown here are part of the intermediate quality inspections which are carried out and documented for each module.

After the final inspection, the completed module is packed in protective covers (as shown in fig. 5.4) and stored. It is now ready to be attached to a laboratory test setup as described in chapter 5 and to be characterized. In total 75 modules from 20 wafers reached this stage during the main production run in 2017 and 2018. The results of 62 fully tested modules are given in section 7.4 together with the description of the entire characterization and optimization process[3].

[3] Four modules were used in Phase 2 and went through the mass testing procedure only afterwards, further 9 modules failed early stages of the testing, were damaged during handling or lack the required data for analysis.

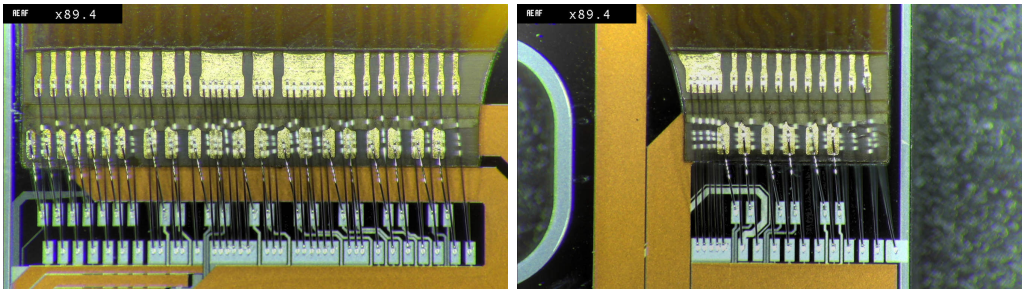


Figure 7.10.: Kapton wire bonding [163]. The wire feet (wedges), are placed well aligned on the solder pads. The two rows of overlapping arches are visible. Also the wires are well aligned and no deformation or damage is visible.

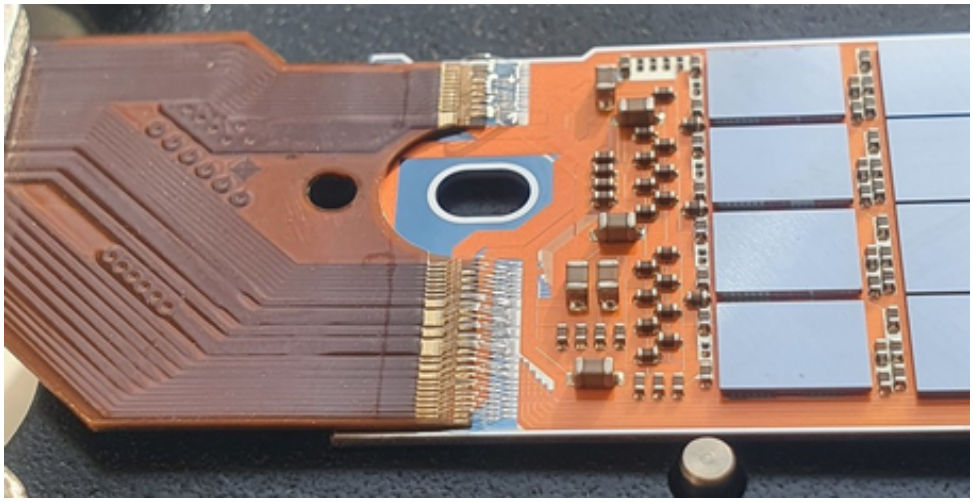


Figure 7.11.: Kapton attachment [163]. Entirely attached Kapton cable to the end-of-stave of a PXD module.

7.3. Quality assurance

The quality assurance measures during the production of PXD modules were briefly described in the sections above for the individual production steps. This can only be an incomplete list as the production itself was not in the responsibility of the author. However, all testing, optimization and characterisation of the production modules after Kapton attachment belongs to the scope of this thesis. This includes also the quality management during the module characterization phase.

The Ishikawa diagram in fig. 7.12 illustrates the different aspects pursued in order to achieve high quality production modules. The six main aspects, which are described in detail below, are an elaborated design of all mechanical parts, documentation, software quality, monitoring, databases and quality control.

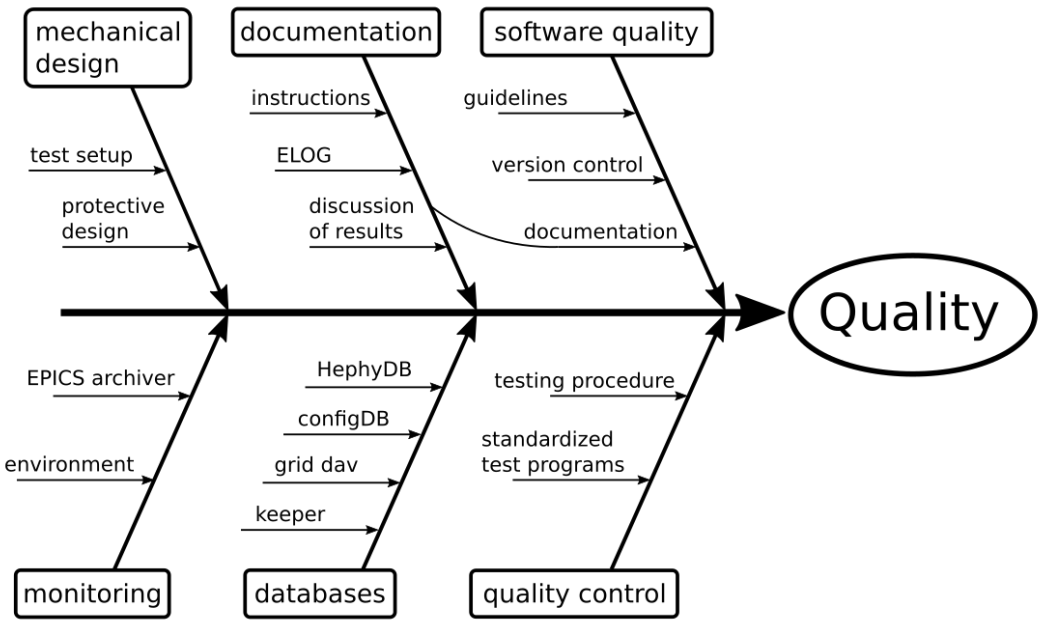


Figure 7.12.: Quality assurance measures during module characterization phase.

7.3.1. Protective design of mechanical parts

The components of the module support set were already described in section 5.2.1. Due to the modular structure with outer and inner covers the level of protection is always aligned with the individual steps of the testing procedure. During storage and transport to and from the test setup the outer shell protects all components (module and Kapton cable) from external influence.

The design of the support structures makes it possible to safely handle the modules. When a module is installed to the setup only the base jig is touched by the operator. The inner cover still protects the most sensitive thinned area and is only removed after safe installation to the setup. The long support structure for the Kapton cable secures the bonding joint to the module and acts as stress relief. In addition, it preserves the preformed shape of the Kapton cable.

The following measures were added from experience after handling the fist modules:

- A dedicated holding clamp at the end-of-stave and vacuum suction have to be applied always in combination to guarantee a sufficient cooling during operation.

- An alignment pin on the base jig ensures the straight position of the module. A small bracket at the far end of the module prevents the module to be lifted above this alignment pin, which would damage the module, when it is pressed down again.

- All screws present in the immediate environment of the modules (during testing and also during ladder gluing) feature a hexagon socket minimizing the risk of slipping with the screw driver and hitting the module.

7.3.2. Documentation

Documentation is one of the most important aspects for a high quality production, especially regarding a collaborative effort. The task of software development for the PXD modules as well as the testing of the final production modules was split between three different groups across Germany, each operating their own test setups. It had to be ensured that at all locations the same tests and measurements were performed to achieve a comparability between the results. Also the repeatability of each test for all modules was a concern while the software was still evolving.

The main aspects of documentation during the testing phase of the PXD modules can be grouped into four parts. First, instructions for the operators specified the handling of the modules and the test setups as well as the testing procedure itself. Second, an Electronic Logbook (ELOG) [164] was used to automatically document all measurements including analysis results and to manually add remarks or observations. Third, software documentation belongs also under this heading, however, it is described later under *software quality*. The fourth aspect concerns the final step of each module characterization: The obtained results were presented and shared with colleagues to achieve a joint assessment for each module.

7.3.2.1. Handling and testing instruction

The installation as well as the dismounting of PXD modules to or from the testing setups required several steps which had to be carried out in the correct order. Two sheets with instructions were added to each setup to remind the operator and to guarantee the correct execution. The exact instructions can be found in appendix C as **Module Installation Instruction** and **Module Dismounting Instruction**.

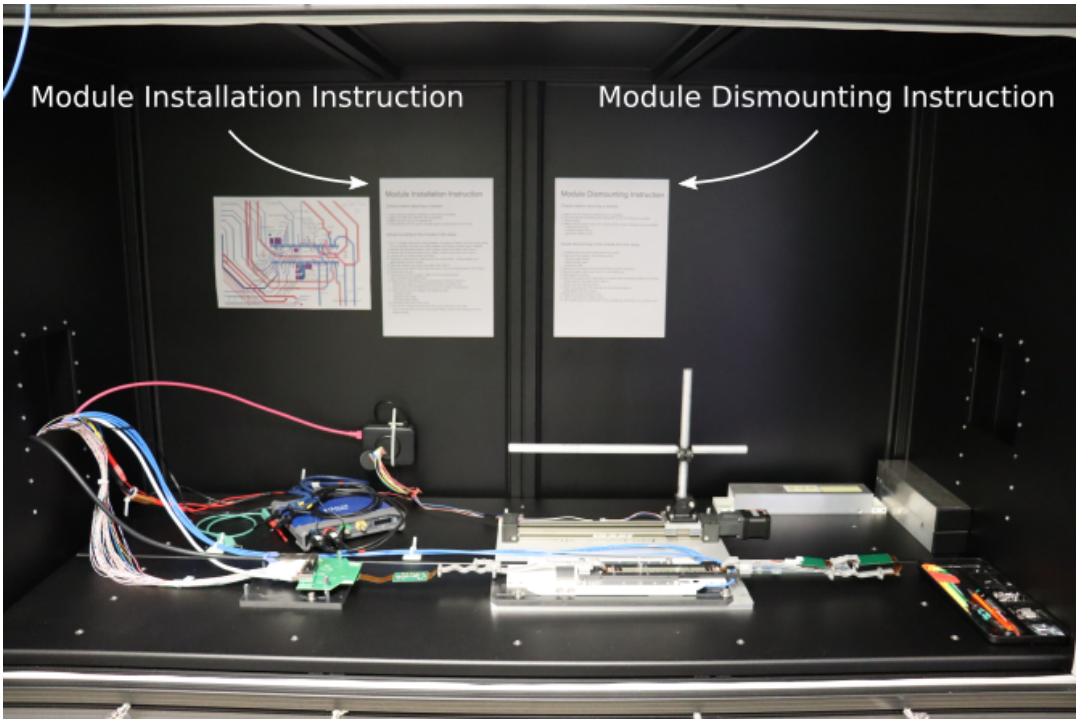


Figure 7.13.: PXD mass testing setup with module installation and dismounting instructions.

After closing, the inherently opaque black boxes hide the entire inner part of the module setup. Hence, a further list was designed as **setup tracer** (also in appendix C) and attached to the outside of each setup in order to minimize the frequency of opening and closing the back boxes just for verification purposes. The tracer provides frequently used configuration numbers for the module number and DHE ID which had to be set during initial software configuration depending on the module type. It also features a form for the module name as well as the installation and deinstallation dates. In addition, it has a field to enter the manually found positions of the motor stage (required for the source scan) and a field for information about the installed radiation source.

Documentation about individual system components, installation instructions and design files were collected on the online collaboration platform **confluence**[4]. For the testing procedure itself a dedicated **PXD Mass Testing Handbook** was written containing information about prerequisites, used software versions and detailed execution instructions for each test. It is described later in section 7.4.1.

At the MPP, two module setups and one ladder setup were operated in parallel. The used Ethernet cables for the various purposes (like network connection, slow control, data, JTAG) were color coded in order to have a clean and manageable installation. Each setup was inspected and verified with voltage measurements and a test run with a dummy module, before the first "hot" production module was attached.

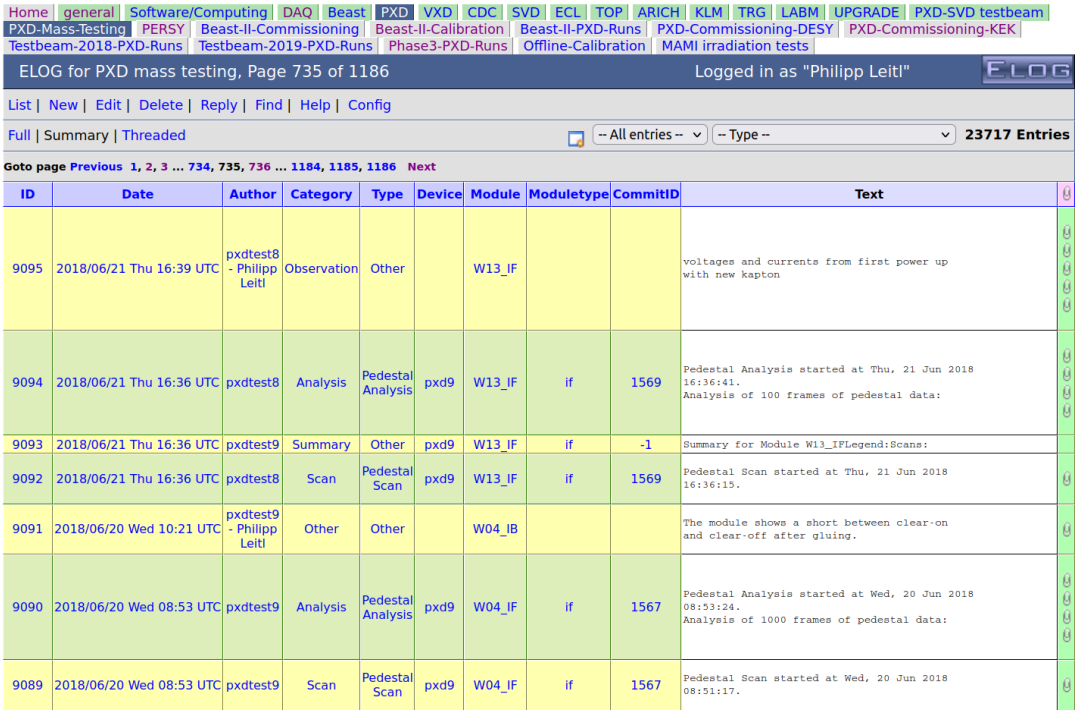
7.3.2.2. ELOG - online logbook

As laboratory logbook an online ELOG instance was used. This comes with the advantage that every collaborator can contribute to the same logbook. The entries are attributed to the individual modules and therefore easily filtered and searched. Furthermore, information about the operator, creation time and used setup are stored (see fig. 7.14).

The PXD ELOG was used for manual entries as well as for automated entries by the testing scripts. The operators entered information about particular test results by hand to the logbook as specified through the handbook instructions. In addition, all unusual observations and possible incidents were added. Besides the manual submission of entries, the application programming interface (API) of the ELOG service was used to automatically create entries every time a measurement or analysis script was run [96].

[4] https://confluence.desy.de/

Later, the ELOG was also extended to be used by the Belle II collaboration as run and shift logbook for the running experiment at KEK. Also for this purpose automated entries are created with information and statistics about the current run [96].



Home | general | Software/Computing | DAQ | Beast | PXD | VXD | CDC | SVD | ECL | TOP | ARICH | KLM | TRG | LABM | UPGRADE | PXD-SVD testbeam
PXD-Mass-Testing | PERSY | Beast-II-Commissioning | Beast-II-Calibration | Beast-II-PXD-Runs | PXD-Commissioning-DESY | PXD-Commissioning-KEK
Testbeam-2018-PXD-Runs | Testbeam-2019-PXD-Runs | Phase3-PXD-Runs | Offline-Calibration | MAMI irradiation tests

ELOG for PXD mass testing, Page 735 of 1186 — Logged in as "Philipp Leitl"

List | New | Edit | Delete | Reply | Find | Help | Config

Full | Summary | Threaded — -- All entries -- — -- Type -- — **23717 Entries**

Goto page Previous 1, 2, 3 ... 734, 735, 736 ... 1184, 1185, 1186 Next

ID	Date	Author	Category	Type	Device	Module	Moduletype	CommitID	Text
9095	2018/06/21 Thu 16:39 UTC	pxdtest8 - Philipp Leitl	Observation	Other		W13_IF			voltages and currents from first power up with new kapton
9094	2018/06/21 Thu 16:36 UTC	pxdtest8	Analysis	Pedestal Analysis	pxd9	W13_IF	if	1569	Pedestal Analysis started at Thu, 21 Jun 2018 16:36:41. Analysis of 100 frames of pedestal data:
9093	2018/06/21 Thu 16:36 UTC	pxdtest9	Summary	Other	pxd9	W13_IF	if	-1	Summary for Module W13_IFLegend:Scans:
9092	2018/06/21 Thu 16:36 UTC	pxdtest8	Scan	Pedestal Scan	pxd9	W13_IF	if	1569	Pedestal Scan started at Thu, 21 Jun 2018 16:36:15.
9091	2018/06/20 Wed 10:21 UTC	pxdtest9 - Philipp Leitl	Other	Other		W04_IB			The module shows a short between clear-on and clear-off after gluing.
9090	2018/06/20 Wed 08:53 UTC	pxdtest9	Analysis	Pedestal Analysis	pxd9	W04_IF	if	1567	Pedestal Analysis started at Wed, 20 Jun 2018 08:53:24. Analysis of 1000 frames of pedestal data:
9089	2018/06/20 Wed 08:53 UTC	pxdtest9	Scan	Pedestal Scan	pxd9	W04_IF	if	1567	Pedestal Scan started at Wed, 20 Jun 2018 08:51:17.

Figure 7.14.: Entry list view of the ELOG for PXD mass testing.

7.3.2.3. Discussion of results

After a module went through the entire characterization process, the results were presented in a weekly meeting with colleagues and experts including also the teams from the other test locations. This gave the opportunity to discuss particularities of individual modules and simultaneously to inform the collaboration about the testing progress. The exchange of experience proved very helpful in addressing commonly experienced issues. A common assessment was often the important basis for further decisions, like agreeing on the grading of a module or determine the further procedure for a problematic module.

7.3.3. Software quality

The development of the PXD laboratory software framework (see. section 5.3.3) started 2014 and is a still ongoing process with more than 30 contributors until today. The most important aspects concerning the software quality turned out to be **coding guidelines**, which gave the project a defined structure, a shared **version controlled repository** utilizing software development tools for issue tracking, feature discussion and pull requests, and **software documentation**.

7.3.3.1. Software guidelines

After the initial prototype testing phase and in view of the upcoming mass testing, coding guidelines defining the structure for each measurement were introduced in 2017. They standardize the structure of the software repository and of the optimization scripts in particular (see also section 5.3.3). As result, an in-depth knowledge of the scripts is not required for the operator to run the optimizations.

Each calibration is an own package under the **calibrations** folder and follows the common structure $Measurement \rightarrow Analysis \rightarrow Upload$. Through configuration files the operator can specify parameters like the ranges for a parameter sweep, measurement modes, number of recorded frames etc. Default configuration files with the available options and default settings have to be provided by the developer.

The **measurement.py** script first prepares the system by applying the required configuration. Then it initiates the data taking and stores the data in a specific structure. A **.latestpath** file is used to save the path to the data, which in turn can be automatically found by the subsequent data analysis script. In addition to the recorded data, also the specified parameters from the configuration file and a snapshot of the system configuration ("PV dump") is saved. After the measurement, all changes to the system are reverted to restore the initial configuration. An automated ELOG entry is created containing time and date as well as additional information about the used setup.

The **analysis.py** script takes only the previously recorded data and saved configuration information from the measurement and does not interact with the system. This enables the analysis of data at a later point in time and independent of the particular setup. The analysis results are stored under the same folder as the recorded data. Again, an automated ELOG entry is created.

The **upload.py** script reads the analysis result and applies the optimized settings either to the system directly or the operator requests the creation of a new commit in the configuration data base with updated settings. The new commit becomes the new standard configuration for the respective module.

In addition to these project specific coding guidelines, also a list of general style checks were added and enforced with pre-commit hooks [165], e.g pep8 [166], flake8 [167] and docformatter [168]. A further improvement of the software reliability was achieved by introducing an automated testing routine based on pytest [169]. For this, the basic system response had to be simulated to also test functions which work on online system data.

7.3.3.2. Software version control

The common software repositories are distributed and managed within the collaboration using the git software version control system [170]. There is one large repository for the lab_framework and several further repositories for the numerous IOCs.

The individual developments were organized in close consultations during weekly meetings to avoid multiple developments for the same task by different groups. Mutual code reviews and pull requests ensured code quality, compliance with the coding guidelines and applicability to all other test setups. Furthermore, an online ticket system[5] for tracking feature developments as well as bugs is used. Important versions are tagged to define a certain software state which cab be used across all test setups ensuring again comparability of the test results.

7.3.3.3. Software documentation

An easy to browse software documentation with text search is available online[6]. This resource is automatically compiled by the Python documentation generator Sphinx [171] from the docstrings given in the source code. Therefore, an extensive and descriptive documentation of all functions and classes by the developers is a mandatory obligation for all contributors. In addition, more detailed descriptions to special topics are collected also on confluence.

[5] former https://agira.desy.de/projects/BIIPXDH/
now https://gitlab.desy.de/belle2/detector/pxd/pxd_sc_lab_framework/-/issues
[6] https://pxd.belle2.org/PXD_Lab_Software/

7.3.4. Monitoring

The monitoring during the testing phase covered the test setup and module states as well as the environmental conditions in the laboratory.

7.3.4.1. EPICS archiver

The system state of a running PXD module is defined by more than 10 000 PVs provided from several different IOCs. Even though most PVs are static or change only occasionally, it is not possible for an operator to constantly keep track of all important changes. Hence, an instance of the EPICS Archiver Appliance [117] was installed on a PC in the laboratory network. It had read rights on all test setups within the laboratory and automatically monitored all active PVs with a sampling rate of about 1 Hz.

A custom-made Python script utilizing the URL interface of the Archiver Appliance was written which allows a comfortable configuration. All PVs, which should be monitored at a PXD test setup, were added to a lookup table. The operator only has to specify the setup or module specific number. All PVs are then automatically added to the archiver.

The recorded data is visualized by the Archiver Viewer [120]. It provides a web interface for a quick graphical display of the time development of the PV values. For a more detailed analysis of the recorded data, it can be retrieved from the archiver with a further custom-made script written by the author. The data which is provided by the archiver in JSON format gets converted into numpy arrays as standard data format used in the lab_framework. In addition, the aapy module [121] which is available on github was adapted to fit the PXD specific data compression intervals and can thus be used to retrieve also the compressed data from the archiver[7].

The EPICS Archiver was a very important monitoring tool during the module testing phase. It allowed a detailed analysis of module operations like the ramping of voltages during state transitions. The **Archiver Power-Down Plot** on the next page, for example, visualizes 20 voltages and corresponding currents which quickly change within just a bit more than a minute during the standard power down procedure. Also sudden incidences could be studied in hindsight.

[7] fork available at https://github.com/philipp-leitl/aapy

archiver data plot - W03_OF2 - start: 2019-03-11 19:13

These monitoring tools of the EPICS PVs are also used during the PXD operation at Belle II. However, as forty modules have to be monitored in parallel, the number of actively monitored PVs per module was significantly reduced to reduce the load on the archiver.

7.3.4.2. Environmental monitoring

Besides the state of the test system itself also the environmental conditions within the laboratory were monitored. Air temperature and air humidity were constantly measured and recorded. This is especially important through the summer month when the surface temperature of the cooling block and the PXD module may fall below the dew point. As the laboratory at the MPP is air-conditioned, including temperature and humidity control, no problems occurred here. However, damaged and destroyed modules at all other testing locations due to this issue underlined the importance of environmental monitoring.

7.3.5. Databases and data storage

The task to preserve the arising data and information during the module testing phase was split onto four different systems depending on the type of data. Two databases were used to keep track of the hardware states (**production database**) and the optimized configuration parameters (**configuration database**). Equally, two data storage systems were used to save the recorded module data and analysis results (**grid dav**) and more general data like photo documentation, filled checklists and output of other survey devices (**keeper**).

7.3.5.1. Production database - HephyDB

Each hardware component of the final PXD system but also of the test setups was documented and tracked in the project specific production database. This tool was developed for the production of the SVD at the Institute of High Energy Physics at the Austrian Academy of Sciences (HEPHY), hence the name **HephyDB**. It was equally suitable for the production of the PXD and, therefore, was shared with the PXD collaboration.

The HephyDB is used via a web interface[8]. Hardware components are structured in

[8] available at http://hephy.at/hephydb/hephydb/

Item type → *Item subtype* → $Version$. Each physical instance is represented by a corresponding item in the database. Common information about items of the same type, subtype or version are automatically assigned to all instances. Individual information can be added with an arbitrary number of custom tags and a comment field. A search function and filters allow to browse all entries. The HephyDB also allows to combine individual items in order to form a new item. In this way, ASIC items and a Kapton cable item are attached to a sensor item reflecting the real production process to finally form a PXD module item.

All items as well as all users are associated with a location. Items can be transferred to other locations through a process which mimics the real procedure. Only users with the same location as the items can prepare a transport by collecting all items into a virtual transport. Besides the destination also a recipient at that location has to be specified. The recipient gets notified by email as soon as the transport is marked as sent. In turn, the sender gets notified after the recipient acknowledged the receipt.

Special items were equipped with a checklist. For the PXD modules it contained all production steps from the ASIC assembly including probe card testing to the final x-ray inspection after Kapton attachment and all subsequent optimization measurements. After the concluded characterization of a module, the operator has to enter the found grading.

The HephyDB production database allowed to track all hardware components during production and characterization. In addition, during all status changes also the responsible user is recorded, so that a full documentation of the interaction with the hardware items is available. The history of each item can thus be retraced. The HephyDB was an indispensable tool to keep the overview over all produced modules and service items and their current state and location, heavily facilitating all installations from test setups up to the final integration into Belle II.

7.3.5.2. Configuration database - ConfigDB

Starting from simple configuration files, a scalable system was developed at the University of Heidelberg [118]. The Configuration Database (ConfigDB) is a PostgreSQL database containing the individually optimized configuration parameters for each PXD module. It is structured in files, where - during the module testing phase - each file was associated with a single module and therefore denoted by the module name. Later also a large PXD file was composed from the individual module files.

The standard branch of a file is called “trunk”, arbitrary side branches with custom names are possible. The individual entries in the branches are called commits. A new commit is always added like a new pearl to the already existing string of commits, no entry is ever overwritten. The structure is illustrated in fig. 7.15.

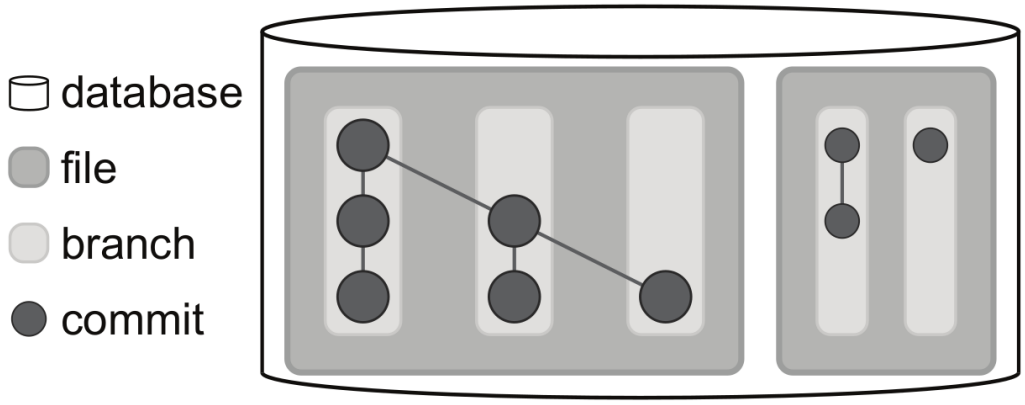


Figure 7.15.: Structure of the ConfigDB [118]. Several files with several branches, each containing a string of commits, can be stored.

A single commit for one PXD module stores more than 3 400 PVs with module-specific values[9]. The data is stored in an XML-like tree structure with “DHE” and “PS” as parent nodes and several iterations of child nodes. Each node adds a part to the combined PV name and in the leaf, at the end of the line, the corresponding PV value is stored.

Each commit is identified by a single integer number, the commitid. The ConfigDB IOC provides the commitid PV and retrieves all configuration data for the specified commit from the database. The loaded values are then available for the other IOCs to apply them onto the system.

One central instance of the ConfigDB at Heidelberg was used for the module testing phase. It was a collaboration-wide accessible instance for all test setups which allowed to load the module specific optimized values at all testing sites. At the Belle II experiment a dedicated instance is running in the protected network. The XML export and import utility was used to transfer the optimized values between the ConfigDB instances.

[9] The rest of the more than 10 000 PVs for a module setup contain static, module-independent values like hardware limits of the PXD Power Supply or predefined alarm thresholds, and monitoring PVs for e.g. temperature, data rates and sensed voltages and currents.

7.3.5.3. Module raw data and analysis backup - grid dav

The amount of recorded data per module characterization run exceeds several GB of storage. In order to free storage space on the laboratory workstations and to share the data with the collaboration, a central storage of all module characterization data including analysis results is used. The Max Planck Computing and Data Facility (MPCDF) provides a dCache system [172] for this purpose. It is freely accessible through WebDAV at https://grid-dav.rzg.mpg.de:2882/PXD_precharacteriztion/.

The measurement data have to be uploaded by the operator with the globus software [173] which manages the access rights on basis of gird certificates. Only users which are members of the Belle II VO have write permission.

7.3.5.4. Storage of inspection data and documentation data - keeper

All remaining data, which arose during the module testing phase, were stored on an instance of the file sync and share solution Seafile [174]. The Max Planck Digital Library (MPDL) provides this service under the name Keeper[10]. Data can be easily uploaded and shared through a web browser.

Stored data are for example photo documentation, thermal images, microscopic pictures, but also digitized copies of filled paper checklists and any further measurement data. For the inspection of the gluing joint between two PXD modules forming a ladder (see chapter 8) also the desktop client was configured so that the images taken by the technician were automatically uploaded.

7.3.6. Quality control

The last aspect of quality assurance addressed in this thesis concerns the quality control of the PXD modules. A **standardized testing procedure** with several optimization steps was developed. In addition, a detailed instruction manual, the **PXD mass testing handbook**, was written to ensure the completeness and comparability of results independent of the used testing setup and the operator. The handbook and the testing procedure as well as the results are presented in the next section.

[10] https://keeper.mpdl.mpg.de/

7.4. PXD module characterization

With conclusion of the Kapton cable attachment, the last production step, the modules are ready to be attached to a module test setup (detailed description in chapter 5). It poses the infrastructure for module operation comparable to the experiment configuration, only reduced down to one module. Therefore, it is possible to verify the module performance to be expected in the experiment.

Until this point the functionality of the modules was only tested rudimentary to spot production defects and attempt a repair where applicable. For the PXD module characterization the complete PXD module system is available and the aim is an in-depth performance optimization by varying operation parameters. A detailed performance analysis builds the basis for a conclusive module grading.

First the **PXD mass testing handbook** is described. It was written to guide the operator through the optimization process, hence, ensuring comparability of the results between all tested modules as well as enabling also testing by operators not involved in the software development. The handbook contains descriptions of execution for each test script naming the required preparations, varied parameters and standard settings, but sparing the operator the details about the **automated measurement routines** and **optimization algorithms**. They are presented next in section 7.4.2.

This chapter closes with an overview of the **main production module performance**. Observed issues during testing are presented, like Switcher damages during operation, a pre-irradiation effect and disconnected drains. The optimal parameters found over all tested modules are shown as well as the performance indicators used for the final module grading.

7.4.1. The PXD mass testing handbook

The PXD mass testing handbook poses a self-contained manual document for all operators who deal with the standardized optimization process for PXD main production modules. It comprises general information about the hardware of the module setup, used software versions and configurations, directives for the mechanical handling of the modules and instructions how to perform each optimization measurement. The handbook minimizes the requirement of previous knowledge about PXD module operation. Knowledge about the automated module configuration, data taking and analysis algorithms is not required at all. Thus, the number of possible operators is increased with a minimum of training period.

The handbook is created as LaTeX document and is part of the lab_framework repository. Updates are pushed to the central repository similarly to code changes and are likewise available for all collaborators. Whenever an update in one of the measurements requires an adaptation of the handling by the operator, the change can be transmitted simultaneously.

7.4.1.1. Software versions and configuration

The handbook lists the version numbers of all required software packages and EPICS IOCs as well as the used DHE firmware version. It contains also instructions on how to update and install the correct version of the lab_framework repository and of the pyDepfetReader package. In addition, setup specific adjustments of the configuration files (host.ini and master.setup.ini) as well as the correct definition of the dheid are explained. Finally, the configuration of the EPICS archiver and also the creation and usage of configDB commits is described.

7.4.1.2. Mechanical handling

The instructions on how to install a PXD module into the laboratory module setup and how to dismount it again were added to the test setup itself as stated in section 7.3.2. However, for the sake of completeness and because of the complexity of the procedure and a high risk to damage the modules during handling the instructions are also stated in the handbook.

7.4.1.3. Instructions for optimization measurements

After all preparations of the software configuration and the hardware setup the module is ready for the optimization process. Each calibration routine is stored in an own subfolder of the lab_framework as explained in section 5.3.3. The handbook defines the correct order in which the calibrations have to be performed. Furthermore, it contains instructions on how to perform the individual calibrations, the recommended start values for the operation parameters to be optimized and additional information for the specific task. Where applicable, a reference for the expected outcome is given so that the operator can directly compare the present results. The handbook also regularly reminds the operator of the obligatory documentation tasks within the ELOG and the hephyDB.

7.4.2. Standardized testing and optimization procedure

The standardized testing and optimization procedure of the PXD main production modules consists of nine measurements, which each module had to go through in the specified order (see fig. 7.16). Two measurements require several manual tasks by the operator ("first power-up" and "temperatures", indicated with a hand symbol in the flow chart), while the other measurements are mostly automated (indicated with a gear symbol).

The estimated duration of the measurements as shown in fig. 7.16 represent the ideal case and may differ, especially concerning time for result verification and documentation. Sometimes measurements have to be repeated with different settings and unforeseen issues always require adjusted treatment, which takes additional time.

For an ideal case, the entire procedure for one module takes about one week. The more lengthy measurements run over night. With the two module test setups at the MPP, it was possible to fully test and characterize two modules per week. Problematic modules were discussed in expert meetings and put aside for detailed investigation by experts, if required.

A description of each measurement follows below. Also the cumulated results over all 62 tested modules are shown for each measurement.

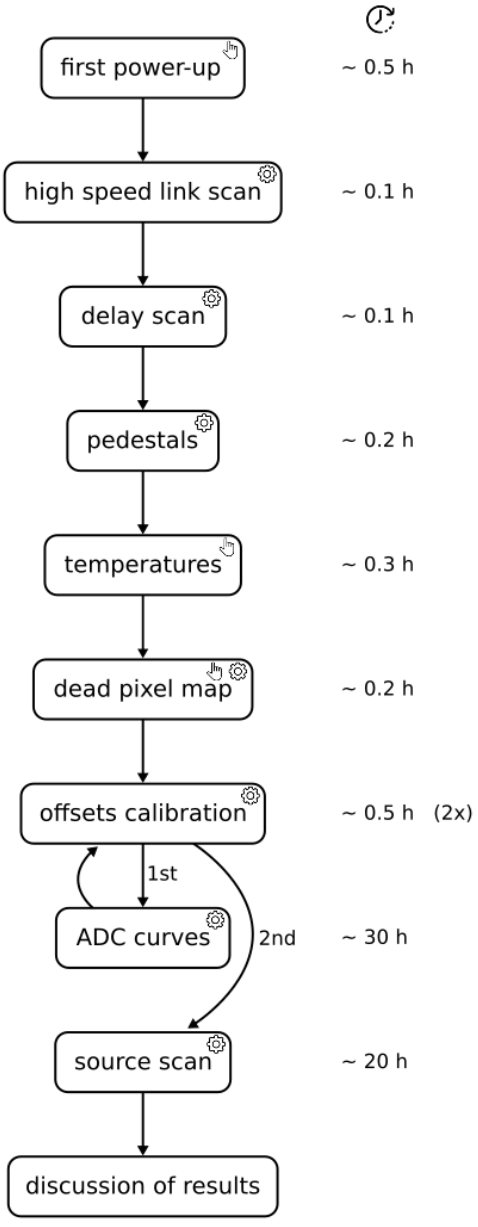


Figure 7.16.: Standardized mass testing procedure. The flow chart indicates the applicable order of the measurements. The right column shows the estimated duration for each measurement.

7.4.2.1. First power-up

Powering up a new module for the first time is a critical procedure. The testing operator needs to examine any deviations from the expected behavior while becoming familiar with the individual conditions of each module. That is particularly important for the voltages, currents, and temperatures.

Therefore, the automated sequence is interrupted at specific steps during the first power-up. Each time the operator must check and document the voltages, currents, and temperatures. Voltages that do not reach the set values and currents that hit the defined current limits indicate a problem in the electrical circuit. Temperatures that are too high indicate a problem with the cooling in the setup. If either of these issues occurs, it is necessary to stop further power-up of the system. These issues require expert resolution before the continuation of the testing process.

If the first power-up proceeds normally, the operator verifies the JTAG communication by retrieving the JTAG ID code from the DCDs. Moreover, the operator activates the DEPFET matrix by applying an appropriate low Switcher gate-on supply (gate-on) voltage. The source current should reach about 100 mA. Finally, the operator performs the first data readout by recording a pedestal map.

After a successful "first power-up", all basic functionalities of a PXD module are confirmed, like the electric circuit, JTAG communication, data links, and matrix operation. The operator creates a new commit with the updated gate-on voltages and documents the progress in the ELOG and HephyDB.

7.4.2.2. High speed link scan

The data transmission from a PXD module to the back-end electronics is realized through four high speed data links with a transmission rate of 1.6 Gbps per link. Each DHP drives its own differential high speed link which is received by the FPGA on the DHE card. The links utilize the Aurora 8B/10B protocol. The simplex transmitter channels feature automatic initialization and maintenance of the channel. The 8b/10b encoding provides features like DC balance, clock recovery, and error detection capability, while reducing the effective data rate to 1.2 Gbps. When a high error rate is detected, the DHE marks the links as "lost" or "down".

Within the DHPs the transmission interface is implemented as differential signal transmission logic through a custom-made, configurable Current Mode Logic (CML) driver with a main and a pre-emphasis stage. The pre-emphasis allows to compensate the

damping losses of the high-frequency component in the transmission lines, e.g. cables (see fig. 7.17).

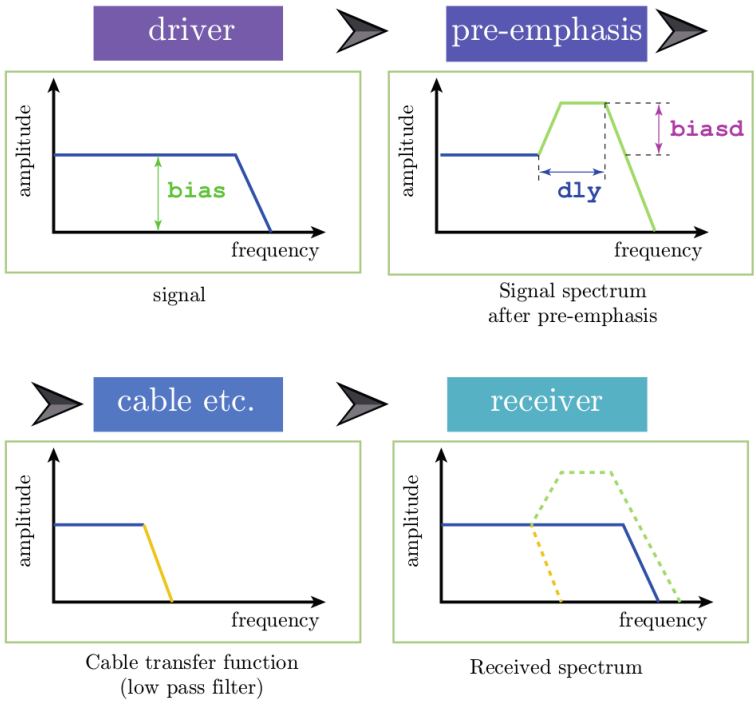


Figure 7.17.: Spectrum of DHP high speed link signal in transmission line [51, 175]. The cable acts as low pass filter and damps the high-frequency component of the signal. A suitable pre-emphasis at the driver restores the signal shape at the receiver.

The pre-emphasis is achieved by placing a second CML driver behind the first one with inverted signal order, a time delay, and a lower current source. While this decreases the voltage difference between the differential transmission lines for the low-frequency part, it increases the voltage difference for the high-frequency part (see fig. 7.18).

Three parameters of the transmitter implementation can be varied to adjust the output signal:

- The strength of the current source for the first CML stage is proportional to the peak-to-peak amplitude of the serial link output. It can be modified by the **bias** setting which is represented as 8-bit value within the "global" JTAG register of the DHP (`IDAC_CML_TX_BIAS`).

- The strength of the current source for the second CML stage is proportional to

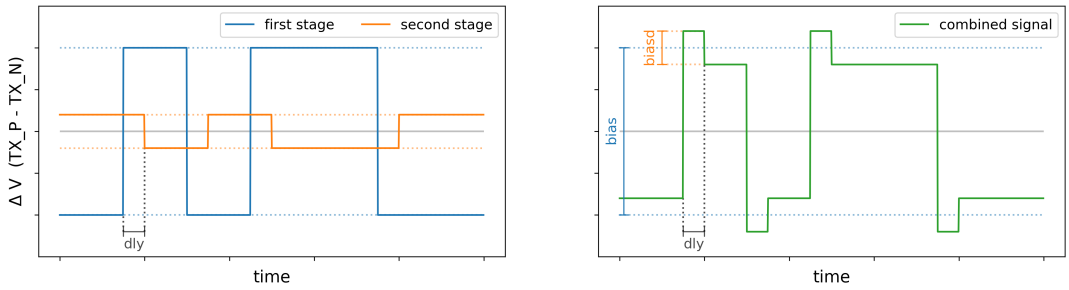


Figure 7.18.: Signal superimposition of first and second stage of the CML driver. Left: The `bias` setting determines the amplitude of the first stage, the `biasd` settings determines the amplitude of the second stage. A delay shifts the stages relative to each other. Right: The combined signal has a pre-emphasis overshoot.

the amplitude of the pre-emphasis overshoot. It can be modified by the **biasd** setting which is also represented as 8-bit value within the "global" JTAG register of the DHP (`IDAC_CML_TX_BIASD`).

- A **delay** between the first and second stage of the CML driver defines the width of the pre-emphasis overshoot. The delay setting is represented as 2-bit value within the "global" JTAG register of the DHP (`pll_cml_dly_sel`).

The signal path of the high speed data links consists of the copper traces on the PXD module, bond wires, Kapton cable, Patch Panel connector and cable, and connector and traces to the receiver on the Dock Box PCB (in total about 3 m). There the signals are transferred to optical signals which are guided through optical fibers to the DHH system on top of Belle II (about 15 m)[11]. Therefore, the configuration in the laboratory test setups corresponds to the final installation concerning the high speed signal paths on copper lines.

During the optimization measurement, the 2d parameter space of `bias` and `biasd` is scanned. For each setting the link status ("up" or "down") as well as the reported eye opening value is recorded. The eye opening is measured on the DHE in arbitrary units between values of 0 and 31. It is proportional to the voltage difference between the differential data lines at the receiver. Hence, it provides an estimate for the quality of the data link and the suitability of the chosen parameters.

A typical result of a full parameter scan in fig. 7.19 (left) shows working links for the majority of the parameter space. Only for `bias` values below 50 the link quality drops. The same characteristics were observed for several modules, hence the parameter space

[11] Signal damping is no issue for optical fibers of that length, however, a proper contact of the connectors is vital. This is monitored in the Belle II experiment by signal amplitude measurements in the DHH system.

was reduced as in fig. 7.19 (right) and the step size was set to 5 for both parameters to reduce the testing time during the mass testing.

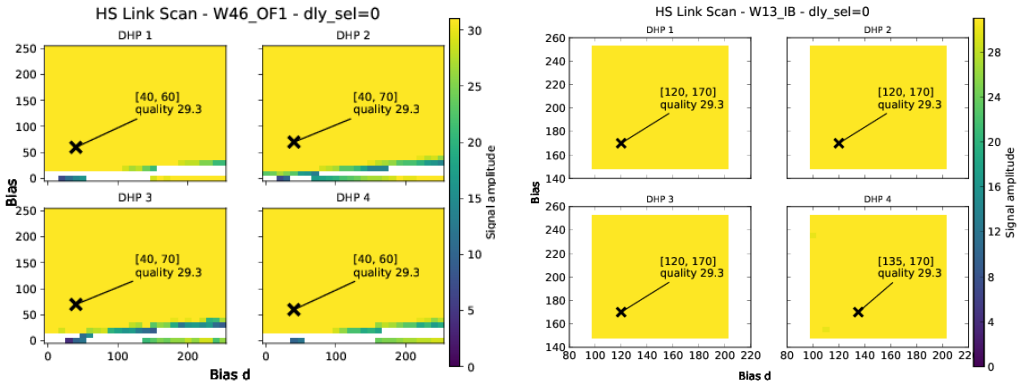


Figure 7.19.: Results of high speed link scans with different parameter ranges. Left: A scan of the entire parameter range (0 - 255 for `bias` and `biasd`) reveals unstable links for `bias` settings below 50. Right: In the reduced parameter range for the mass testing almost all settings reach the highest quality score.

The analysis script automatically detects the optimal parameters for each link by calculating a quality score for each setting as weighted sum over the recorded values including the next neighbors and next-to-next neighbors. For this measurement the timing between Python scripts, EPICS, DHH, and JTAG is especially important [176]: The settings have to be applied to the system through the long command chain and the status needs to be updated before the corresponding eye value is recorded.

Figure 7.20 shows the results over all tested modules. The most frequent setting for `bias` is 120 with a second maximum at 220 / 225. The most frequent setting for `biasd` is 125. The delay setting was always kept at 0. After the completion of the mass testing, more detailed studies with oscilloscope measurements confirmed the suitability of the found settings. With higher resolution, the optimal setting for the PXD configuration was found to be `bias` 100, `biasd` 235, and `delay` 0 [153].

In conclusion, the high speed links proved a good link stability for a large parameter range during the mass testing. Finer measurement methods were able to further narrow down the optimum. Still, the *high speed link scan* is a helpful tool to quickly determine the capability of the data link connections and to find working parameters without further testing infrastructure.

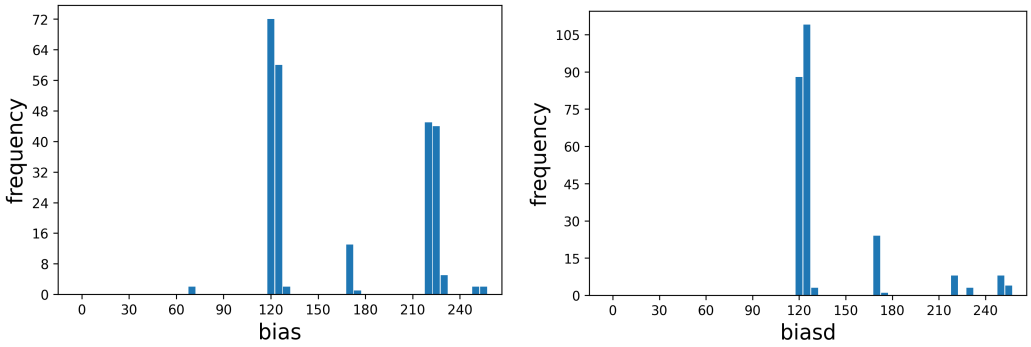


Figure 7.20.: High speed link scan results from mass testing. The results contain data from 62 fully characterized PXD modules. The step size in the parameter scans was set to 5. The delay parameter was always set to 0.

7.4.2.3. Delay scan

For data transmission between DHP and DCD the ASICs are connected through transfer lines on the silicon module. Each of the 256 ADCs of a DCD generates 8 bit of data every 32 clock cycles. This data is transferred via $256 \times 8 \div 32 = 64$ single-ended lines. According to the geometry of 8 ADC column pairs within each DCD, the transfer lines are grouped into eight 8-bit wide output buses (see fig. 7.21). A data transfer rate of 19.5 Gbps between the ASICs is reached.

The signal integrity depends crucially on the correct timing between the two ASICs. If the signal is sampled too early or too late, a wrong value for the corresponding bit is recorded. Therefore, delay elements are implemented in the DHP to adjust the sampling point. Two parameters are available for the optimization. The **global delay** DAC (`dcd_clk_sdly`) has a size of 4 bit and shifts the output signal of the external DCD clock, which is sent to the DCD, with respect to the internal DCD clock and affects therefore all input lines in the same way. In addition, there are 64 **local delay** DACs (`dcd_rx_sdly`). They have a size of 4 bit each and add a delay to the individual input lines.

In order to test the integrity of the data transmission, a test pattern is implemented into the DCD (see fig. 7.22), which can be activated through the corresponding `TestInjEn` DAC in the DCD's global shift register. The received data is compared with the known template by the analysis script and the number of errors is counted for each transmission line. For a complete delay scan the entire parameter range of global delay and local delays are applied to the PXD module and the results are recorded. The analysis script creates a 2d plot for each of the 64 transfer lines and indicates the number of errors for each parameter combination (see fig. 7.23).

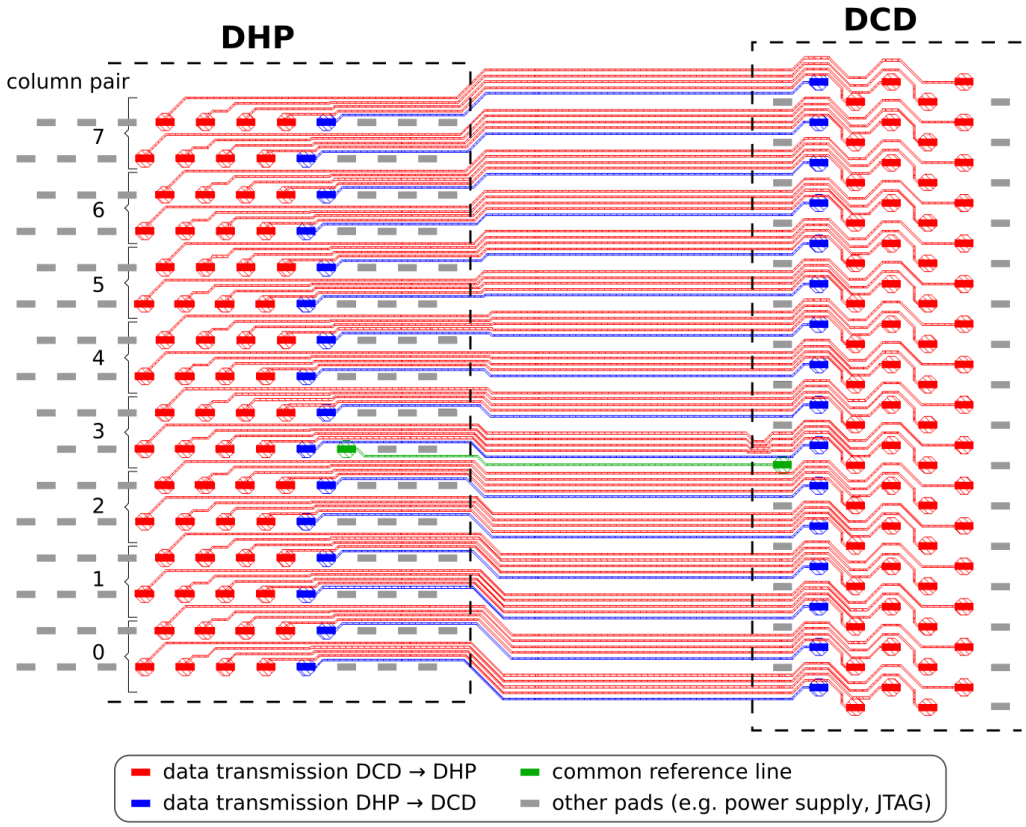


Figure 7.21.: Data transfer lines between DHP and DCD. The 64 data transfer lines from the DCD to the DHP (red) are grouped into 8 column pairs. Each column pair has also two transfer lines from the DHP to the DCD (blue) for the 2-bit digital-to-analog converter (DAC) for offset correction. One common reference voltage (green) is used as threshold for all data transmission lines. That allows to reduce the number of lines by half plus one, compared to a standard differential signal scheme for each individual line.

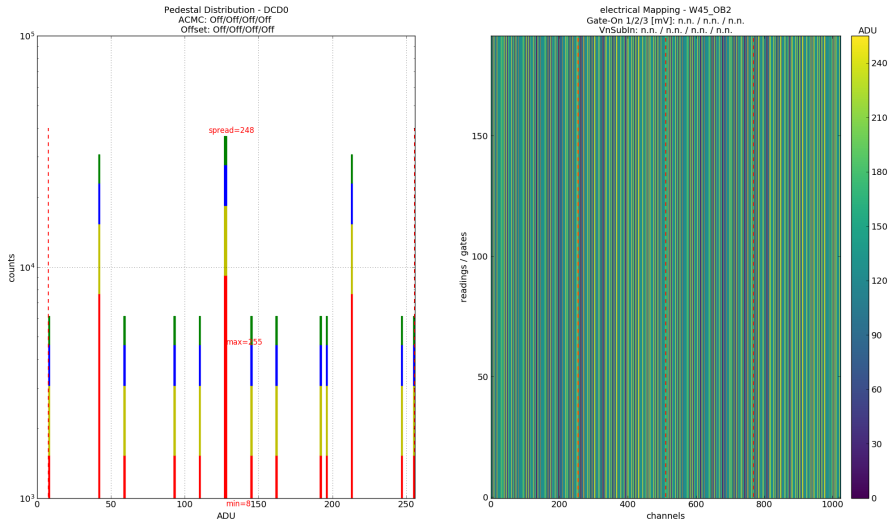


Figure 7.22.: DCD test pattern for data transmission verification. Left: Histogram of predefined ADU values. Right: Representation in electrical format. A constant value is assigned to each ADC, hence constant values are displayed along the vertical axis.

The optimization algorithm, which automatically calculates the best settings, is described in detail in [51]. For the global delay settings the maximum of consecutive error-free readings is counted for each transfer line. Then, for each global delay setting the minimum of these values is taken and compared to the other global delay settings. The global delay with the largest of these minima is chosen, i.e. the best global delay for the worst performing line. Finally, the local delay settings are determined as the setting in the middle of the error-free range for each transfer line.

For all tested PXD modules without major electronics defect it was possible to find delay settings which ensured error-free data transmission on all transfer lines. Vice versa, a channel without error-free delay settings points to a major issue within the module. For most of the early modules a global delay of 0 was found as optimum. Therefore, the parameter range was reduced to a constant global delay of 0 for the mass testing routine to reduce testing time. For all healthy modules, local delay settings were found which ensured an error-free data transmission.

A **global delay setting of 0** was established as result of the delay scans during the mass testing. Only two modules (W44_OB1 and W46_OB1) were assigned a global delay of 1 and for both also a value of 0 was possible for an error-free data transmission. All optimized **local delay settings are within 5 ± 2** (see fig. 7.24). These optimized delay settings are stable and do not need adjustment over time as long as the used clock frequency and bias conditions are constant.

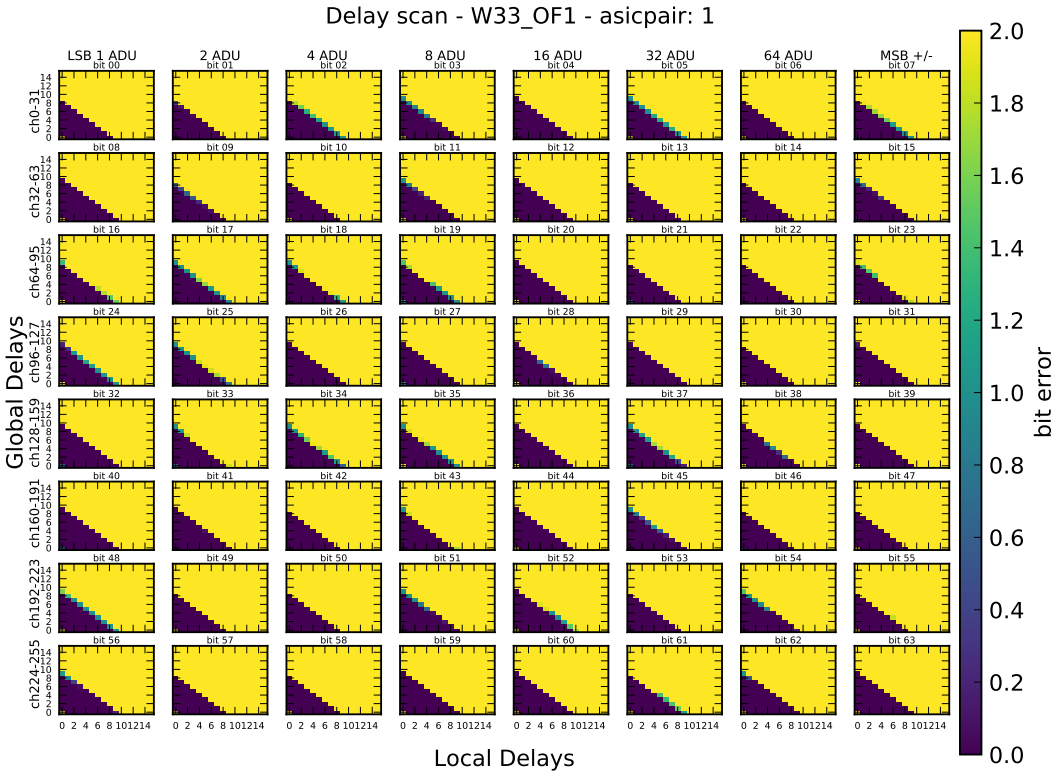


Figure 7.23.: Result plot of delay scan analysis. For each of the 64 transfer lines of one ASIC pair an own subplot is created. In this measurement, the entire parameter range was scanned. For each line an error-free band in the lower left corner is visible.

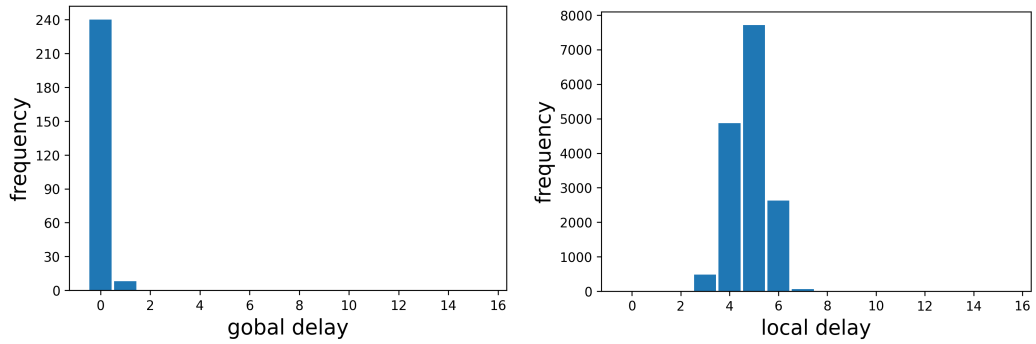


Figure 7.24.: Delay scan results from mass testing. The results contain data from 62 fully characterized PXD modules. Optimized delay settings were found to be 0 for global delay in combination with 5 ± 2 for local delay.

7.4.2.4. Pedestals

Building on the results from the first two optimizations (high speed link and delay scan) now an error-free data transmission enables the first look on pure matrix data. At this stage the operator may shift the pedestal distribution slightly within the dynamic range by adjusting the gate-on voltages or the `VNSubIn` DAC. The otherwise not yet optimized status of the matrix performance is then documented by taking 1 000 pedestal frames. Already this early pedestal scan reveals a good impression of the DEPFET matrix. Several issues can be spotted, like pre-irradiation effects and disconnected drains (discussed later in section 7.5). In addition, a noise calculation is performed. The typical noise for PXD modules lies below 1 ADU [96] (see also later in section 7.5). Deviations point to problematic issues within a module.

Furthermore, the pedestal distribution is an important indicator for the module performance. Ideally, all pedestal values lie well within the dynamic range of the ADCs and build a narrow distribution below about 200 ADU, so that a hit of an ionizing particle can be detected reliably. Hence, one of the goals of the mass testing procedure is the optimization of the pedestal distribution. The most important tools in this respect are the 2-bit offset compensation and the common mode corrections which are explained below. Figure 7.25 shows the comparison of pedestal distributions before (left) and after (right) the matrix optimization routine for module W03_OF2.

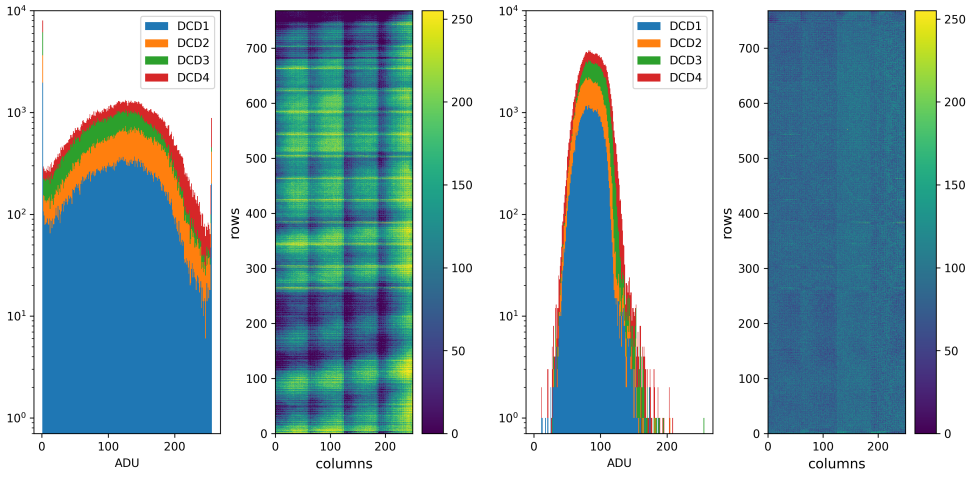


Figure 7.25.: Comparison of pedestal distribution before and after optimization. Left: The initial pedestal distribution exceeds the dynamic range of the ADCs. Right: After the optimization the pedestal distribution is narrower. Local differences within the matrix are flattened.

7.4.2.5. Temperatures

The importance of temperature monitoring during module operation has already been repeatedly pointed out. This part of the testing procedure requires the operator to actively watch and document the module temperatures during different powering conditions.

Three states are set and monitored for at least 5 minutes:

- STANDBY (only digital part powered and matrix off),
- PEAK but matrix blocked (gate-on voltages same as gate-off voltage),
- PEAK with nominal gate-on voltages.

The current consumption increases for each step, especially when the matrix is activated. This is visible in the dcd-avdd line which powers the analog part of the DCDs. An increase of almost 600 mA in the last step results in a temperature rise of about 6 °C on the module. Typical values are listed in table 7.1.

Table 7.1.: Typical PXD module temperatures and dcd-avdd currents with standard deviation in test setup operation.

	STANDBY	PEAK (matrix blocked)	PEAK
temperatures [°C]	42 ± 7	42 ± 7	48 ± 7
dcd-avdd current [mA]	2085 ± 61	2085 ± 61	2651 ± 65

A threshold of 80 °C was set for the continuous temperature monitoring to trigger an emergency off in order to protect the electronics and solder joints on the modules. During operation in PEAK and with proper cooling, occasional maximum temperatures of up to 65 °C were reached. This is still reasonably below the threshold to allow for a stable module operation. It also confirms the capability of the water cooling system including custom made cooling blocks and cooling adapters for the inner modules (see section 5.2.2). However, due to the water temperature of 16 °C to 18 °C the dew point has to be considered during warm and humid weather conditions.

The temperature measurement within the mass testing procedure was an additional confirmation that the installed module was properly cooled. This is required for a save module operation and a prerequisite for the further optimization measurements which need several hours of uninterrupted data taking. In addition, it provided some statistics about PXD module temperatures.

7.4.2.6. Dead pixel map

The creation of a "dead pixel map" serves as preparation for the following "offsets calibration". The calculation for the 2-bit offset DACs as well as the the online calculation for the common mode correction within the ASICs gets distorted by broken pixels. Both calculations are explained below. In this step of the mass testing routine, it is important to identify the broken pixels of a module's matrix and create a "dead pixel map" so that these pixels can be excluded from the calculations. In fact, the settings in the ASIC registers only allow to mask entire channels. However, when only a part of a drain line is broken, the advantage of masking some broken pixels still outweighs the masking of the remaining working pixels.

Two types of broken pixels are looked for: pixels with abnormally low drain current (e.g disconnected pixels) and abnormally high currents (e.g. hot pixels with a short). In order to detect the disconnected pixels, the operator needs to adjust the gate-on voltages or the `VNSubIn` DAC to shift the pedestal distribution into the upper dynamic range. In this way, working pixels show a high ADU value, whereas pixels which are not connected will show a low ADU value, typically below 20 ADU. This threshold is then used to identify the not connected pixels in a pedestal map. The same is repeated for a pedestal distribution shifted to low ADU values, where the hot pixels still exceed a threshold of 200 ADU. An example of a broken pixel map is shown in fig. 7.26.

This measurement requires some manual adjustment by the operator and also the exact values of the thresholds can be adjusted by the operator. The created "dead pixel map" is stored in the module's test data and will be used by the following optimization.

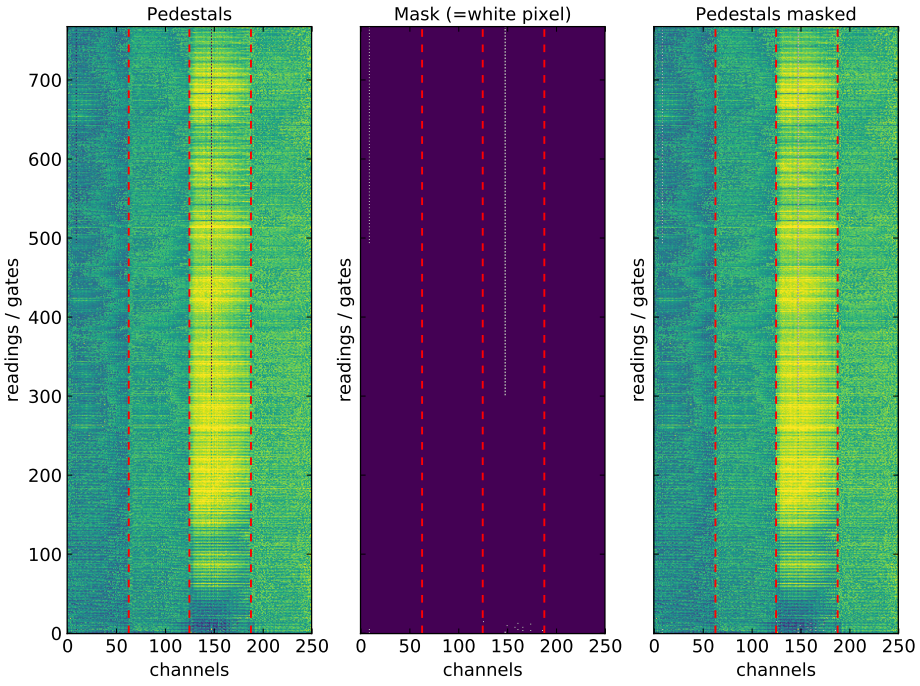


Figure 7.26.: Broken pixel mask of module W45_OB2. One partially broken drain is visible in the region of DCD1 and one in the region of DCD3.

7.4.2.7. Advanced offsets calibration

For an individual pixel the bias voltages can be adjusted to result exactly in the desired pedestal drain current. For the entire PXD module matrix, however, only limited bias options are available. The matrix is divided into only three gate-on regions, each controlling one third of the matrix. Hence, 64 000 pixels need to have the same bias settings, while deviations within the production material and production processes cause differences between the pixels. These result in a distribution of the pedestal drain currents. Two methods were developed by the ASIC designers to address this issue:

1. **Offset compression by additional current source**: An additional current source within the DCD allows to add current to the received drain current before digitalization. The strength of the current source, I_{DAC}, can be adjusted for a DCD globally (PV name `IPDAC`). In addition, for each pixel a 2-bit factor can be specified individually which multiplies I_{DAC} for that pixel. The factors (0, 1, 2, 3) are stored in the DHP and transferred via two transmission lines per column pair (see fig. 7.21). The operating principle on the pedestal distribution is demonstrated in fig. 7.27.

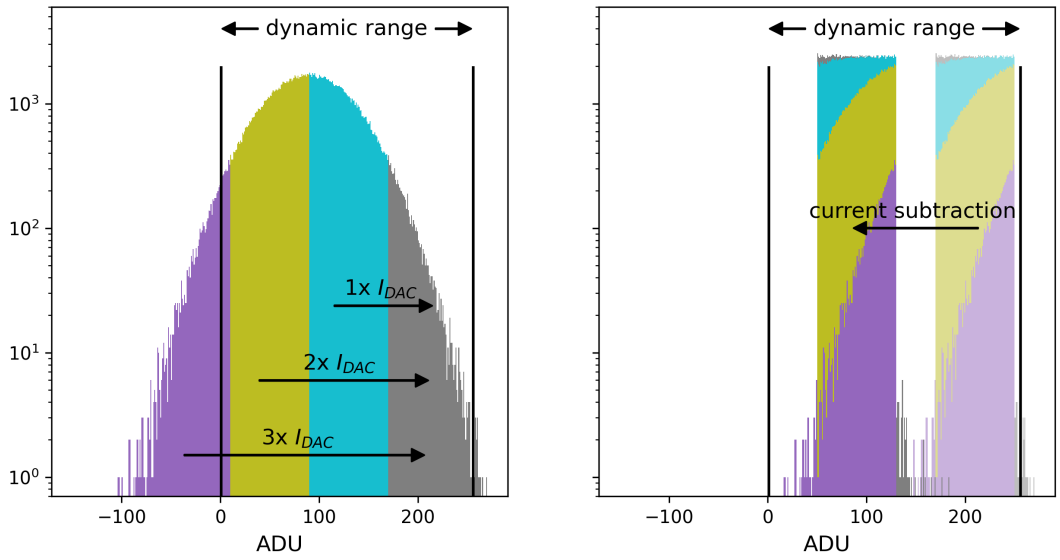


Figure 7.27.: Principle of 2-bit offset compression. The pedestal distribution is cut into four parts. Starting with the part with the lowest ADU values, each part gets a factor for the I_{DAC} current assigned, from 3 to 0. The additional current shifts the lower parts into the same ADU range as the part with the highest ADU values. A further current subtraction by `VNSubIn` or `VNSubOut` shifts the entire pedestal distribution to the desired lower end of the dynamic range.

2. **Common mode correction**: The sequential readout of 192 gates ("rolling shutter mode") causes different readout times for each gate. Noise with a frequency below the sampling rate affects each gate differently, but is common for all pixels in a gate which are read simultaneously, hence "common mode". For each gate the common mode can be corrected.

   - **Analog Common Mode Correction (ACMC) in DCD**: The common mode noise is compensated by an analog feedback. There is no hit detection, e.g. hits will bias the calculated common mode but the effect is considered negligible [177]. However, as the analog feedback acts before the digitalization, it is able to bring back currents into the dynamic range which would otherwise exceed the dynamic range because of large common noise. This allows a hit recovery, which is later on not possible. The common mode is calculated from the input currents on all channels with the possibility to exclude individual channels, e.g. not connected and broken drains. The corresponding `EnCMC` bit has to be set in the pixel chain register of the DCD [178]. The dead pixel map is used to set the correct configuration bits.

   - **Digital Common Mode Correction (DCMC) in DHP**: The DHP performs a digital common mode estimation with a "two parse average technique". After the pedestal subtraction the mean over all signal values of gate i is calculated (again excluding the not connected and broken pixels):

     $$\overline{sig}_i = \frac{1}{N} \sum_j sig_{i,j} \tag{7.1}$$

     with pixel signal $sig_{i,j}$, number of connected drains N, gate i and drain j.

     Then, all signal values of gate i are compared to $\overline{sig}_i$ plus a threshold. When $sig_{i,j}$ exceeds this value, a hit is assumed. In a second average all signal values, where a hit is assumed, are replaced with $\overline{sig}_i$. The new mean value CM_i is the calculated common mode of gate i:

     $$CM_i = \frac{1}{N} \sum_j \begin{cases} sig_{i,j} & \text{if } sig_{i,j} < \overline{sig}_i + th \\ \\ \overline{sig}_{i,j} & \text{if } sig_{i,j} \geq \overline{sig}_i + th \end{cases} \tag{7.2}$$

     with common mode threshold th (PV name `threshold` and commonly used value 7). Finally, the common mode is subtracted from the initial signal values to receive the common mode corrected signal values before the data enter the hit finder of the DHP [175].

     $$\widetilde{sig}_{i,j} = sig_{i,j} - CM_i \tag{7.3}$$

The initial optimization algorithm for the 2-bit offset compression does not take the common mode correction into account [112, 179]. Still, a significant reduction of the pedestal spread is possible and this optimization was used during the mass testing of the PXD modules. However, a new approach was developed by the author. The idea of the new optimization algorithm is to no longer look at both tools independently but rather profit from their combination. Hence, the new algorithm optimizes the offsets per gate instead of for the entire matrix. The performance criteria and quality estimation of the scanned settings are otherwise identical to the previous version of the algorithm [112]. Afterwards, the common mode correction automatically levels out the differences between the gates. The capability of the new algorithm is demonstrated on real module data (see 7.29).

The example of module W03_OF2 shows a module of grade A with a very good matrix performance. The advantages of the new approach are even higher for modules with a different pedestal response along the gates, like pedestal shifts on one side of the module due to uneven pre-irradiation (see section 7.5.2). The new approach was developed while the final modules were already installed as PXD at KEK. As a result of this new approach, we have been able to reduce the pedestal spread of the modules in the installation by almost half.

At the end of the measurement, the operator has to shift the pedestal distribution into the lower dynamic range by adjusting the `VNSubIn` value. Hence, the outcome of the offset calibration are optimized values for the 2-bit offsets per pixel, one `IPDAC` value and one `VNSubIn` value per DCD. The results of the optimization in the laboratories with the old approach show `IPDAC` values around 25 and `VNSubIn` values around 42 (see fig. 7.28). In section 9.3 it will be shown that the new approach has no significant impact on these distributions.

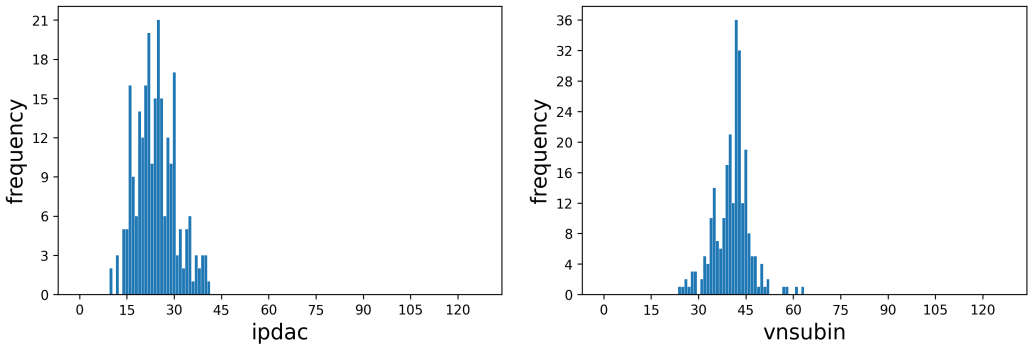


Figure 7.28.: Offset calibration results from mass testing. The results contain data from 62 fully characterized PXD modules. The `IPDAC` and `VNSubIn` parameters were scanned in steps of 1. Both distributions are centered around their maximum. The most frequent `IPDAC` value is 25. The most frequent `VNSubIn` values is 42.

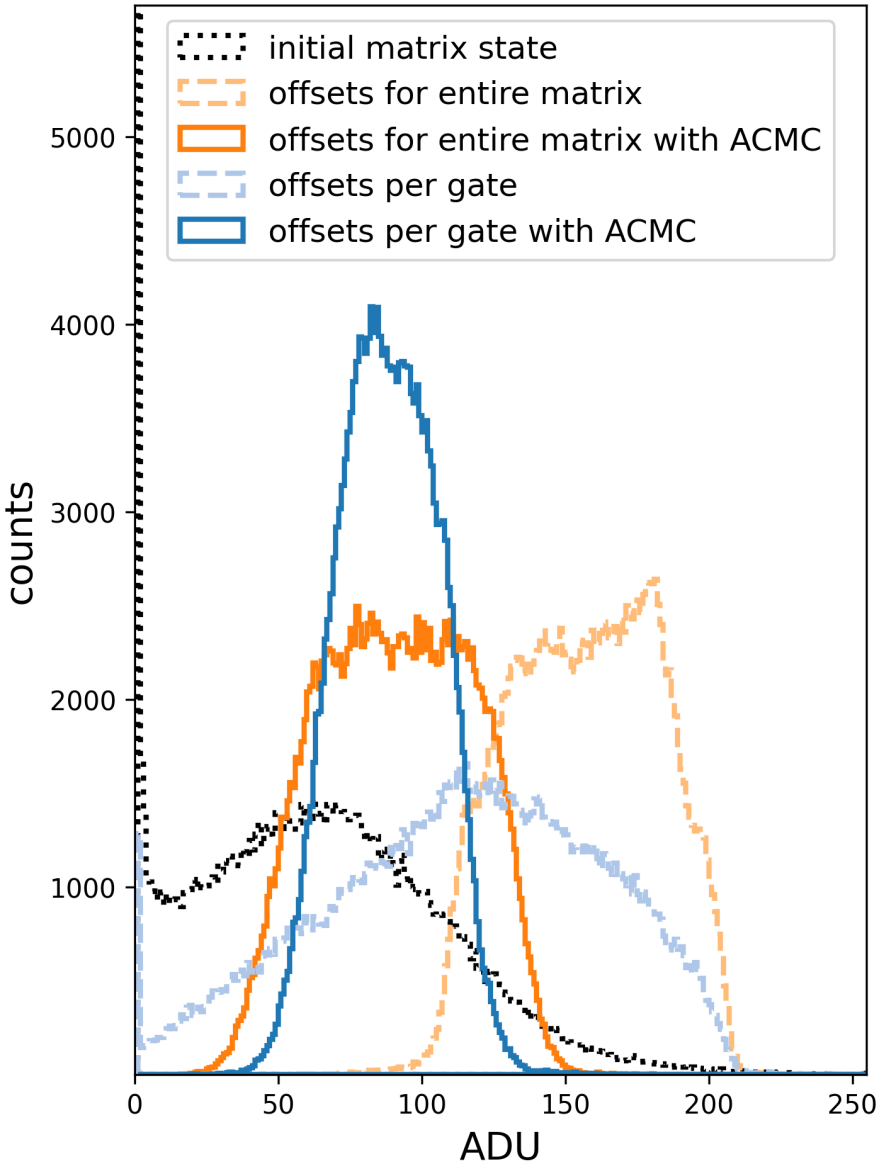


Figure 7.29.: Synergy effect of 2-bit offset compression with ACMC. Both approaches are demonstrated with data from the module W03_OF2 and with identical `VNSubIn` settings [45, 40, 43, 44]. The initial pedestal distribution (black) exceeds the dynamic range. The former approach (orange) treats the offset optimization and ACMC independently. While addressing the entire matrix with the offset optimization can already reduce the pedestal spread significantly, the application of ACMC hardly reduces the pedestal spread any further. The new approach (blue) optimizes the offsets per gate and takes advantage of the ACMC's capability to level out the differences between the gates. The resulting pedestal spread is reduced compared to the former approach.

7.4.2.8. ADC curves

The main purpose of the DCD ASIC is the conversion of the analog DEPFET drain current into a digital reading. Each DCD has 256 ADC channels which work in parallel. On the PXD module, 250 ADC channels are connected to the DEPFET matrix, 6 remain not connected. Four DCDs per module cover the entire 1 000 drain lines of the module matrix.

The basic principle of one ADC channel is explained in the following. More details about the implementation of the ASIC logic are given in [178, 180].

- In a first step, the input current from the drain line can be adjusted by three different sources. The global current source `VNAddIn` adds current, while the global current sink `VNSubIn` subtracts current. In addition to these ASIC wide settings, for each pixel an individual current can be added through the 2-bit `IPDAC` system for offset compensation (see above).

- The modified current reaches a resistive current receiver, which is based on a trans-impedance amplifier. Adjustable feedback resistors R_f (`EN30`, `En60`) and capacitors C_f (`EnCap`) influence the characteristics of the amplifier. The result is an output voltage which is converted back into a current at the resistor R_s. Also the value of R_s can be changed (`HiGain`). The ratio R_f/R_s defines the current gain of the receiver.

- Again, the output current can be increased by a global current source (`VNAddOut`) or decreased by a global current sink (`VNSubOut`) before it enters the actual ADC.

- The conversion uses a current-mode pipeline ADC based on current-memory cells. One ADC channel consists of eight double cell blocks. Each double cell block contains two current memory cells and two comparators, which process the current by going through four states. The current is compared to a reference value and a low and a high threshold. If the current is below the threshold, an additional current is added. If it is above the threshold, the current is subtracted. If it is between the thresholds, no operation is performed. Finally, the current from the two cells is merged, synonymous to a multiplication by two, and then forwarded to the next block. In total, the procedure is a cyclic analog-to-digital conversion with eight cycles. The result is a signed 8-bit digital code quantifying the input current. The least significant bit is dropped, so that the sign bit and the remaining 7-bit code can be transferred by the 8-bit parallel bus to the DHP. Therefore, the output values range between -127 and 127. For convenience they are translated to the usually used range of 1 to 255 ADU.

The following additional configuration and test circuits are implemented:

- A calibration circuit can apply test signals and measure voltages or currents. It can be connected either to the input of the amplifier or to the input of the ADC (`AmpOrADC`).

- A decoder generates the control signals (sync, read and write) for the control of the ADC. It receives the sequence signals from the digital block of the DCD and generates the required wave forms.

- The pixel configuration register contains three configuration bits per ADC channel for fast current injection (`EnInjLoc`), slow current injection (`EnDC`) and enabling the amplifier for the common mode loop (`EnCMC`).

Important criteria for the optimization procedure are the properties of the ADC transfer curves, which characterize the translation of input current into digital output value. An example of an ADC transfer curve is shown in fig. 7.30. Ideally the transfer curves are linear, but typical defects are: reduced range, gain error, offset, integral and differential non-linearities (INL, DNL), and missing codes. Detailed studies about ADC curve errors and influence of configuration settings are discussed in [51, 112, 180].

The linearity of an ADC response is best tested with a linear current source connected to the ASIC's input. A dedicated input pin (`CurMon`) at the DCD is foreseen for this purpose. The chip can be configured to fed the input current to each ADC (`EnDC`), but only one at a time. The DHE provides an own current source which can be used. Also an external source measure unit (SMU) can be used for higher precision measurements. This comes with the cost of a long measurement duration which is not feasible for mass testing.

The solution for mass testing was to use the already present DEPFET matrix on a module as input to optimize 1 000 ADCs at once. Drawbacks of this approach are the non-linearity of DEPFET IV curves and that the absolute input currents are not known. However, only this reduction in measurement time made it possible to add this optimization to the standard procedure. Still, the ADC curve optimization takes about 30 hours per module and is therefore the longest measurement in the mass testing procedure.

The most important settings for the ADC optimization are the configuration settings of the current-memory cells (`ipsource`, `ipsource2`, `ifbpbias` and `ipsource_middle`) and the bias voltages of the comparators (dcd-amplow and dcd-refin). First studies with prototypes found a suitable starting point and a scan range which was covered by the mass testing measurements (see table 7.2). However, deviations for individual

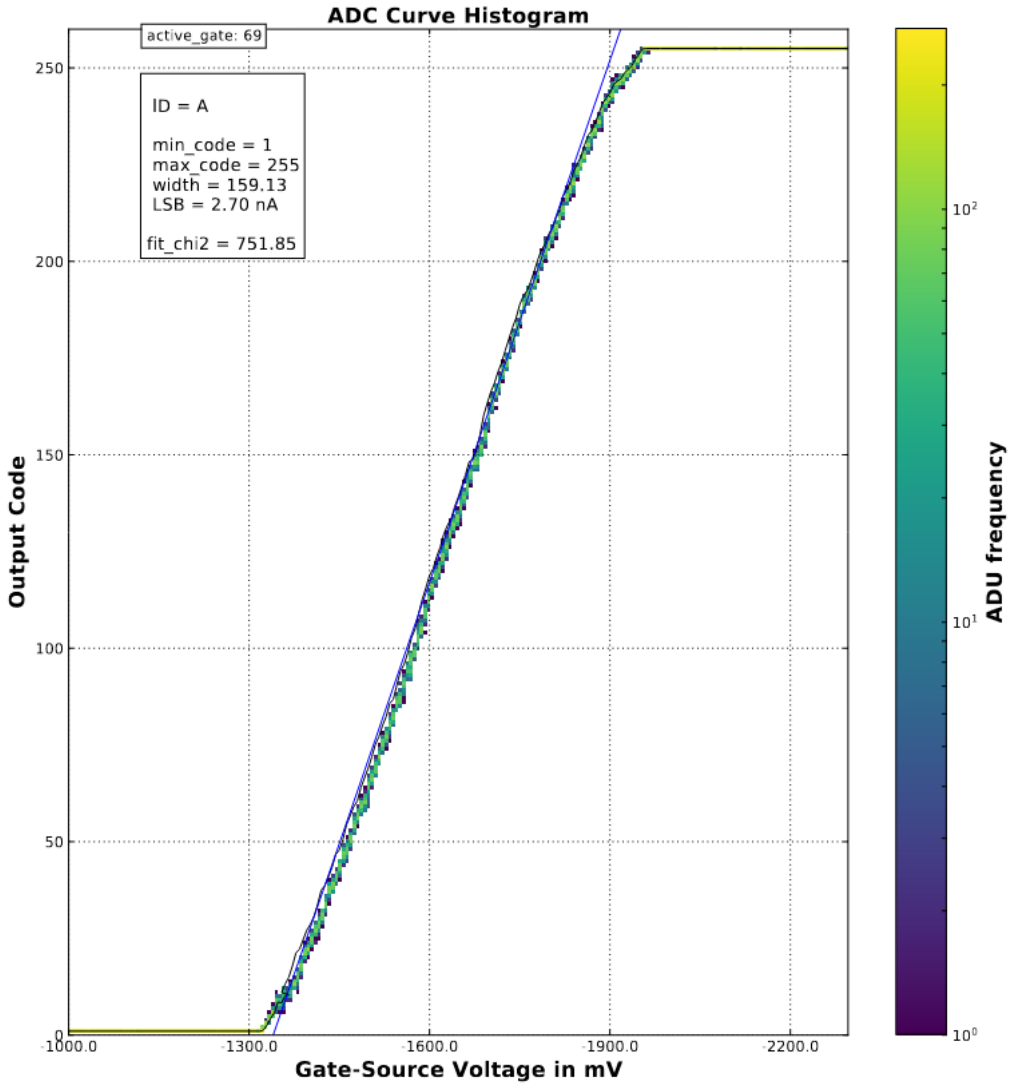


Figure 7.30.: ADC curve example from module W03_OF channel 28. For more negative gate-on voltages the drain current increases. This is correctly reproduced by the digital output codes. Each gate-on setting is sampled several times. The resulting transfer curve does not span the entire current range, but the linearity is close to the ideal straight line.

modules are always possible. The first two parameter scans were 2-d scans between the parameter pairs `ipsource` & `ipsource2` and dcd-amplow & dcd-refin. The two remaining settings were then scanned in a 1-d scan.

Table 7.2.: Typical ADC parameter ranges used during mass testing.

parameter	start	end	step size
ipsource	60	85	5
ipsource2	60	85	5
dcd-refin [mV]	650	800	25
dcd-amplow [mV]	200	400	25
ifbpbias	60	90	5
ipsource_middle	70	85	1

For each scanned parameter configuration ADC curves for all channels are recorded. The resulting transfer curves are graded according to the mentioned known defects. A common score for a parameter setting is found by multiplication of the scores for the individual criteria. For each parameter scan the best setting is automatically chosen and applied to the system, before the next parameter scan is started.

The results of 62 fully characterized PXD mass testing modules are shown in fig. 7.31. The most frequent setting for `ipsource` is 80. For `ipsource2` it is 70. The distributions of the bias voltages are less centered compared to the distributions of the DAC settings. The most frequent value for dcd-amplow is 300 mV. For dcd-refin the most frequent values are 700 mV, 725 mV and 750 mV. For `ifbpbias` and `ipsource_middle` the distributions peak between 75 and 80.

After the ADC curve calibration the 2-bit offset optimization is performed a second time to take the new DCD settings into account.

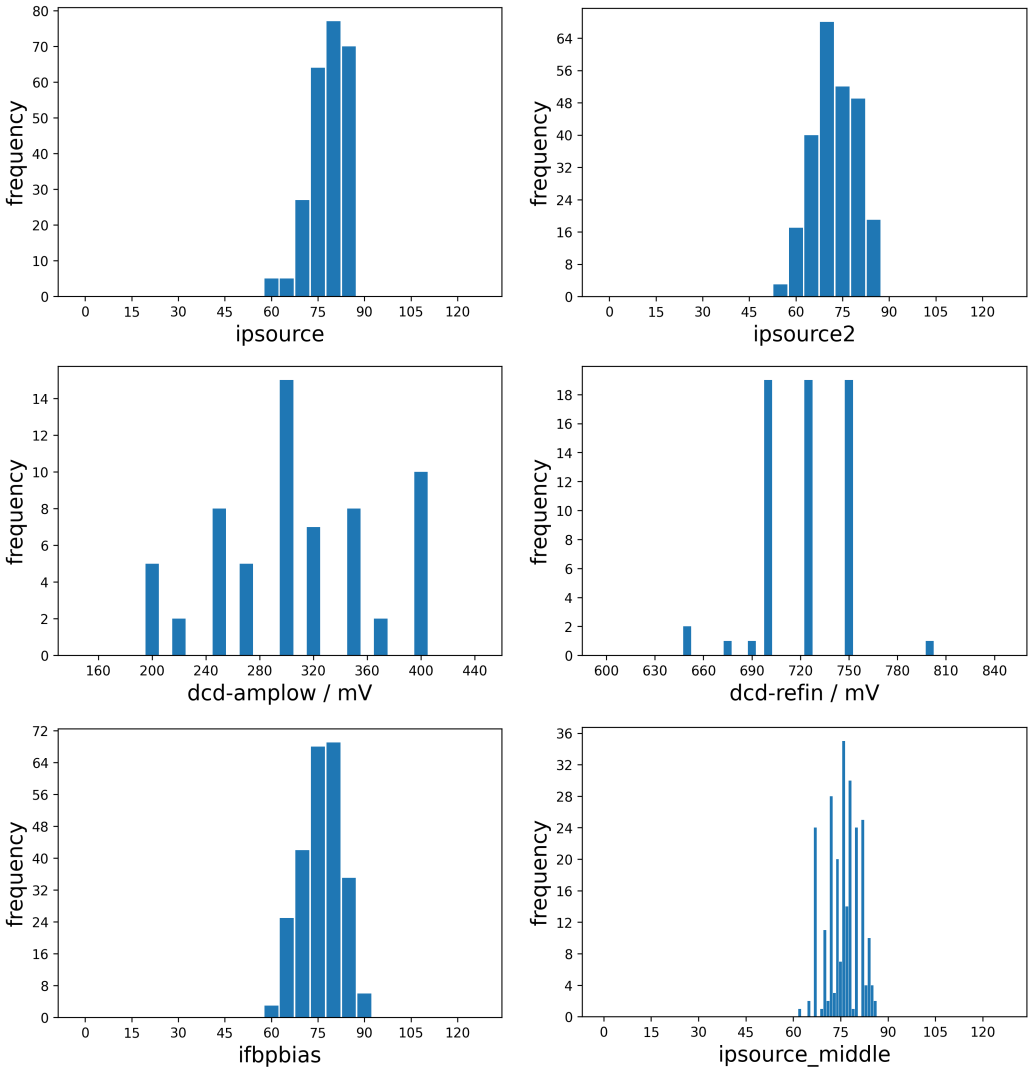


Figure 7.31.: ADC curves calibration results from mass testing. The results contain data from 62 fully characterized PXD modules. For range and step size of the parameter scans see table 7.2.

7.4.2.9. Source scan

All preceding measurements and optimizations aimed to prepare the system for efficient and error-free signal data acquisition. The final step in the mass testing protocol optimizes the matrix bias voltages and serves as definitive assessment of a PXD module's functionality. A radioactive source, Cadmium-109 or Strontium-90, is placed above the module's matrix and the hits of the ionizing particles are recorded. A custom made linear translation stage enables an illumination of the entire matrix (see section 5.2.5).

The source scan serves two purposes:

- DEPFET bias voltages are varied to optimize the matrix performance. Unfavorable values lead to a loss in detection efficiency. For absolute efficiency measurements a high energetic particle beam and a tracking system are required, neither of which are feasible in the laboratory. However, a relative measurement of the different bias conditions is sufficient to determine the optimal setting.

- The analysis of the measurement allows to determine the percentage of working pixels. Pixels, that do not report a hit, and pixels with noise above 5 ADU are subtracted from the total number of pixels. The percentage of working (also 'alive') pixels is then used as one of the criteria to grade a module after it has concluded the mass testing routine.

In order to achieve the optimization of the DEPFET bias voltages, the voltages hv, drift, and clear-off are varied. For each combination of the three parameters the entire matrix is illuminated with a radioactive source and the hit distribution is recorded. The ranges and step sizes typically used during the mass testing are listed in table 7.3. Within the mass testing routine, the analysis of the already recorded data was started while data taking with further configurations was still ongoing. Hence, it was possible to keep the duration for measurement and analysis combined at about 20 h to cover the entire 3-d parameter space.

Table 7.3.: Typical source scan ranges used during mass testing.

parameter	start	end	step size
hv [V]	-60	-74	-2
drift [V]	-4	-6	-1
clear-off [V]	2	5	1

For certain combinations of the bias voltages ring-like patterns occur in the recorded hit maps of the PXD DEPFET matrices (see fig. 7.32). Variations of the bulk doping

concentration within the initial wafer material are suspected to impact the charge collection efficiency at these settings. The aim of the source scan optimization procedure was to find bias conditions for the module's matrix that avoid this effect and provide highest hit detection efficiency.

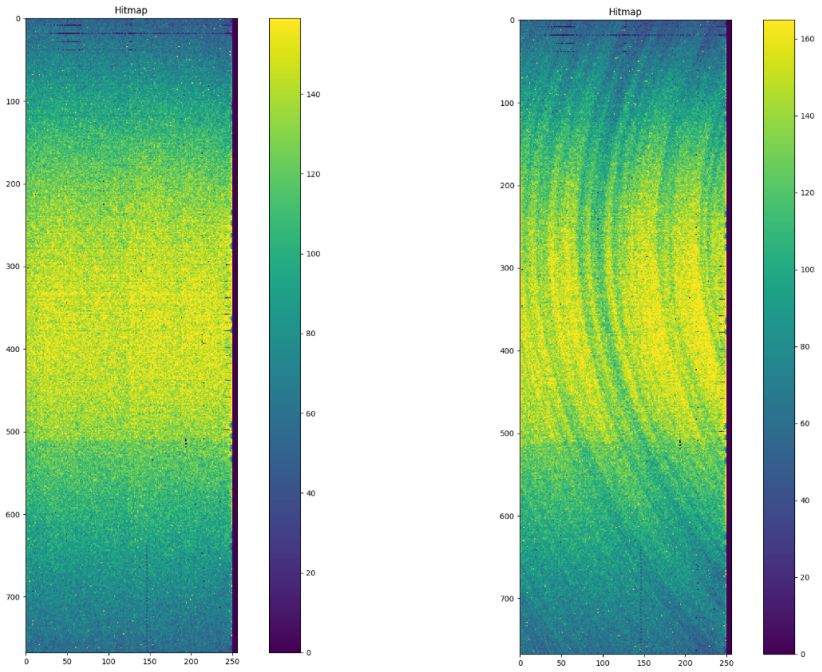


Figure 7.32.: Occurrence of rings in the hitmap of module W41_IF [181]. For optimal bias settings (left) a flat and homogeneous hitmap is achieved. For not ideal bias settings (right) ring-like patterns occur. Concerning the position of the module on the production wafer and also taking the geometry of ring-like patterns in the other modules from the same wafer into account, the patterns are concentric around the center of the wafer.

For the main part of the mass testing during the production in 2018 no automated algorithm was in place to select the best parameters as it is not trivial to define a quality figure based on the recorded hitmaps. During the mass testing it was the task of the operator to examine the hitmap plots for the different settings and chose the one with the least visible influence of the doping variations. The results are shown in fig. 7.33. The most frequent settings are: **2 V for clear-off**, **-6 V for drift** and **-70 V for hv**.

Later, two attempts were made to define a quality criteria: one by addressing the homogeneity of the hitmaps [182] and one automatically searching for ring patterns (ringness score) [181]. A more general approach and a detailed discussion about the associated optimization of the DEPFET biasing was then presented in [113]. The hv potential needs to be varied to find a plateau of maximal charge collection between

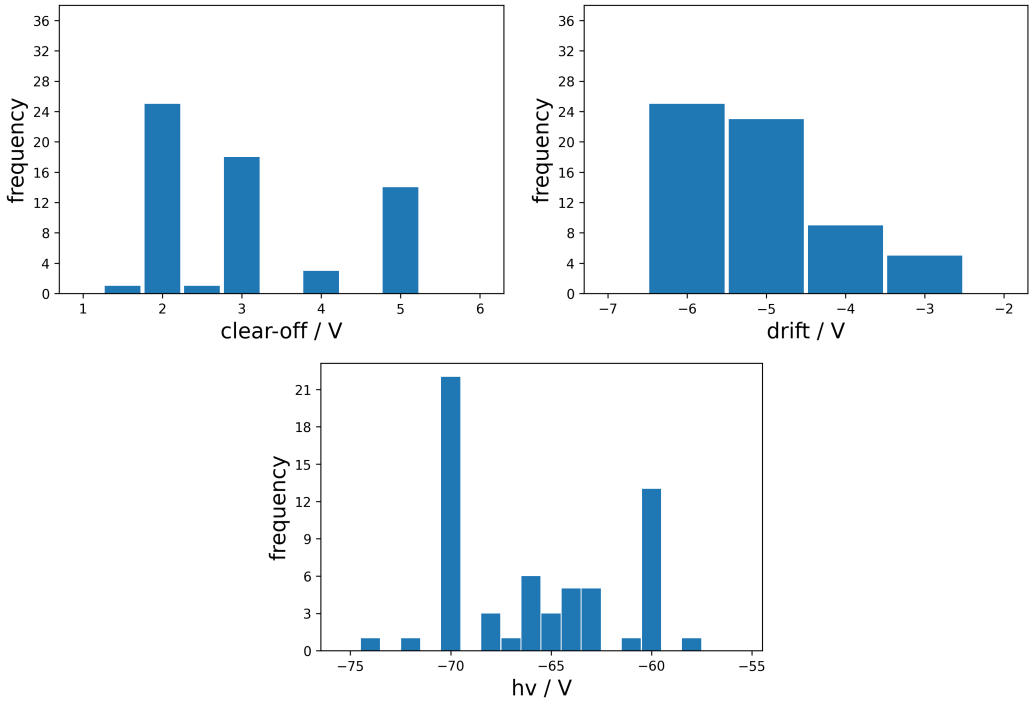


Figure 7.33.: Source scan calibration results from mass testing. The results contain data from 62 fully characterized PXD modules.

over- and under-depletion. The drift and clear shielding potentials (clear-off) influence the width of this plateau, while the variations of the bulk doping concentration shift the response of differently doped regions relative to each other. Consequently, the optimization searches for the maximal width of the plateau, which minimizes the influence of the doping variation. As result, the optimal settings were determined to be: **2 V for clear-off**, **-5 V for drift** and **-60 V for hv** [113]. This is in agreement with the values of clear-off and corresponds to the second most frequent values for drift and hv found during the mass testing.

The second result of the source scan measurement is the number of alive pixels per module. An overview of this number for 38 modules is shown in fig. 7.34. 21 modules achieved more than 99.7 % alive pixels, another 10 modules are still above 99.0 %, 4 modules are between 98.0 % and 99.0 % and one module reached 97.7 %. Two problematic modules are outside the plotted range with only 71 % and 75 %. For the remaining 24 out of a total of 62 characterized modules, the number was not documented during the test. The number of alive pixels was used as one of the criteria to classify the tested modules (see below in section 7.5.6).

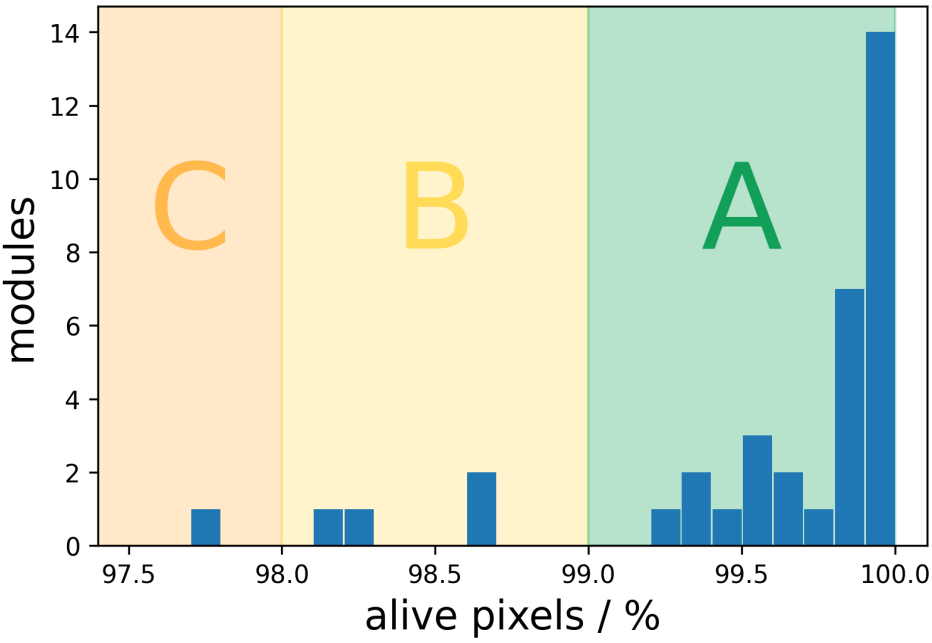


Figure 7.34.: Alive pixels per module determined by the source scan measurement. Regions with different background color indicate the ranges assigned to quality classes A (more than 99 %), B (between 98 % to 99 %), and C (between 95 % to 98 %). The results contain data from 38 fully characterized PXD modules.

7.4.2.10. Discussion of module calibration results

The conclusive step of the mass testing procedure is a presentation of the testing results to the PXD experts during the weekly collaboration meeting. The operator responsible for the calibration collects all results of the individual measurements and addresses especially the particularities of the studied PXD module. After a discussion of the the results, a common decision about the assigned grading class is taken. The decision is based on experience and in comparison to other modules. Also specific performance indicators are taken into account (see section 7.5.6). Problematic modules are sent to experts for further investigation.

The open discussion with colleagues and the presentation in the general meeting ensured an optimal information of the collaboration. However, an additional review of the results by an expert from another laboratory could have improved the completeness of the results, particularly the documentation.

After a PXD module completed the mass testing routine, it is safely stored again (see fig. 7.35) and waiting for the next production step. When a matching partner module is found, both are glued to form a PXD ladder.

Figure 7.35.: Module storage in nitrogen atmosphere. Every module stays protected in its own transport set. Modules, which are stored for a longer period, are covered in sealed plastic bags for additional protection against dust particles.

7.5. Main production module performance

This section gives an overview of the performance of PXD main production modules during the mass testing. It starts with the description of harmful powering incidents which damaged some gate lines of Switcher ASICs. A pre-irradiation effect from x-ray inspection is described which resulted in a shift of pedestal values for exposed pixels. The occurrence and distribution of disconnected drains as one of the main reasons for broken pixels is analyzed. The pedestal distributions and respective noise distributions of the tested modules are presented. The optimal parameters for a PXD module are given as determined by the mass testing procedure. Finally, the performance indicators used to classify the tested modules are described and the distribution of the graded modules over the different classes is presented.

7.5.1. Inefficient gates - Switcher damage during module testing

Several modules suffered from a "power down issue" during mass testing. In rare cases a not optimal configuration of the automatic power down procedure resulted in a bias condition at the Switcher ASIC which damaged part of the Switcher[12]. The exact mechanism is not known. The effect was not reproducible as most of the power down processes under the same conditions worked without issue.

Best documented are the incidents which affected modules W02_IF and W03_IF on December 8, 2017. An example plot of voltages and currents during the harmful power down process as recorded by the EPICS Archiver is shown in fig. 7.36. A normal power down process is shown in section 7.3.4 for comparison.

The result were damaged gate lines with significantly reduced hit detection efficiency. Permanently increased switcher currents were visible at the next power up of the affected module. The current in the sw-sub line rose from usually $-9\,\mathrm{mA}$ up to $-26\,\mathrm{mA}$ and the current in the clear lines Δclear (clear-on - clear-off) rose from usually $45\,\mathrm{mA}$ up to $110\,\mathrm{mA}$. The inefficient (or "dead") gates were detected in a subsequent source scan (see fig. 7.37). In addition, a shift of the pedestal values of pixels in the affected gate by about $-100\,\mathrm{ADU}$ was observed on another module (see section 9.4.5).

Taking all observations into account, a possible explanation for the observed symptoms could be a permanently increased clear potential, which prevents a charge collection in the internal gate. Pedestal taking is still possible, which shows that the switch

[12] The OVP board of the Power Supply could probably have prevented the damage, but was not yet ready for installation.

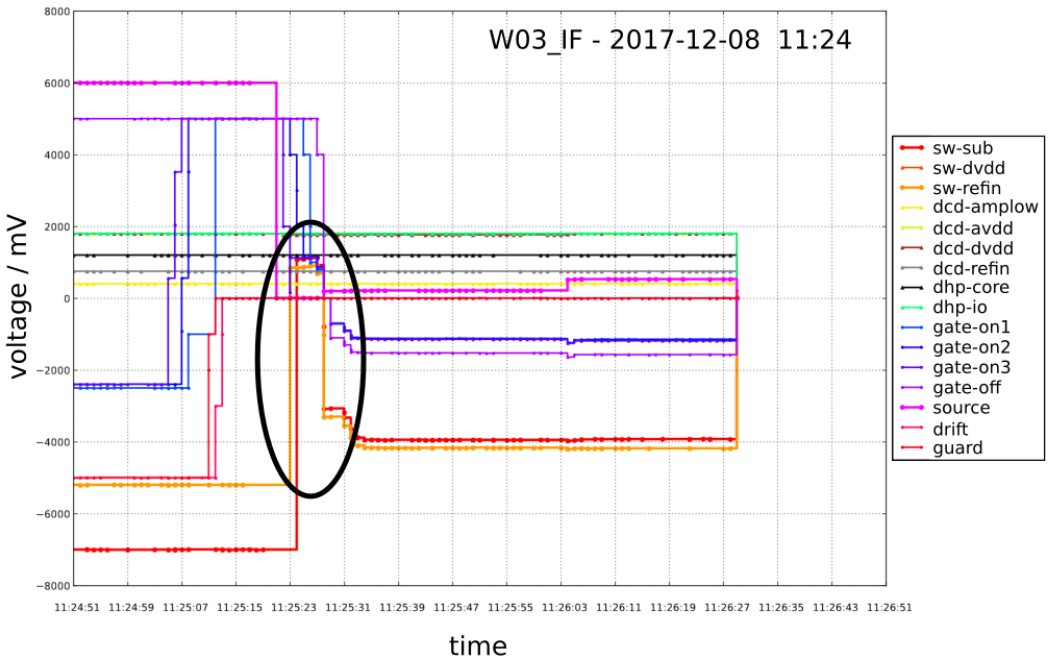


Figure 7.36.: Monitored voltages during switcher power down incident of module W03_IF. When the source voltage was ramped down during the power down process, several lines went into the current limit. The corresponding voltages were pulled away from the nominal values. A sudden increase of the Switcher voltages sw-sub and sw-refin to positive values is visible (highlighted by the black ellipse). This condition lasted for about 5 s to 6 s.

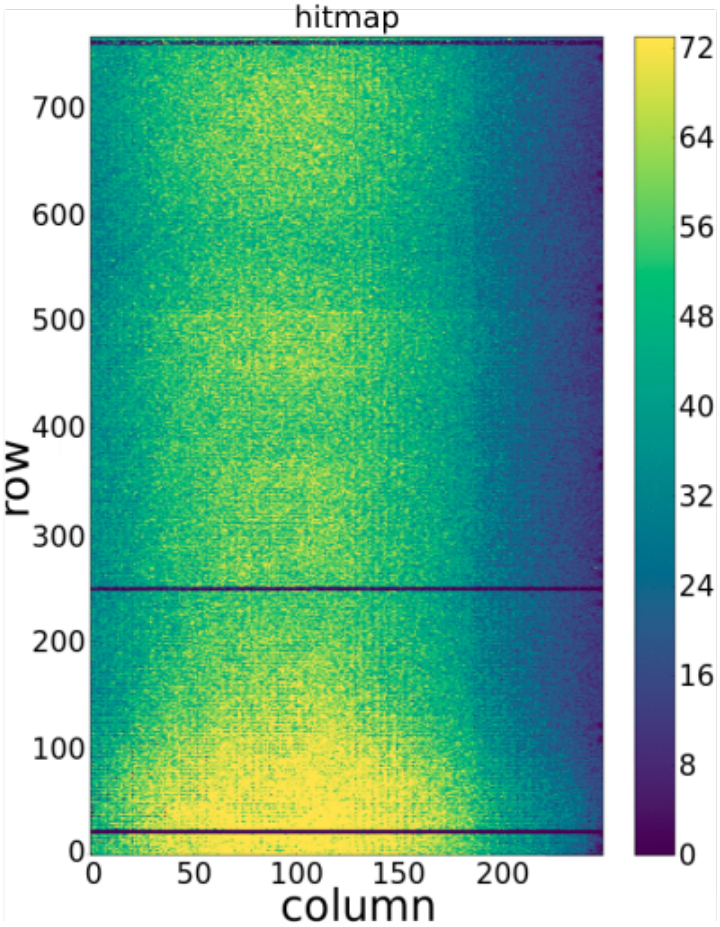


Figure 7.37.: Damaged switcher gates in W03_IF. The hitmap shows the accumulated number how often each pixel reported a hit during the source scan. Due to the geometry of the radioactive source and the stage a gradient in the hitnumbers is visible across the matrix. Three inefficient gates with almost no hits appear as dark, horizontal lines.

between gate-on and gate-off inside the Switcher is still working. A damaged switch between clear-on and clear-off, however, could explain the increased current in these lines, flowing from the higher voltage (clear-on) to the lower (clear-off). If the resulting potential at the output pin of the Switcher and therefore at the clear contacts of the pixels is pulled up closer to clear-on, generated electrons are no longer collected in the internal gate but instantly pulled away to clear. Thermally induced electrons, which normally accumulate during the integration time of 20 µs, contribute to the pedestal values. Their absence could explain the reduced pedestal values of the affected gates. Likewise, generated electrons by ionizing particles can not be collected in the internal gate and no hits are detected.

The described issue led to several modules starting Phase 3 with already initial inefficient gates, in total 13 ineffeicient gates for the entire PXD (see section 9.4.7). Still, the PXD modules installed at Belle II collected much more inefficient gates during Phase 3 due to severe beam loss incidents as discussed in section 9.4.

An overview of affected modules is given in table 7.4. Four of the five affected modules were still integrated into the PXD. The inefficient gates reduce the number of working pixels and the current limit of the affected lines has to be adjusted. However, the operation of the module is otherwise not affected. W03_IF, for example, was already glued to a ladder, when it suffered from the power down issue. W05_OB1 was damaged during an irradiation campaign [113] and suffered 5 inefficient gates. It was not foreseen for installation in the PXD.

Table 7.4.: Inefficient gates of PXD modules before start of Phase 3.

module name	W03_IF	W43_IB	W47_IF	W02_IF	W05_OB1
module number in PXD	1.01.1	1.01.2	1.07.1	1.08.1	-
number dead gates					
in source scan	3	-	4	2	5
at start of Phase 3	3	4	4	2	-

After the power down incidents with the described damages in modules W02_IF and W03_IF the power down sequence was reviewed and the fast ramping of voltages, especially the source voltage, was identified as critical step. The delay between the control signals to change the applied voltages was increased as measure against further power down incidents. This resulted in a slightly increased transition time between the PXD powering states, i.e. longer power up and power down time of the detector ($\mathcal{O}(1\,\mathrm{s})$), but gained a higher operation stability and module safety. No further powering induced incidents were observed afterwards.

7.5.2. Pre-irradiation effect

Some modules showed a significant shift in the pedestal values of the DEPFET pixels at the matrix borders close to the ASICs. This effect is visible in the initial pedestal map of a module without any pedestal optimization applied (see fig. 7.38 left). The reason is a threshold shift of the DEPFET pixels due to irradiation.

After bump bonding of the ASICs to the modules (see section 7.2.2), the quality of the bonding was verified by x-ray inspection. Several aspects could be checked, like the orientation of the ASICs towards the module, completeness of all bump balls, and shorts between the bump balls. Individual modules, which had to be reworked, had additional x-ray inspections. In order to minimize the dose applied to the radiation sensitive DEPFET pixels, shields were used to cover the matrix. However, a flush cover of the matrix could not be achieved and the borders of the matrix close to the ASICs collected more dose than the rest of the matrix.

The optimization procedure and especially the 2-bit offset compression is capable to bring the irradiated pixels back into the dynamic range (see fig. 7.38 right). However, most of the offset compensation is spent on this effect and the resulting pedestal distribution of the affected DCD is still quite broad.

The differences between exposed and covered regions diminish with increasing integrated dose received during the operation at the accelerator. Nevertheless, after this effect was detected and explained, no shields were used for further x-ray inspections. This adds initial dose to the entire matrix, but results in a more homogeneous response of the matrix and, therefore, improves the optimization results. Optimized values are valid for a longer period of time and recalibration is required later.

7.5.3. Disconnected drain lines

Disconnected drain lines are partially or entirely not working drain lines in a DEPFET matrix. The corresponding pixels have very low pedestal values (close to the minimum of 1 ADU) as almost no current receives the DCD input. Broken pixels are explained by an open or other defect in the drain line. The number of affected pixels per disconnected drain line depends on the location of the defect, as the pixels closer to the DCD are still working. An example for a partially disconnected drain line can be seen in the region of DCD4 in the pedestal map of W46_OF1 (see again fig. 7.38). Disconnected drain lines are one of the main reasons for non-functional pixels in DEPFET matrices of PXD modules.

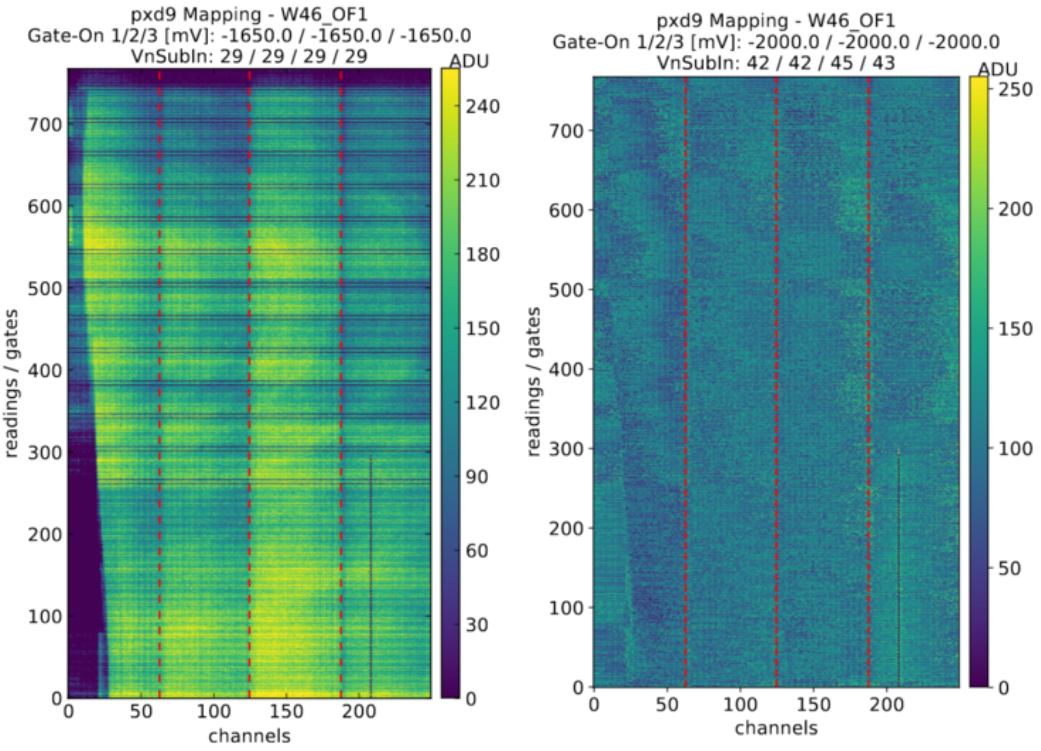


Figure 7.38.: Pre-irradiation effect in pedestal values of module W46_OF1. The left pedestal map shows the initial state of the module without any optimization of the pedestals distribution. The borders of the DEPFET matrix close to the ASICs, which received a higher dose during the x-ray inspection, show lower pedestal values. The right pedestal map shows the optimized state after module characterization.

Pedestal data of the optimized modules were used for the analysis of disconnected drain lines. In each drain line a row of pixels with ADU values below 1.75 ADU was searched, starting from the far end of the matrix. If five or more pixels in a row were below the threshold, the drain line was labeled as disconnected drain line.

Out of 62 tested modules, 33 were without any disconnected drain line. Most affected modules showed 1 to 3 disconnected drain lines (19 modules). In the remaining 10 modules more than 3 disconnected drain lines were found with a maximum at 28 disconnected drain lines in W09_OF2. A detailed overview with the results of all tested modules is shown in appendix D.

The outer modules dominate the comparison of module types in absolute and relative numbers of disconnected drain lines with most disconnected drain lines found in outer backward modules (see fig. 7.39). The comparison of the production wafers is dominated by the wafers with numbers 12, 09, 13 and 11, in decreasing order (see fig. 7.40). However, the number of tested modules varies strongly between the different wafers, e.g. all six modules from wafer 09 were tested, whereas only one module of wafer 10 completed the mass testing procedure.

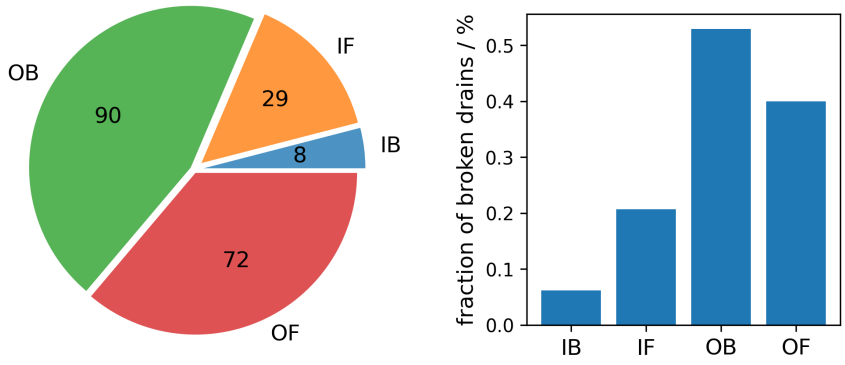


Figure 7.39.: Distribution of disconnected drain lines over the four different module types. Left: The pie chart shows the absolute numbers of disconnected drain lines. Right: The bar chart shows the numbers of disconnected drain lines relative to the total number of tested drain lines per module type.

Hot drain lines are conceptual identical to disconnected drain lines but originate from a short in the drain line and therefore show very high values close to the maximum of 255 ADU. Hot drain lines appeared about an order of magnitude less often compared to disconnected drain lines. Only 10 modules with one or more hot drain lines were found. There was no hot drain line without also at least one disconnected drain line on the same matrix (see again appendix D).

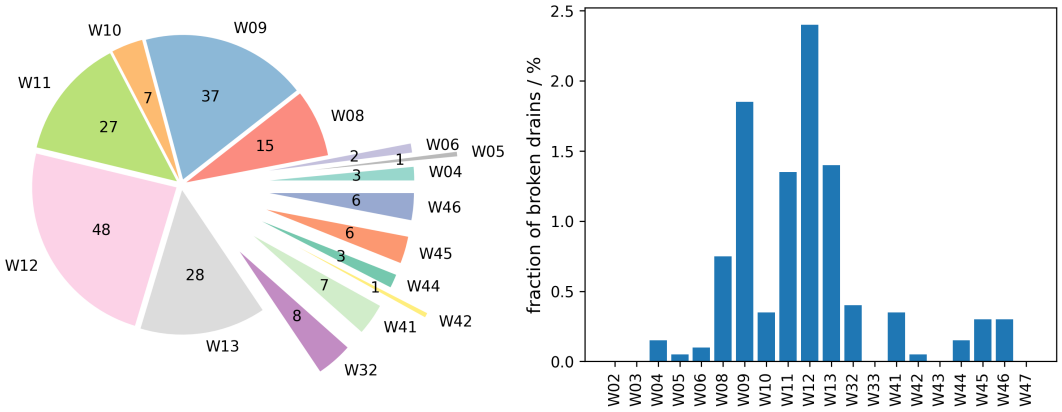


Figure 7.40.: Distribution of disconnected drain lines over production wafers. Left: The pie chart shows the absolute numbers of disconnected drain lines per wafer. Right: The bar chart shows the numbers of disconnected drain lines relative to the total number of tested drain lines per wafer.

7.5.4. Final pedestal distributions

A narrow pedestal distribution is one of the goals of the module optimization. The maximum of pixels should be in the lower dynamic range, which leaves enough contingency for additional signal, so that a hit can be detected reliably. The noise in the pedestal values is also an important figure which contributes to the signal-to-noise ratio of the detector. This section describes the methods used to determine these figures and gives an overview of the pedestal and noise distributions of the optimized modules.

7.5.4.1. Pedestal spread

A single figure describing the pedestal spread is required to guarantee an easy comparability between modules and between different configurations of the same module. It should quantitatively describe the pedestal spread and should be easy to comprehend. Several frequently used figures were tested for this analysis (shown in fig. 7.41). However, a custom criteria is better suited to describe the PXD specific pedestal distributions.

- Simply taking **minimum and maximum value** of the pedestal distribution is not expedient as individual outliers (e.g. dead and hot pixels) can inflate an otherwise narrow distribution.

- A **Gauss fit** is not suited, because optimized pedestals usually form a sub-Gaussian distribution, while worse pedestal distributions with large tails get underestimated by the fit.

- Also the **standard deviation (STD)** reacts late to tails or fractions of the pixels outside the main distribution.

- The **root-mean-square (RMS)** is also not suited as it depends on the location of the distribution within the dynamic range.

- The typical definition of a box plot contains a box with length of the **interquartile range (IQR)** and whiskers at 1.5 times the IQR. This has the advantage that the length between lower and upper ends of the whiskers contains the additional information about the spread of the inner 50 % of the pixels. However, individual outliers can again influence the measured range drastically. A good distribution with a sharp edge can still get a large whisker, if a single outlier lies above the edge but within 1.5 times the IQR. In addition, a larger accumulation of pixels outside the main distribution (e.g. due to some larger defect in the matrix or bad configuration of a region) can get ignored as outliers (both issues visible in fig. 7.41).

⇒ A **custom cut at the lower and upper 0.5** % of the distribution can prevent these issues. By ignoring the most extreme percentage of the distribution, it is immune to individual outliers, but will still respond to larger defects or regions of suboptimal configuration. While the definition of the limits is arbitrary, the **1 %-criterion** is in accordance to the criterion used for class A modules in the source scan (maximum of 1 % non-functional pixels).

The application of the **1 %-criterion** yields a typical pedestal spread of about 150 ADU for the optimized PXD modules (see fig. 7.42 left). While this new definition of the pedestal spread was not used during the module classification, the shape of the pedestal distribution played a role on basis of expert judgement. This is represented by the on average higher values for modules of Class B and Class C. However, a clear cut on the pedestal spread value to classify the modules would not be feasible. The typical mean value of the pedestal distributions is 100 ADU (see fig. 7.42 right). This value can be adjusted easily, e.g. by changing the value for `VNSubIn` or `VNSubOut`. A differentiation between module classes on basis of the pedestal mean is therefore not possible.

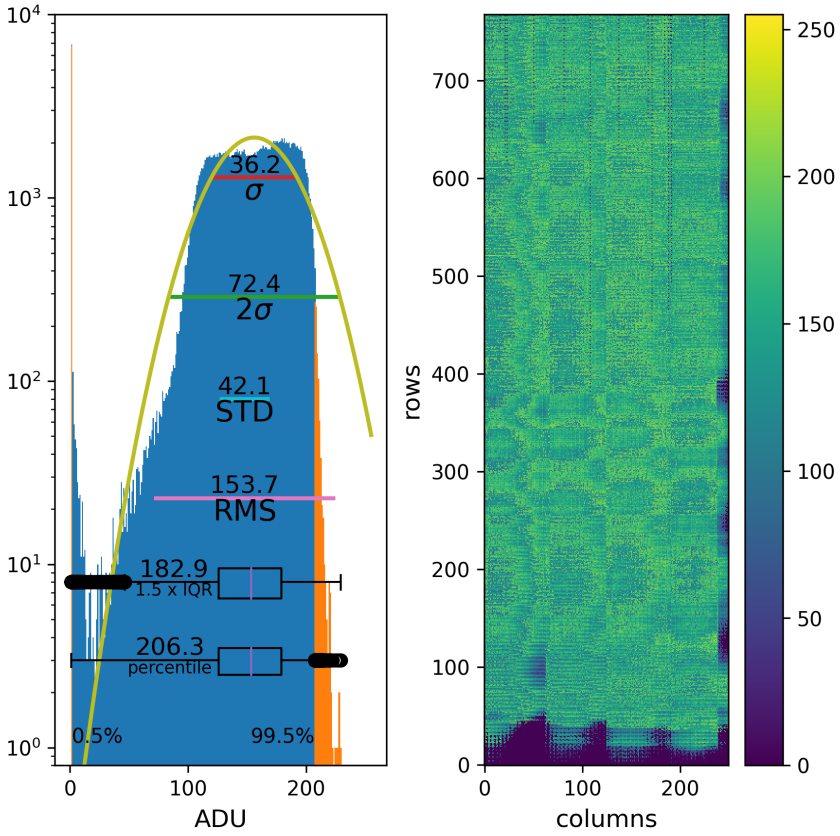


Figure 7.41.: Different figures for the definition of pedestal spread. Histogram of pedestal values (left) and geometric matrix representation (right) of module W08_OB2. The optimized Gauss does not describe the distribution accurately, σ and 2σ are not meaningful. STD and RMS underestimate pixels outside the main distribution. This is also the case for the typical definition of the box plot using the IQR, although less pronounced. The custom definition (also plotted as box plot) uses the 0.5 and 99.5 percentiles to only ignore 1 % of the pixels (highlighted in orange).

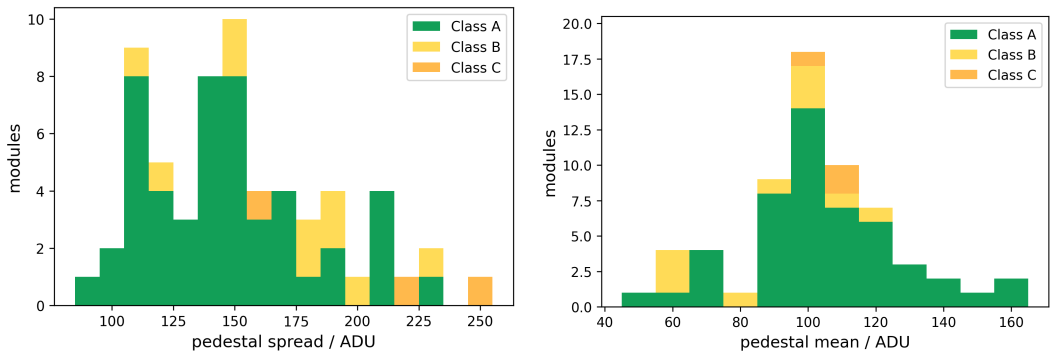


Figure 7.42.: Pedestal spread and pedestal mean distribution of optimized PXD modules.

7.5.4.2. Pedestal noise

Another important figure concerning the PXD pedestal data is the noise. The pedestal noise per module is determined by first calculating the noise values per pixel. The noise per pixel is defined as the standard deviation on the pedestal value of that pixel over all recorded data frames of a pedestal scan (usually 100 to 1 000 frames). A Gauss fit on the histogram of the noise values per pixel is used to determine the mean of the distribution (see fig. 7.43 left). For optimized modules the Gauss fit delivers best results compared to a Landau or Langau fit (see also section 6.6.5), however, a tendency to a fat tail towards higher values remains underestimated. The noise value per module is defined as the mean of the fitted Gauss function.

The distribution of noise values per module for all tested main production modules peaks at 0.75 ADU to 0.8 ADU (see fig. 7.43 right). This is in agreement with other studies ([96]) and values measured at KEK after installation of the PXD (see section 6.6.5). More than 90 % of the tested modules have a noise value below 1.0 ADU.

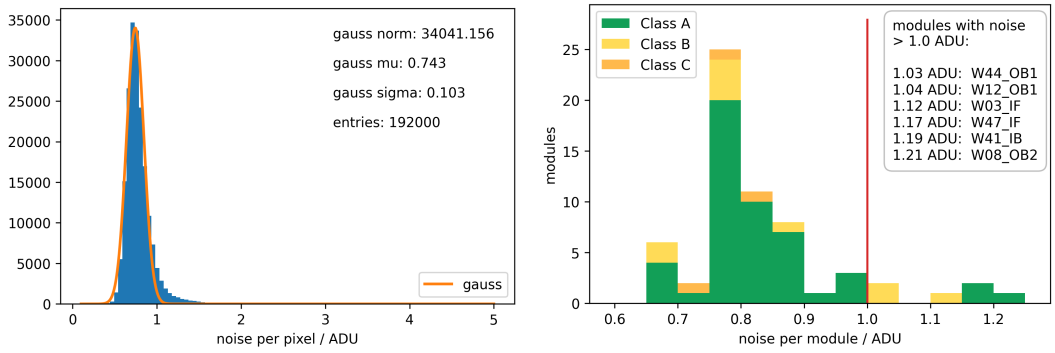


Figure 7.43.: Pedestal noise of optimized PXD modules. Left: Histogram of noise values per pixel containing all 192 000 pixels of the DEPFET matrix of module W08_OB1. The fitted values of the Gauss function are listed in the plot. Right: Histogram of noise values per module for all 62 fully characterized PXD modules.

The noise values per module depend on the individual configuration (e.g. gain setting) but also on the installation setup and other external influences. Module W41_IB, for example, had a noise value of 1.19 ADU in the last mass testing pedestal scan. However, its noise value dropped to 0.87 ADU after installation at KEK at the start of Phase 3 (see again section 6.6.5). Instead of the noise value per module, the distribution of noise values per pixel is more significant, as it allows to verify, if parts of the matrix show unusual high noise. This can be seen by additional peaks or large high noise tails in the histogram.

7.5.5. Optimized configuration parameters

The aim of the module characterization was the optimization of the main production PXD modules and their grading on basis of the measurement results. The optimized configuration parameters are listed in table 7.5 as determined by the standardized testing procedure including results from 62 fully characterized PXD modules.

Table 7.5.: Optimized configuration parameters.

parameter	PV name	value		unit
high speed links			from [153]	
bias	`idac_cml_tx_bias`	125^{+100}_{-5}	(100*)	
biasd	`idac_cml_tx_biasd`	125^{+45}_{-5}	(235*)	
delay	`pll_cml_dly_sel`	0		
delays of data transfer lines				
global delay	`dcd_clk_sdly`	0		
local delay	`dcd_rx_sdly`	5 ± 1		
2-bit offset calibration				
current source I_{DAC}	`dacipdac`	24 ± 6		
VNSubIn	`dacvnsubin`	42^{+3}_{-7}		
ADC curves				
ipsource	`dacipsource`	80 ± 5		
ipsource2	`dacipsource2`	70^{+10}_{-5}		
dcd-amplow	`dcd-amplow:VOLT:set`	300^{+75}_{-50}		mV
dcd-refin	`dcd-refin:VOLT:set`	725 ± 25		mV
ifbpbias	`dacifbpbias`	75^{+10}_{-5}		
ipsource_middle	`dacipsource_middle`	76^{+6}_{-5}		
matrix bias			from [113]	
clear-off	`clear-off:VOLT:set`	3^{+2}_{-1}	(2*)	V
drift	`drift:VOLT:set`	-5 ± 1	(-5*)	V
hv	`hv:VOLT:set`	-66^{+6}_{-4}	(-60*)	V

Instead of mean and standard deviation of the individual parameter, the median value with upper and lower limits are given. The limits are chosen so that 68 % of all values

lie within the given range, following the value for the standard deviation. However, this way the results are not averaged values but discrete values, which are actually applied at the optimized modules. Values with a star (*) were found in later studies using a different method to determine the optimal parameter value. The reference is given above these values. However, the results from the main production characterization contain by far the largest data set with data from 62 fully characterized PXD modules.

Similarly, table 7.6 lists the median values of all bias voltages and corresponding currents of the 62 PXD modules as applied in PEAK state after the optimization procedure. Again, the range covers the inner 68 % of the distribution. Voltages, which were not adjusted but stayed at the design values, have a range of $\pm\,0\,\mathrm{mV}$.

These two tables are the condensed result of the main production module characterization. The values are, therefore, reference values for an optimized PXD module operation of unirradiated modules. With increasing total ionizing dose, which the modules accumulate during operation at the SuperKEKB accelerator, adjustments of voltages and configuration parameters are required. The described optimization measurements are therefore still needed for continued optimization and adjustment of the installed modules.

7.5.6. Performance indicators

Finally, each of the tested PXD module was assigned a quality class based on its performance during the characterization procedure. The criteria for the assignment were mainly the number of working pixels as determined by the source scan and the shape of the optimized pedestal distribution (pedestal spread and homogeneity). However, the latter one is a weak criterion and influenced by e.g. a pre-irradiation shift and individual hot or dead pixels as outliers. Also the individual results from all characterization measurements and especially each anomaly was taken into account. Therefore, expert experience still remained necessary in judging the module performance and dedicated expert meetings were held to commonly grade a module.

A scheme of five classes was used to group the tested modules. Modules from the first three classes were potential candidates for the assembly of the PXD. The last two classes collected modules with severe issues and modules which could not be operated. The classes and their criteria are:

- **Class A**: These modules are the first choice for the installation into the detector. They showed a very good/good performance with more than 99 % working pixels in the source scan. They achieve an error free data transmission to the

Table 7.6.: Operation voltages and currents of main production modules after optimization. Given are the median value and a range which covers the inner 68 % of the distribution.

power supply line	voltage	current
sw-sub	$-7000 \pm 0\,\mathrm{mV}$	$-9 \pm 0\,\mathrm{mA}$
sw-dvdd	$1800 \pm 0\,\mathrm{mV}$	$-21 \pm 1\,\mathrm{mA}$
sw-refin	$-5200 \pm 0\,\mathrm{mV}$	$0 \pm 0\,\mathrm{mA}$
dcd-amplow	$300^{+75}_{-50}\,\mathrm{mV}$	$-716^{+20}_{-28}\,\mathrm{mA}$
dcd-avdd	$1800 \pm 0\,\mathrm{mV}$	$2792^{+52}_{-100}\,\mathrm{mA}$
dcd-dvdd	$1800 \pm 0\,\mathrm{mV}$	$842^{+12}_{-8}\,\mathrm{mA}$
dcd-refin	$725 \pm 25\,\mathrm{mV}$	$226^{+44}_{-46}\,\mathrm{mA}$
dhp-core	$1200 \pm 0\,\mathrm{mV}$	$670^{+20}_{-14}\,\mathrm{mA}$
dhp-io	$1800 \pm 0\,\mathrm{mV}$	$294^{+13}_{-9}\,\mathrm{mA}$
bulk	$10\,000 \pm 0\,\mathrm{mV}$	$0 \pm 0\,\mathrm{mA}$
clear-on	$19\,000 \pm 0\,\mathrm{mV}$	$27^{+1}_{-2}\,\mathrm{mA}$
clear-off	$3000^{+2000}_{-1000}\,\mathrm{mV}$	$-21 \pm 1\,\mathrm{mA}$
gate-on1	$-2325^{+325}_{-175}\,\mathrm{mV}$	$-6^{+0}_{-1}\,\mathrm{mA}$
gate-on2	$-2300^{+300}_{-200}\,\mathrm{mV}$	$-6^{+0}_{-1}\,\mathrm{mA}$
gate-on3	$-2300^{+300}_{-200}\,\mathrm{mV}$	$-6^{+0}_{-1}\,\mathrm{mA}$
gate-off	$5000 \pm 0\,\mathrm{mV}$	$26 \pm 1\,\mathrm{mA}$
ccg1	$0 \pm 0\,\mathrm{mV}$	$0 \pm 0\,\mathrm{mA}$
ccg2	$0 \pm 0\,\mathrm{mV}$	$0 \pm 0\,\mathrm{mA}$
ccg3	$0 \pm 0\,\mathrm{mV}$	$0 \pm 0\,\mathrm{mA}$
source	$6000 \pm 0\,\mathrm{mV}$	$98^{+4}_{-20}\,\mathrm{mA}$
drift	$-5000^{+1000}_{-1000}\,\mathrm{mV}$	$0 \pm 0\,\mathrm{mA}$
guard	$-5000 \pm 0\,\mathrm{mV}$	$0 \pm 0\,\mathrm{mA}$
hv	$-66\,000^{+6000}_{-4000}\,\mathrm{mV}$	$-67^{+55}_{-312}\,\mu\mathrm{A}$

DHE and between the ASICs (see high speed links and delay scan). Their pedestal distribution after optimization is narrow and lies completely within the dynamic range (except potential individual outliers).

- **Class B**: The modules of class B are the second choice for the installation into the detector. They showed an overall satisfactory performance with more than 98 % working pixels in the source scan and an error free data transmission to the DHE. The modules might have small errors in the data transmission between the ASICs and/or a broad pedestal distribution after optimization with few pedestals outside of the dynamic range. In total less than 2 % of the pixels are affected by these issues.

- **Class C**: These modules are the third choice for the installation into the detector. They showed an overall sufficient performance with more than 95 % working pixels in the source scan. Further criteria for class C are considerable errors in the data transmission between the ASICs and/or a broad pedestal distribution after optimization with considerable fraction of the pedestals outside of the dynamic range.

- **Class D**: Modules of class D are not foreseen for the installation into the detector. They showed a deficient performance and achieved less than 95 % working pixels in the source scan. Further criteria for class D are:
  - critical errors in the data transmission between the ASICs,
  - broad pedestal distribution after optimization with large fraction of the pedestals outside of the dynamic range,
  - one or more highspeed links for data transmission to DHE not working,
  - currents out of limits which prevent or heavily influence the data taking,
  - shorts on the module or in the matrix which prevent or heavily influence the data taking.

  If one or more of these criteria is met, the module is assigned class D. These modules can not be installed in the experiment, but they might be still usable as electrical dummy for setup qualification.

- **destroyed**: The last class collects all modules which can not be operated. The reasons might be manifold, ranging from electrical to mechanical issues. This concerns all modules, which were damaged during operation, also physically broken modules with cracks in the silicon. These modules can not be repaired and are therefore marked as destroyed. They might be still usable as mechanical dummies.

The distribution of assigned classes of all produced modules from batches P3-1 up to P3-7 and batch Phase 2 is shown in fig. 7.44. This includes 75 modules, of which

a majority of 72 % achieved class A. Eleven modules were graded as class B, five as class C. Leaving only five modules, which were not suitable for installation: two were graded as class D and three were marked as destroyed. A further separation within class A would have been possible (e.g. additional threshold in the number of working pixels), but was not required, as almost all of these modules were needed to build the PXD.

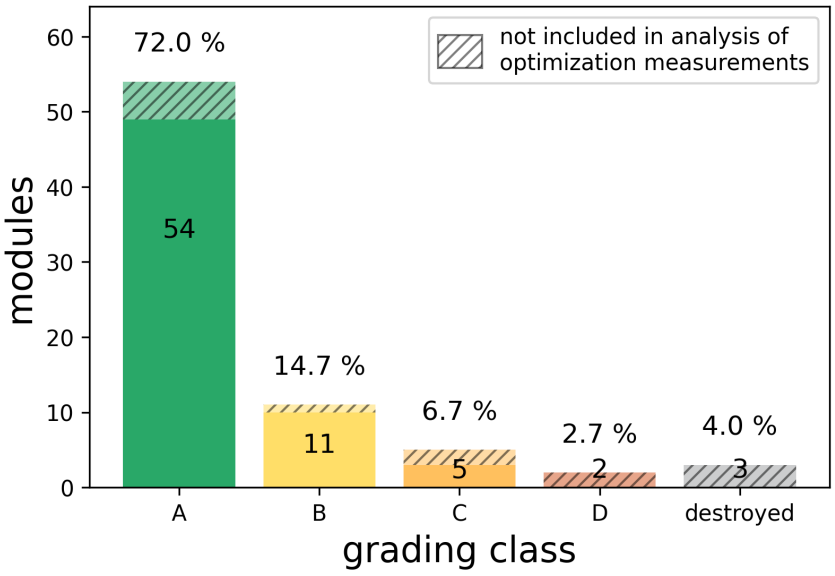


Figure 7.44.: Distribution of assigned classes of all modules tested according to the mass testing routine. Shown are assigned classes of 75 modules, including all 71 modules from batches P3-1 up to P3-7 plus additional 4 modules from batch Phase 2, which were used as BEAST modules and went through the mass testing procedure after Phase 2. In addition to the 62 fully characterized modules, which were used for the analysis of the individual optimization measurements, 13 further modules are added to this graph (striped). These are the four Phase 2 modules (three class A, one class C), modules which failed early stages of the testing or were destroyed, and modules lacking documentation or availability of required data for the analysis.

The amount of 54 class A modules was distributed over the different module subtypes (IB: 12, IF: 10, OB: 15, OF: 17) and therefore sufficient to equip an entire PXD (IB: 8, IF: 8, OB: 12, OF: 12) completely with class A modules. However, the mechanical process of gluing two modules together to form a rigid ladder posed an exceptional challenge, which required a redesign of the process after several modules were damaged. This was also the reason, why not the entire PXD could be equipped in time before the start of Phase 3.

8. Ladder Gluing and PXD Assembly

To cover the full length of the acceptance region, the sensitive area of the PXD must be 9 cm for the inner layer and 12 cm for the outer layer. Together with the EOS, this gives a length of 13.6 cm for the inner and 17 cm for the outer ladders. The size of the production wafers therefore requires the ladders to be split into two modules each[1], resulting in four different module types (IB, IF, OB, OF) that have to be glued to ladders prior to assembly.

Once glued, the ladders are mounted on the SCBs to form two half-shells. These will later enclose the beam pipe at the IP of SuperKEKB. The first commissioning step took place at DESY. Both half-shells were installed on a dummy beam pipe and all modules and services were tested before being shipped to Japan.

8.1. Gluing procedure

The gluing process starts with the selection of matching modules. Besides the prescribed module types (IB with IF and OB with OF), the main selection criterion was the class assigned from the characterization, but individual module performance was also taken into account. However, not all modules were tested prior to the start of the ladder gluing, so only a limited number of tested modules were available for each selection.

8.1.1. Process description

The entire procedure was extensively tested using mechanical dummy modules to verify the work flow and the strength of the glue joint. A strict protocol was established and a detailed checklist was followed during each gluing process. The radiation hard two-component adhesive (Araldite 2011) is applied using a Musashi dispensing robot,

[1] Outer ladders are too large for 150 mm diameter of "6 inch wafers" and only one inner ladder per wafer is not cost effective.

which ensures a specified and reproducible amount of adhesive is applied to the edges of the modules. Three ceramic stiffeners, 5 mm long and 0.5 mm wide, with a triangular profile, are inserted into grooves on the back of the modules to reinforce the glue joint.

During the production process, the grooves are edged into the handling wafer of the modules, which serves as a support structure below the implanted top wafer. For gluing, the modules are therefore transferred to special handling jigs that allow them to be turned upside down (see fig. 8.1 left). These handling jigs feature a porous ceramic surface at the sensitive area of the matrix touching the module's surface. A vacuum pump is attached to the porous ceramic to hold the modules in place. The handling jigs are mounted on an alignment tool to form the glue joint with micrometer screws under a microscope. Additional glue is applied to the grooves and the stiffeners are inserted manually from above using a vacuum tweezer (see fig. 8.1 right).

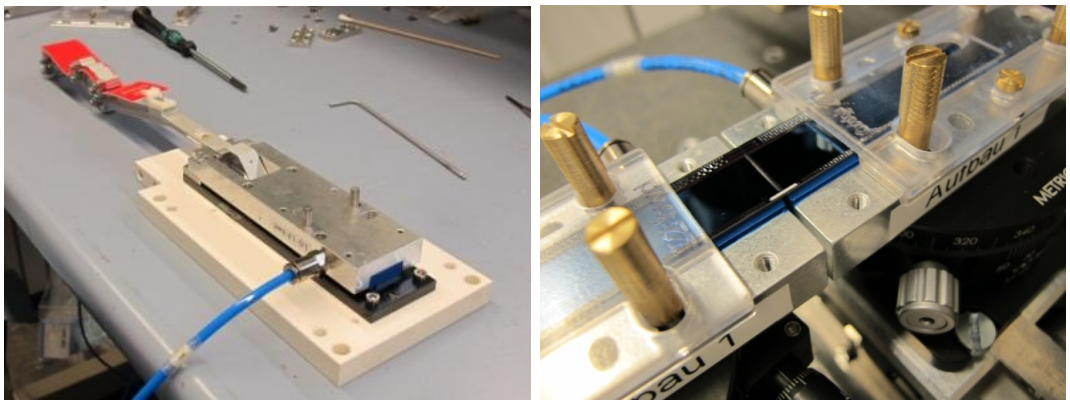


Figure 8.1.: Vacuum jig and alignment tool for gluing procedure with modules turned upside down [183]. Left: The vacuum jig is mounted on top of the module. The Kapton cable is attached to a holding structure of the vacuum jig and the applied vacuum holds the module while it is lifted from the base jig. Right: The ceramic stiffeners can be inserted from above.

After a curing time of 48 hours, the ladder is transferred to a ladder base jig and turned face up again. A high-resolution digital microscope is used to inspect and documentation the gluing joint (see fig. 8.2). After the inspection of the glue joint, the ladder is installed to the ladder test setup and the functionality of both modules is verified.

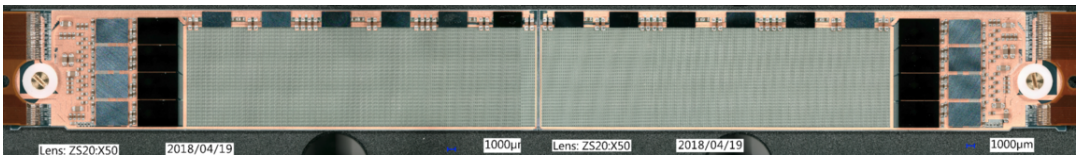


Figure 8.2.: Ladder L1_028 after gluing of backward module W03_IB and forward module W02_IF [184]. The ladder is fixed with a PEEK washer and a screw with specified torque on both sides.

8.1.2. Experience and results

A high-resolution Keyance VHX-6000 digital microscope is used to inspect and document each glue joint. The recorded images and measurements are stored on the Keeper service by the technician. In 18 gluing processes of production modules carried out using the procedure described, a glue gap of approximately $108 \pm 9\,\mu m$ was achieved. The lateral displacement Δx was approximately $10 \pm 7\,\mu m$ and the height difference Δh was approximately $7 \pm 15\,\mu m$ (see fig. 8.3).

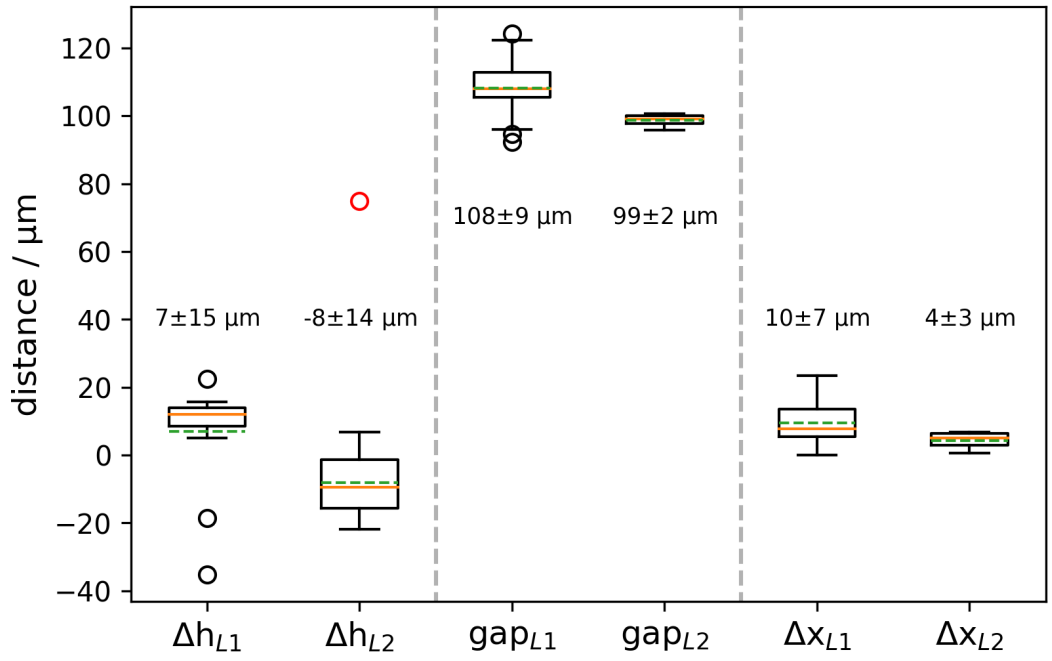


Figure 8.3.: Measured glue joint geometry of the first PXD production. The height difference at the glue joint Δh, the gap distance, and the lateral displacement Δx are shown. Different handling jigs are used for layer 1 and layer 2. The values are therefore given separately. An outlier in Δh_{L2} of almost $80\,\mu m$ (red) resulted from an operator error and was excluded from the calculation of the mean and standard deviation value, which is annotated for each group.

The process described achieved the required glue joint geometry and stability. However, it was found that touching the sensitive area with the handling jig could damage the modules. Although the porous ceramic was blown out with compressed air after each use, it was not possible to completely prevent the accumulation of dirt particles. During the subsequent gluing process, the dirt particles were pressed against the module surface. Eventually, the BCB passivation layer was penetrated and the metal layers were damaged (see fig. 8.4). This resulted in short circuits within the matrix, which could affect several drain lines or prevent the operation of the entire matrix.

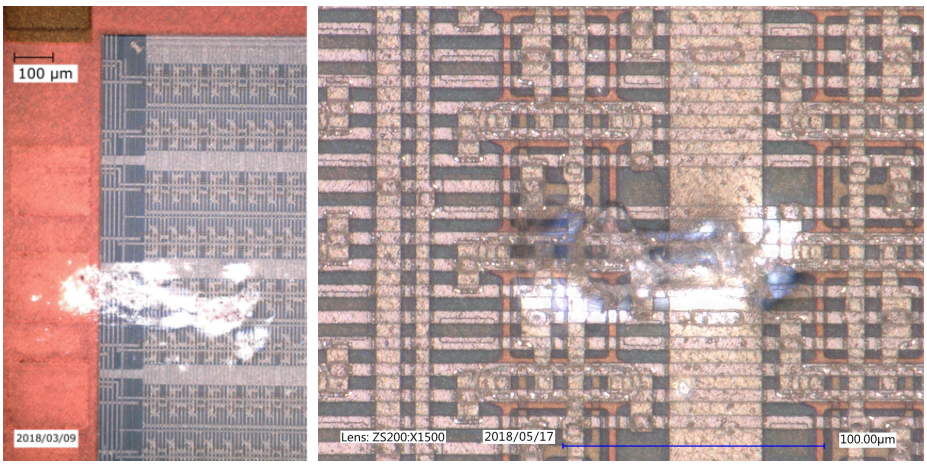


Figure 8.4.: Matrix damage through particle clamped between module and handling jig during gluing process. Left: Large impact on the matrix in the upper left corner of W44_OB1. The bright spot is the broken BCB passivation layer. Right: The impact on the matrix of W09_IF is smaller but resulted in a short between metal lines as well.

In total, 36 production modules were glued to 18 ladders using the process described, including all ten ladders for the PXD, which was installed at KEK in 2018. However, four modules in three ladders were damaged by particles during the gluing process. In addition, there was an overlap with link instabilities in the test setups that were not related to the gluing process, but this was not clear at the time. It was therefore decided that the risk of damaging the modules was too high to continue. The ladder gluing was stopped until a new procedure could be developed. The cost of this was that the PXD could not be completed. Only ten ladders, the inner layer plus two ladders of the outer layer, were installed. Simulations showed that the luminosity and therefore the hit rate in the PXD is low enough in the early operation of SuperKEKB that one layer of the PXD is sufficient for precise vertex reconstruction. While the first PXD was integrated to the Belle II detector, a new production of modules was started and the gluing procedure was reworked.

8.1.3. Reworked gluing procedure

The most important change in the reworked gluing procedure is the elimination of flipping the modules. The modules are glued face up and the module surface is not touched. The ceramic stiffeners are inserted from below using a newly designed lifting tool. First, the stiffeners are placed on the lifting tool, then an appropriate amount of glue is applied to the module edges and on the stiffeners by the dispensing robot. The lifting tool is installed on the alignment tool. The modules are also installed on the alignment tool and the glue joint is formed. The lifting tool is pushed upwards and the stiffeners self-align into the grooves (see fig. 8.5). The process is monitored by the technician through a microscope. Any overtravel or force on the modules is mechanically eliminated by the design of the lifting tool.

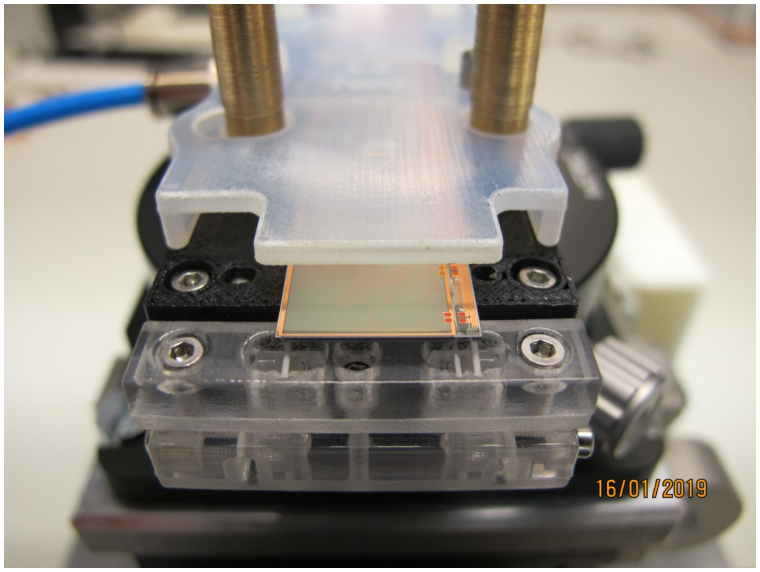


Figure 8.5.: Lifting tool for face up gluing procedure [105]. The ceramic stiffeners are positioned on the tool and inserted by lifting the tool from below the glue joint. The second module is removed in this picture for visibility.

An inspection tool based on a RaspberryPi computer with a camera module was developed to inspect the position of the stiffeners (see fig. 8.6). After removing the lifting tool, the technician positions the camera under the glue joint and activates it by pressing a button on the user interface. The video is displayed on a screen next to the workspace. This visual inspection enables the technician to determine whether manual adjustment of the stiffeners with a needle is necessary. Once the stiffeners are in the correct position, a photograph of the glue joint is taken. This image is then automatically transferred to the Keeper service for documentation purposes.

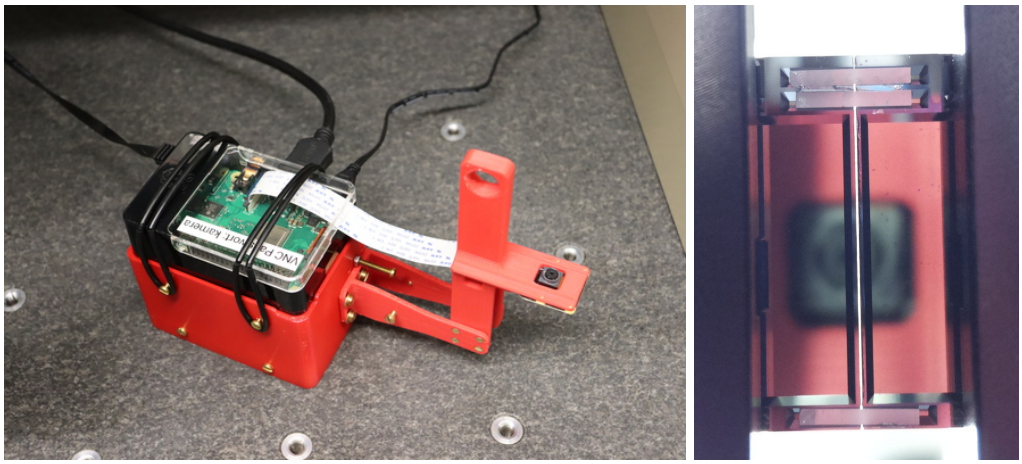


Figure 8.6.: Inspection camera and glue joint from below. Left: A custom made support structure allows to position the camera below the glue joint. Right: The position of the ceramic stiffeners can be controlled after the removal of the lifting tool. The reflection of the camera is visible on the thinned silicon.

Further improvements in the quality assurance were achieved by implementing the dual control principle with a second operator. Additionally, a new analysis tool was introduced to visualize changes within a module before and after the gluing process. It shows changes in pedestal values, applied voltages and currents (see fig. 8.7). This tool is commonly used to compare the state of a module needs to be compared at two points in time, such as before and after a transport. Using the reworked gluing procedure, all remaining production modules were glued without causing any further damage. This allowed for the installation of a completely new PXD with both layers during the first long shutdown of the experiment in 2022/2023.

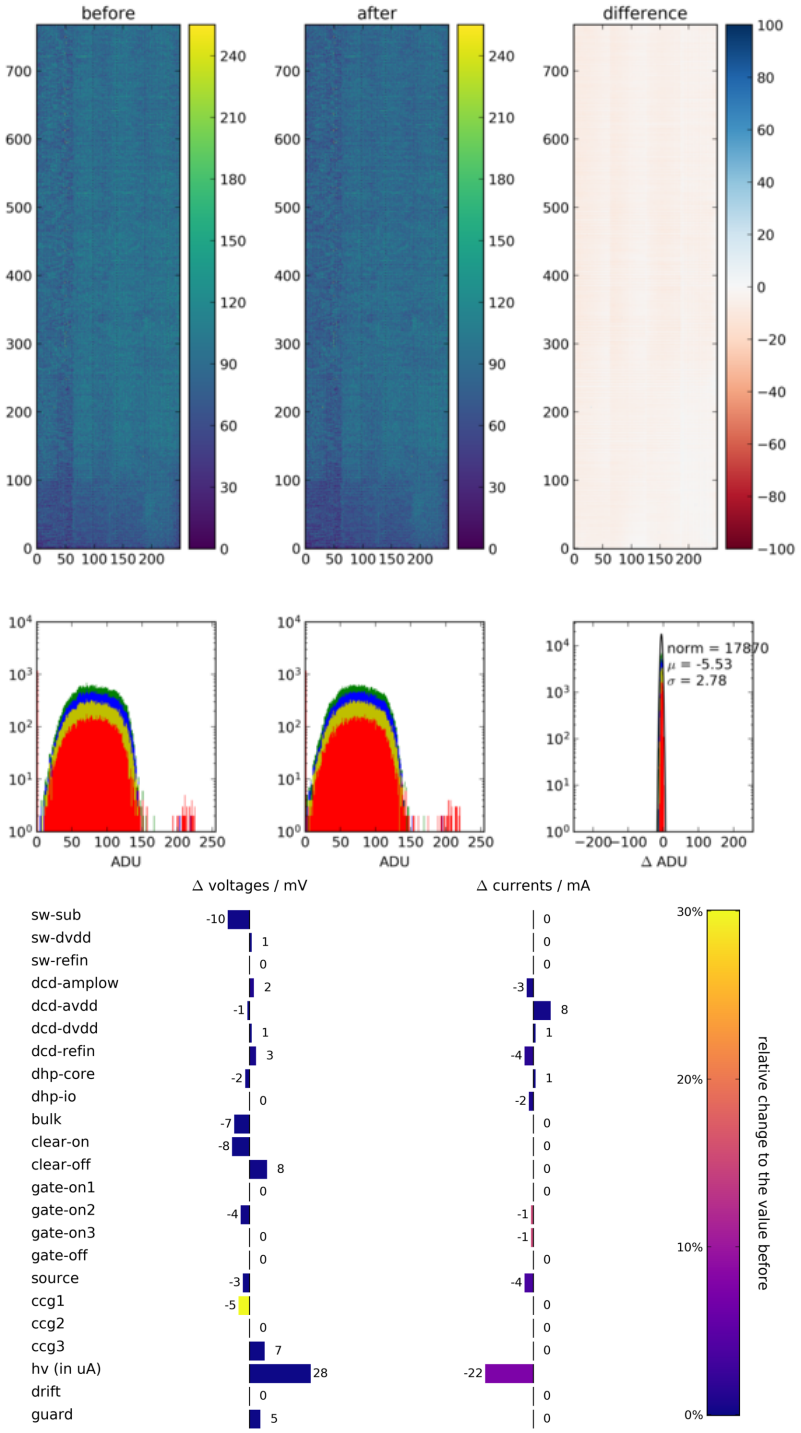


Figure 8.7.: Comparison of module states before and after gluing for module W04_OB1.

8.2. PXD assembly

After gluing, ten ladders were mounted onto two half shells. Eight ladders were installed in the inner layer, while two outer ladders covered the inner module with the lowest performance. For the commissioning of the composed PXD, the two half shells were then transferred from MPP to Deutsches Elektronen-Synchrotron (DESY), where a CO_2 cooling system and a sufficiently large clean room were prepared.

8.2.1. Half-shells

For mechanical reasons, the PXD is composed of two half-shells that enclose the beam pipe at the IP of SuperKEKB. The upper half-shell for Phase 3 is referred to as HS-1p3, while the lower one is referred to as HS-2p3 (shown in fig. 8.8). The SCBs serve as the final support structure for the PXD modules (see fig. 4.13). Each ladder is attached to the corresponding SCB on both sides using a single M1.2 screw. The torque applied enables sliding movement along the elongated hole of the forward modules, compensating for thermal expansion during the transition from ambient temperature to $-30\,°C$ of the CO_2 cooling system.

The mounting process follows again a carefully designed procedure that requires custom-made tools and a specific sequence. The detector geometry requires that inner modules be installed before outer modules. Additionally, only the most recently installed module can be removed as it blocks the access to the previous module. The technicians followed a detailed protocol with a checklist, including visual inspections and electrical tests after the installation of each module.

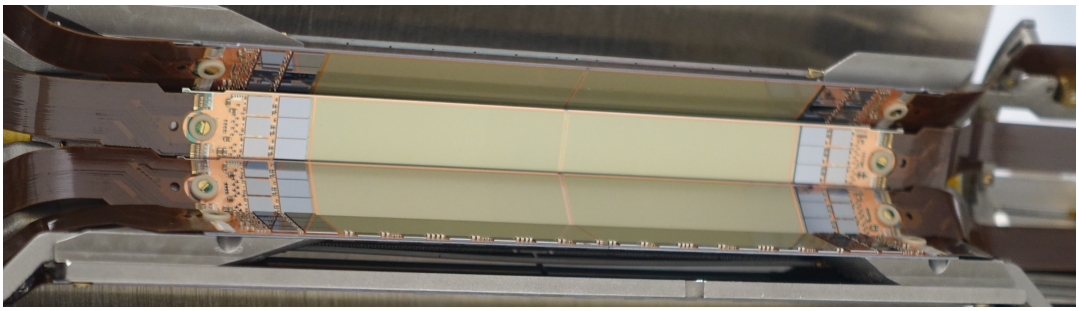


Figure 8.8.: Half-shell HS-1p3 from inside after ladder assembly [105]. The top side of the modules with the ASICs is facing the beam pipe. The windmill structure allows a complete coverage in ϕ. The gap between the sensitive areas of glued modules is about 850 µm (glue joint and supporting silicon frame). The position of the gap in the outer layer is shifted relative to the one in the inner layer to optimize the coverage.

Figure 8.10 shows the final arrangement of PXD modules in the detector for Phase 3. In both the slow control and analysis software, modules are identified by number based on their position (e.g. module 1.01.1 for W03_IF) rather then by name. Table 8.1 provides a list of all installed modules and their corresponding numbers.

8.2.2. Final verification at DESY

Once installed on the SCBs, the modules can only be cooled by a CO_2 cooling system. The final IBBelle system had already been installed at KEK. Therefore, the final test of the PXD detector took place at DESY (see fig. 8.9), where experience with the operation of smaller CO_2 cooling plants was collected during the thermal mock-up studies with the Multipurpose Apparatus for Research on CO_2 (MARCO) [185, 186]. The CO2lean cooling system from ETH Zurich was used as replacement for MARCO that had already been shipped to KEK for the commissioning phase. All services, including PXD Power Supplies, cables, DockBoxes, and DHH systems, were tested in the final arrangement. The slow control, LocalDAQ, and analysis software were adjusted to the composed configuration. For the first time, multiple PXD modules were operated in parallel. Once each component was verified, the entire setup was packed and shipped to Japan.

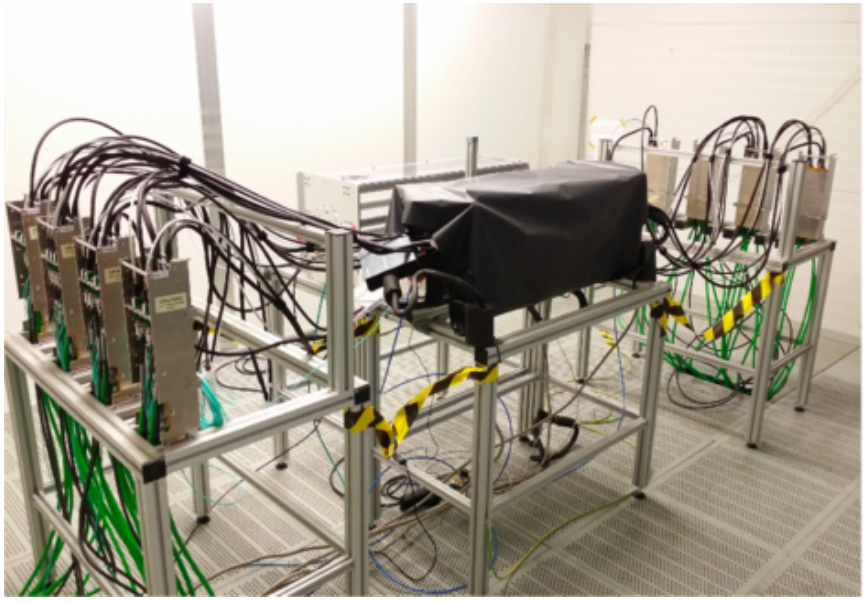


Figure 8.9.: PXD setup at DESY [187]. The PXD was operated in a light shielded and dry volume (center). Four DockBoxes were installed on both sides. Only half of the cables and services a connected for the ten installed modules compared to the original design.

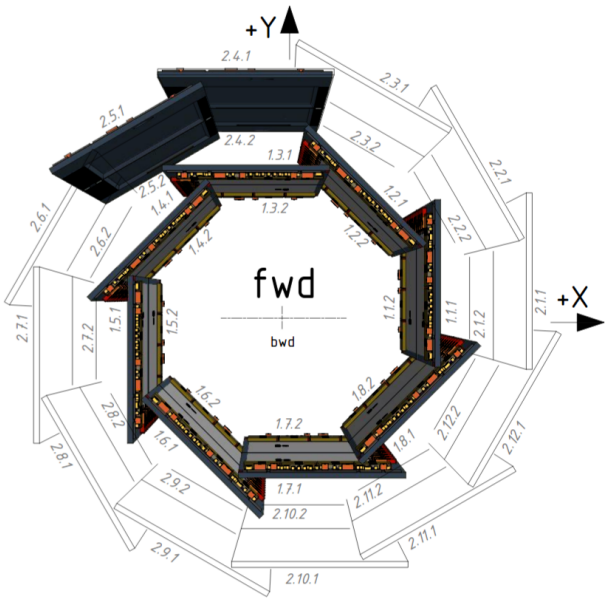


Figure 8.10.: PXD geometry - installed modules.

Table 8.1.: Installed PXD modules and their position in Phase 3.

module number	position	module name	half shell
1011	1.01.1	W03_IF	top / HS-1p3
1021	1.02.1	W42_IF	top / HS-1p3
1031	1.03.1	W45_IF	top / HS-1p3
1041	1.04.1	W13_IF	top / HS-1p3
1051	1.05.1	W32_IF	bottom / HS-2p3
1061	1.06.1	W41_IF	bottom / HS-2p3
1071	1.07.1	W47_IF	bottom / HS-2p3
1081	1.08.1	W02_IF	bottom / HS-2p3
1012	1.01.2	W43_IB	top / HS-1p3
1022	1.02.2	W45_IB	top / HS-1p3
1032	1.03.2	W01_IB	top / HS-1p3
1042	1.04.2	W13_IB	top / HS-1p3
1052	1.05.2	W44_IB	bottom / HS-2p3
1062	1.06.2	W41_IB	bottom / HS-2p3
1072	1.07.2	W02_IB	bottom / HS-2p3
1082	1.08.2	W03_IB	bottom / HS-2p3
2041	2.04.1	W32_OF1	top / HS-1p3
2051	2.05.1	W41_OF1	top / HS-1p3
2042	2.04.2	W09_OB2	top / HS-1p3
2052	2.05.2	W12_OB2	top / HS-1p3

9. PXD Operation at KEK

After the first version of a PXD was successfully built and tested in Germany, albeit a number of only 20 instead of 40 modules, the PXD was transferred to Japan, and the focus of activities shifted accordingly. This chapter describes the commissioning of the PXD in the Belle II experiment hall and the combination with the adjacent VXD, as well as the insertion into the final position. The adjustments of the slow control, that were required for the integration into the growing Belle II system, and the organization of shifts for detector operation are briefly addressed. A comparison between the optimized values from the laboratory and the operation values applied during Phase 3 is shown, before the beam loss incidents during Phase 3 and their impact on the PXD is discussed in more detail.

9.1. PXD commissioning

The PXD half-shells were transported separately by plane to KEK in August and September 2018. An own clean room was built on the base floor B4 of the Tsukuba experiment hall. In this clean room, the half-shells were mounted onto the actual mean pipe (see fig. 9.1). All modules were operated, verifying again the functionality of modules and all services. Also the SVD was commissioned in the same clean room. The MARCO system was used for cooling PXD and SVD. Once they passed their own tests, both detectors were combined to form the 6-layer silicon VXD for the Belle II experiment (see fig. 9.2). A subsequent cosmic ray test confirmed the functionality of the combined data acquisition system and collected data for the first alignment studies.

After the successful tests in B4, all services, cables and DockBoxes were disassembled again and installed at their final position in the Belle II detector. Only the PatchPanel cables remained connected to the Kapton cables of the PXD modules. A cable cage fixed their positions and ensured the required geometry for insertion into Belle II. The VXD including the beam pipe and the cable cage was lifted with the hall crane to the center of Belle II and inserted into the innermost volume. The ends of the PatchPanel cables were attached to the connectors of the DockBoxes. The CO_2 pipes

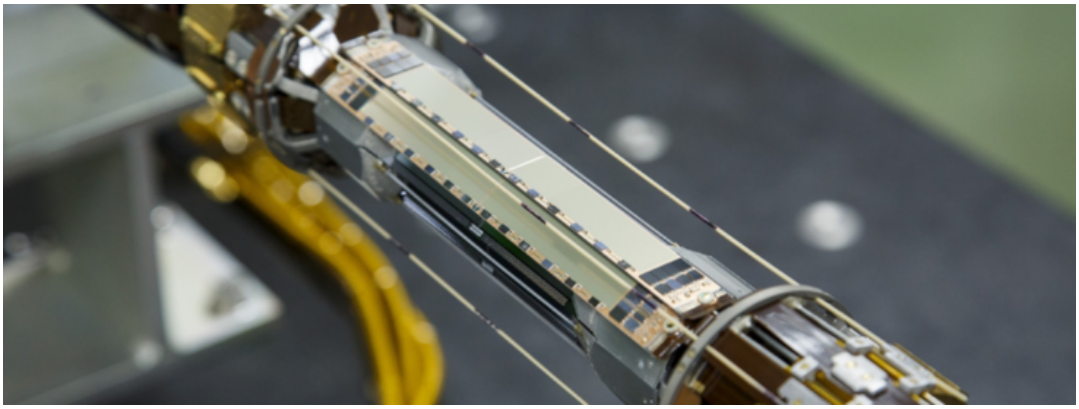


Figure 9.1.: PXD on beam pipe [188].

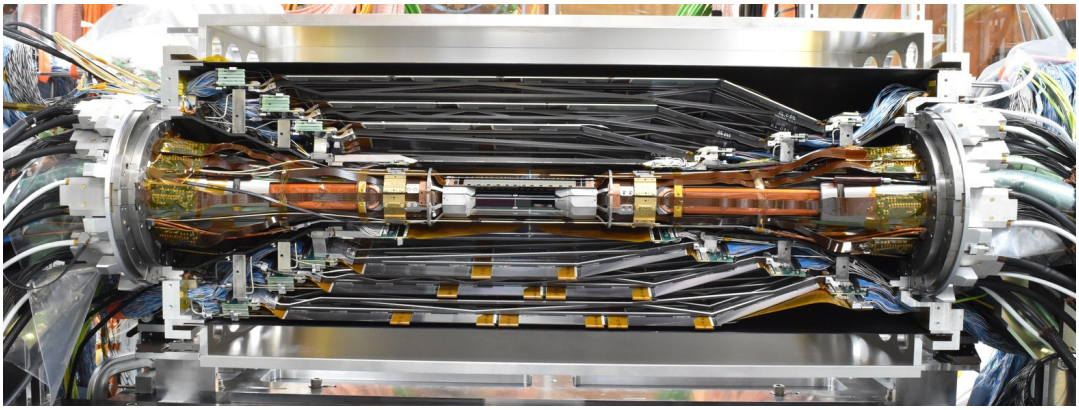


Figure 9.2.: PXD and half of SVD during marriage [88].

from IBBelle were connected to the SCBs and the origami pipe cooling system of the SVD.

Once the PXD could be operated again, all modules were tested and prepared for data taking. This included optimization of the link parameters and of the pedestals as described in section 7.4.2. The slow control system of the PXD was so far mainly used for standalone laboratory and test beam operation. Further development and extensions were required for the operation at the Belle II experiment. The components and their implementation are described in detail in [189]. Advancing automation allowed the successive transition to detector operation by non-experts.

9.2. PXD shift - proceeding automation

The operation of the SuperKEKB accelerator and the Belle II detector is organized in three shifts per day. For the Belle II detector there are two control room shifters, at least one shifter per subdetector, plus additional shifters for DAQ. The PXD shifts are to be filled by PXD collaboration members and can be carried out also from remote. While the PXD shift was a task for operational experts in the beginning, automation of power-up and all other operations required for a smooth operation of the PXD allowed non-experts taking shifts with an expert only as backup on-call. The OPIs of CS-Studio were adjusted to fit the needs of operating the PXD in the experiment. A pane with only few OPIs is sufficient to monitor the state of the PXD during data taking (see fig. 9.3).

The following measures assure the quality of the PXD shift. A shifter manual defines and explains the shifter duties. Before collaboration members can book a shift slot, they have to take part in a shifter training, pass the shifter quiz and complete a shadow shift as admission requirement. The assessment of the PXD performance and the flagging of recorded data is one of the main tasks during the shift. Four main data quality monitoring (DQM) histograms for the PXD are then provided to the shifter. These are generated from PXD data that is sent from ONSEN via the *Event Builder 2* to the *Express Reco*, where the basf2 software is used to analyze the data. The four histograms for the PXD show track cluster charge, common mode, efficiency, and integrated number of fired pixels (occupancy) per module. Reference values are given for comparison and the background color automatically indicates the current condition. Additional histograms are available for detailed investigation by experts. Each recorded run has to be flagged by the shifter to indicate the usability of the data for physics analysis.

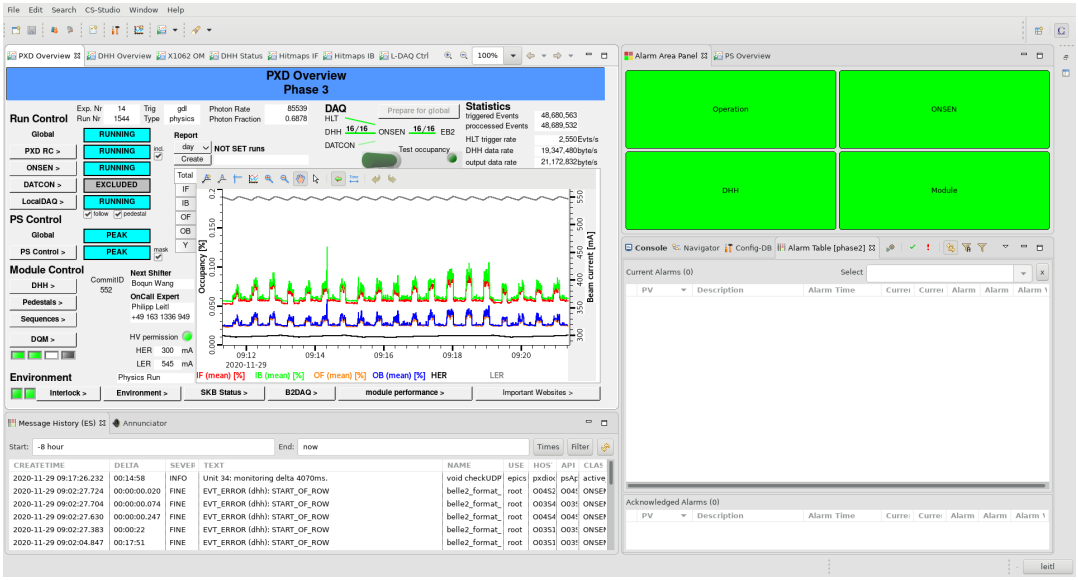


Figure 9.3.: CS-Studio GUI for PXD shifter. The *PXD Overview* OPI summarizes all important information for the operator. The plot in the center shows the live occupancy values. A common color scheme indicates the status of subsystems and facilitates monitoring. The automated alarm system and system message display enables fast error handling.

During the operation in Phase 3 the automation of the slow control system was constantly pushed forward. Through further integration into the global run control, the entire PXD can now be easily calibrated and brought into data-taking state with a single click by the control room shifter. This led to a significant reduction in workload for the PXD shifter.

During run time, a maintenance day was scheduled usually every second week for local runs and calibration of subdetectors. These slots were used by PXD experts for re-calibration and further optimization of the PXD modules. Equally, also the longer shutdown periods were used for further improvements.

Figure 9.4.: PXD remote shift. The daughter of the author "babysitting" the detector.

9.3. Comparison of optimized values: laboratory vs experiment

This section compares the values of the operation parameters as found during module characterization in the laboratories with the values during operation at the experiment. The aim is to confirm the usability of the optimized values and to investigate their stability over time.

The final installation of the PXD is less critical in terms of **data link stability** compared to the earlier designs that used a direct copper connection between the modules and the DHH system. The implementation of optical links between dock boxes and DHH system reduced the active copper path and therefore relieved the requirements on the CML drivers in the DHPs. As result, a broad parameter space of the driver configuration settings `bias` and `biasd` yielded stable links. The high speed link scan was not sensitive enough to find the maximum. Therefore, the CML driver parameters were set to the same values for all modules orientating on the values found in a more specific oscilloscope measurement [153] (see section 7.4.2.2). The values are 115 for `bias`, 225 for `biasd` and 0 for `delay`. These values were used during the entire Phase 3 operation and yielded consistently stable data links.

The **delay settings** for the data transmission between DCDs and DHPs ensure the correct synchronization between the two ASICs. A shift of these values due to gamma irradiation was observed above doses of 1 kGy [190]. The delay scan (see section 7.4.2.3) was therefore repeated during the summer shutdowns of Phase 3. For individual transmission lines fluctuations of ± 1 of the automatically determined optimal values were observed. However, the original values from the module characterization in the laboratories always allowed an error free data transmission and were therefore kept for the entire operation during Phase 3.

Offset calibrations were performed as part of the regular pedestal optimization to compensate for their continuous shift through irradiation effects. The transition to the advanced offset calibration utilizing the synergy effect with the ACMC (see section 7.4.2.7) led to a notable reduction of the pedestal spread compared to the configuration found during the module characterization in the laboratories. A small but not significant impact is visible on the distribution of the relevant ASIC settings `IPDAC` and `VNSubIn` (see fig. 9.5).

The **configuration parameters for the ADCs** in the DCDs as determined by the module characterization were not changed during Phase 3 operation. The optimization procedure is quite time consuming and complex (see section 7.4.2.8). While the impact of gamma irradiation on these values was also briefly addressed in [190], no significant

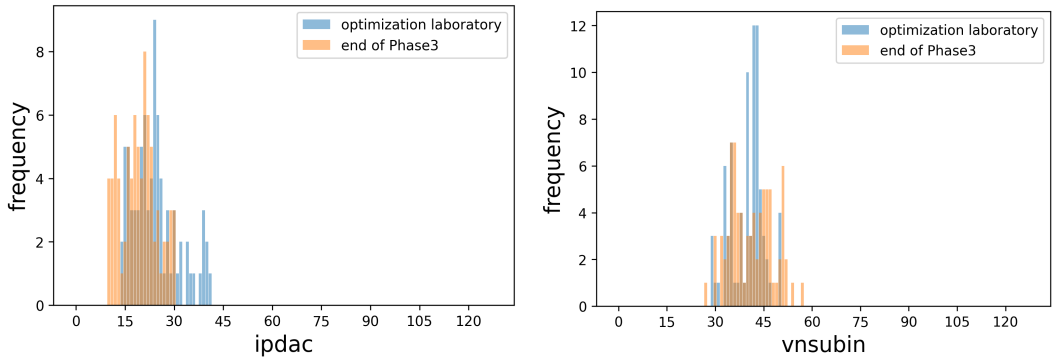


Figure 9.5.: Comparison of offset calibration settings between laboratory and experiment. The two points of comparison are the optimization in the laboratories and the end of Phase 3. Shown are only values from the 19 working modules building the PXD. Left: For `IPDAC` the distribution got slightly wider and shifted to lower values. Right: For `VNSubIn` the distribution got slightly wider.

degradation of the quality of ADC transfer curves were found. The ADC curve scan was therefore not repeated during Phase 3 and the used parameter values were kept constant.

Few changes are present in the matrix bias voltages clear-off, drift, and hv compared to the values found in the **source scans** (see fig. 9.6). The values for drift stayed constant and for only four modules clear-off was adjusted while staying in the initial range of 2 V to 5 V. The value of hv was adjusted for all but four modules, shifting the distribution to more negative values by about 2 V. In the experiment, it is not possible to place a radioactive source above the modules and to perform a source scan like in the laboratory (see section 7.4.2.9). A degradation of the detection efficiency and the occurrence of ring-like structures in the hitmaps, however, can be detected and the hv values were adjusted accordingly.

Further changes in the gate-on and DEPFET capacitive coupled clear gate (clear gate) bias voltages were necessary due to the threshold shift of the DEPFET I-V curves through irradiation. Compared to the values of almost unirradiated[1] PXD modules from the mass production characterization, the gate-on voltages were shifted by about -2 V (see fig. 9.7 left). This corresponds roughly to the expected value from the gamma irradiation measurement [190] for an estimated dose of 6 kGy accumulated during Phase 3 [191]. Also the clear gate voltages were adjusted to suppress increasing back injection. The values moved from the initial values of 0 V to about -1.0 ± 0.5 V (see fig. 9.7 right).

[1] The modules receive initial dose from the x-ray inspections during production (see section 7.2).

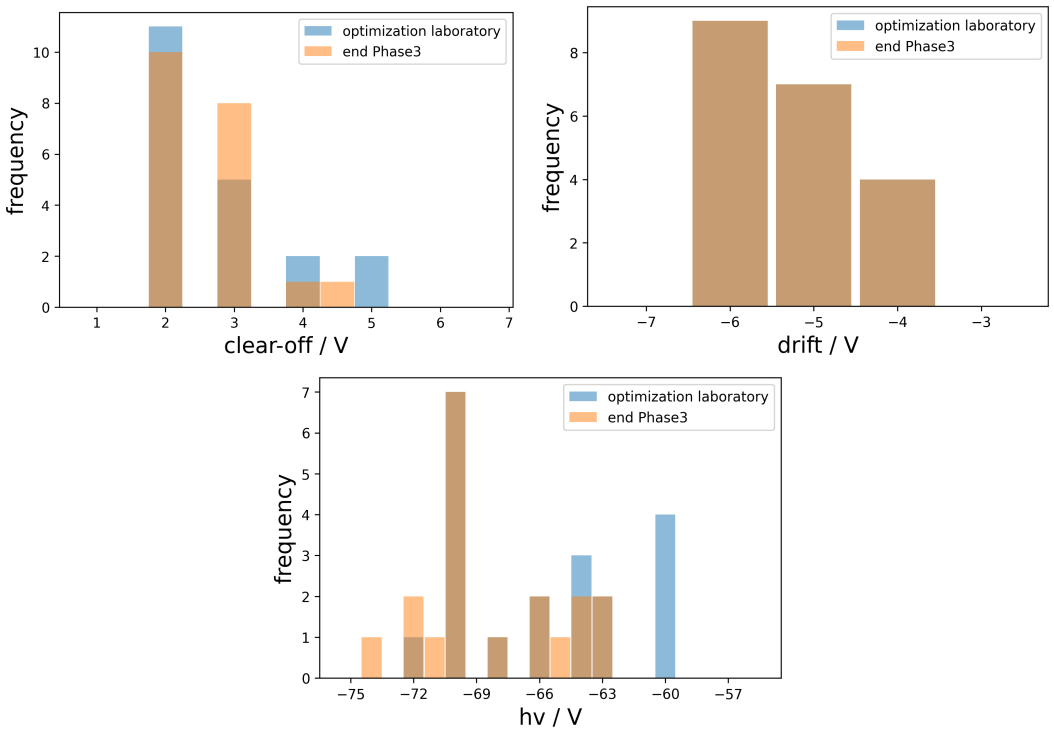


Figure 9.6.: Comparison of matrix bias settings clear-off, drift, and hv between laboratory and experiment. The values for drift stayed constant. Only for four module the value for clear-off was adjusted. The distribution of hv values was shifted to more negative values.

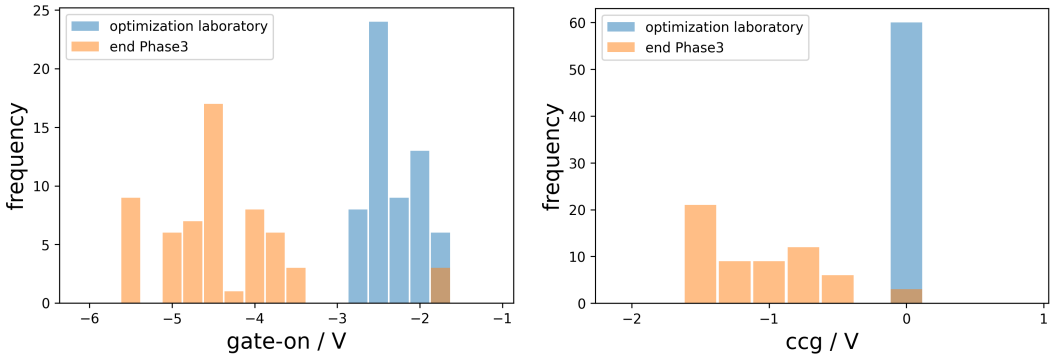


Figure 9.7.: Comparison of gate-on and clear gate bias settings between laboratory and experiment. Both settings were adjusted to compensate for radiation damages. The gate-on values were shifted by about $-2\,\mathrm{V}$, while the clear gate values were shifted by about $-1\,\mathrm{V}$. For the broken module W01_IB the three gate-on and three clear gate values remained unchanged.

In summary, the PXD modules were successfully prepared for the experiment. The values found during mass production module characterization proofed reliable throughout the operation in Phase 3 Settings for the high speed data links, ASIC communication delays, and ADC parameters remained unchanged for the entire period. Other settings require ongoing adjustment to compensate for radiation damages, like gate-on, clear gate, and the offset values including `IPDAC` and `VNSubIn` for pedestal optimization. Here, the development of optimization procedures and algorithms for module characterization payed off, especially the optimization of the pedestal distributions.

However, further studies and developments are still required for the future operation of the PXD, as only a fraction of the planned lifetime was reached so far. Effects from irradiation have been seen already in threshold voltage shift of DEPFET I-V curves. While this is covered by the adjustable gate-on voltage in the design of the modules, a new effect of increasing hv currents was observed that required rework of PXD Power Supplies. The total ionizing dose accumulated during Phase 3 was estimated to be about 6 kGy [191]. This is only a small fraction of the assumed 200 kGy total ionizing dose during the entire lifetime [192]. The major ramp-up in luminosity of SuperKEKB in the next years will be an exciting and challenging time for detector operation and might reveal some unexpected surprises. The sudden beam loss incidents discussed in the next section are one example.

9.4. Beam loss incidents and their impact on the PXD

During the operation of the PXD at the IP of SuperKEKB damages in the PXD sensor modules occurred. The failure of entire gate lines of some of the Switcher ASICs and simultaneously increased currents in the clear lines correlated with sudden beam loss events in the accelerator [193]. Inefficient gates were already observed during mass testing. An attempted explanation of the observed symptoms is given in section 7.5.1. The number of affected gate lines increased with increasing number of sudden beam loss events. Two algorithms were developed to analyze the affected gates in the recorded data and an automated notification for the PXD shifter was implemented in case of the appearance of additional failing gate lines. The algorithms were used to analyze the development over time and to identify the four most severe beam loss events so far. The analysis of the damages revealed a higher susceptibility of the Switcher ASIC towards the last two gates. Irradiation campaigns of test structures with Switcher ASICs reproduced the observed damage. Several protection measures and improvements were discussed within the PXD and SuperKEKB collaborations and implemented.

9.4.1. Beam stability and beam losses

In the early Phase 3 operation of Belle II most of day time operation was used for fine-tuning of the SuperKEKB accelerator, performing so called "machine studies". In order to achieve optimized collision conditions numerous machine parameters are varied by the accelerator group. While some settings have to be adjusted for constantly changing beam conditions to keep the current working point others are scanned actively to find the optimum performance. During those "machine studies" the detectors are usually turned off due to the higher risk for beam losses. The operational experience gained by such studies increased the luminosity as well as the stability of the accelerator [194].

While running in "operation mode", i.e. "luminosity mode", with fully powered detectors, beam conditions may still change spontaneously and the beams can leave the intended orbit. This results in an increased synchrotron radiation of the bunches. A beam monitoring system is used to detect those situations and automated measures are taken to get the particle bunches back on track. If this fails and the trajectories of the bunches can not be corrected again, the beams can hit structures like collimators or the beam pipe resulting in potentially harmful radiation levels for the detectors. To prevent this, the monitoring system is able to trigger a beam abort as soon as defined limits are exceeded. All bunches are then deviated to hit a dedicated beam dump target. This can be realized within a few turnarounds of the bunches in the

accelerator ring after the abort signal was issued. In the cases discussed below the beam dump happened after three to four turns, corresponding to 30 µs to 40 µs, after the abort trigger was issued.

9.4.2. Detector protection and monitoring systems

Even though designed for the detection of ionizing radiation and constructed to cope with high exposure rates, all particle detectors have limits regarding their tolerable radiation doses. The susceptibility to radiation damage is highest as long as the operation voltages (e.g. bias and depletion voltages) are applied. Therefore, the abort signal is also forwarded to the power supplies of the individual subdetector systems and they are shutdown in parallel to the beam abort to protect the subdetectors as efficiently as possible. For such cases a special emergency shutdown procedure is used which is faster than the usual power down scheme.

In addition to the SuperKEKB beam monitoring system, an environmental and radiation monitoring system is integrated into the volume of the Belle II detector [89, 195, 196]. It is especially designed to monitor not only the radiation dose rates but also temperature and humidity at the IP and inside the vertex detector. Diamond sensors controlled and read out by purpose-designed Diamond Control Units (DCUs) measure the radiation dose rates. Negative temperature coefficient (NTC) thermistors and fiber optic sensors (FOSs) measure the temperatures at the cooling pipes and in between the layers of the VXD to protect the installed electronics from overheating. The humidity inside the VXD volume, which is flushed with dry nitrogen, is measured via "sniffing pipes" connected to external humidity sensors. The combination of temperatures and humidity allows to monitor the dew point in order to prevent condensation or ice formation at cooled surfaces.

All environmental sensors are integrated into a central interlock system for the vertex detector: VXD Local Hardwired Interlock (VLHI) [89, 197]. It is implemented using a Programmable Logical Controller (PLC) providing industrial standards in terms of programming flexibility and long-term reliability [198]. Additional inputs are a manual interlock, the central Belle II interlock system (solenoid, water leak, E-Hut power) as well as the interlock signals from the SuperKEKB accelerator (beam monitor). The environmental monitoring system can provoke a beam abort as well.

All safety precautions are taken to keep the risk of detector damages as low as possible. The necessity of these efforts and also their limits are impressively demonstrated by such incidents where the detectors were damaged nonetheless.

9.4.3. Harmful beam loss events during Phase 3 operation

Spontaneous changes are particularly dangerous as reactions and corrections must be applied within short time. Unlike thermal or humidity changes, which occur on a time scale of seconds or even minutes, changes in the beam conditions up to beam loss events can become harmful within a few microseconds. There are different possible scenarios which can lead to intolerably high radiation doses in the detectors [193]. The following two are described as they were discussed to be the cause for the most severe damages observed in the PXD [199]. I will focus on four particular events which showed the largest impact.

- Type 1 events were caused by a malfunction of the power supply of the QC2LE magnet, a magnet of the QCS system on the HER before the IP [199]. The power supply got out of sync with the accelerator, its switching frequency slowed down and the beam orbit drifted away. Subsequently, the next magnet, called QC1LE, was hit by the beam and the deposited energy heated the superconducting magnet, which quenched. An overview of the QCS and the involved parts is shown in fig. 9.8.

- The cause of Type 2 events, called "sudden beam loss" events, is not fully understood yet. Simultaneously observed pressure burst in the LER led to the first assumption of a collision of the LER beam with dust particles. However, it falls short to explain the vertical beam loss during such events. The "fireball hypothesis" of ionizing electric discharge is currently discussed but could not be confirmed yet [193]. In the events discussed below, the energy loss of the beam resulted in a horizontal shift of the beam orbit, then the beam abort was triggered.

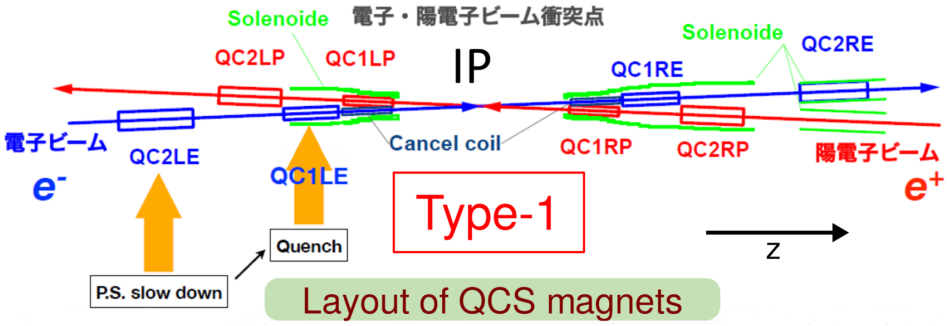


Figure 9.8.: Layout of QCS system with indication of type 1 beam loss event [199]. The HER with the electron beam is depicted in blue and the LER with the positron beam is depicted in red.

The DCU detected all of those beam loss events in form of radiation bursts. However,

the specific configuration of the DCU system determines the time and therefore the total amount of received radiation before the abort signal is issued. The defined threshold values have to fulfill a difficult balance: Too harsh values would trigger many beam aborts which prevent a stable beam operation. This leaves no margin for fine-tuning beam parameters to increase the collision performance. Too loose values, otherwise, would accept larger damages in the subdetectors. Even with an appropriate threshold value, a delay of the abort signal due to any time consuming operation has to be excluded:

- On May 28, 2019, the DCU sensors were configured such that they reached their saturation quickly but multiple integration times, i.e. multiple beam turnarounds, were required until the recorded dose exceeded the threshold. The beams were dumped only about 110 µs after the increase of radiation was detected [200].

- On May 27, 2020, another configuration issue led to an increased detector irradiation. The LER beam was dumped and the DCU system started to write data to disk for later diagnostics. As the radiation level due to the LER beam dump was not high enough to trigger a beam abort, the HER beam continued to circulate. The DCU system was blind during the readout of the detailed data and therefore did not recognize the high radiation from the worsening HER beam [201]. The HER beam was finally stopped by the beam monitoring system. Without data from the DCU, information about the length and strength of the irradiation due to the HER beam loss are not available.

Both issues led to a delayed abort signal and resulted in received dose levels in the inner detectors which caused permanent damages.

Additionally, beam loss events are potentially harmful not only for the detectors but also for the accelerator structures. The beam loss incident on June 9, 2019, was of type 2 and it was the most severe one during Phase 3 operation. A beam current loss of about 150 mA corresponding to a third of the beam current within three to four revolutions was observed before the beam was aborted. The head of the LER D02V1 bottom collimator was visibly damaged (see fig. 9.9). The recovery of the cooling system took two days due to a complete evaporation of the liquid He of the QCSR [199, 202].

In conclusion, the results of the most severe beam loss events during Phase 3 operation were QCS quenches, a damage of the collimator structure and damages in the innermost detectors, namely $\mathcal{O}(10)$ additional pinholes observed in the SVD [204] and the damages in the PXD discussed in more detail below.

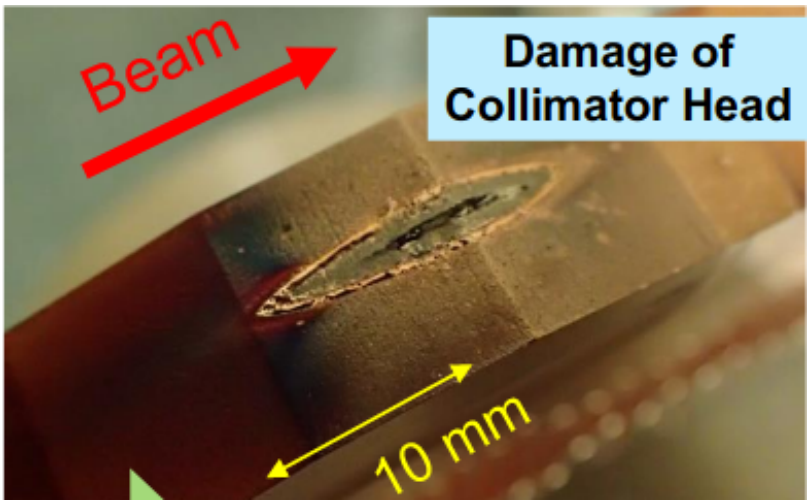


Figure 9.9.: Picture of damaged collimator head of D02V1 [203].

9.4.4. Observed damages in the PXD modules

When a beam loss event triggers an emergency shutdown all detector systems are off. Already during the subsequent power up of the PXD indications of induced damages can be visible. Observed issues were increased currents by 50 % to 100 % especially in the clear lines. For certain incidents and individual modules the clear currents reached even the safety limits and therefore the automated power-up sequence of the detector was stopped. Also reported warning messages from the OVP system of the PXD power supplies showed that the applied voltages at the modules left the nominal operation range, when the modules were hit by the radiation burst.

The development of the clear currents of the module 1.07.1 is shown in fig. 9.10 as example. The plotted time range covers the two most severe beam loss incidents during operation in 2019. After the first incident the currents in the clear lines exceeded the set limits which prevented an operation of this module. It was possible to recover a functional state by carefully increasing the corresponding current limits for the clear lines. The current in the clear-on line increased from about 40 mA to about 60 mA and in the clear-off line from about -20 mA to about -40 mA. In addition, the currents showed unusual fluctuations during operation resulting in an increased number of noisy pixels. Due to re-tuning of the clear-gate and gate-off voltages the currents returned to the previous values and the module entered a stable state [205]. After the second incident the clear currents increased again, this time even further by additional about 5 mA. Since then, the module was operated in this state.

The impact on the currents was most prominent for module 1.07.1 but also other

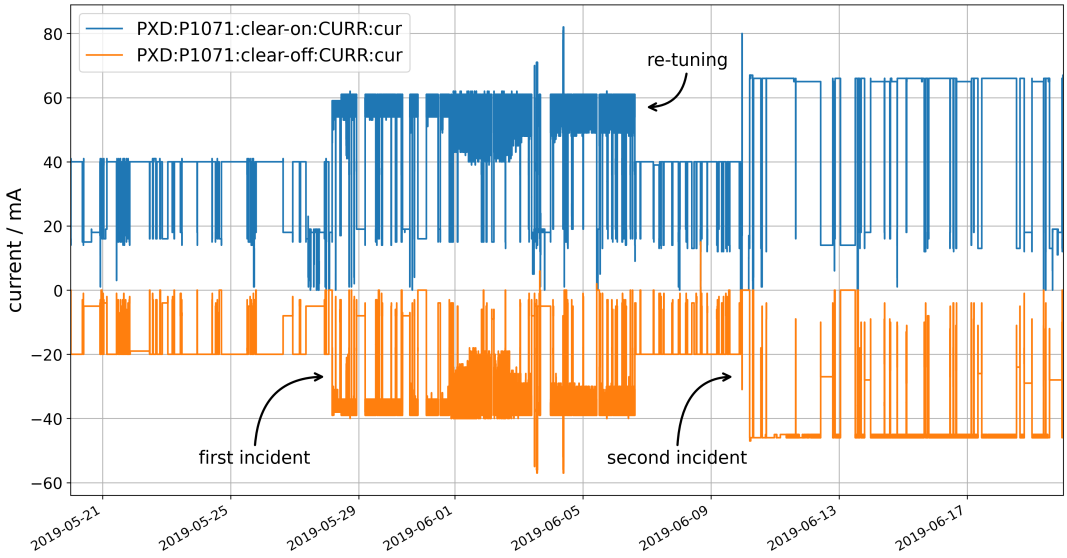


Figure 9.10.: Development of currents in the clear-on and clear-off lines of module 1.07.1 as result of beam loss incidents and re-tuning of bias voltages. The frequent drops to about half of the maximum value display the points in time when the module was not in PEAK but in STANDBY. Visible are several jumps of the maximal values caused by the two beam loss incidents and re-tuning in between. The simultaneous change in both lines is about the same amount but with different sign which indicates that the additional current flows from clear-on to clear-off.

modules showed increased clear currents after the first severe beam loss incident (see fig. 9.11). Nine out of 20 modules showed increased clear currents. Those modules are mainly grouped in the +x direction of the detector. Only for one module (1.01.1) the currents decreased significantly. This module was in an unusual high current state before and recovered to more typical currents. The increased clear currents are not an issue themselves (as long as they stay within the safety limits) but they are related to damages in the ASIC electronics. This becomes evident in the subsequent data taking.

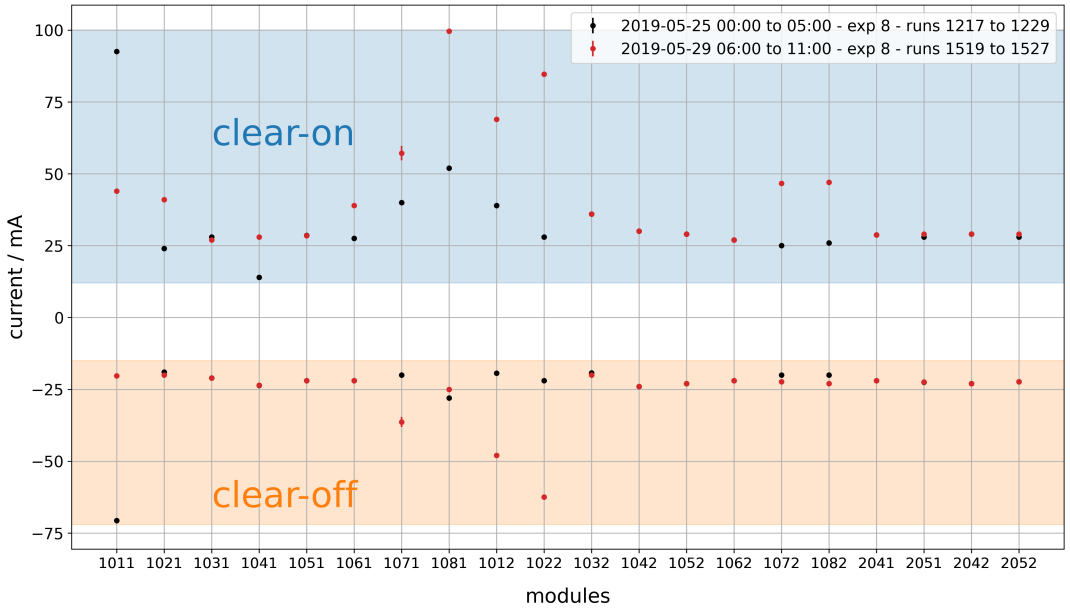


Figure 9.11.: Change of the clear currents for all modules after the first severe beam loss incident on May 28, 2019. A period of five hours constant operation in PEAK before (black) and after (red) the first severe incident was used to calculate the mean values of the clear currents for each module. During this periods the currents were stable except for module 1.07.1 after the incident so that the error bars are smaller than the plotted markers.

A comparison of the hitmaps before and after the incidents reveals additional insensitive regions in which almost no hits are detected. Figure 9.12 shows the development of the hitmaps of all inner modules over time. The first plot represents the initial state at the beginning of Phase 3 data taking. The following plots show the hitmaps in the next data taking runs after the first three most severe beam loss incidents.

Modules which did not participate in data taking are left blank in fig. 9.12. Module 1.03.2 was not operational from the start but the geometrical gap is covered by two outer ladders not shown in the plots. Module 1.07.1 and 1.08.1 could not be operated for several days after the first and second incident, respectively. The matrices are

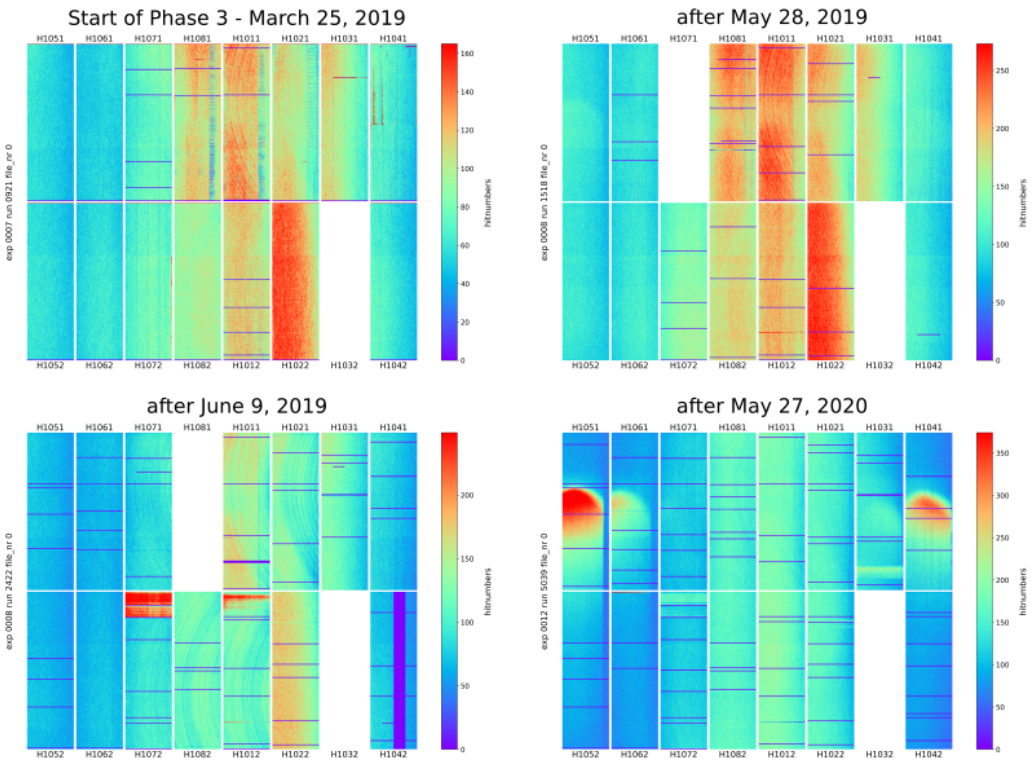


Figure 9.12.: Comparison of PXD hitmaps before and after beam loss incidents. The number of inefficient gates, represented by the dark horizontal lines, increased after each severe beam loss event. The plotted hitmaps show a integrated count how often a pixel's readout value was above the zero-suppression threshold. No hit clustering is applied. The color scale is common for all modules of the particular subplot (not between the different subplots). In this way the hitnumbers of the different modules are set into correlation.

not shown in their geometrical orientation relative to each other but rather in a 2D plane corresponding to a roll out of the cylindrical arrangement of the PXD. The overlapping of the modules results in less hits on the right side of the individual matrices. Neighboring modules cast a shadow and shield at least soft photons (keV). The higher hitnumbers on the modules in +x direction (in the middle of each subplot) agree with background simulations and analysis [206, 207].

The actual damage of the PXD is visible in the increasing number of dark horizontal lines in the hitmaps. They appear always in groups of four geometrical DEPFET rows corresponding to one electrical gate. There are almost no hits detected in those gates, therefore, they are called inefficient or "dead" gates. This is not an effect of the corresponding pixels in the matrix, but rather the result of a damage in the Switcher ASIC. The observation of increased currents in the clear lines, which are bias voltages switched by regulators in the Switcher ASICs, supports this hypothesis. It was finally confirmed in irradiation tests, which reproduced the damage [208].

Out of nine modules which showed a significant change in the clear currents after the first severe beam loss incident (and where hitmap data was available) only one module (1.04.1) did not show additional inefficient gates (see fig. 9.13).

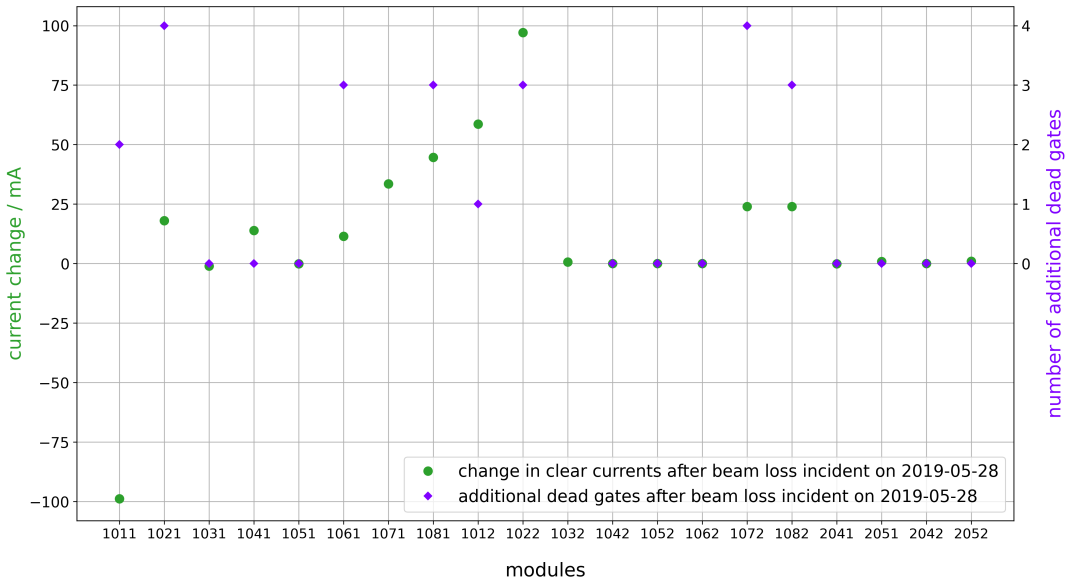


Figure 9.13.: Change of clear currents and number of additional inefficient gates per module after the first severe beam loss incident. The same period of time / data was used as for fig. 9.11. No marker for the number of additional "dead" gates is set where no hitmap data is available because the module was not operational.

However, while the increased currents can be a good indication for the appearance of additional inefficient gates there is no compulsory correlation between the size of the current change and the number of additional inefficient gates (see fig. 9.14).

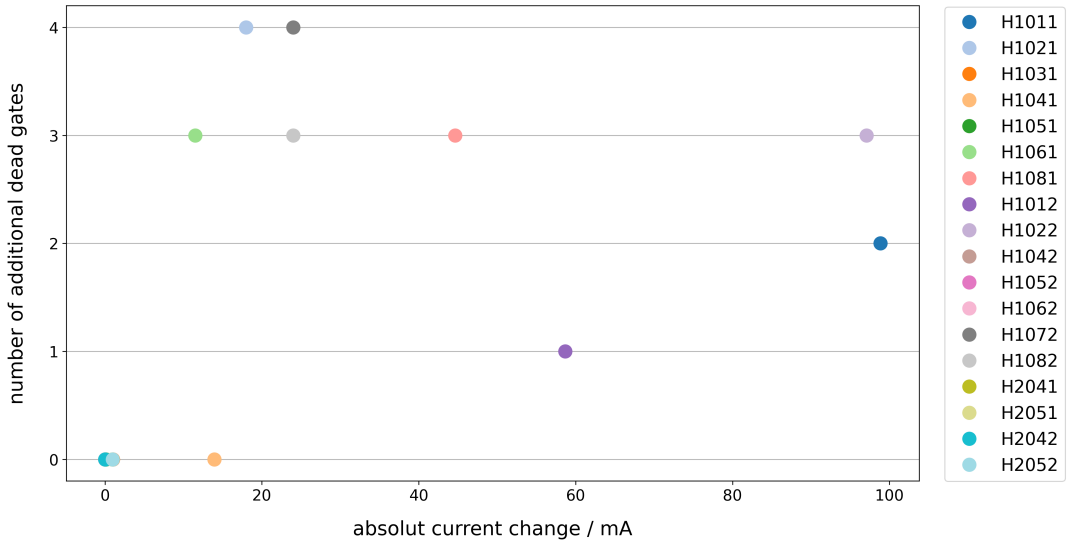


Figure 9.14.: Correlation between current change in clear lines and number of additional "dead" gates per module. All but one module with a significant change in the clear currents show an increased number of inefficient gates. A correlation between the size of the current change and the number of additional inefficient gates is not visible.

Furthermore, a strong anisotropy of the damages was seen after the first beam loss event. The cause for the beam loss was the failure of the power supply of the QC2LE, whereupon the electron beam drifted away towards the +x direction. Consequently, the modules in the +x direction obtained the largest irradiation dose and suffered damages in form of lost gates as illustrated in fig. 9.15. For exactly all of the affected modules the OVP triggered during the incident which indicates that the safety limits for voltages and currents were exceeded. The other modules were largely spared by this first event. However, until the end of the 2021b run and after three further severe beam loss events additional inefficient gates are present in almost every module[2]. For completeness polar distributions of additional inefficient gates after two further severe beam loss events are shown in fig. 9.16.

In the next section different algorithms for the automated detection of inefficient gates will be described. The development of these gates over time is analyzed and linked with the high irradiation events.

[2]Only module 2.05.2 (W12_OB2) did not show any inefficient gate so far.

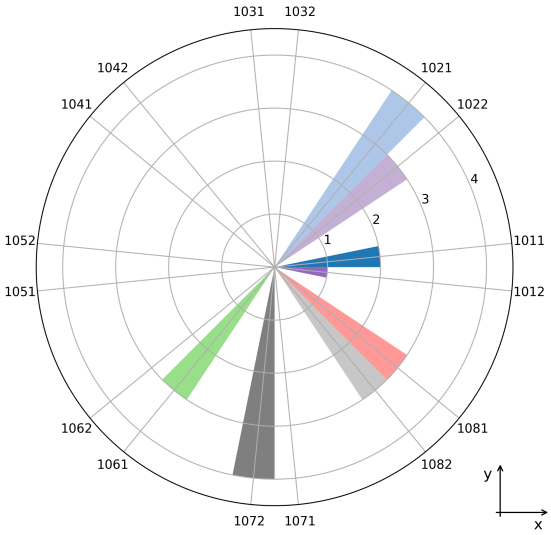


Figure 9.15.: Additional inefficient gates per module after the first severe beam loss event plotted in polar coordinates to indicate the anisotropy. Forward and backward modules are plotted next to each other to make the individual cones visible although the modules themselves are actually placed at the same angle. Color scheme according to the previous plots.

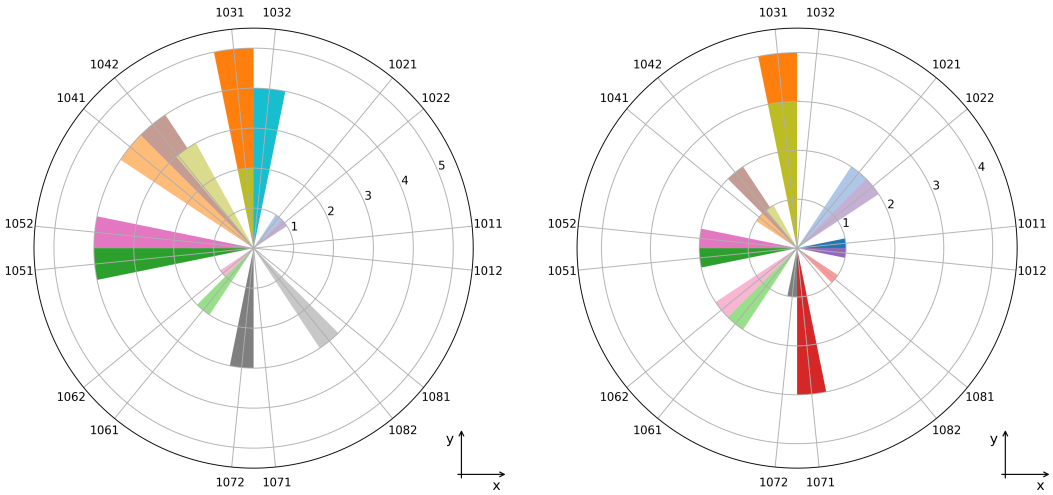


Figure 9.16.: Polar distribution of additional inefficient gates after further severe beam loss incidents. On the left the results of the incident from June 9, 2019, is shown and on the right from May 27, 2020. The cones of the outer modules 2.04.1 and 2.05.1 are placed above the ones of the inner modules 1.03.1 and 1.04.2, respectively, which are larger and therefore not hidden.

9.4.5. Automated detection of inefficient gates in LocalDAQ data

The appearance of inefficient gates is clearly visible in the plotted hitmaps as regions with less or almost no hits (see fig. 9.12). Therefore, the first detection algorithm developed uses this data as input. Later a second method using additional information from the signal values is described. For completeness, a third possibility by comparing pedestal values is mentioned as well. Regarding the online monitoring, the hitmap data has the advantage that a hitmap for each module is anyhow created by the PXD Online Monitor using a certain fraction of the recorded data from the LocalDAQ. The plotted hitmap and several histograms are provided for the PXD shifter in real time. On this basis the "dead gate detection" was implemented as new online feature to the already existing tools. Dependencies on functionalities further down the data stream like clustering or track reconstruction are not required.

The task to find certain structures in an image points to a pattern recognition problem. Those are typically addressed by a variety of machine learning algorithms. The given problem was also first approached with the methods of supervised learning and different classifiers for a support vector machine were evaluated. However, in the course of further feature extraction within the first method in order to improve the results, it became evident that inefficient gates can be detected by an appropriate threshold value and machine learning is not required for this task. However, a further development of the second method using machine learning is still conceivable.

The hitmaps are created by simply counting how often each pixel "fired", meaning how often the readout value was above the zero suppression threshold. No clustering is performed. The studied regions of inefficient pixels occur always in groups of four geometrical DEPFET rows corresponding to one electrical gate. Consequently, for the data analysis as well as for the following plots the electrical mapping is used (compare section 4.2). In this way the patterns originating from electrical properties are clearly visible.

Both methods using the hitmap data depend on a normalization of the hitnumbers per pixel. This is achieved on different ways but becomes in both cases very advantageous as the absolute hitnumber values depend on several factors which not only vary between different measurements but also within one measurement inhomogeneous distributions of the hitmaps along the pixel matrix occur. Several possible dependencies of the absolute hitnumbers are listed in table 9.1.

Table 9.1.: Factors influencing the homogeneity of hitmap data.

factor	**experiment**	**laboratory**
duration of the measurement	the longer the exposure time the more hits will accumulate	
module settings	mostly the zero suppression threshold but also the biasing voltages and internal noise conditions	
position of the module relative to the source	higher intensity for smaller distances from the source	
	first layer vs. second layer or higher beam background in +x direction	position of the source holder
intensity of the source	beam conditions	activity of the source
homogeneity of the irradiation	additional soft photon spot from synchrotron back scattering, partial shielding by detector structures	spot like irradiation from collimated radioactive sources

Comparison to neighboring gates - neighbors method

The idea behind the "comparison to neighboring gates" is that the achieved values are normalized to a close region around the gate which is studied. This helps to level out the inhomogeneity along the matrix and highlights the sharp transitions between working and "dead" gates. In the following the technical details of the current state of this algorithm is described. An overview of the development steps is given in appendix E.

A clip at the 99th percentile of all hitnumbers of a matrix is set to cut away especially noisy pixels as well as those pixels in the last gate which are set deliberately to fire in each frame to overcome a timing bug in the DHP. Using this truncated data a $mean_{i,j}$ of the hitnumber values around each pixel (i, j) is calculated where only the n next electrical neighbors on the same drain line j and the pixel itself are taken into account. Index i denotes the gate, index j the drain line. At the front and at the end of the matrix always the same first (or last) $n+1$ gates are used. An overflow to the other side like the scheme for the rolling shutter readout mode is not assumed. These considerations result in the following formula:

$$mean_{i,j} = \frac{1}{n+1} \sum_k hitnr_{k,j} \quad \text{with } k = \begin{cases} [1, n+1] & \text{if } \; i \leq \frac{n}{2} \\ [n_{gates} - n, n_{gates}] & \text{if } \; n_{gates} - i < \frac{n}{2} \\ [i - \frac{n}{2}, i + \frac{n}{2}] & \text{else} \end{cases} \tag{9.1}$$

As standard value the mean is calculated over the ten next neighbors ($n = 10$). For PXD9 modules $n_{gates} = 192$, for Hybrid5 modules $n_{gates} = 16$. The hitnumber of each pixel is set into relation to the mean (while making sure to avoid division by zero) resulting in a relative hitmap as shown in fig. 9.17. Those pixel values are close to 1 for working pixels and close to 0 for "dead" pixels.

$$val_{i,j} = \frac{hitnr_{i,j}}{mean_{i,j}} = \begin{cases} \approx 1 & \text{for working pixels} \\ \approx 0 & \text{for "dead" pixels} \end{cases} \tag{9.2}$$

Finally, the median per gate is compared to a threshold value of 0.66 to separate the inefficient gates. As example, fig. 9.17 shows the inhomogeneous raw hitmap data of module 1.05.1, the processed relative hitmap and the resulting median values per gate. However, this method will fail when n or more gates in a row are affected.

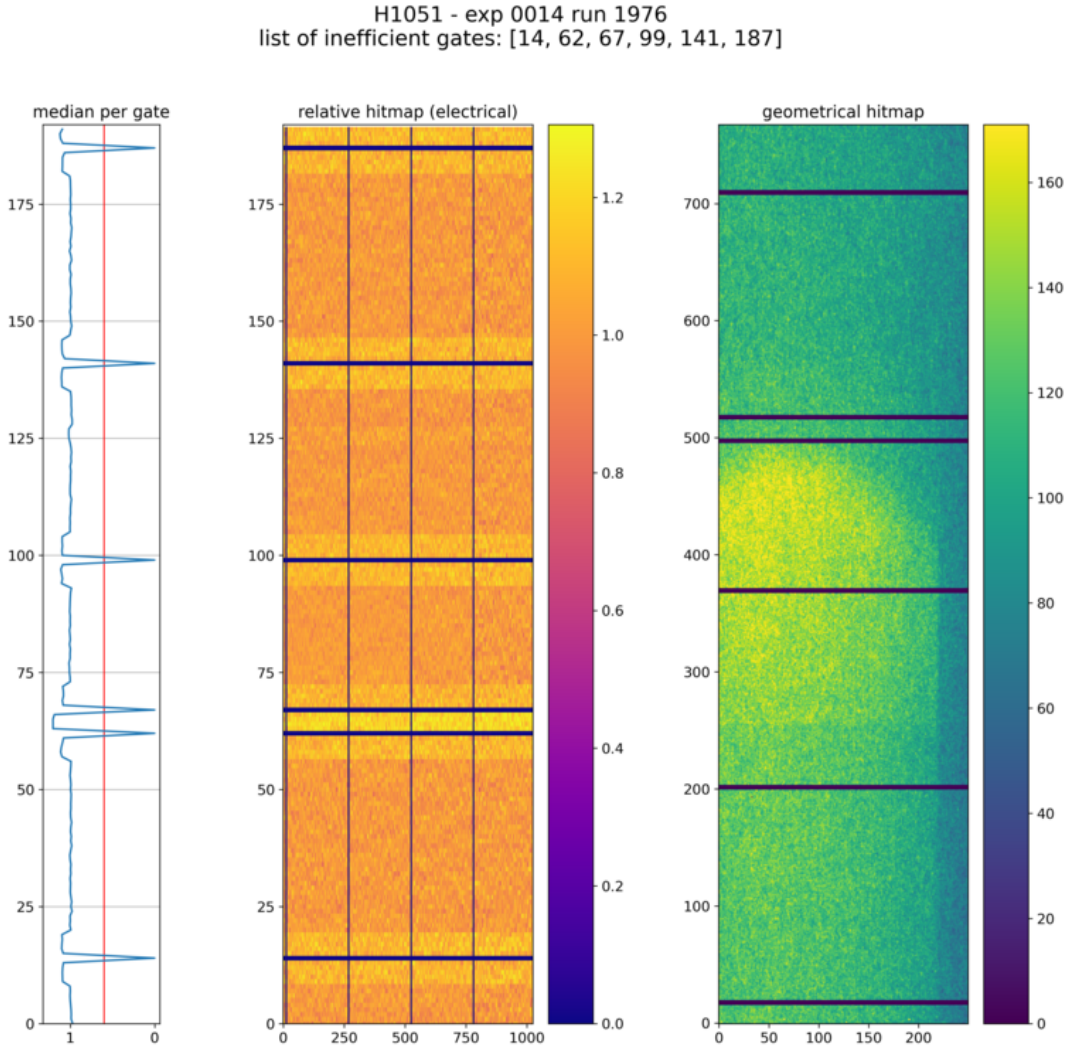


Figure 9.17.: Illustration of the "dead" gate detection algorithm using the comparison of neighboring gates for module 1.05.1 experiment 0014 run 1976. On the right the raw hitmap data is plotted in the geometrical mapping. The inefficient gates are visible as dark horizontal lines in the otherwise (inhomogeneous) illuminated matrix. In the middle the normalized pixel map is shown in the electrical mapping, therefore the order along the gates is inverted compared to the right plot. The uneven hitnumber distribution due to the synchrotron back scattering and the partial shielding from the adjacent module is leveled out. On the left side the median values per gate are depicted. For working gates the value is about 1 and for inefficient gates the value drops significantly below the threshold of 0.66 to about 0. The dead gates detected in this way are listed on top of the plots.

Correlation between hitnumber and signal value - histogram method

Despite the considerations to start with only the hitmap data an additional method to detect inefficient gates was developed. The possibilities to characterize pixels are enhanced when the signal values are also taken into account. A 2D histogram can be drawn where all pixels of an irradiated matrix enter with their hitnumbers versus their mean ADU value. According to their location within the histogram the pixels are assigned to different classes. The basic concept is illustrated in fig. 9.18.

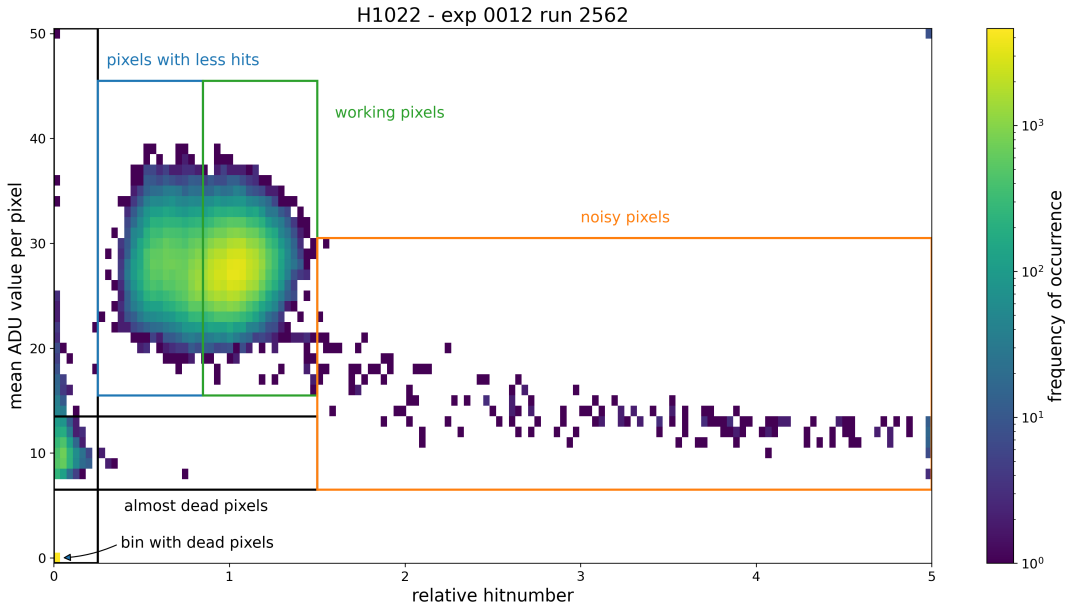


Figure 9.18.: 2D histogram of relative hitnumber vs. mean ADU value for module 1.02.2. The logarithmic color scale indicates the clustering of pixels at certain "hot spots". The histogram is cut at the upper edges of both axes and pixels with higher values are accumulated in the maximal bin. The boxes drawn on top of the distribution indicate that the pixels can be grouped into different classes.

The majority of the pixels of the well performing module 1.02.2 are concentrated in the approximately circular region around a relative hitnumber of 1 and a mean ADU value of about 30. Those are classified as "working pixels". Having a close look at their distribution a second local maximum is visible which is shifted towards lower hitnumber values. These pixels belong still to the group of well performing pixels but are assigned to a second class as their location on the matrix (shown in fig. 9.19) explains their lower hitnumbers. Pixels which never contributed a hit accumulate in the $(0, 0)$ bin and are labeled as "dead". It turns out that the inefficient gates are not exclusively composed by those "dead" pixels but contain also pixels which

report a hit occasionally. The relative hitnumber of those pixels is lower compared to working pixels and in addition their mean ADU values are lower as well, mostly just above the zero-suppression threshold of usually 7 ADU. A further class of pixels appears for increasing relative hitnumbers. Those are labeled as "noisy" pixels. They emerge from the healthy parameter space and spread over a wide range of increasing hitnumbers with decreasing mean ADU values. The bin in the upper right corner represents the eight pixels in the last gate (two for each ASIC pair) which are configured to give a hit in each frame. This is done to avoid an unwanted state in the DHPs which can lead to data losses. Table 9.2 gives an overview of the defined pixel classes.

Table 9.2.: Pixel classes corresponding to the regions defined in the relative hitnumber vs. mean ADU histogram.

class	label	description
0	not classified	pixels which are outside the defined regions
1	working pixels	pixels with good performance
2	working, but less hits	still good parameter range but less hits
3	inefficient pixels	"dead" and "almost dead" pixels
4	noisy pixels	increased hitnumbers indicate noise contribution
-	DHP timing bug pixels	eight pixels in the last gate which fire each event

The boundaries of the individual regions or classes were set manually on basis of empirical analysis of all installed PXD modules for different runs with various conditions. Further study should be carried out to evaluate the feasibility of a classification based on machine learning algorithms, possibly by also taking additional information into account, like the pedestal data.

After identifying the different groups of pixels it is possible to visualize their location on the DEPFET matrix. This is shown in fig. 9.19 where the geometrical mapping is used for easier identification of geometrical patterns.

Only a few pixels lie outside the defined regions and end up in class 0. The majority of the pixels are classified as working pixels and assigned to class 1. The pixels with slightly lower hitnumbers are found along the right edge of the matrix. This is already visible in the hitmap and originates from the shadow which the adjacent module is casting onto the matrix. The location of the shadow is represented by the pixels of class 2. The five inefficient gates are correctly identified by the pixels of class 3. The small number of noisy pixels in class 4 belongs mostly to one gate.

For the definition of the regions of the classes it is crucial that the hitnumbers become independent from all the factors listed in table 9.1 except the inhomogeneity

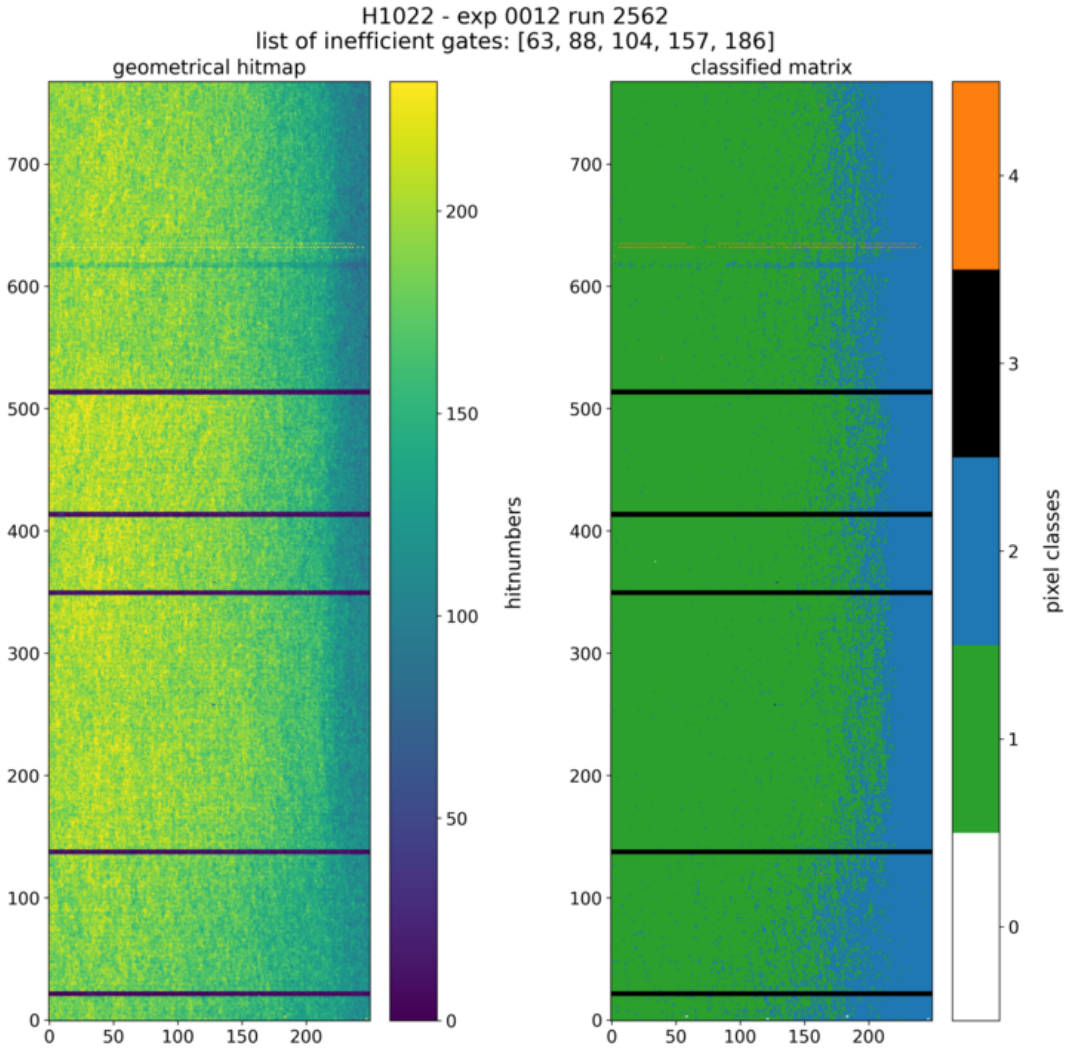


Figure 9.19.: Hitmap of module 1.02.2 next to a map of classified pixels according to their location in a 2D histogram of relative hitnumber vs. mean ADU value. The pixels in the working parameter range but with less hitnumbers are collected in class 2. Their position on the matrix corresponds to the location of the shadow from the adjacent module. The five inefficient gates which are visible in the hitmap are correctly identified by the pixels of class 3 and listed on top of the plots: gates 63, 88, 104, 157, 186.

within the matrix, which will be represented by the shape of the pixel distribution in the histogram. Therefore, two methods were used to achieve the normalization of the hitnumbers. The first method simply sets the occupancy of individual pixels in relation to the occupancy of the matrix during the complete measurement. The second method tries to find the accumulation of well performing pixels in the ADU-hitnumber plain and sets the hitnumbers in relation to those. The second method is more robust against a large number of noisy pixels and therefore set as standard, but requires a larger data set for proper fitting. If it fails, the first method is used as backup.

For the first method the occupancy of a single pixel is defined as its accumulated hitnumber $hitnr_{i,j}$ over the number of all analyzed events n_{events}. The occupancy of the entire matrix is the sum of the hitnumbers of all pixels divided by the number of all analyzed events and the number of all pixels n_{pixels}. Again index i denotes the gate, index j the drain line.

$$occ_{pix\ i,j} = \frac{hitnr_{i,j}}{n_{events}} \qquad occ_{mat} = \frac{\sum_{i,j} hitnr_{i,j}}{n_{events} \cdot n_{pixels}} \tag{9.3}$$

$$\frac{occ_{pix\ i,j}}{occ_{mat}} = \frac{hitnr_{i,j} \cdot n_{pixels}}{\sum_{i,j} hitnr_{i,j}} \tag{9.4}$$

The ratio between occ_{pix} and occ_{mat} is independent of the number of events (assuming a large enough data set) and pixels with the same characteristic as the majority of the pixels end up with values around 1. As long as most of the matrix is functional and the illumination is rather homogeneous this is the spot were the working pixels are found. A large number of noisy pixels with high hitnumbers, however, will shift the spot of working pixels towards lower values. The susceptibility to this effect is reduced by clipping at the 99th percentile when summing all hitnumbers for the occ_{mat}.

The second method tries to find the exact location of the spot of "healthy" pixels by first fitting a normal distribution to the ADU values and selecting those pixels with values $\pm\sigma$ around the mean. For these selected pixels a second normal distribution is fitted to their hitnumber values ignoring values below the first and above the 99th percentile. The resulting mean value represents the center of the spot of the working pixels and all hitnumbers are then referenced to this value. A comparison of both methods for an extreme scenario with many noisy pixels is shown in fig. 9.20.

This method for the detection of inefficient gates on basis of the correlation between hitnumber and signal value is also working for modules with additional irradiation

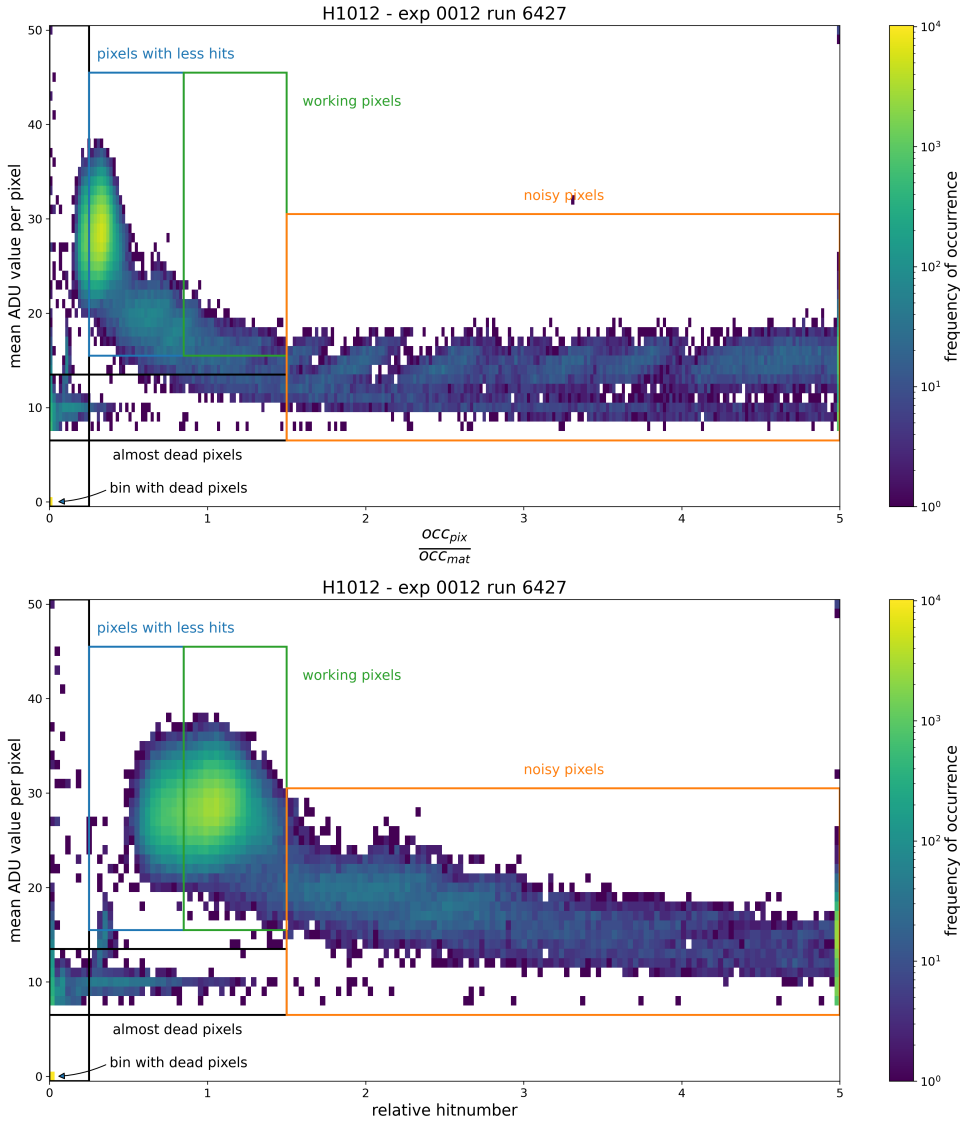


Figure 9.20.: Comparison of different normalization methods for the hitnumbers in the 2D histogram of relative hitnumber vs. mean ADU value. For the normalization to the matrix occupancy occ_{mat} the large amount of noisy pixels results in a shift of the working pixels towards lower occ values partly out of the region defined as "working". Furthermore, many pixels of the first part of the noisy band are classified as "working". As shown in the lower plot, the second method correctly detects the spot of working pixels. This results in a significantly improved assignment of the individual pixels to the different classes.

from the soft photon background. In contrast to the comparison to neighboring gates the inhomogeneous irradiation is not canceled out but represented in the shape of the pixel distribution in the 2D histogram. The pixels exposed to the additional irradiation form a subset with increased hitnumbers with simultaneously decreased signal values. An example for this situation is shown in fig. 9.22 for module 1.05.1 which is located in -x direction and therefore maximally exposed to the additional background. For the current definition of the classification regions the distribution of well performing pixels expands into the "noisy" region, but this has no effect on the initial goal to detect inefficient gates. In addition, this example shows the enhanced discrimination ability of this method. By also taking the information of the signal values into account the distribution of "almost dead" pixels, which reaches hitnumber values associated with working pixels, can be separated due to their lower mean ADU values, typically below 14 ADU.

Finally, the gates of a module are rated by the amount of inefficient pixels they contain. If a gate is affected due to a damage in the Switcher ASIC it always affects all pixels of this gate. Therefore, the method of "comparison to neighboring gates" looks at a combined feature of the entire gate, namely the median over all pixel values. For this method, however, the classification was already done on basis of individual pixels. Thus, the status of a gate can be defined by simply counting the amount of pixels of the different classes. In principle this would be possible for the previous method as well although there are only two classes. As criterion for an "inefficient" gate the limit is set to more than 80 % "dead" pixels in that gate which translates to at least 820 "dead" pixels for a PXD9 module with 1024 pixels per gate including the not connected DCD inputs. The number of dead pixels per gate for the 3648 gates of all 19 modules is shown in fig. 9.21.

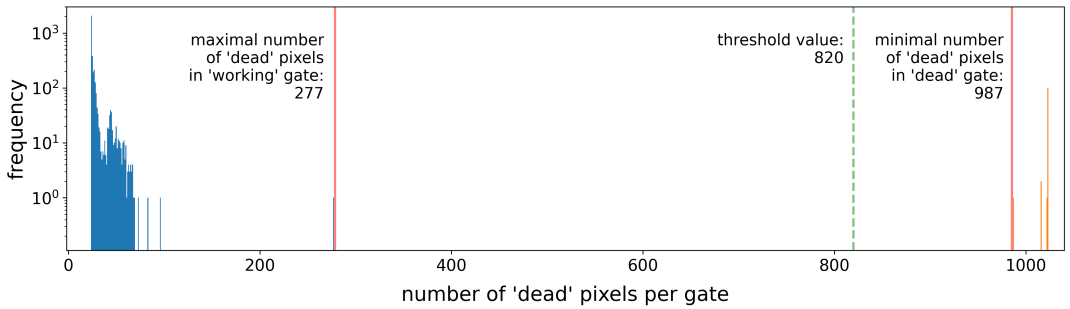


Figure 9.21.: Dead pixels per gate for all modules in exp 0014 run 1205. The distribution of "working" gates starts at a value of 24 as the not connected DCD inputs are not removed. There is only one outlier of the "working" gates above 100 "dead" pixels. The threshold value of 80 % is indicated by the dashed green line.

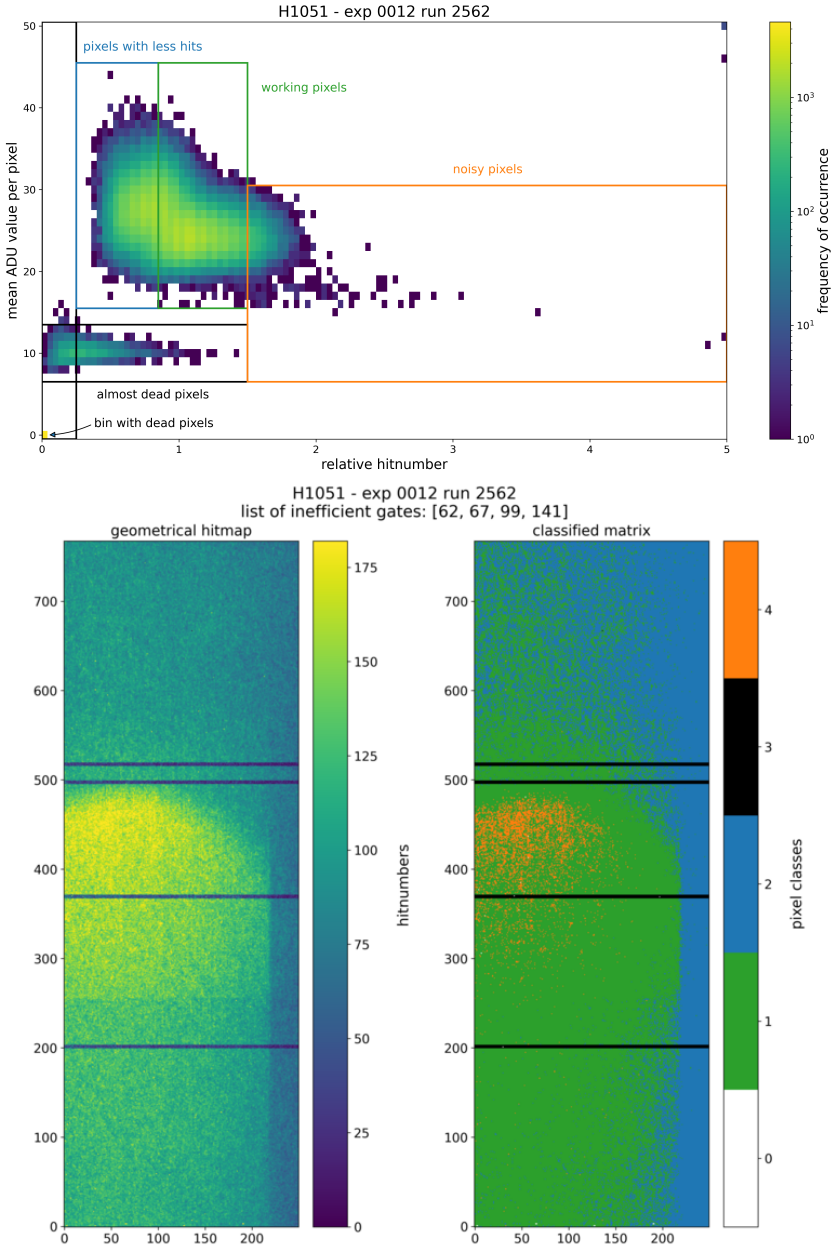


Figure 9.22.: 2D histogram of relative hitnumber vs. mean ADU value and classified hitmap for module 1.05.1 with additional soft photon irradiation. The pixels exposed to the additional irradiation form a subset with a distribution in the 2D histogram shifted to higher hitnumbers but lower ADU values. The separate group of "almost dead" pixels is classified reliably due to their lower ADU values.

The advantage of the histogram method compared to the neighbors method is the enhanced discrimination ability between working pixels and "almost dead" pixels. Both report sometimes equal hitnumbers but they can be separated with the additional information from the signal values. Furthermore, the histogram method has a larger tolerance for noisy data and it is possible to define more than just two classes of pixels. However, a slightly larger data set is required and the calculation time takes about 10 ms longer: about 23 ms per module for the neighbors method vs. about 33 ms per module for the histogram method.

The theoretical limit for the neighbors method are n adjacent "dead" gates, whereas the histogram method should work as long as at least half of the pixels are still working. However, the practical limits are already reached earlier, which is demonstrated by the failure of an entire Switcher as shown later in the time development of inefficient gates.

Change in the pedestal values

The presented methods on basis of the hitmap data have one major limitation. To obtain the required data the matrices have to be illuminated by some kind of source. For the installed PXD modules this means one has to wait for the next run with beam. However, the downtime of the accelerator after a beam loss event depends strongly on the status of the magnets and a recovery from magnet quenches can take up to several days. During this time a statement about possible new damages in the PXD modules can only be given qualitatively on basis of changes in the current consumption, if at all.

Against this background a further possibility to detect new inefficient gates is mentioned here as well. By comparing the pedestal values before and after an incident a first impression can be obtained, as demonstrated for a test module in the laboratory (see fig. 9.23). This comparison uses raw pedestal data without offset correction and without ACMC. Especially the latter has the ability to level out differences between gates and can therefore hide this effect. The sensitive matrix was not covered during the pedestal data taking but exposed to ambient light. It is not clear which impact this has on the detection ability.

In general, pedestal values depend on multiple operational parameters. They also change over time and under external influences so that a recent pedestal scan from shortly before the incident is required as reference to compare with. There is an automated scheme of pedestal taking at each end of a run implemented for the PXD. But by default the offset corrections and ACMC are enabled and an additional step would be required to turn them off. Although the last pedestals could be several hours

old a comparison with pedestal data taken right after a beam loss incident would be conceivable. Furthermore, the results from this method are always limited to relative changes and no statement about the absolute number of inefficient gates can be made. At least the pedestal data has the advantage that a first result can be achieved faster and independently from a radiation source.

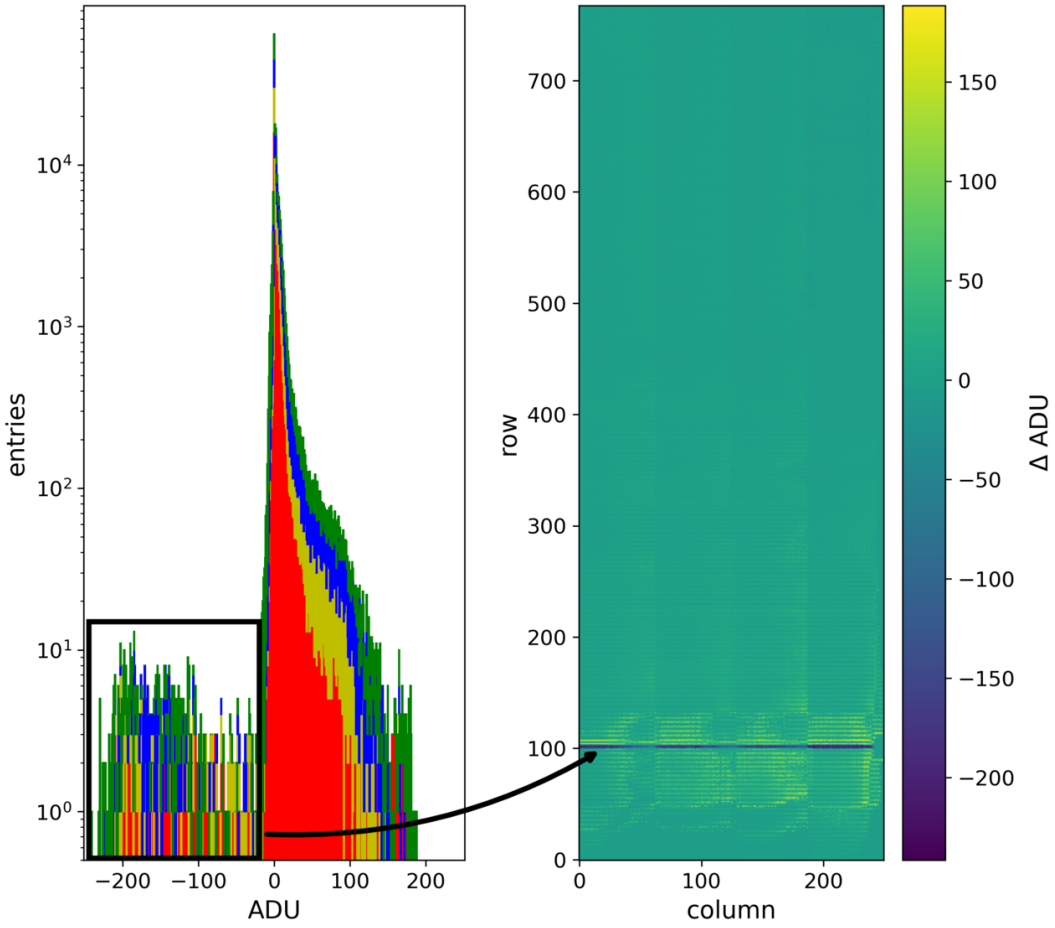


Figure 9.23.: Difference of pedestals right before and after the appearance of a new inefficient gate. The module W09_OB1 was used to investigate the emergency shutdown procedures. During those tests an increase of the clear currents was observed concurrently with the appearance of an inefficient gate. The pedestal difference indicates significantly lower values for the affected gate.

9.4.6. Implementation into the shifter GUI

Both detection methods based on the hitmap data were integrated into the software framework and into the PXD Online Monitor. The input data is provided in both cases by the PXD LocalDAQ data, which is recorded in parallel to the global Belle II data taking. The results of the "dead" gate detection within the Online Monitor are available for the PXD shifter in real time.

There is one threshold set to trigger the calculation which refers to the overall number of data frames recorded in the current run. A second threshold takes the accumulated hits per module into account to ensure a large enough data set to yield proper results. In the beginning of a new run when the calculation is triggered for the first time the second condition may not be met for all modules, as especially the modules in the outer layer have a lower occupancy. Thus, the calculation might be performed only for a subset of all modules in the first iteration, but with ongoing data taking the check for the thresholds is repeated regularly in the course of a run and with accumulating data eventually all module are analyzed.

The latest results are compared to the previously recorded ones and in case of a deviation in the number of inefficient gates the PXD shifter is notified automatically. One example for the Online Monitor OPI is shown in fig. 9.24. The four inefficient gates of module 1.01.1 are visible as horizontal dark lines in the hitmap plotted on the left. This number matches with the calculation result displayed in the lower right. For the overview of all modules an additional OPI is available which displays the currently acknowledged state as reference in red on top of the last calculation results in blue (see fig. 9.25). This information is also condensed to one indicator LED which is shown in the shifter's overview OPI and turns red when a deviation from the reference is detected.

9.4.7. Time development of inefficient gates

With the tools described above the development of inefficient gates since the start of Belle II data taking in 2019 was analyzed until the summer shutdown in 2021. Only the first LocalDAQ file of each run was used, which corresponds to the first couple of minutes after run start, assuming there are no changes in the number of inefficient gates in the course of a run. The current run is stopped when a major beam loss occurs and the subsequent data taking starts with an incremented run number.

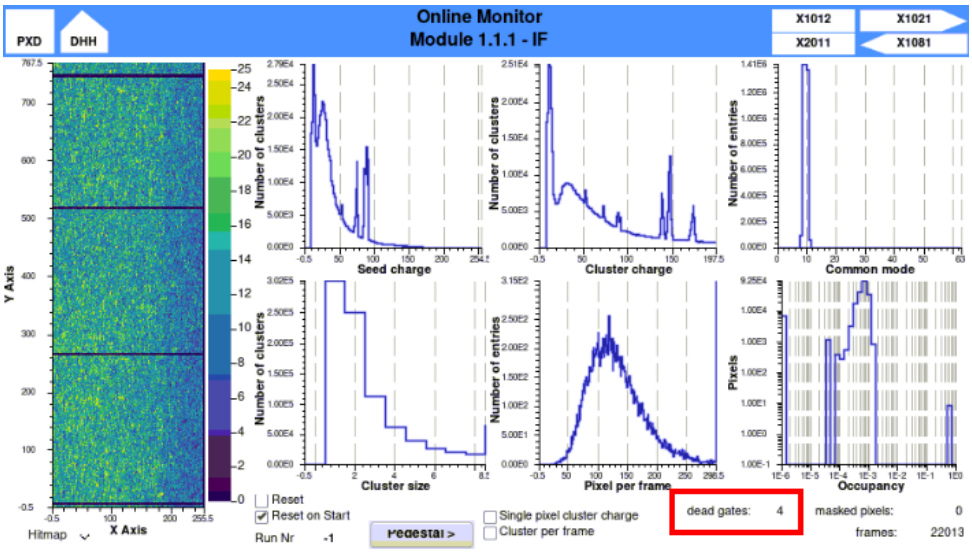


Figure 9.24.: Online Monitor OPI for module 1.01.1 with additional counter of inefficient gates. The number of "dead" gates is highlighted with a red frame in this depiction. The four inefficient gates are also visible in the live hitmap displayed on the left as dark horizontal lines.

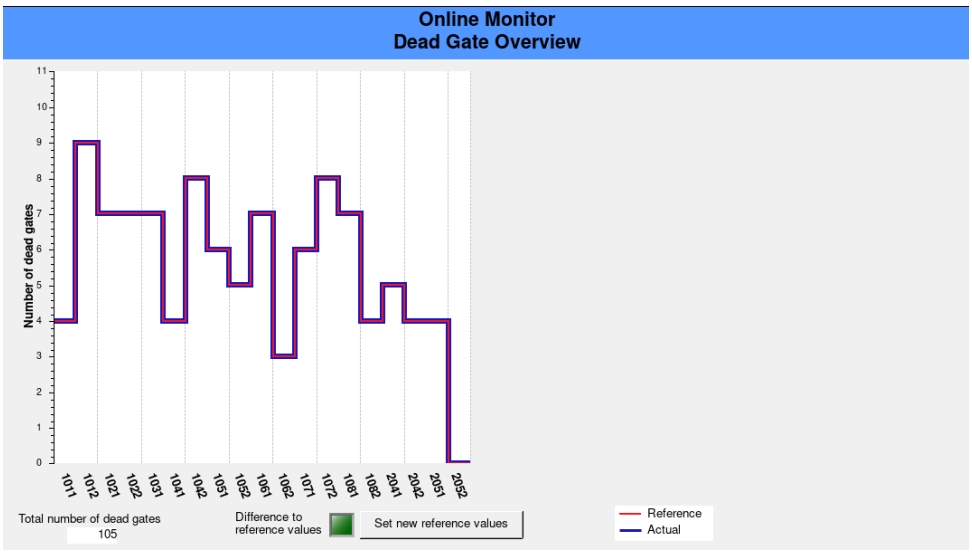


Figure 9.25.: Online Monitor OPI with "dead" gate overview. All modules are listed on the horizontal axis. The values from the last online calculation ("Actual" in blue) are compared to the last acknowledged state ("Reference" in red). All inefficient gates are summed up and the total number is displayed in the lower left as well.

The following criteria were applied to filter the data set in a first step. Only "physics" runs are taken into account where the radiation produced by the beams ensures a large enough occupancy for a reliable "dead" gate detection. Runs with less than 16 active PXD modules are omitted as well as runs with very noisy conditions within the PXD which yield wrong results. In the beginning of Phase 3 the last gate of each module was deliberately masked to avoid an timing issue in the DHP (until experiment 8 run 829). These masked gates are also found as "dead" by the detection algorithms but are removed in the counting. A data set of more than 8 TB of LocalDAQ files for the remaining 3729 runs entered in this analysis. The results show several sharp jumps in the total number of inefficient gates which precisely coincide with four major beam loss events indicated by red arrows in fig. 9.26.

The initial number of inefficient gates is larger than zero. Before the start of Phase 3 four modules had already two to four inefficient gates (13 inefficient gates in total) which were already detected during the module characterization (see section 7.5.1). These were not caused by irradiation but by an accident during operation in the laboratory resulting in harmful voltage conditions for the Switchers as described later in section 9.4.9.

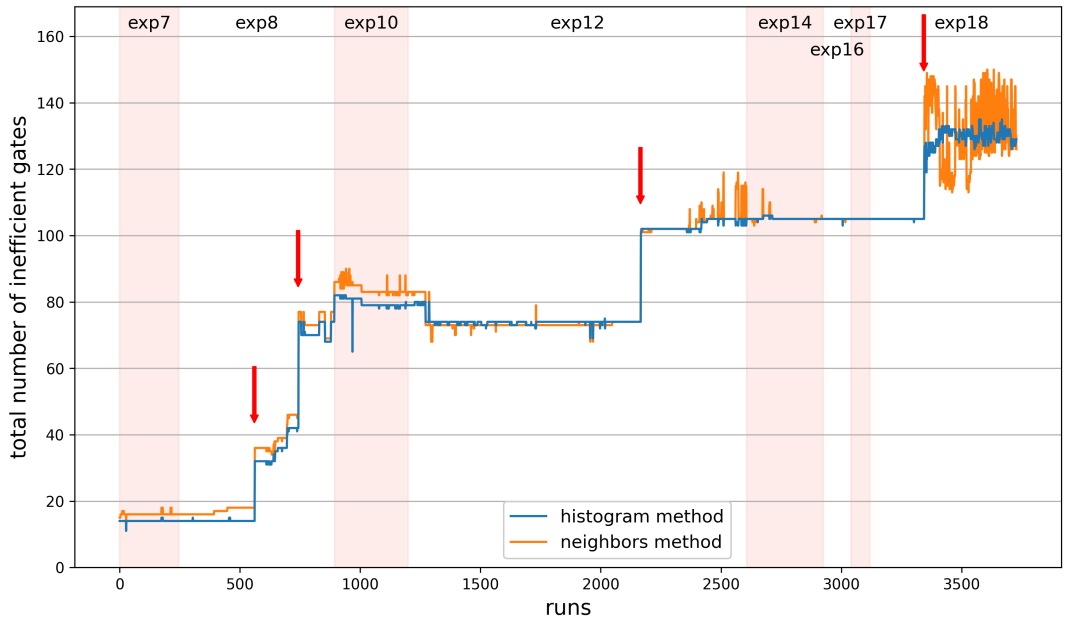


Figure 9.26.: Development of dead gates since the start of Phase 3. For each of the selected runs the total number of inefficient gates is calculated with the histogram and the neighbors method. The four major beam loss events during Phase 3 operation, which coincide with the largest increases of inefficient gates, are marked with red arrows. The different experiment numbers are indicated by alternating background colors.

After the first and second beam loss incident the modules 1.07.1 and 1.08.1, respectively, were not operational for some time due to increased currents in the clear lines. When data from these modules was recorded again - after a new configuration of their power settings - the "dead" gate detection method takes their results again into account and a jump in the number of inefficient gates occurs some time after the related beam loss event.

In experiment 10 and beginning of experiment 12 noisy gates or parts of a noisy gate were deliberately masked during data taking to decrease the module specific occupancy. These gates did not accumulate hits and therefore they appear as inefficient in the analysis. The information which gates were masked at which run was not documented and a distinction between inefficient gates and masked gates is hardly possible afterwards. Therefore, the masked gates contribute as inefficient gates in the results. This practice of actively masking (partial) gates was stopped in the beginning of experiment 12, hence, the number of total inefficient gates decreases at this point again.

In the end of experiment 12 the results especially from the histogram method became unstable. Adjusted thresholds for the "dead" gate detection algorithm and a higher noise tolerance (see fig. 9.20) yielded stable values again.

The last analyzed incident happened in experiment 18 and mainly damaged the inner module 1.03.1 and its flanking module in the outer layer 2.04.1. In the inner module the entire last Switcher failed. The detection algorithms are not optimized for the failure of an entire Switcher and gates with large noise influence the results as well, as it is the case in module 2.04.1 after the incident. Therefore, the results from the detection algorithms fluctuated strongly and the Online Monitor issued false alarms to the PXD shifter. This issue was resolved by introducing a mask specifying the affected regions for the online calculation. All masked gates count as inefficient gates (not represented in fig. 9.26).

The four largest increases in the total number of inefficient gates are exactly correlated with the most severe beam loss incidents during SuperKEKB operation reported by the Diamond System group [200, 201, 209]. A tabular overview of these four especially critical beam loss incidents with the largest impacts on the PXD is given in table 9.3. The numbers for additional "dead" gates contain only gates which worked steadily before the corresponding incident. Negative numbers indicate gates which were classified as "dead" before but reappeared working again. When they classified as "dead" again they are not counted a second time. Some examples for this oscillating behavior are gates 157 and 190 of module 1.01.1 and gates 37 and 75 of module 1.03.1.

Table 9.3.: Overview of most severe beam loss incidents

date	28.05.2019	09.06.2019	27.05.2020	10.05.2021
time	01:32:28	22:11:06	07:47:04	14:26:22
experiment number	0008	0008	0012	0018
run number	1419	2281	4941	1008
additional "dead" gates	23	40 -1	23 -1	9 +31[‡] -5
development until next major incident	+2	+2 -5	+3	+2[§]
modules with increased clear currents	8	15	5	8
modules with triggered OVP	9	19	16	17
modules with additional "dead" gates	8	15	13	6
DCU	in saturation, abort after 110 µs	0.025 Gy in 40 µs	HER abort not recorded	0.012 Gy in 30 µs
estimated dose in PXD[¶]	> 0.006 Gy	0.19 Gy	-	0.09 Gy

In the runs between the major incidents only nine gates changed their classification status. This was probably caused by less severe beam loss incidents or by different operational settings for the individual module.

The relation between increased clear currents and additional "dead" gates was already described in section 9.4.4. This effect was observed in the first two incidents where the number of modules with increased clear currents corresponds to the number of modules with additional "dead" gates. Later this correlation is no longer visible as modules which were already affected behave differently:

- additional "dead" gates without a change in the currents,
- current increase or current decrease without additional "dead" gates and
- additional "dead" gates with current increase or current decrease occurred.

[‡]Entire switcher 5 of module 1.03.1 was affected, 32 gates minus one which was "dead" already before.

[§]In the last case the change was not until the next major incident but only until the end of the analyzed data set including experiment 18.

[¶]For the estimated dose in the PXD a scaling factor of 7.5 is used on the DCU value [96, 210].

The current consumption in the clear lines can vary in both directions by more than 100 mA after an incident. The same is true for the observed correlation with the triggered OVP. It only holds for modules which were not affected so far.

The integrated dose per incident is taken from the DCU [200, 201, 209]. In addition, the archived data of the diamond sensors from the corresponding EPICS PVs was used which log the dose rate in mrad s^{-1}. A rough fit to the archived values to estimate the integrated dose matches with the reported values. An additional conversion factor of 7.5 times the DCU values was used to estimate the integrated dose in the PXD [96, 210]. However, only for two incidents a reliable measurement from the DCU is available for the reasons given in section 9.4.3.

In summary, at the end of experiment 18, after more than two years of operation, 146 gates of the PXD are inefficient. Two more gates were also inefficient for some time but were currently back into working state. This results in a total inefficient region of the PXD's sensitive area of 4.00 % due to inefficient gates. Out of the total number 13 gates were damaged during operation in the laboratory and were inefficient already at the start of Phase 3. The majority of failing gates during the operation at SuperKEKB, 126 inefficient gates, can be directly attributed to four major beam loss incidents. In total 135 gates were damaged during the operation in Phase 3 corresponding to 3.71 % of the initial sensitive area of the PXD.

9.4.8. Investigations on damage mechanism

For the investigation of the damage mechanism it is necessary to have a close look at the damage pattern. Taking the latest state after experiment 18, the histogram of all 146 inefficient gates across all modules reveals an anisotropic distribution and a few maxima are found in fig. 9.27. Certain gate numbers are more often affected than others. The total number of 192 gates per module can be divided by the number of six Switchers which are placed along the DEPFET matrix on each module. All Switcher ASICs are of the same type and support 32 gate lines each. The corresponding regions are indicated by alternating background colors in fig. 9.27 and it appears that the most frequently affected gate numbers occur towards the end of the switcher regions.

The histogram of the inefficient gates over the 32 Switcher channels in fig. 9.28 confirms this observation. The last fourth of the switcher channels contains almost half of all inefficient gates, whereby the last two channels peak with values twice as high as for any other channel. This result indicates that the last Switcher channels are most vulnerable to high radiation bursts.

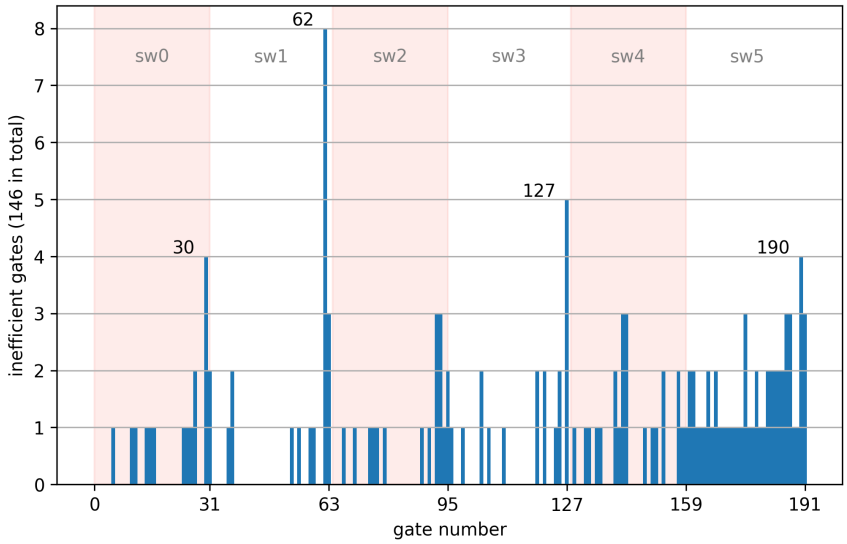


Figure 9.27.: Histogram of all inefficient PXD gates after experiment 18. The division into six different Switchers with 32 gates each is valid for all modules and is indicated by alternating background colors. The sequence of the Switchers is defined by the readout direction. The four most frequent gate numbers are 62, 127, 30 and 190.

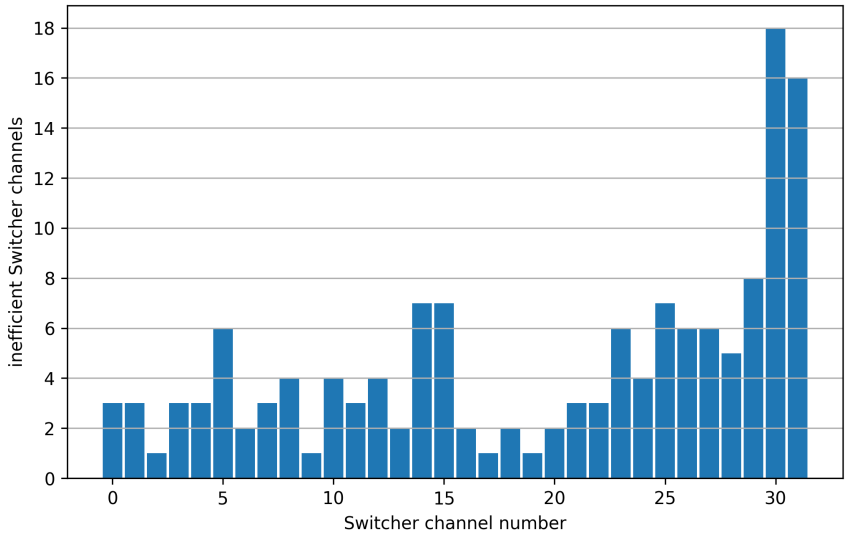


Figure 9.28.: Histogram of accumulated inefficient Switcher channels. The 192 gates of a DEPFET matrix spread over six Switchers with 32 channels each. An inefficient gate is more than twice as likely to appear in one of the last two gates compared to the other gates.

The effect is almost independent from the location of the Switcher ASIC on the module. After the latest incident the entire last Switcher of module 1.03.1 was affected. When this exceptional contribution is subtracted only a minor excess in the last two Switchers remains (see fig. 9.29).

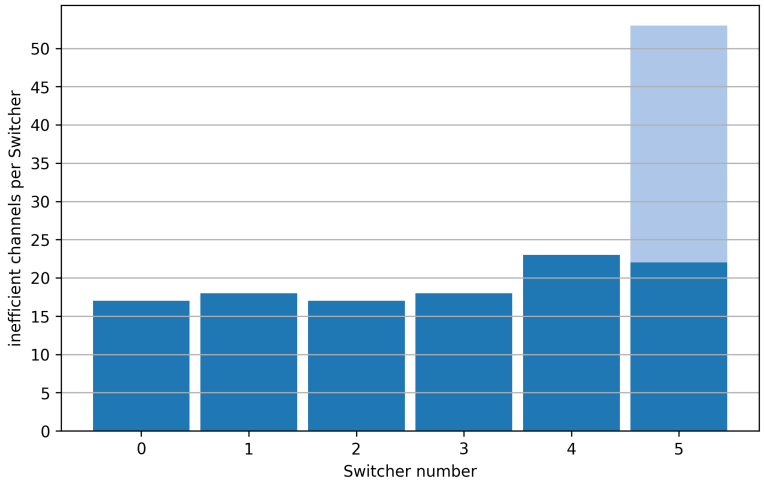


Figure 9.29.: Histogram of inefficient gates per Switcher. After the incident in experiment 18 the entire last Switcher of module 1.03.1 was affected. Therefore, module 1.03.1 alone contributes with 32 inefficient gates to Switcher number 5 (indicated by a lighter color). Otherwise there is only a minor excess in the last two Switchers.

While there is no significant difference in the distribution of affected gate numbers between forward and backward modules, there are 13 more inefficient gates in the forward modules (see fig. 9.30) corresponding to a plus of about 25 %. It appears that the higher energetic electron beam poses a larger risk for the PXD, i.e. in particular to the Switcher ASICs, to cause this kind of radiation damage. However, a critical location along the beam pipe does not appear when the affected Switchers are lined up according to their position in the PXD (see again fig. 9.30).

Although several studies were performed about the radiation hardness of DEPFET structures and of the ASICs used for the PXD [96, 112, 190, 211–213], the described damage pattern of failing Switcher gates after high irradiation burst was not observed before. This can be explained by the different conditions at the experiment and during the irradiation campaigns. Irradiation tests try to reach integrated doses expected for several years of operation within limited time and therefore use large dose rates. But usually the test devices are irradiated with a constant rate still orders of magnitude lower than what was observed at the IP during beam loss events. Large doses of up to 0.19 Gy within 40 µs uncovered a weak point in the Switcher ASIC which in turn resulted in failing of individual gate lines up to the failure of an entire Switcher.

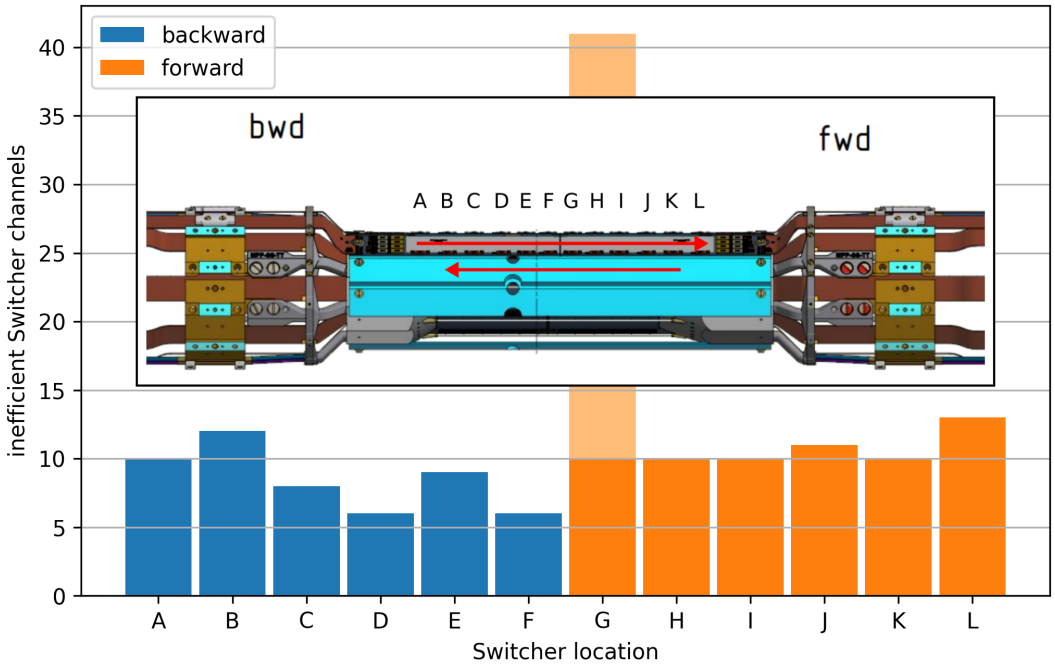


Figure 9.30.: Histogram of inefficient gates per Switcher location. In the forward modules 13 more dead gates are found compared to the backward modules representing a clear effect of 25 %. Whereas a slight preference for the outer locations can only be suspected. The assignment to the Switcher locations has to consider the four different layouts of the PXD modules and the different read-out directions between the two layers (indicated by red arrows). For simplicity it is assumed that the corresponding Switcher locations of inner and outer modules are identical in z. After the incident in experiment 18 the entire last Switcher of module 1.03.1 was affected. Therefore, module 1.03.1 alone contributes with 32 inefficient gates to Switcher location G (indicated by a lighter color).

For a better understanding of the damage mechanism dedicated irradiation campaigns were performed at the Mainz Microtron (MAMI) irradiation facility[6]. Hybrid5 systems served as device under test. They feature all system components required to readout a small DEPFET matrix (16 x 64 pixels), but only one of each ASIC type is present. Instead of an all-silicon structure the components are placed on PCBs and wire bond adapters, hence the name hybrid. Several Hybrid5 systems were used to irradiate Switcher ASICs in a working DEPFET setup with a pulsed electron beam. Integrated doses between 5 Gy and 50 Gy per 40 µs pulse were achieved [214–216]. The described damage of failing Switcher gates was successfully reproduced [208].

The Hybrid5 boards were placed so that the electron pencil beam reached a FWHM of about 1 mm when hitting the Switcher. The area of the Switcher was scanned so that the beam hit the Switcher at different positions to identify weak points in the ASIC (see fig. 9.31). First results could pin down the vulnerable part to be the regulators for the clear and gate voltages and showed that the Switcher is less susceptible when turned off during irradiation [208]. It is suspected that the high irradiation bursts create latch-ups in the semiconductor structures which shorten supply lines and are especially critical for the lines providing the highest voltages, e.g. clear and gate lines. However, the damage mechanism is still not entirely understood and further investigation with irradiation tests is ongoing.

9.4.9. Additional protection measures

The especially harmful beam loss events and the resulting damages in the detectors and accelerator structures gave rise to a discussion about improvements of the beam abort system and the detector shutdown procedure. Measures were taken on all systems contributing to the abort chain to speed up the required actions and to protect the infrastructure and detectors more efficiently.

Two of the measures taken on the accelerator side resulted in a combined reduction of the delay for the beam abort of about 10 µs which corresponds to one revolution cycle of the beam in the storage ring [203]:

- The SuperKEKB group introduced a second abort gap in the bunches train. So far there was only one gap between the stored bunches which allowed an abort only once per turn. With the second gap the beams can be aborted now twice as often which reduces the abort delay by up to 5 µs.

[6] The author did not participate in these irradiation campaigns. The results are presented here for the sake of completeness of the topic.

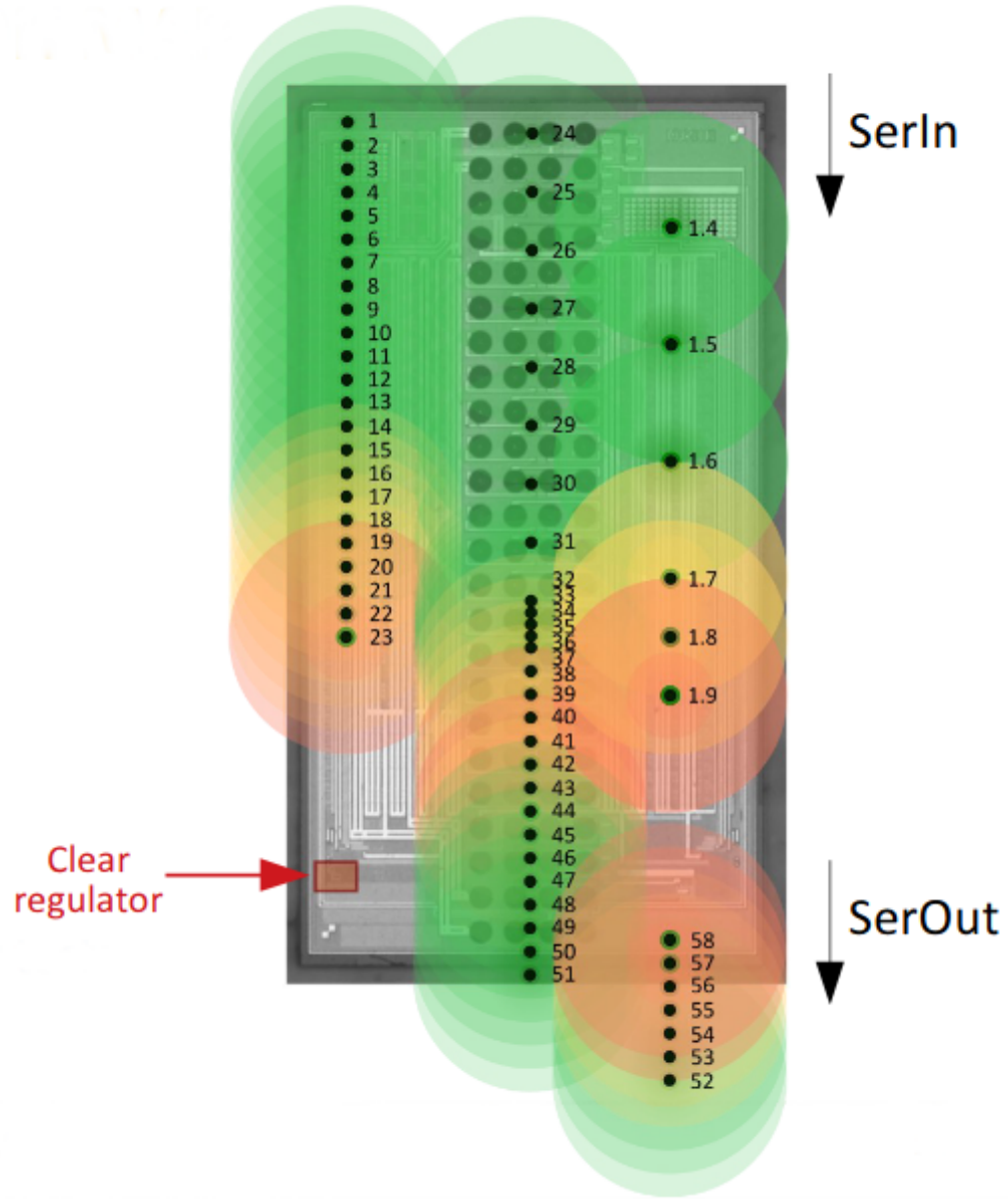


Figure 9.31.: Irradiation map during MAMI irradiation [214]. Each point marks an irradiation burst, the circle size indicates the estimated full width at half maximum of the electron beam. Green color indicates no damage introduced by the irradiation. Yellow stands for non-permanent damage. Red highlights the positions where permanent damage was introduced and therefore the vulnerable spots of the Switcher ASIC are located.

- A former fixed delay of 4.2 µs for the LER (2.8 µs for the HER) in the abort chain to synchronize to the abort gap could be removed completely.

- An additional collimator was installed in spring 2020 for a better control of beam conditions at the IP. In total SuperKEKB utilizes now 30 collimators [201].

The following improvements of the radiation monitor system increased the safety of the detector environment:

- The threshold values and integration parameters of the DCU system were repeatedly revised and optimized for the potentially harmful situations.

- With Scintillator Light and Waveform Sensors (CLAWS) a further system was added to the beam abort monitoring which was already used in Phase 2 for monitoring beam background arising from injections of new particle bunches [194]. With sub-nanosecond time resolution it can relate the measured particle rates to individual bunches. CLAWS was adjusted and new sensors were placed so that the system provides additional input for the beam abort decision. The installation and integration was successfully realized in 2021 and CLAWS already demonstrated its potential by detecting radiation bursts up to 10 µs (4.4 µs on average) faster than the DCU system [217, 218].

The detector safety system of the PXD was also reviewed. The presumed latch-up effects inside the Switcher ASICs cause short circuits and will stay active even after the radiation burst is over [219]. Only a fast shutdown stops the parasitic currents and prevents further damages due to overcurrent. Therefore, the following improvements to speed up the shutdown of the PXD were realized:

- The PLC's response time of the VLHI with up to 8 ms is sufficient for the environmental monitoring of temperature changes and water leaks [220], but it is not fast enough to protect the PXD against spontaneous radiation bursts. Therefore, a new interlock box was installed in November 2019, featuring an additional interlock input directly from the DCU to the power supplies of the PXD. This signal bypasses the VLHI system and reduces the processing of the shutdown signal by three orders of magnitude [221].

- The shutdown process of the power supply itself was sped up by 250 µs by removing internal delays. The required modifications on the microcontroller cards were performed in the summer shutdown in 2020 [222].

In addition, the option of an active pull down of the supply voltages was discussed to further speed up the shutdown process. The initial implementation of the emergency

shutdown simply switches the output stages of the regulators into a high impedance state. The remaining charges spread across the module until the discharge is complete. While this established procedure will be kept for interlock signals concerning the relatively slow environmental monitoring, additional transistors should be activated by an input signal from the radiation monitor system. They open a low ohmic path for the currents from the force lines of the supply voltages directly to the corresponding ground lines; basically provoking a short (see fig. 9.32). The currents need to be limited by small safety resistors adjusted for each line to prevent damages to the electronics like electromigration. These considerations gained even more in importance as one result from the irradiation campaigns showed that the current implementation of the emergency shutdown (even with delays removed) is not fast enough to protect the Switcher ASICs even when the shutdown is triggered already 10 µs before the radiation burst arrives [208].

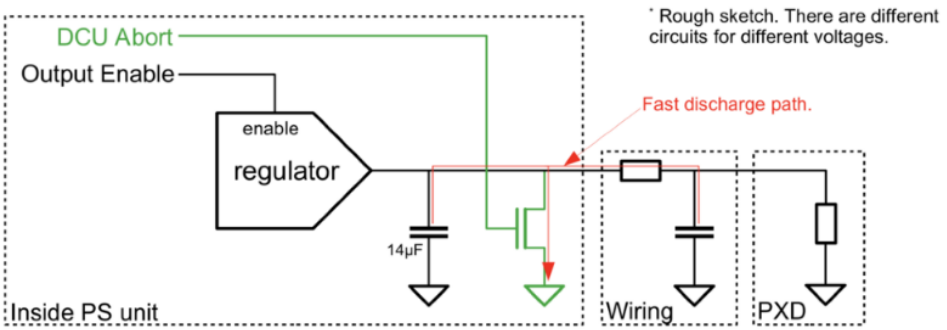


Figure 9.32.: Sketch of active emergency shutdown for PXD power supplies [223]. The initial implementation is drawn in black, the proposed additional part in green. The proposed path for the discharge current is drawn in red.

We designed and produced a prototype PCB which provides the proposed circuitry as an adapter board; no change of the power supply was required at this stage. The board was integrated into an existing testing setup by simply inserting it into the power supply cables which connect the power supply outputs to the setup (see fig. 9.33).

The functionality of the prototype board was verified in the laboratory with the successful operation of a PXD9 module. The active emergency shutdown was repeated more than 20 000 times without noticeable harm to the module or any other system component. The prototype circuitry was subsequently integrated to the existing design of the power supply front PCB by colleagues from ZITI in Heidelberg. Also this version was tested in the laboratory with a modified version of a PXD power supply. Oscilloscope measurements on the force lines show the removal of the internal delay: The processing time of the emergency shutdown trigger is decreased from over 250 µs to only about 3 µs. Almost all supply voltages show a much faster

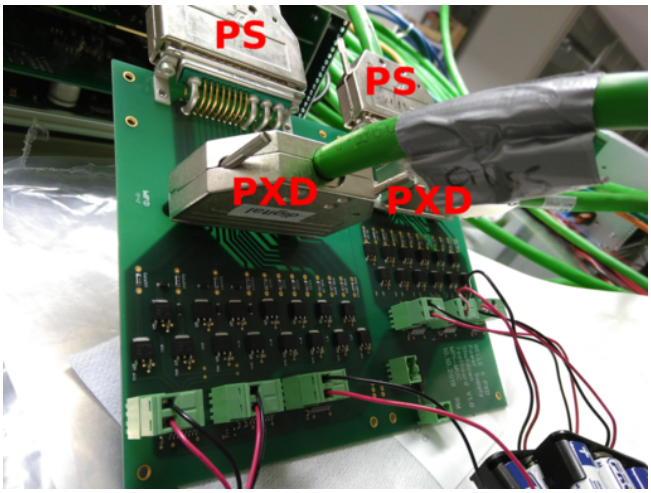


Figure 9.33.: Prototype of active emergency shutdown board. The additional circuitry is inserted into the power supply cables. The supply for the switching transistors is provided by batteries as the required internal voltages of the power supply are not available at that stage.

damping time as well (see fig. 9.34). The clear-on and sw-sub lines show the least improvement. A lower value for their current-limiting resistors would speed up the discharge.

Further measurements with adjusted resistor values and with the probe tips on the sense lines revealed two issues. The shutdown process starts with a large amplitude but swings back. In the clear-off line there are even oscillations visible (see fig. 9.35). It turns out that the simplified sketch of the circuitry in fig. 9.32 misses the impedance of the system, especially of the long power cables. The exact behavior of the currents and their paths during the discharge are hard to estimate on a complex system like a PXD module. Further studies will require a proper simulation.

The second issue concerns an introduced damage to the tested module after a change of resistor values. The pedestal difference map in fig. 9.23 reveals the appearance of a new inefficient gate during the testing of the active emergency shutdown. Potentials which are not compliant to the safety specifications for the individual lines can equally introduce damages to the Switcher ASIC even if they are applied only for a short time. This was repeatedly observed during main production testing and also once during an X-ray irradiation campaign [96, p. 142]. Before the active version of the emergency shutdown can be used, it has to be ensured that the procedure itself does not pose a thread to the system. A simulation of the circuitry will be helpful to study the compliance with the safety limits.

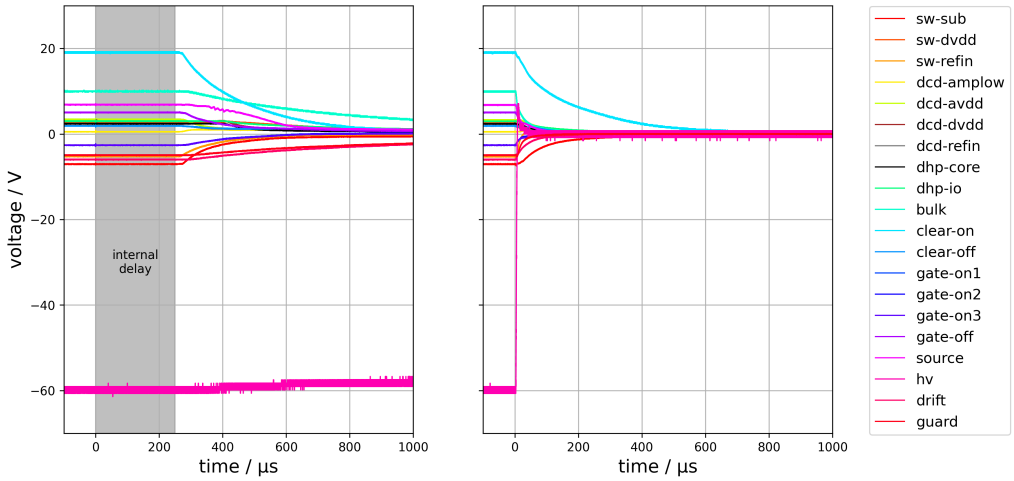


Figure 9.34.: Comparison between different implementations of the emergency shutdown. Initial implementation with delays and passive discharge (left). Situation with removed delays and active pull down (right). In both cases the force lines of the corresponding supply lines were measured at vias of the Lab-Patch-Panel.

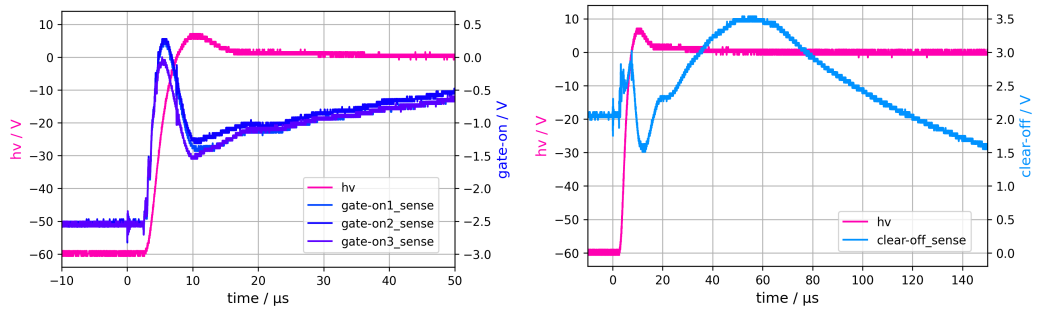


Figure 9.35.: Oscillations in the sense lines during active emergency shutdown. The force lines are actively pulled down to their ground potential at the output of the power supply. The sense lines are connected to their force line only at or close to the module and therefore show the situation on the module more precisely. The gate-on lines reach the ground potential relatively fast but swing back to about half their initial value before they approach their ground potential much slower (left). The clear-on line shows oscillations with amplitudes up to one and a half times of the initial value before it declines likewise slowly (right).

While the measurements indicate that a speed-up of the emergency shutdown in the order of several hundred microseconds is possible with an active pull-down of the voltages, not well defined potentials on the module can cause damages to the electronics. Ideally, the active pull-down should happen more closely to the module, e.g. in the Dock Boxes, where the decoupling capacitors store the electric charge and the impedance of the power cables has less effect. Unfortunately, this area is subject to very strict space constraints in the experiment and changes are not foreseen at this state of the experiment.

Finally, a modification of the Switcher ASIC to increase its radiation tolerance would ultimately solve this issue. On basis of the available analysis and irradiation campaign results the designer of the Switcher ASIC formulated a probable explanation of the damage mechanism: A transistor in the voltage regulator circuit may act as unwanted sensor. The generated transient current originating from ionizing radiation could disturb the regulator and the resulting overvoltage damages the driver. The proposed solution consists of a reduction of present resistances and the introduction of a capacitance and a clamp circuit [224]. However, the assembled ASICs on the modules of the installed PXD could not be exchanged and the Belle II experiment had to continue with the current state of the detector.

Besides the efforts to mitigate the damaging impacts on the installed detector, a long shutdown of the Belle II experiment took place in 2022 and 2023. This occasion has been used to replace the PXD. An entirely new detector version, PXD 2, completed the initial design of 40 modules in two layers. The new modules passed the same quality assurance measurements as described in section 7.4. Unfortunately, an improved version of the Switcher ASIC could not be finished before production and was not implemented. Nevertheless, the replacement will remedy all collected damages during Phase 3 and the PXD 2 will provide its best performance for Belle II for a time with higher luminosity, increased beam stability and improved safety measures.

10. Summary and Conclusion

The Pixel Vertex Detector (PXD) for the Belle II experiment, an essential detector component for high precision tests of CP violation in the B meson system, provides a very high vertex resolution in the high background rate environment of the SuperKEKB collider with a very low material budget. This is achieved by implementing DEpleted P-channel Field Effect Transistor (DEPFET) technology in a monolithic self-supporting module design. The various components of the detector, including auxiliary services, form a complex system. The smallest independently operating building unit is a PXD module.

In this thesis, a full account of the design, construction, properties, optimization and testing of the DEPFET modules, as well as the deployment of the entire PXD in the Belle II experiment, is presented. In the first part, the electromagnetic compatibility (EMC) of the PXD module design was investigated. The conducted common-mode emission was measured as well as the susceptibility to conducted differential-mode and common-mode noise with respect to the power domains and individual power lines. These measurements represent the first EMC characterization of a pixel detector for a high-energy physics experiment, including the first consideration of radiated noise from a beam pipe. The highest susceptibility was found for conducted noise in the range of 8 MHz to 20 MHz, corresponding to the gate readout rate. These measurements completed the EMC plan for the PXD and verified the robustness of the module design, which was later confirmed by the undisturbed operation of the PXD as part of the Belle II detector.

The second part of this thesis deals with the development and implementation of a module characterization procedure including quality management for the main production PXD modules. A system of mechanical and monitoring measures, documentation instructions, software quality, databases and quality control measurements was established. Quality assurance software was written for optimization algorithms to improve the PXD module performance. 75 production modules entered the standardized testing procedure for characterization and optimization and were graded according to their performance. This is the first work to address the performance of so many PXD modules. The majority of 72 % achieved the highest class A, meaning that they have more than 99 % working pixels and are best suited for use in the experiment. A first version of the PXD with a fully populated first layer and two outer ladders was as-

sembled and commissioned at the Belle II experiment in Japan.

The third part of this thesis covers the successful data taking of the PXD detector in the first run period from 2019 to 2022. The optimization of the PXD modules continued during the operation at the experiment. However, the comparison of the configuration parameter settings between the values found during the module characterization in the laboratories and the values used at the end of the physics runs in 2022 verified the validity of the optimization procedures in the laboratory. After sudden beam loss events during the operation of the SuperKEKB accelerator, broken gate lines appeared in the pixel matrices of the PXD. The damage pattern was investigated, which led to the identification of the most vulnerable part of the Switcher ASIC. An automated broken gate detection algorithm was developed and implemented in the local quality control software. Additional protection measures against high radiation bursts were implemented.

The first PXD was successfully operated at the Belle II experiment and achieved excellent performance, meeting its ambitious design goals. Its tracking data provided important contributions to physics analyses of particle lifetime measurements and CP violation. The established procedures developed in this thesis were also applied to the production of new modules. A new and fully equipped PXD 2 was assembled and installed during the 2022/23 shutdown. It will provide its superb vertexing capabilities to the Belle II experiment in the coming years of increasing luminosity, hopefully contributing to many new insights into the open questions of particle physics.

A. Module performance during EMC measurement campaign

We had to deal with several limitations of the module performance during the EMC measurement campaign. Only a fraction of the data channels aka. pixels of the DEPFET matrix could be read out due to a not working data link, an affected gate-on3 supply and 20 broken drains (see section 6.3.2). In addition, several hundred noisy pixels had to be addressed. Their distribution and development over time and the role of the CDN in this issue is discussed in this section.

It will be demonstrated that the majority of noisy pixels could be assigned to a limited number of noisy drains. Those noisy drains were masked during the data taking. The overall number of noisy pixels decreased during the measurement campaign. A significant improvement was achieved after an insufficient power supply of the DCDs, originating from current limiting components of the CDN, was detected and patched. The effect is clearly visible in the recorded voltage and current settings of the module. This issue had no effect on the susceptibility analysis of the recorded data as discussed in section 6.5.2.3.

The geometrical distribution of noisy pixels across the module's matrix is shown in fig. 6.8b. However, the stacked bar plot of noisy pixels per drain line in fig. A.1 gives a better impression of the distribution of noisy pixels over the drain lines. The occurrence of noisy pixels is accumulated at certain drains but not homogeneously distributed around them. There are several drain lines which contain the majority of the noisy pixels and can therefore be seen as noisy drains or ADCs. The histogram in fig. A.2, which shows the distribution of the number of noisy pixels per drain, confirms this picture. The noisy pixels are accumulated in a small number of about 20 noisy drains. The vast majority of more than 93 % of the analyzed drain lines do not show any noisy pixel over all the calibration runs during the measurements. Bin 0 is therefore not plotted so that the details of the distribution at higher values can be seen.

The color gradient in the two previous plots might already indicate that the amount of noisy pixels reduced over the course of the measurements. This is confirmed in fig. A.3. The total number of masked pixels is naturally higher than the number of

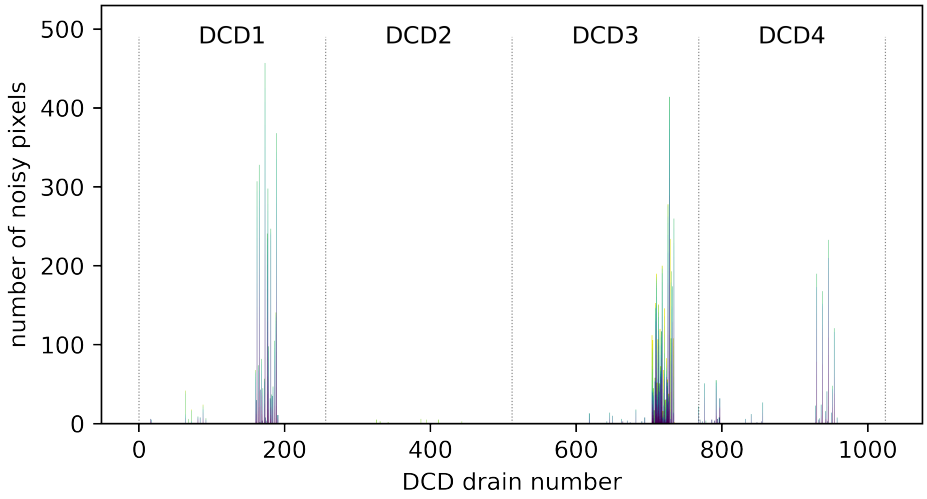


Figure A.1.: Noisy pixels per drain line stacked over all calibration runs without noise injection. The noisy pixels of a new run are placed on top of the already accumulated number for the very same drain line. The color gradient indicates the proceeding run number.

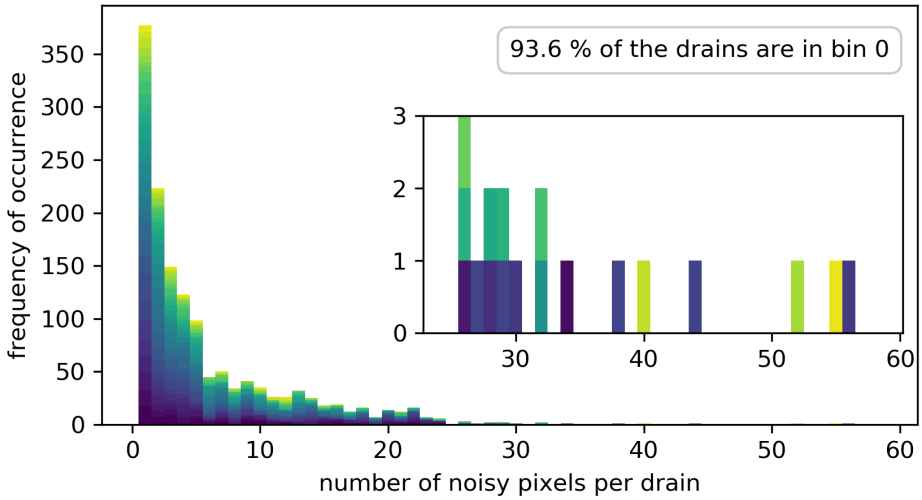


Figure A.2.: Histogram of noisy pixels per drain line over all calibration runs without noise injection. Over 93 % of the analyzed drain lines did not contain any noisy pixel. They are accumulated in bin 0, which is not plotted to allow for a scale where the details in the tail remain visible. The inset graph magnifies the rare events where more than 25 noisy pixels were seen in one drain line. The color gradient again indicates the proceeding run number.

noisy pixels as we set a limit of just more than 8 noisy pixels per drain to mask the entire 192 pixels in that drain.

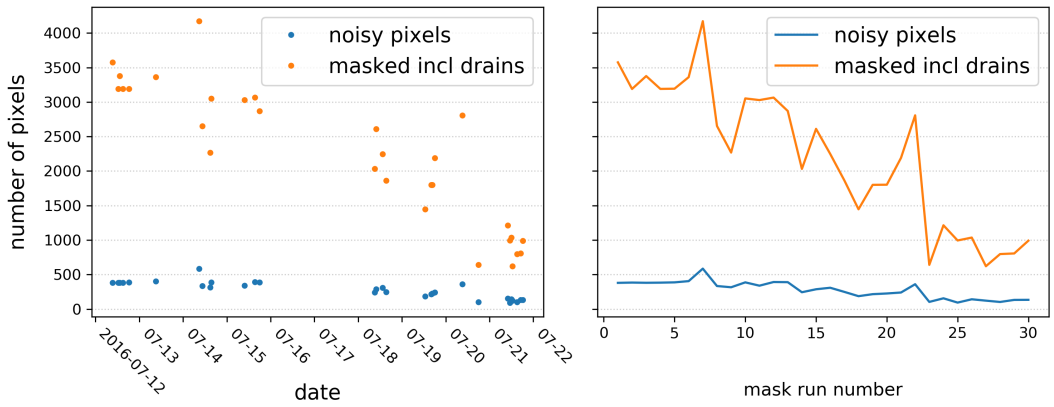


Figure A.3.: Development of the number of noisy pixels during the measurement campaign. Left: The timestamps of the recorded data files display the actual time development; no measurements were taken during night or at the weekend. Right: The ordinal number of the corresponding mask run in combination with the connection of the plotted points helps to see the step downwards between mask run number 23 and 24 in the overall decreasing tendency.

While we have no explanation for the general declining trend, the significant step towards the end of the measurement campaign can be explained by a change of the CDN configuration. As already mentioned in the setup description, the additional decoupling circuit utilized for the EMC measurements is not a standard part of the PXD system configuration. When we operated the test module with the inserted CDN, we judged the overall performance to be still the same as before. This was also true for the performance of the system at the test stand in Zaragoza where no problematic issues were obvious. The deviation of the nominal voltage in the dcd-avdd line was only detected towards the end of the measurement campaign, on the 20th of July. The nominal voltage for this line is 1.9 V but the sensed voltage at load was displayed to be only 1.5 V when the matrix was enabled. As long as the matrix voltages were switched off, the voltage was still at the nominal value. An automatic notification of the operator in a situation like this was introduced later but was not present at that time.

During the construction of the CDN we did not choose the right specifications for the maximal power and current through the resistors and inductors for those power lines carrying the most current, e.g dcd-avdd with up to 3 A. The voltage drop at those components was too high for the PXD Power Supply and it was not able to deliver the nominal voltage at load even with the maximum possible voltage at the regulator output.

As a workaround, first the dcd-avdd line was removed from the CDN bypassing the additional circuit which resulted in a voltage at load of 1.8 V. On the next day the configuration for the dcd-avdd and agnd lines was adapted to only bypass the resistor and inductor of the CDN but still was connected to the capacitor. In this way the voltage at load was back at the nominal value of 1.9 V and the induced noise currents could still take the same paths as before.

The development of the voltages and currents of the power supply lines associated to the DCDs are shown in figure A.4 over all measurements taken during the complete measurement campaign. In opposite to the analog supply line (dcd-avdd) the digital line (dcd-dvdd) and the two other DCD supply lines (dcd-refin and dcd-amplow) did not show any deviation from the set voltages nor a reaction in the voltages to the change in the CDN configuration.

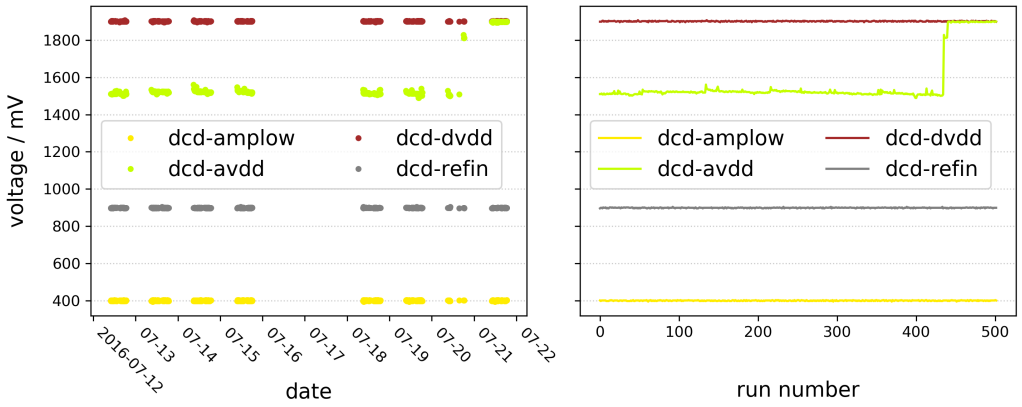


Figure A.4.: Development of voltages on the power supply lines of the DCDs. For the most time during the measurement campaign the analog supply for the DCDs did not reach the nominal voltage but was limited to about 1.5 V. Only after the change to the CDN towards the end of the measurement campaign the dcd-avdd line reached the nominal 1.9 V.

However, the adjustment of the CDN resulted in a finally unhindered current flow and the current values did change to a varying extent (see fig. A.5). Still it is save to assume that the digital configuration of the ASICs was not affected by this issue at any time as the JTAG configuration happens already during the power up and before the matrix voltages are applied. At this state all nominal voltages have been provided correctly already before the adjustment. A failure in the configuration would have also led to an undefined system state and would have been noticed in the behavior of the system and in the data taken.

In order to provide a complete picture of the development of all power lines a combined plot of all voltages and currents is shown in fig. A.6. As the absolute values cover a rather large range the plots for the voltages and currents are both split into

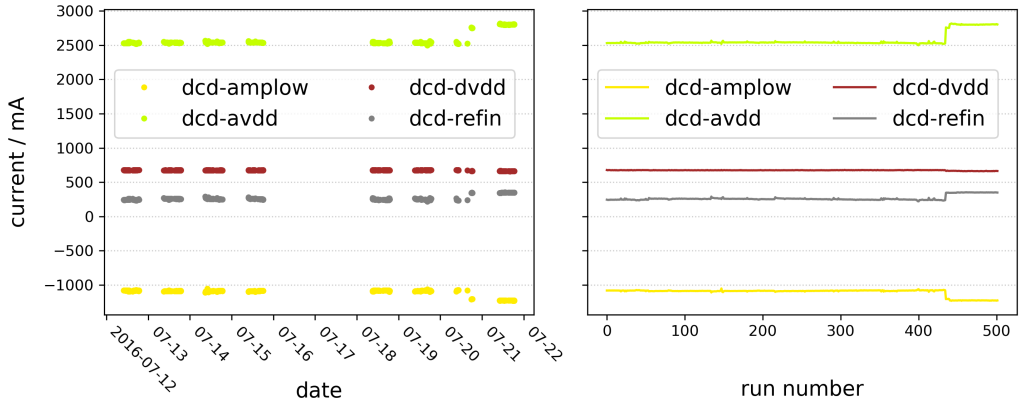


Figure A.5.: Development of currents in the power supply lines of the DCDs. The change to the CDN resulted in a current increase in the dcd-avdd, dcd-refin and dcd-amplow lines.

two individual plots with different scales. The time of particular interest when the changes in the CDN were implemented is indicated by a faint red background color. The detailed presentation of all power supply lines contains all information about the applied voltages and currents and, although the clock frequency was lower than nominal, it can be seen as reference of the standard settings which were used for the pilot production module. In this context it should also be mentioned that the sw-sub and sw-refin lines were not yet used but those lines were connected by a solder jumper on the Power Breakout Board to dgnd and sw-dvdd, respectively.

However, the relative change of the values is better visualized in fig. A.7 and fig. A.8. The voltages at load are plotted relative to the corresponding set voltage. It becomes clear that the dcd-avdd was the only power supply line which deviated from the set value. For all other lines the PXD power supply succeeded to reach the requested values.

There is no set value for the current consumption as it depends on the operation mode of the module and the current state or configuration of the ASICs. The reference for the relative currents plotted was therefore chosen to be the corresponding value from the last measurement. The dcd-refin, dcd-amplow and dcd-avdd lines show the largest deviations and a systematic offset to lower values as long as the non-optimal CDN configuration was present. Also other lines deviate for certain measurements from the reference value but they fluctuate between specific values around it. Those deviations and their magnitude are a result of the measurement accuracy of roughly 1 mA (depending on the line) of the internal current measurement of the PXD power supply. Due to this fact the lines with only a few or even 0 mA displayed current show occasionally huge relative deviations above 100 % and are not plotted. However, the significant change in the DCD supply lines is clearly visible. After the

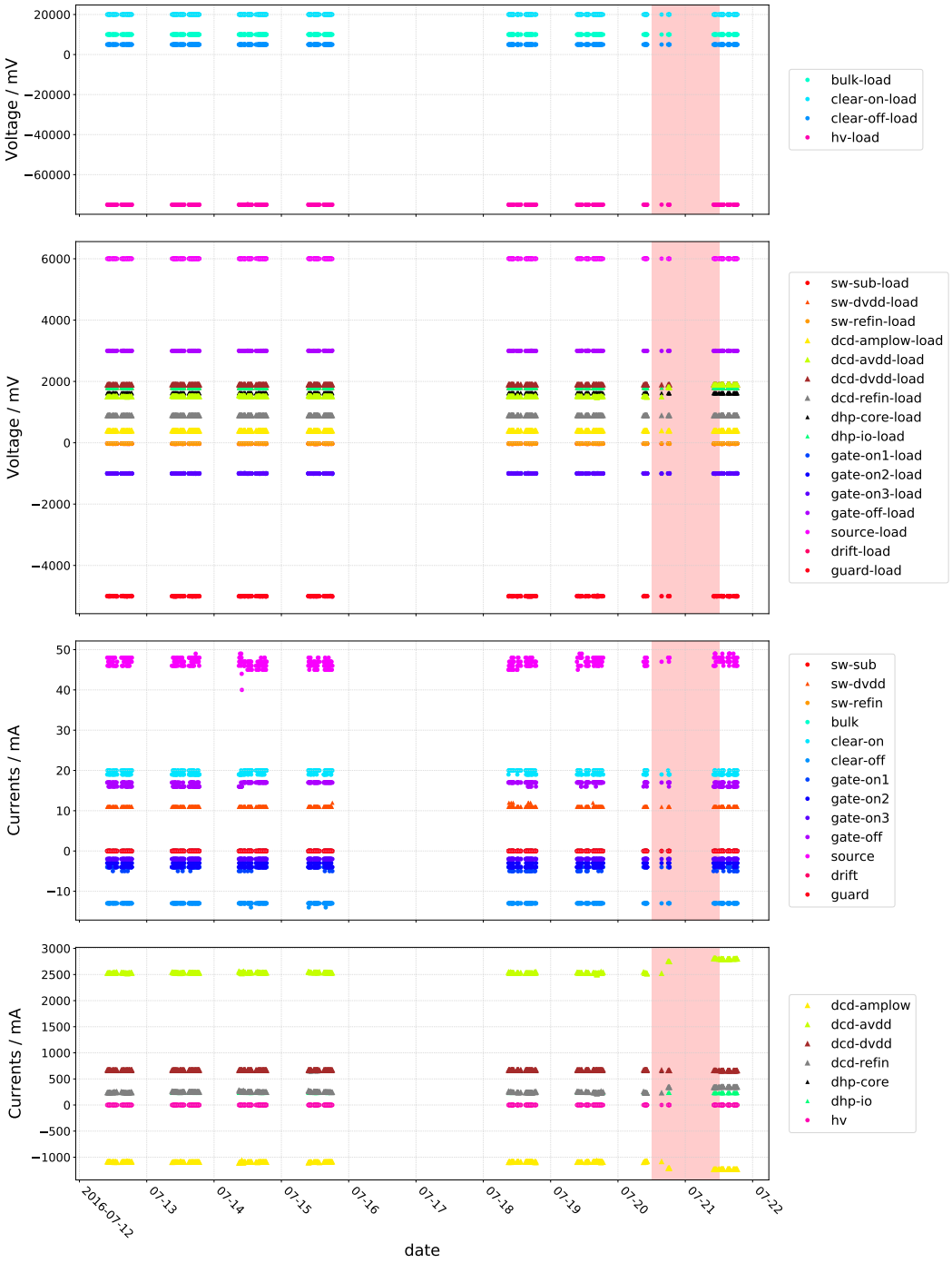


Figure A.6.: Development of all power supply lines during the EMC measurement campaign.

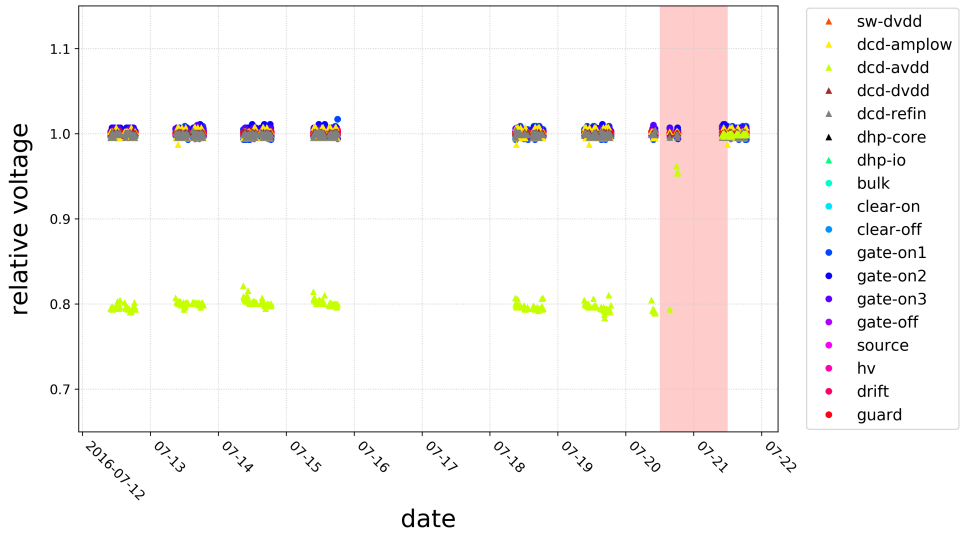


Figure A.7.: Development of relative voltages during the EMC measurement campaign. For each power supply line the sensed voltage at load is shown relative to the corresponding set voltage over all performed measurements.

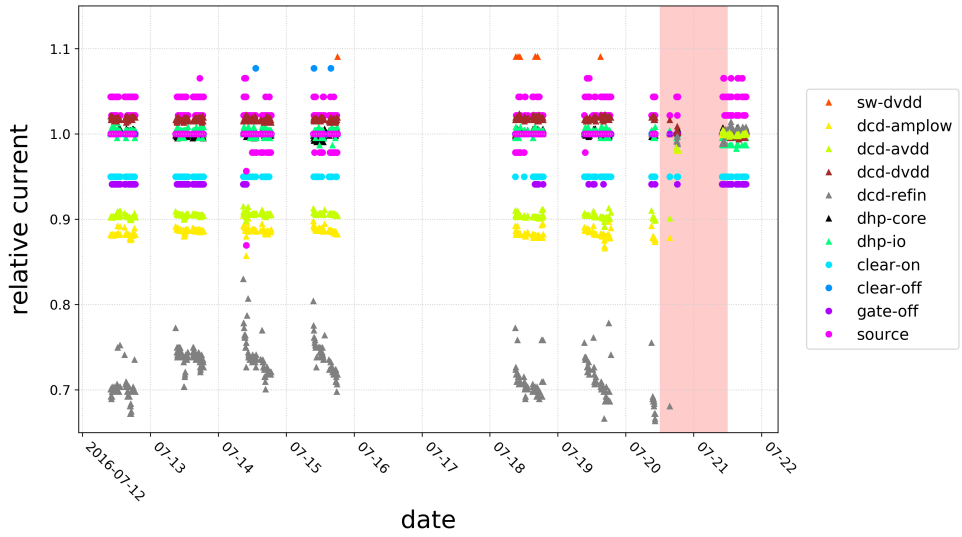


Figure A.8.: Development of relative currents during the EMC measurement campaign. For each power supply line the current is shown relative to the corresponding current in the last measurement. Lines with very small currents are not plotted as their value in the last measurement was either 0 mA or the low measurement accuracy would lead to delusive values for the plotted deviation.

adjustment of the CDN the DCD currents reached the nominal and stable operation state.

As already seen in the development of the noisy pixels (fig. A.3) their overall number decreased as a result of the CDN adjustment, which means that a more stable operation of the readout channels was achieved. To quantify how large the impact of the non-optimal power supply on the already performed measurements was, the measurement of several data points was repeated. These reference points verify that the system's response to injected noise was barely affected. In section 6.5.2.3 it will be shown that the resulting noise response values of the DCDs get more homogeneous but the characteristic shape of the response curves stays the same.

Lessons learned and further interesting studies

If further EMC measurements in a controlled area were to be planned,

- the proper specifications for the CDN components should be taken into account during the preparations,
- the set of power lines to be tested in the individual measurements should be revised and the order of measurements including intended frequencies should be scheduled in advance,
- the PXD module should be operated at the nominal clock frequency of 76.33 MHz,
- corresponding perturbation frequencies should be tested directly, e.g. for the DCD clock, the ADC digitization frequency or the frame rate,
- the influence of different grounding schemes should be analyzed, e.g. if the connections of shields should be closed or opened at different points,
- now it would also be possible to test the capabilities of the ACMC and the DCMC online,
- if possible, also signal data would be desirable to directly measure the influence on the SNR,
- analysis scripts should be prepared in advance so that at least a first look into the data is possible,
- radiated electromagnetic filed emissions of a PXD module were not recorded so far,
- conducted noise emissions for frequencies above 50 MHz might be interesting, as well, e.g. GCK.

B. Transfer functions

All calculated transfer functions are added to this appendix to complete the documentation of results from the EMC measurement campaign of a PXD9 module.

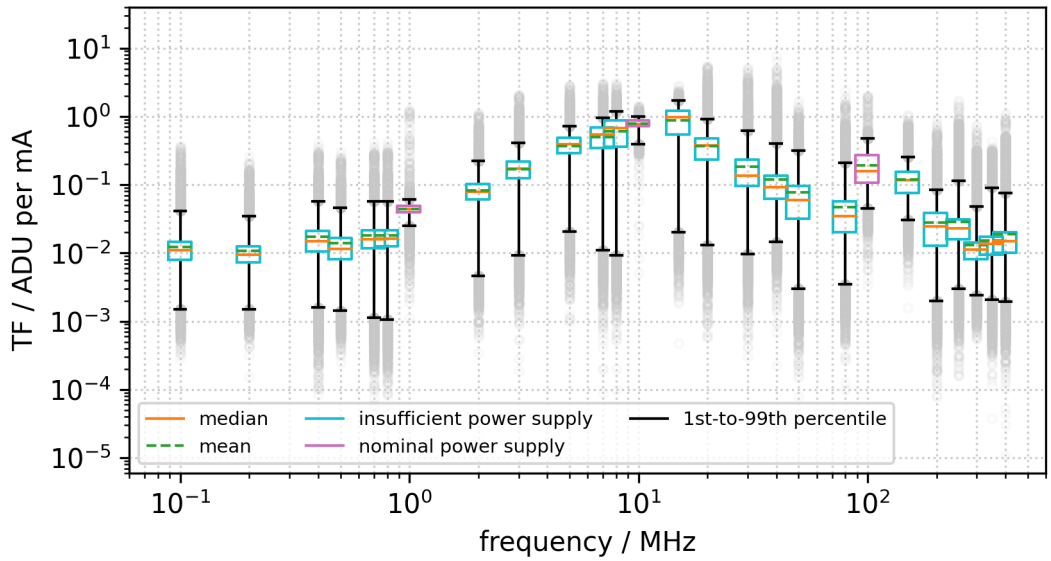


Figure B.1.: Transfer function for conducted differential-mode noise injected into the digital supply domain. The noise was injected into dcd-dvdd, dhp-core, dhp-io and sw-dvdd lines.

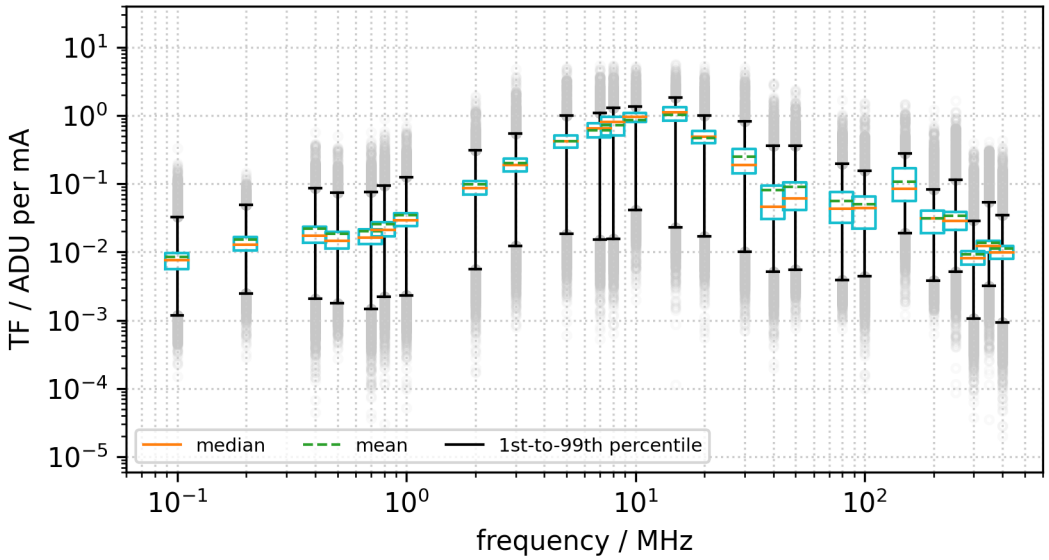


Figure B.2.: Transfer function for conducted common-mode noise injected into the digital supply domain. The noise was injected into dgnd, dcd-dvdd, dhp-core, dhp-io and sw-dvdd lines.

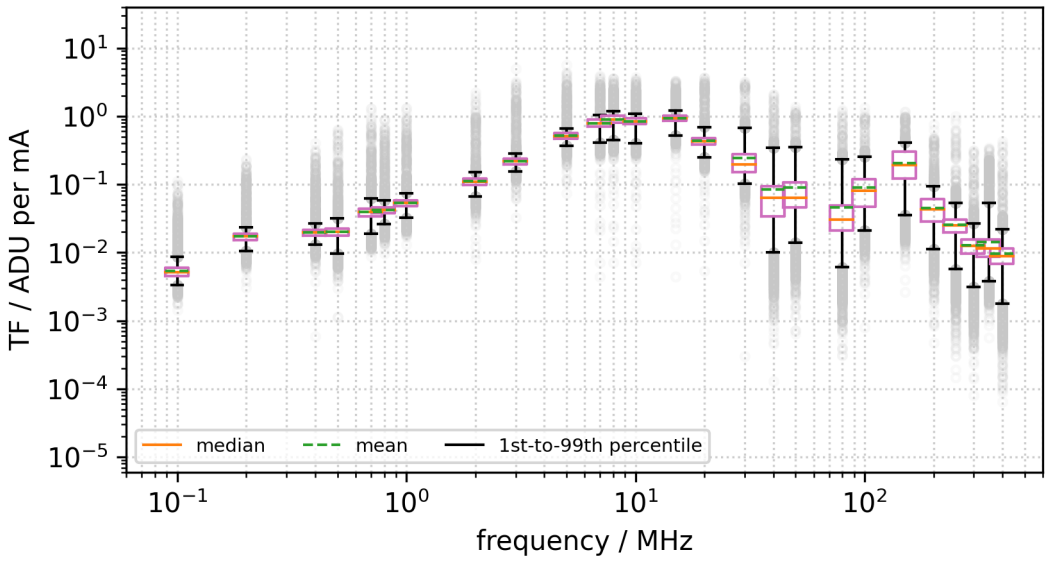


Figure B.3.: Transfer function for conducted common-mode noise injected into the digital supply domain (nominal power supply). The noise was injected into dgnd, dcd-dvdd, dhp-core, dhp-io and sw-dvdd lines.

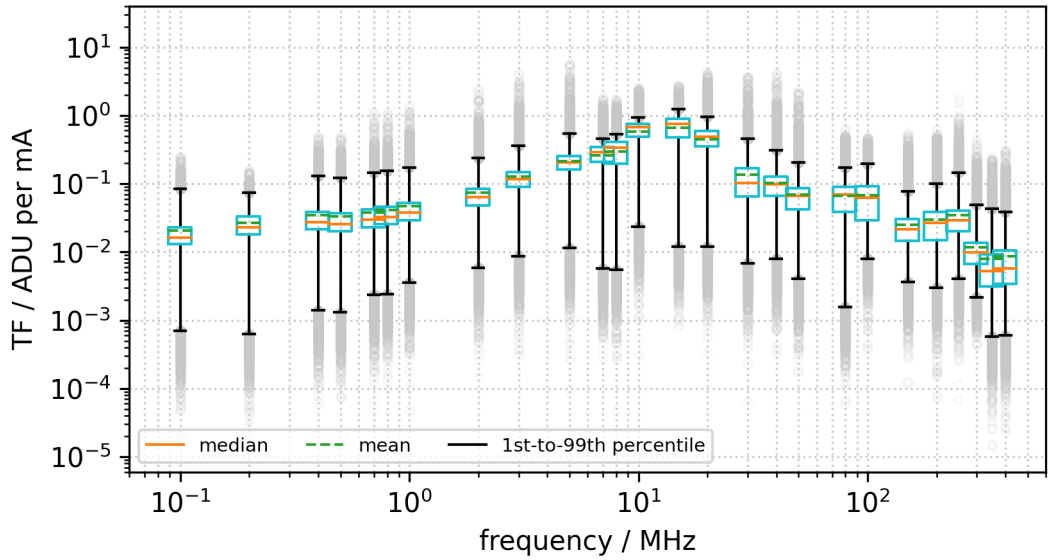


Figure B.4.: Transfer function for conducted differential-mode noise injected into the analog supply domain. The noise was injected into dcd-avdd, source and dcd-refin lines.

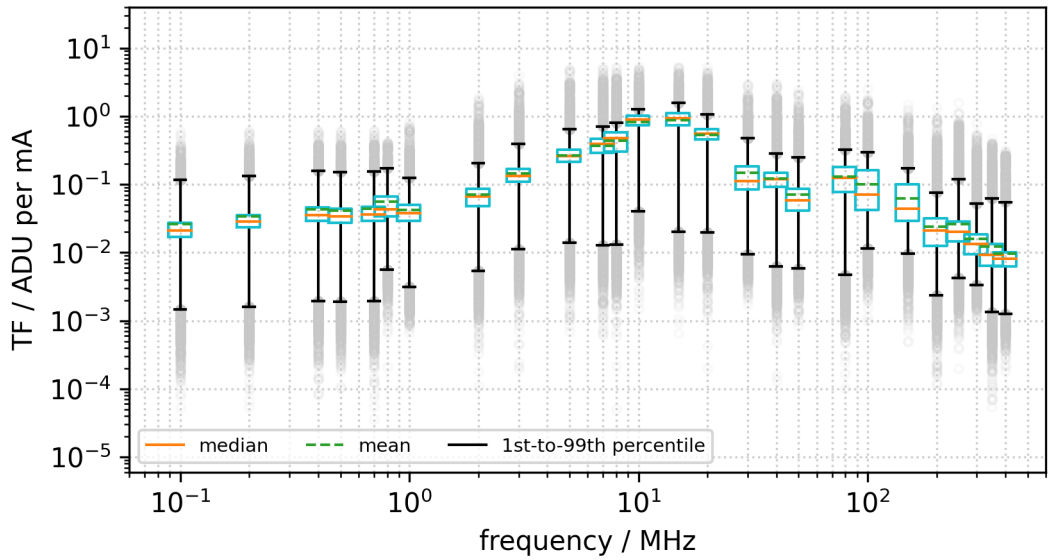


Figure B.5.: Transfer function for conducted common-mode noise injected into the analog supply domain. The noise was injected into agnd, dcd-avdd, source and dcd-refin lines.

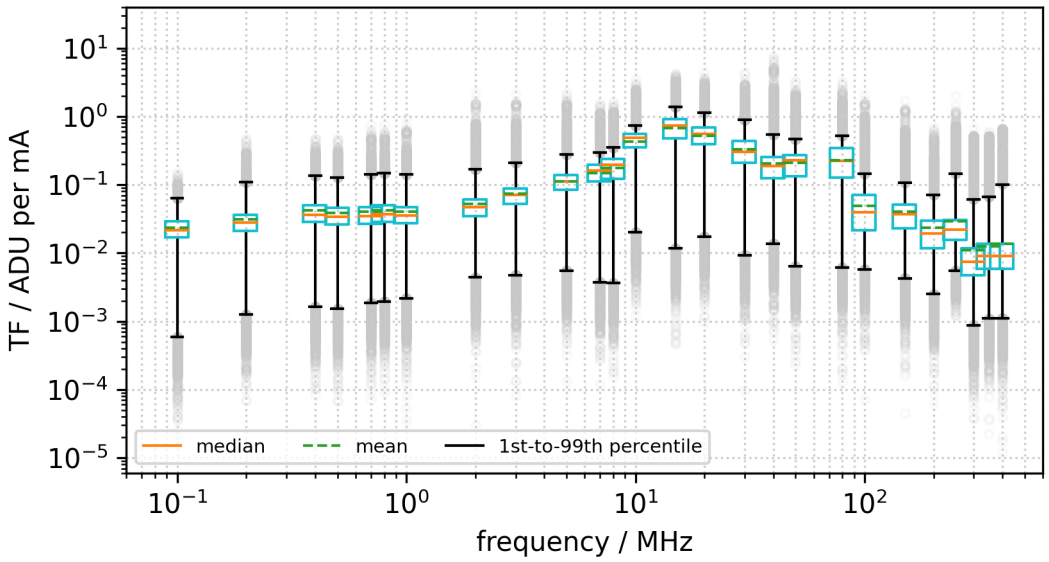


Figure B.6.: Transfer function for conducted common-mode noise injected into the analog supply domain plus dcd-amplow line. The noise was injected into agnd, dcd-avdd, source, dcd-refin and dcd-amplow lines.

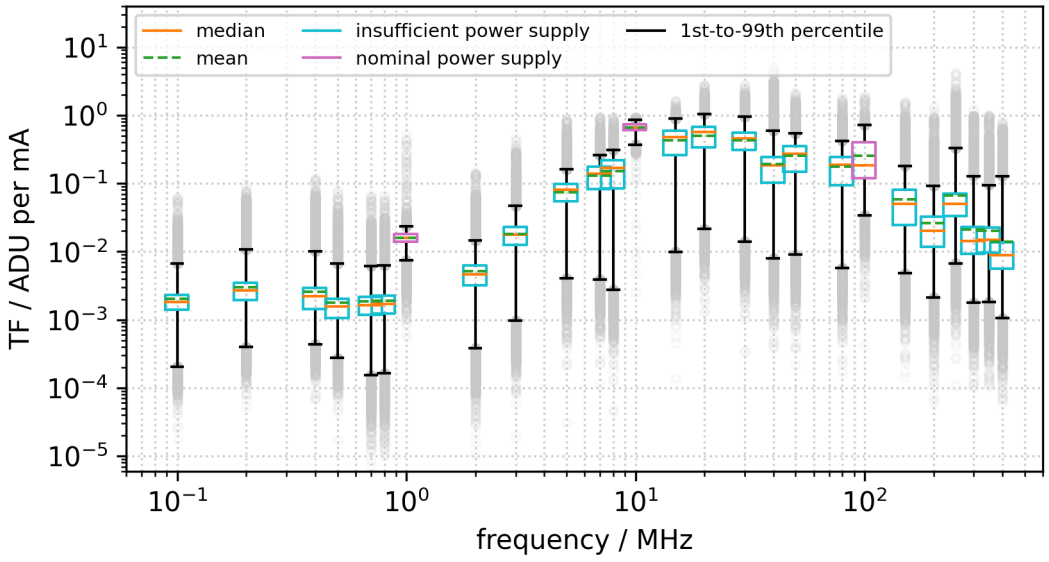


Figure B.7.: Transfer function for conducted differential-mode noise injected into the dcd-amplow line. The noise was injected into the dcd-amplow line.

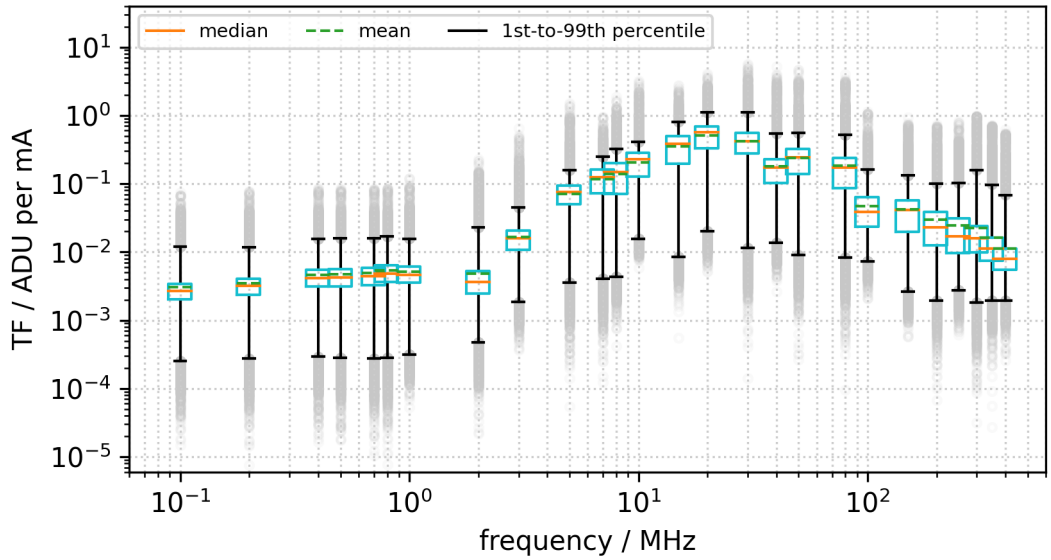


Figure B.8.: Transfer function for conducted common-mode noise injected into the dcd-amplow line. The noise was injected into agnd and dcd-amplow lines.

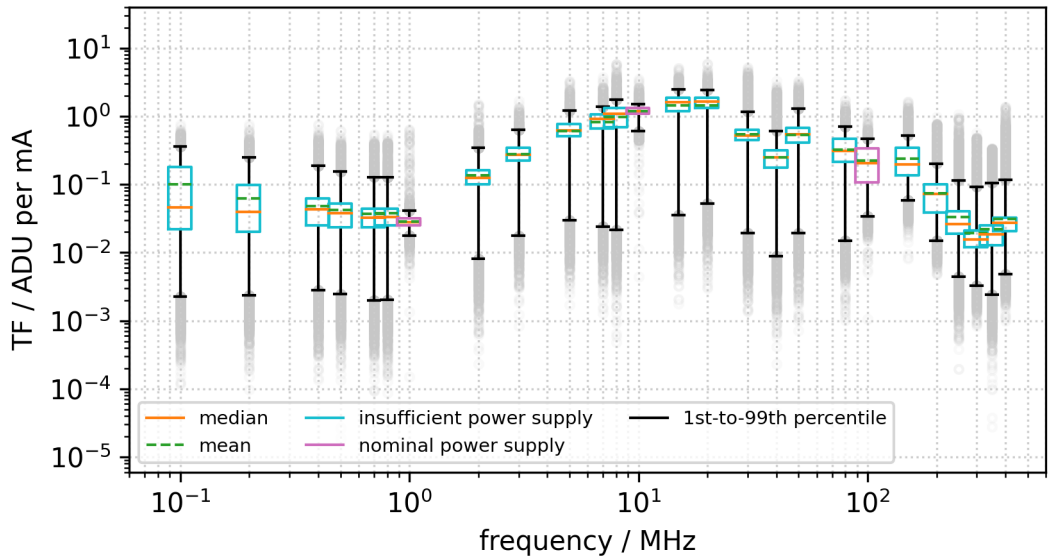


Figure B.9.: Transfer function for conducted differential-mode noise injected into the gate-on1 line. The noise was injected into the gate-on1 line.

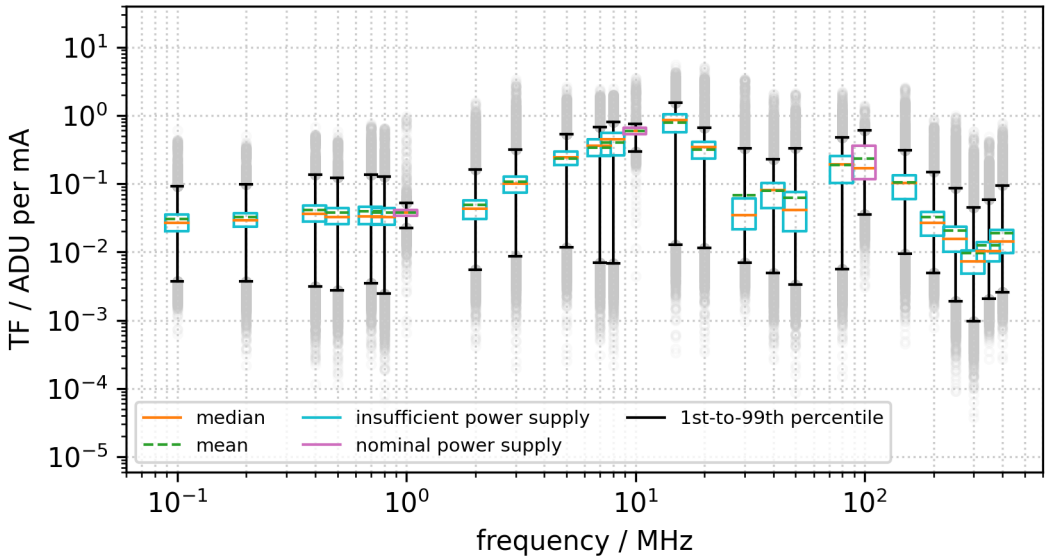


Figure B.10.: Transfer function for conducted differential-mode noise injected into the hv line. The noise was injected into the hv line.

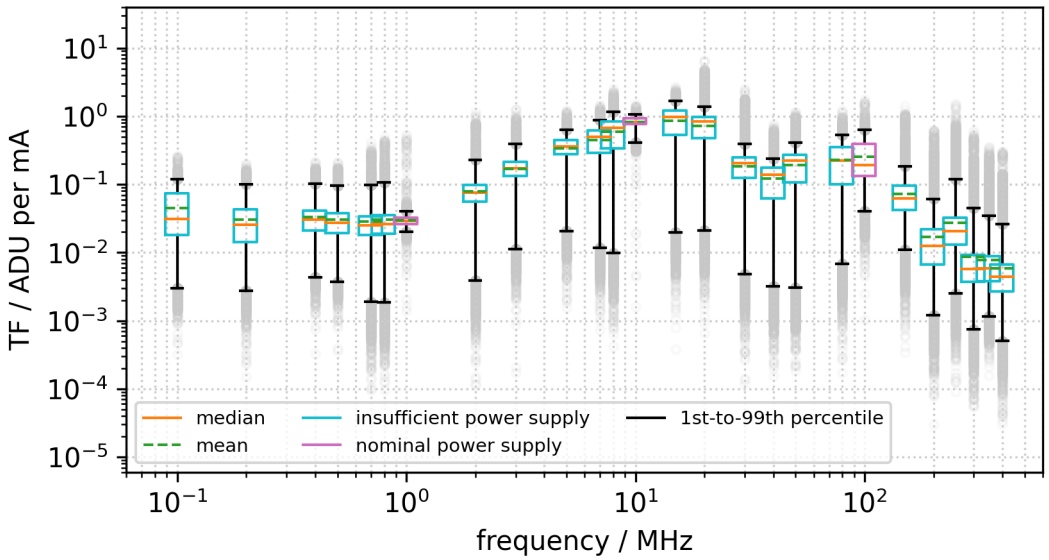


Figure B.11.: Transfer function for conducted differential-mode noise injected into ccg1, drift and gate-on1 lines. The noise was injected into ccg1, drift and gate-on1 lines.

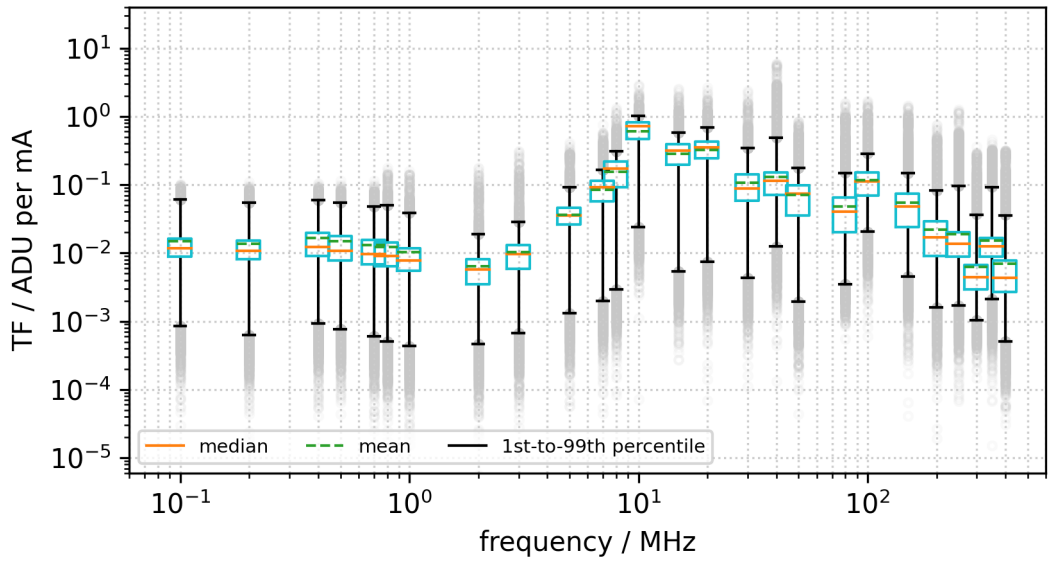


Figure B.12.: Transfer function for conducted common-mode noise injected into all lines connected to the CDN. The noise was injected into dgnd, dhp-core, dhp-io, dcd-dvdd, sw-dvdd, agnd, dcd-avdd, dcd-refin, dcd-amplow, source, gate-on1, ccg1, drift and hv lines.

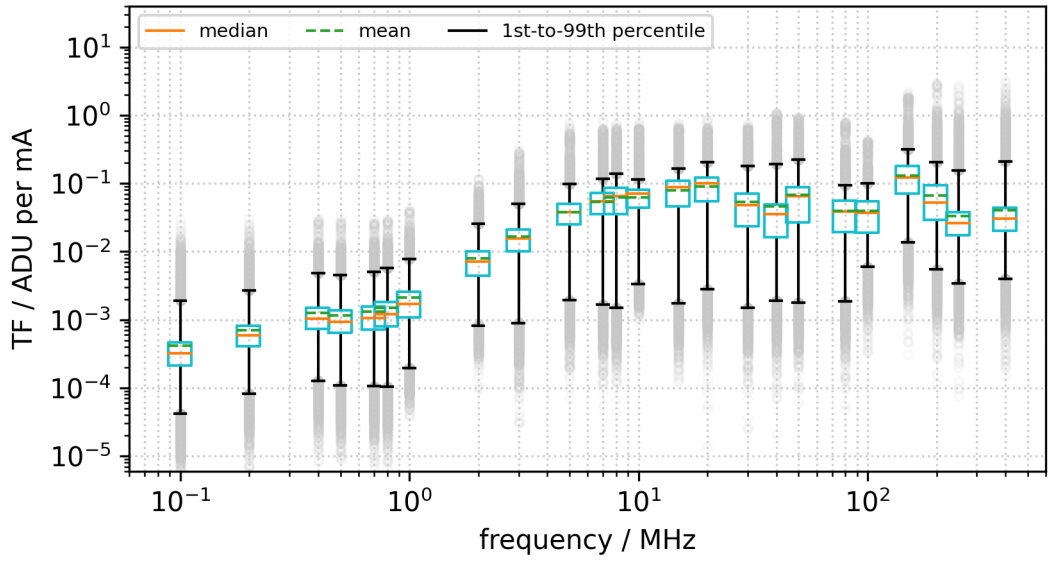


Figure B.13.: Transfer function for radiated noise emitted from beam pipe dummy installed approximately 20 mm above the module.

C. PXD module handling instructions

Module Installation Instruction

Checks before attaching a module:

1. Check that the cooling is switched on an that it is working.
2. Make sure DHE and LMU-PS are not powered.
3. Make sure the vacuum is switched off.
4. Check that the correct version of PatchPanel is prepared (IF, IB, OF, OB).

Actual mounting of the module to the setup:

1. For L1 modules: Mount the cooling adapter and distance holders onto the cooling block. For L2 modules: Remove the cooling adapter and distance holders when installed.
2. Remove the aluminium Kapton cover. (Keep it close to the setup, do not lose it.)
3. Remove the module transport cover. (Keep it close to the setup, do not lose it.)
4. Loosen the four sensor base jig screws.
5. Place the module with the base jig onto the cooling block / cooling adapter and gently tighten the four screws.
6. Keep the transport jig close to the setup, do not lose it.
7. Mount the clamp which holds down the sensor onto the base jig (plastic 3D printed).
8. Activate the vacuum.
9. Take the far end of the Kapton cable out of the Kapton jig and bend it towards the PatchPanel.
10. Make sure the PatchPanel is not connected to the DHE and LMU-PS. Connect the Kapton to the PatchPanel (samtec connector) and make a mark on the PatchPanel to count the number of connections.
11. Only now connect the cables in the following order:
    - Infiniband cable
    - Glenair power cable
    - Ethernet cable (RJ45)
12. Carefully remove the inner cover.
13. Ensure the module lies flat on the base jig by looking from the side. Only continue when you do not see a gap between sensor and base jig to ensure proper cooling.

Module Dismounting Instruction

Checks before removing a module:

1. Make sure the module is powered down completely.
2. Turn off LMU-PS and DHE at the HAMEG PS so that no voltages are applied to the module.
3. Make sure all required parts (incl. screws) of the module transport set are available:
    - module transport jig
    - module transport cover
    - aluminium Kapton cover

Actual dismounting of the module from the setup:

1. Carefully place the inner cover above the module.
2. Disconnect the cables in the following order:
    - Ethernet cable (RJ45)
    - Glenair power cable
    - Infiniband cable
3. Disconnect the Kapton from the PatchPanel (samtec connector).
4. Bend the Kapton cable back and fix it in the Kapton jig.
5. Deactivate the vacuum.
6. Take off the clamp which holds down the sensor onto the base jig (plastic 3D printed). (Keep is close to the setup, do not lose it.)
7. Loosen the four base jig screws.
8. Place the module with the base jig onto the transport jig and gently tighten the four screws.
9. Attach the module transport cover.
10. Attach the aluminium Kapton cover.
11. All modules have to be put back into the storage box when they are not longer used.

Module Setup: pxdtest1

Module Number:	1011	1012	2011	2012
DHE IDs:	2	3	34	35

Installed Module:

inst. date	name	deinst. date

inst. date	name	deinst. date

Motorstage Positions:

matrix start: 0

matrix end:

idle position:

Installed Source:

D. Broken drain lines

Here, hot and disconnected drain lines are combined under the term “broken”. Their cause, appearance and effects are described in section 7.5.3. As additional information the distribution of hot drain lines is shown in fig. D.1. An overview of all found broken drain lines for each tested module is given in fig. D.2.

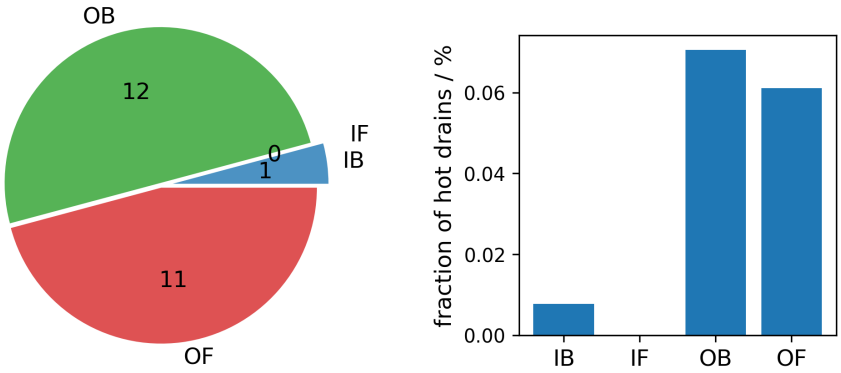


Figure D.1.: Distribution of hot drain lines over the four different module types. Left: The pie chart shows the absolute numbers of hot drain lines. Right: The bar chart shows the numbers of hot drain lines relative to the total number of tested drain lines per module type.

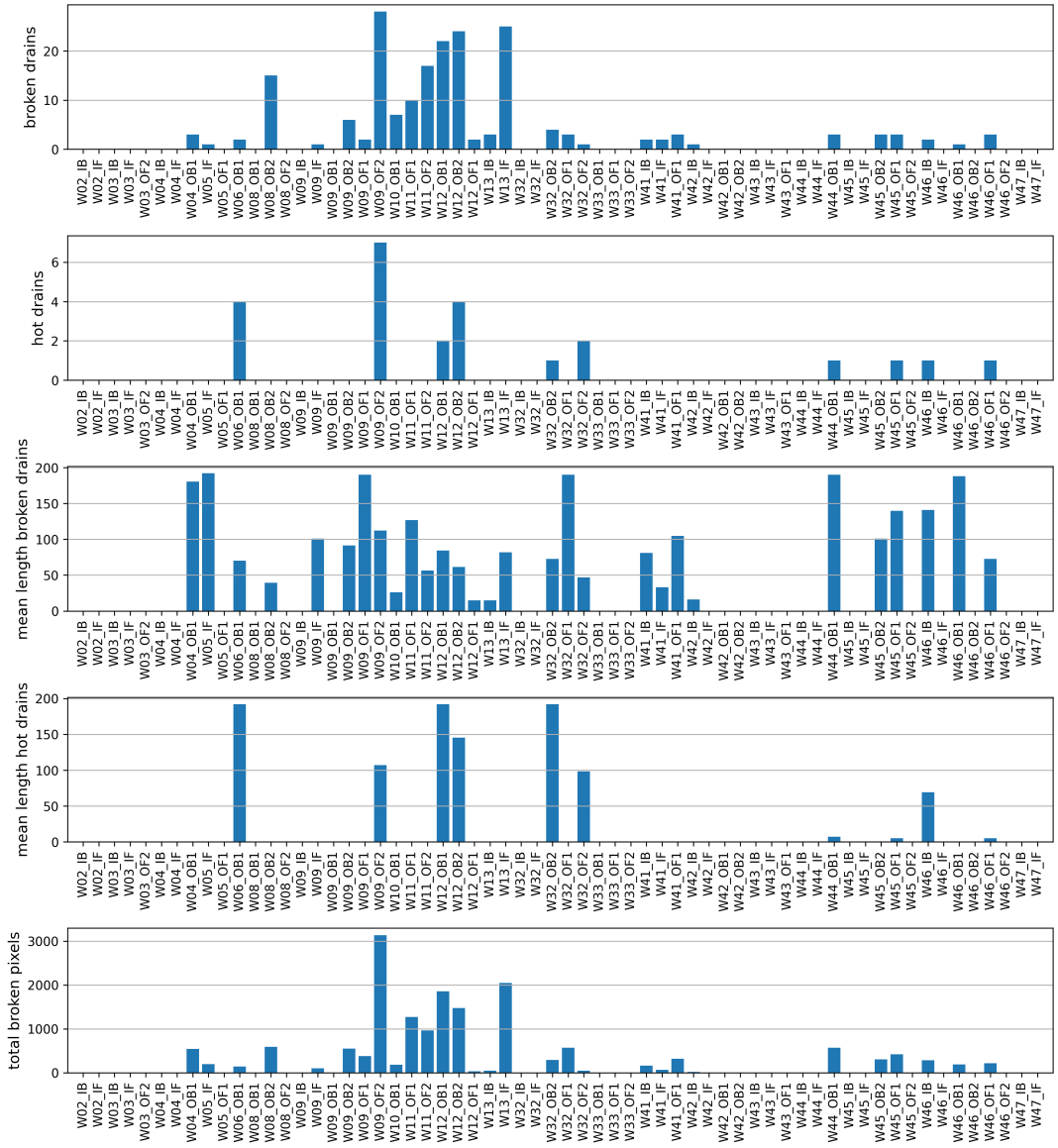


Figure D.2.: Overview of broken drain lines for all tested modules.

E. Development of inefficient gate detection algorithm

Comparison to neighboring gates

In a first approach I thought it is sufficient to compare the sum of hits per gate. A clear drop of the sum value is visible for each inefficient gate when the sum for each gate is plotted next to the hitmap of module 1.01.1 (see fig. E.1). This is an ideal situation of a well performing module with very low noise and a homogeneous illumination. A ring like pattern is visible in the hitmap but not as significant as to impact the sum of the individual gates. The four inefficient gates are easily identified, their sums lie below a threshold defined as a quarter of the median of all sums.

For other modules and different run conditions the picture can change drastically. In this cases it is better to use the median which filters the outliers and delivers more robust results. In fig. E.2 a comparison between sum and median values is shown for a quite noisy hitmap of module 1.04.1. In fact, the hitmap is both times the same but the additional plot shows once the sum of hitnumbers per gate (left side) and once the median of the hitnumbers per gate.

With the last example I address a further issue where the inhomogeneous hitmap due to soft photon irradiation results in large differences in the median values of the working gates along the matrix. The additional soft photon spot originates from backscattering of synchrotron radiation from the crotch part of the beam pipes. The curved shape arises due to the shadow of the titanium part of the beam pipe [225]. Mainly three modules on the forward side in -x direction are affected, namely 1.04.1, 1.05.1 and 1.06.1. This issue was addressed by a comparison of the hitnumbers of each pixel with the hitnumbers of the pixels in the neighboring gates.

This method has the ability to level out the additional irradiation from the soft photon spot (see fig. E.3). The individual pixel values are calculated as

$$val_{i,j} = \frac{hitnr_{i,j}}{hitnr_{i-1,j} + hitnr_{i+1,j}} \tag{E.1}$$

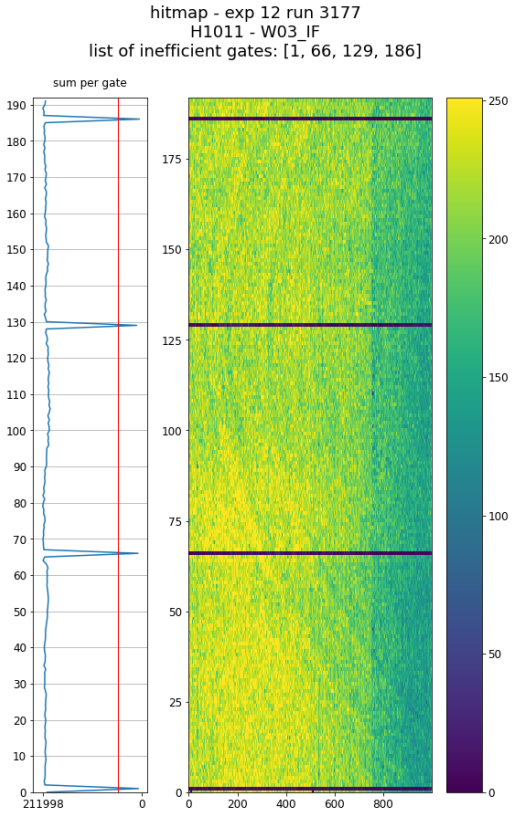
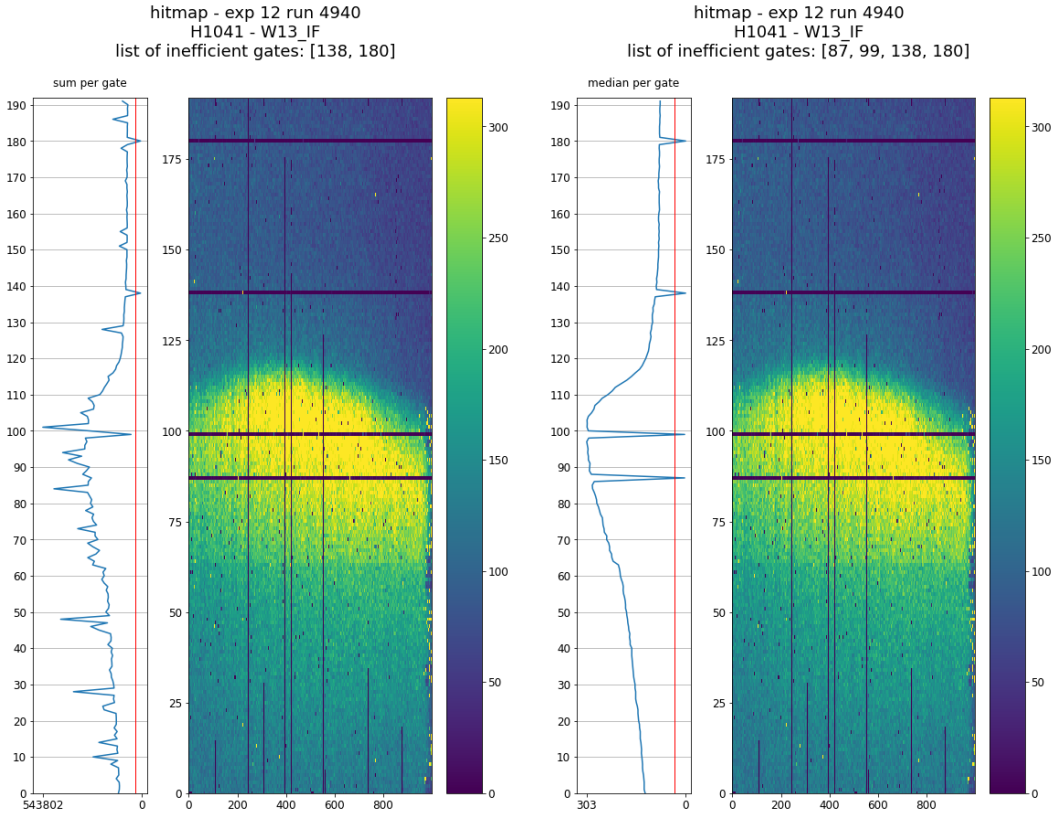


Figure E.1.: Hitmap of module 1.01.1 with illustration of the sums of hitnumbers per gate.



(a) sum per gate **(b)** median per gate

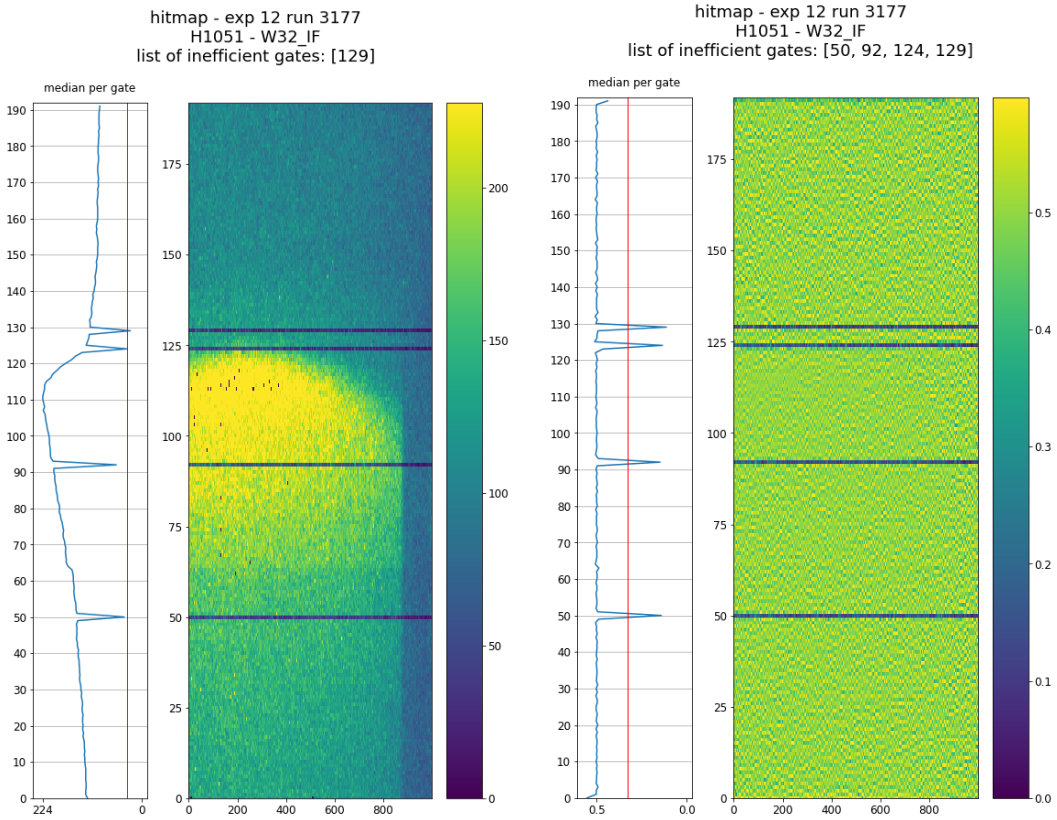
Figure E.2.: Hitmap of module 1.04.1 with illustration of the (a) sums of hitnumbers per gate and (b) median of the hitnumbers per gate. The hitmap is both times the same.

where for the fist and last gate the matrix is "extended" according to the rolling shutter readout mode by taking the last and first gate for comparison respectively. This results in values close to 0.5 for working pixels and close to zero for inefficient pixels[1]. In this way a fixed value of 0.33 can be set as threshold to determine inefficient gates for all different conditions. As only restriction remains a large enough data set for the initial hitmap. Reliable results were already achieved with a bit more than an average of 1.5 hits per pixel but stability improves with higher values.

The algorithm was used in the described state on live data during physics data taking. This revealed its limitations as it was still quite susceptible to noisy data. The comparison to the next neighbors comes with an additional inherent constraint: More than two inefficient gates in a row can not be detected. An inefficient gate surrounded by likewise inefficient gates will not show the required drop in the hitnumbers compared to its neighbors. So far, more than two inefficient gates in a row were not observed yet but this scenario is not excluded to the current knowledge.

The algorithm was further optimized and its current state is described in section 9.4.5.

[1] Artifacts in the working gates next to inefficient gates with very low hitnumbers were avoided by taking the value of the previous gate twice when the next gate showed significantly less hits and vice versa. As this was only done for cosmetic reasons for the plots and introduced instabilities in the calculation it was dropped again



(a) unprocessed hitmap **(b)** preprocessed hitmap

Figure E.3.: Hitmap of module 1.05.1: (a) unprocessed raw data and (b) with hitnumbers referenced to the values of the pixels in the neighboring gates.

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Glossary

ASIC pair An ASIC pair consists of one DHP and its corresponding DCD. On each PXD module there are four ASIC pairs. 106, 107, 118, 119

Belle II Belle II is the name of a particle physics experiment at KEK (Tsukuba, Japan) which is running since 2019. It is the successor of the Belle experiment. 3–5, 7, 21–23, 25, 27, 29, 30, 32, 35–45, 56–58, 61, 64, 71, 74, 77–81, 83, 86, 87, 90, 102, 127, 128, 130, 132, 134, 144, 151, 156–159, 165, 192, 208, 215, 217, 225, 248, 263, 265, 266, 297

electrical multi-chip module A so called EMCM is a monolithic silicon structure with the same dimensions of an equivalent PXD9 module and also equipped with all ASICs but it provides only optionally a small DEPFET matrix for testing purposes.. 87, 138, 314

European Committee for Electrotechnical Standardization The European Committee for Electrotechnical Standardization (CENELEC) is responsible for standardisation in the electro-technical engineering field. Voluntary standards prepared by CENELEC help facilitate trade between countries, access new markets, cut compliance costs, and support the development of the EU single market. CENELEC also creates market access at international level through its close collaboration with the International Electrotechnical Commission (IEC). (https://ec.europa.eu/growth/single-market/european-standards/key-players_en). 307

European Committee for Standardisation The European Committee for Standardisation (CEN) brings together the national standardization bodies of 33 European countries. It provides a platform for the development of European standards and other technical documents on various types of products, materials, services, and processes. These include air and space, chemicals, construction and more. (https://ec.europa.eu/growth/single-market/european-standards/key-players_en). 307

European Standardisation Organisations The European Standardisation Organisations are officially recognised by Regulation (EU) No 1025/2012 as providers of European standards. European Committee for Standardisation, European Committee for Electrotechnical Standardization, and European Telecommunications Standards Institute have

been working with the European Commission since 1984, when a cooperation agreement was signed. Revised in 2003, it lays down general guidelines for cooperation. (https://ec.europa.eu/growth/single-market/european-standards/key-players_en). 84, 314

European Telecommunications Standards Institute The European Telecommunications Standards Institute (ETSI) produces globally-applicable standards for information and communications technology (ICT). These standards also include fixed, mobile, radio, converged, broadcast, and internet technologies. ETSI's purpose is to produce and maintain the technical standards required by its members. (https://ec.europa.eu/growth/single-market/european-standards/key-players_en). 307

Experimental Physics and Industrial Control System EPICS is a set of software tools and applications which provide a software infrastructure for use in building distributed control systems to operate devices such as Particle Accelerators, Large Experiments and major Telescopes. Such distributed control systems typically comprise tens or even hundreds of computers, networked together to allow communication between them and to provide control and feedback of the various parts of the device from a central control room, or even remotely over the internet. (https://epics-controls.org/about-epics/). 74, 314

He Helium is the second most abundant element in the observable universe, after hydrogen. Liquid helium is used in cryogenics and in the cooling of superconducting magnets, e.g. at circular particle colliders. The boiling point of helium lies at 4.22 K. Liquid helium below its lambda point (below 2 K) enters a superfluid state called helium II. Its very low viscosity (close to zero) and its very large specific heat combined with excellent heat conductivity make helium II a perfect coolant for superconducting magnets. 227

I-V curve An I–V curve or current–voltage curve is the relationship between the electric current through a device and the corresponding voltage. I-V curves are for example used to determine the characteristic of transistors like the DEPFET. 140

Instituto Tecnológico de Aragón Technology center attached to the Department of Science, University and Knowledge Society of the Government of Aragon, whose mission is to contribute to the technological development of companies and increase their competitiveness. 83, 315

KEK Kō Enerugī Kasokuki Kenky ū Kikō) is a Japanese organization whose purpose is to operate the largest particle physics laboratory in Japan, which is located in Tsukuba of Ibaraki prefecture. 25, 26, 132, 151, 177, 199, 208, 213, 215, 307

LocalDAQ The PXD LocalDAQ is the data acquisition system which is used for the standalone operation of PXD modules. It only requires components from the PXD system and can therefore run independently from the Belle II system. The LocalDAQ is used

in all laboratory setups and at beam tests and irradiation campaigns. It also runs in parallel to the Belle II data taking for DQM and local PXD analyses. The LocalDAQ receives device data over Gigabit Ethernet, features saving data to disc, spying on live data for online monitoring and receiving a complete copy for integration in the EUDAQ framework during beam tests. The LocalDAQ software was developed by Florian Lütticke [112]. 56, 78, 80, 213, 235, 248, 250

Max Planck Halbleiterlabor The Max Planck Semiconductor Laboratory (Halbleiterlabor HLL) is dedicated to develop, process and provide commercially non-available state of-the-art semiconductor radiation detectors for advanced experiments. Specially focusing on high energy, material and astrophysics research. From the very first detector concept followed by simulation, design, electronics implementation and testing, our technology is tailored to the special requirements of specific and challenging detector applications. Important features are in particular the ability to build wafer size defect free double sided detectors on ultrapure silicon. We are one of the few places in the world where a monolithic integration of electronics into the detector fabrication process (signal processing, first amplification) has successfully been solved without degrading the detector performance. (source: www.hll.mpg.de) . 48, 315

OFF Initial state of the power up sequence when no voltages are applied. 98

PEAK The PXD modules are fully powered and reached the operational state. Data taking can be started. 66, 98, 99, 172, 201, 229

Phase 2 In Phase 2 the final focusing magnets were in place as well as most of the outer Belle II detectors. The inner detectors (PXD and SVD) were replaced by a dedicated detector system (BEAST II). The goal of this phase was to ensure a save environment for the installation of the final VXD detector. First electron-positron collisions were recorded in April 2018. 145, 259

Phase 3 The beginning of Phase 3 marks the start of physics data taking of the Belle II experiment at the SuperKEKB accelerator. All subdetectors jointly collect collision data while the SuperKEKB accelerator gradually increases the luminosity. The goal is to reach an integrated luminosity of $50\,\mathrm{ab}^{-1}$. 5, 102, 132, 192, 199, 204, 212–215, 218, 220, 221, 223, 224, 227, 230, 250, 253, 263, 302, 305

QCS Final focusing magnet system on both sides of the Belle II detector closest to the IP. The half on the forward side is referred to as QCSR (right), the half on the backward side QCSL (left) respectively. 35, 36, 226, 227

STANDBY The digital part of the PXD modules are fully powered and the internal registers are configured. The system is prepared and waiting to activate the analog part. 172, 229

SuperKEKB Asymmetric e^+e^- collider at KEK, the upgrade of KEKB. 3–5, 7, 21, 25–28, 30–33, 35, 37, 42, 43, 57, 114, 129, 132, 135, 201, 205, 208, 212, 217, 223–225, 251, 253, 257, 259, 265, 266, 297, 305

Acronyms

ACMC Analog Common Mode Correction. 55, 132–135, 176, 178, 220, 246, 276

ADC Analog-to-Digital Converter. 55, 97, 104, 105, 116, 122, 127, 167, 169, 171, 179, 180, 182, 220, 221, 223, 269, 276

ADU Analog-to-Digital Unit. 55, 95, 97, 108, 119, 124, 125, 132, 133, 135, 169, 171, 173, 175, 179, 184, 189, 193, 195, 197, 199, 239, 240, 242, 244, 245

agnd analog ground. 59, 71, 94, 106, 111, 121, 144, 272, 279–281, 283

AGS Alternating Gradient Synchrotron. 14

AMS Austria Micro Systems. 56

API application programming interface. 150

ASIC Application-Specific Integrated Circuit. 4, 39, 43, 44, 50–56, 60, 64, 76–78, 87, 88, 92, 94, 95, 116–119, 121–123, 129, 130, 137–142, 144, 157, 167, 170, 173, 175, 179, 180, 189, 193, 194, 203, 212, 220, 223, 224, 230, 232, 240, 244, 253, 255, 257–261, 263, 266, 272, 273

ATCA Advanced Telecommunications Computing Architecture. 56

B2TT Belle II trigger and time distribution system. 56, 127

basf2 Belle II Analysis Software Framework. 56, 217

BCB benzocyclobutene polymer. 50, 51, 208

bulk DEPFET bulk. 59, 202

ccg1 DEPFET capacitive coupled clear gate first domain. 59, 94, 111, 202, 282, 283

ccg2 DEPFET capacitive coupled clear gate second domain. 59, 202

ccg3 DEPFET capacitive coupled clear gate third domain. 59, 202

CDN Coupling Decoupling Network. 93, 94, 97, 98, 101–103, 106, 108, 110–112, 118, 119, 121, 122, 124, 130, 131, 136, 269, 271–273, 276

CKM Cabibbo-Kobayashi-Maskawa. 15–18, 21

CLAWS Scintillator Light and Waveform Sensors. 259

clear DEPFET clear. 140

clear gate DEPFET capacitive coupled clear gate. 58, 140, 221–223

clear-off Switcher clear-off supply. 59, 184, 185, 187, 189, 192, 200, 202, 221, 222, 228, 229

clear-on Switcher clear-on supply. 59, 189, 192, 202, 228, 229

CML Current Mode Logic. 163–165, 220

ConfigDB Configuration Database. 157, 158

CS-Studio Control System Studio. 77, 78, 80, 217, 218

DAC digital-to-analog converter. 167, 168, 171, 173, 182

DAQ data acquisition. 56, 57, 217

DCD Drain Current Digitizer. 55, 57, 69, 76, 77, 88, 94–97, 104–106, 108, 110, 111, 116, 118, 119, 121, 122, 127, 128, 130, 138, 139, 141, 163, 167–169, 172, 175–177, 179, 180, 182, 193, 220, 244, 269, 272, 273, 276

dcd-amplow DCD current sink. 59, 94, 102, 111–113, 121, 144, 180, 182, 200, 202, 272, 273, 280, 281, 283

dcd-avdd DCD analog supply. 59, 94, 102, 106, 111, 113, 121, 144, 172, 202, 271–273, 279, 280, 283

dcd-dvdd DCD digital supply. 59, 94, 108, 109, 111, 113, 121, 131, 202, 272, 277, 278, 283

dcd-refin DCD reference input. 59, 94, 106, 111, 113, 180, 182, 200, 202, 272, 273, 279, 280, 283

DCMC Digital Common Mode Correction. 55, 176, 276

DCU Diamond Control Unit. 225–227, 252, 253, 259

DEPFET DEpleted P-channel Field Effect Transistor. 4, 5, 43–55, 58, 65, 87, 90, 94, 95, 97, 104, 105, 116–119, 128, 129, 137–140, 142, 163, 171, 179, 180, 184, 185, 193, 194, 199, 221, 223, 232, 235, 240, 253–255, 257, 265, 269

DESY Deutsches Elektronen-Synchrotron. 212, 213

dgnd digital ground. 59, 71, 94, 108, 109, 111, 121, 131, 144, 273, 278, 283

DHC Data Handling Concentrator. 56, 79, 127

DHE Data Handling Engine. 56, 61, 62, 68, 72, 76, 78, 79, 92, 93, 100, 127, 138, 161, 163, 165, 180, 203

DHH Data Handling Hub. 56, 61, 72, 102, 127, 165, 166, 213, 220

DHI Data Handling Integrator. 56, 77, 79, 127

DHP Data Handling Processor. 55, 57, 61, 77, 88, 95–97, 102, 104, 107, 127, 130, 138, 139, 141, 163–165, 167, 168, 175, 176, 179, 220, 237, 240, 250

dhp-core DHP core supply. 59, 94, 108, 109, 111, 113, 131, 202, 277, 278, 283

dhp-io DHP input output supply. 59, 94, 108, 109, 111, 113, 131, 202, 277, 278, 283

DQM data quality monitoring. 217

drift DEPFET drift. 59, 94, 111, 184, 185, 187, 200, 202, 221, 222, 282, 283

DUT Device Under Test. 92, 93

E-Hut Electronic Hut. 36, 57, 225

ELOG Electronic Logbook. 149–152, 161, 163

EMC electromagnetic compatibility. 5, 81, 83–88, 90–93, 95, 97, 98, 101, 126–128, 130, 132, 134, 136, 265, 269, 271, 274, 276, 277

EMCM electrical multi-chip module. 87, 98–100, 128, 138, 139

EMI electromagnetic interference. 84–87, 116, 118

EOS end-of-stave. 52, 53, 55, 68, 139, 143, 205

EPICS Experimental Physics and Industrial Control System. 73–75, 79, 156, 161, 166, 189, 253

ESOs European Standardisation Organisations. 84

EU European Union. 84, 86

FCNC flavor-changing neutral current. 17

FEE Front-End Electronics. 95, 99, 104, 128, 129

FOS fiber optic sensor. 225

FPGA Field Programmable Gate Array. 56, 163

gate DEPFET gate. 140

gate-off Switcher gate-off supply. 59, 172, 192, 202, 228

gate-on Switcher gate-on supply. 58, 163, 171–173, 175, 192, 221–223

gate-on1 Switcher gate-on supply first domain. 59, 94, 104, 110–112, 117–120, 124, 202, 281–283

gate-on2 Switcher gate-on supply second domain. 59, 202

gate-on3 Switcher gate-on supply third domain. 59, 95, 96, 106, 202, 269

GCK global reference clock. 57, 93, 99, 127, 129, 276

guard DEPFET guard. 59, 202

GUI graphical user interface. 77, 218

HEP High Energy Physics. 84, 86, 87, 90

HEPHY Institute of High Energy Physics at the Austrian Academy of Sciences. 156

HER High Energy Ring. 27–29, 32, 33, 226, 227, 259

HLL Max Planck Halbleiterlabor. 48, 141–143

hv DEPFET high voltage aka. back plane. 46, 59, 94, 111, 184, 185, 187, 200, 202, 221–223, 282, 283

IB inner backward. 50, 54, 205

IF inner forward. 50, 54, 205

IOC Input/Output Controller. 61, 73–77, 79, 153, 154, 158, 161

IP Interaction Point. 30–32, 34–36, 39, 41–44, 46, 52, 205, 212, 224–226, 255, 259

IQR interquartile range. 197, 198

ITAINNOVA Instituto Tecnológico de Aragón. 83, 87, 90, 91, 127, 136

JSON JavaScript Object Notation. 78

JTAG Joint Test Action Group. 56, 76, 77, 138, 144, 150, 163–166, 272

lab_framework laboratory software framework. 79, 153, 154, 161

LAN Local Area Network. 75

LER Low Energy Ring. 27–29, 32, 33, 226, 227, 259

LHC Large Hadron Collider. 20

MAMI Mainz Microtron. 257, 258

MARCO Multipurpose Apparatus for Research on CO_2. 213, 215

MOSFET Metal-Oxide-Semiconductor Field Effect Transistor. 44, 45

MPCDF Max Planck Computing and Data Facility. 159

MPDL Max Planck Digital Library. 159

MPP Max Planck Institute for Physics. 5, 62, 66, 144, 150, 156, 162, 212

MPV most probable value. 133

NTC negative temperature coefficient. 225

OB outer backward. 50, 54, 205

OF outer forward. 50, 54, 205

ONSEN ONline SElection Node. 56, 217

OPI Operator Interface. 77, 80, 217, 218

OVP overvoltage protection. 58, 76, 189, 228, 233, 252, 253

PCB Printed Circuit Board. 57, 70, 71, 87, 95, 138, 165, 257, 260

PEEK polyether ether ketone. 207

PLC Programmable Logical Controller. 225, 259

PLL Phase Locked Loop. 127

PV Process Variable. 74–79, 152, 154, 156, 158, 175, 200, 253

PXD Pixel Vertex Detector. 4, 5, 23, 34, 41–50, 52–54, 56, 58, 60–68, 70, 71, 73, 74, 76–81, 83, 87–93, 95, 97–102, 104, 105, 110, 112, 114, 116, 118, 124–130, 132–135, 137, 138, 140, 142–144, 146–150, 152, 154, 156–163, 165–167, 169–172, 175, 177, 179, 182–184, 186–189, 192, 193, 196–201, 204, 205, 207, 208, 210, 212–221, 223, 224, 226–228, 232, 235, 240, 246, 248, 250–256, 259–261, 263, 265, 266, 271, 273, 276, 277, 298, 301, 302, 305

QCD quantum chromodynamics. 21

RF radio frequency. 93, 112

RMS root-mean-square. 197, 198

SCB Support and Cooling Block. 58, 60, 68, 205, 212, 213, 217

SEU single event upset. 133

SMD surface-mount device. 50, 138, 140, 143

SMT surface-mount technology. 66

SMU source measure unit. 180

SNR signal-to-noise ratio. 48, 125, 276

SO_2 silicon dioxide. 51

source DEPFET source. 59, 71, 94, 106, 111, 113, 127, 140, 163, 192, 202, 279, 280, 283

STD standard deviation. 197, 198

SVD Silicon Vertex Detector. 41, 60, 64, 87, 132–135, 156, 215–217, 227, 301

sw-dvdd Switcher digital supply. 59, 94, 108, 109, 111, 113, 118, 131, 202, 273, 277, 278, 283

sw-refin Switcher reference input. 59, 190, 202, 273

sw-sub Switcher substrate. 59, 189, 190, 202, 273

TRISTAN Transposable Ring Intersecting Storage Accelerator in Nippon. 25

TSMC Taiwan Semiconductor Manufacturing Company. 56

UDP User Datagram Protocol. 78

UMC United Microelectronics Corporation. 56

VLHI VXD Local Hardwired Interlock. 225, 259

VXD Vertex Detector. 41, 58, 215, 225

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