Transferable Organic/Inorganic Nanosheets for van der Waals Thin-Film Transistors on Trap-Passivated Dielectrics

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Zusammenfassung

Heutige Silizium-MOSFET nutzen die besonderen Eigenschaften von Silizium-Nanosheets für leistungsfähige Mikroprozessoren bei geringem Stromverbrauch. Parallel dazu wird an natürlich vorkommenden Übergangsmetall-Dichalcogeniden als ebenfalls vielversprechende Kandidaten für die nächste Generation von Nanosheet-Transistoren geforscht. Anders als beide Vorgenannten ist die Rolle von organischen Nanosheets in diesem Zusammenhang trotz ihrer überragenden Eigenschaften als Photodioden schwer zu fassen. Im Rahmen dieser Arbeit beschäftigen wir uns mit einer neuartigen Transfer-Technologie für organische Halbleiter, die wir selbst entwickelt haben und untersuchen den Ladungsträgertransport in transferierbaren, organischen und inorganischen van der Waals Nanosheets. Wir verwenden ein wasserlösliches Polymer als Unterlage für den Wachstumsprozess, das in einer geeigneten Anordnung benetzt und aufgelöst wird. Diese Methode gestattet die Ablösung dieser Nanosheets von Drei-Zoll-Wafer. Mit der Hilfe von Rasterkraftmikroskopie und Röntgenstreuexperimenten können wir die hohe Kristallinität der transferierten Nanosheets bestätigen. Wir untersuchen die Leistungsfähigkeit transferierter organischer Transistoren mit Kontakt auf der Unterseite, welche aufgrund der im Übertragungsprozess erhaltenen hohen Kristallinität bessere Ergebnisse liefern als solche aus bloß abgeschiedenen Schichten. Anschließend stellen wir Transistoren mit van der Waals Hetero-Übergängen auf Siliziumdioxid mit transferierten organischen Nanosheets und atomar-dünnen Halbleitern her. Die erstgenannten dienen als p-Leiter, die zweitgenannten als n-Leiter. Sowohl Elektronen als auch Löcher tragen zum Ladungstransport bei und zeigen eine ambipolare Charakteristik mit vergleichbaren Werten für die Ladungsträgermobilität.

Die quantitative Analyse des ambipolaren Transistors und eines unipolaren Transistors aus MoS_2 auf einer unbehandelten 100 nm-dicken Siliziumdioxid-Schicht ergibt eine Unterschwellensteilheit von 2,400 $mVdec^{-1}$ bis 1,000 $mVdec^{-1}$. Bei Raumtemperatur kann die Unterschwellensteilheit einen Abfall von bis zu 60 mV pro Dekade des Drain-Stroms erreichen. Jede signifikante Abweichung vom idealen Verhalten in Richtung höherer Werte deutet auf lokale Grenzflächen-Zustände hin. Das Passivieren der Grenzflächenzustände des Aluminiumoxids bei unipolaren, organischen Nanosheet-Transistoren mit kovalent gebundenen, selbstorganisierten Monoschichten ermöglichen steilere Werte der Unterschwellensteilheit. Jedoch verhindern Benetzungsprobleme der SAM mit Chemikalien, die üblicherweise bei der Photolithographie zum Einsatz kommen, die zur Herstellung ambipolarer und unipolarer MoS_2- Transistoren verwendete Oxid-Passivierung. Zur Lösung dieses Problems entwickeln wir eine neue,

lithographie-kompatible Methode zur Grenzschichtpassivierung mit Hilfe einer ultra-dünnen Polymerschicht. Unsere Untersuchungen ergeben, dass der Ladungsträgertransport in Transistoren durch sog. Springen zwischen durch nichtabgesättigte Bindungen hervorgerufenen tiefen Störstellen dominiert wird. Diese treten bei unbehandelten Oxiden auf und führen zu schlechtem Unterschwellen-Verhalten. Hinzu kommt, dass das "Hopping" von Ladungsträgern in tiefen Störstellen die Bestimmung einer korrekten Transistor-Charakteristik verhindert. Hingegen zeigen Transistoren mit einer passivierten 100 nm-dicken Siliziumdioxidschicht Hopping-Transport über Randzustände mit wenigen k_BT unterhalb des Leitungsbands und eine substantiell stärkere Unterschwellensteilheit von 189 $mVdec^{-1}$. Wenngleich durch die Passivierung die benötigte Drain-Spannung auf 5 V reduziert wird, um den Sättigungsbereich zu erreichen, so zeigt der MoS_2-Transistor doch eine nicht-ideale Sättigungscharakteristik.

Dieses nicht-ideale Sättigungsverhaltenen der Transistoren auf unpassivierten, 100 nm-dicken Siliziumdioxidschichten weist darauf hin, dass eine weitere Verbesserung der Unterschwellensteilheit erforderlich ist, um die Dominanz der Grenzflächenzustände gegenüber den intrinsischen Eigenschaften des Halbleiters zu beseitigen. Wir verwenden eine lokale Gatter-Struktur mit Aluminium als Gatter-Metall und verstärken das native Oxid des Aluminiums mit einem Sauerstoff-Plasma-Prozess zur Erzeugung eines hochwertigen, ultradünnen Aluminiumoxids. Aluminiumoxid ermöglicht die Verwendung von konvalent bindenden SAM zur Grenzflächenpassivierung. Durch Verkleinerung der Passivierungsfläche innerhalb der Architektur des lokalen Gatters können wir die Bentzungsprobleme lösen, die zuvor bei solchen SAM-Oberflächen beobachtet worden sind. Die Kapazität des Plasma-Oxids vergrößert sich, verglichen mit dem passivierten 100 nm-dicken Siliziumdioxid, um das Zwanzigfache. Dadurch reduziert sich der Bereich für die Gate-Spannung auf ±0.75 V, was dazu führt, dass die Sättigungsbedingungen bereits bei einer Drain-Spannung von 1 V erreicht werden können. Mit solch ultradünnen Gate-Oxiden weisen MoS_2-Transistoren eine lehrbuchhafte Charakteristik auf: geringe Betriebsspannung, starke Unterschwellensteilheit von 61.6 $mVdec^{-1}$ und Ladungsträgerbeweglichkeiten von ungefähr 5 $cm^2V^{-1}s^{-1}$.

Diese Ergebnisse betonen, dass die Herstellung effizienter Nanosheet-Transistoren mit atomardünnen Halbleitern auf ultradünnen Oxiden möglich ist, sofern die Oberflächen-Eigenschaften gründlich angepasst werden. Im Rahmen dieser Arbeit ist die elektronische Charakteristik von Einzel-Transistor-Bauelemente vorangetrieben worden, was zur Herstellung komplexerer organisch/anorganischer, ambipolarer Transistoren und integrierter Schaltkreise ermutigen soll.

Abstract

The latest silicon metal-oxide-semiconductor field-effect transistor design utilizes silicon nanosheets for high-performance, low-power microprocessors. In parallel, natural nanosheets like transition metal dichalcogenides are studied as promising candidates for the next-generation materials in nanosheet transistors. So far, organic nanosheets have remained elusive, despite superior performance of organic molecules in light-emitting diodes. In this thesis, we develop a novel transfer technique for organic semiconductors and investigate the charge transport in transferable organic/inorganic van der Waals nanosheets. We used a water-soluble polymer as a growth template, which was dissolved in a proper wetting geometry following the deposition of the organic semiconductor, allowing the release of wafer-scale (3-inch) nanosheets from their growth substrates. Using an atomic force microscope and X-ray diffraction, we confirmed that the nanosheets preserved their high crystallinity after transfer. We investigated the performance of bottom-contact transferred organic transistors, which outperformed bottom-contact as-evaporated organic transistors due to the transfer-enabled high crystallinity. Afterward, we fabricated van der Waals heterojunction transistors on silicon oxide with transferable organic nanosheets and atomically thin semiconductors, the former serving as a p-conductor and the latter as an n-conductor. We discovered that electrons and holes simultaneously contribute to charge transport, exhibiting ambipolar characteristics with similar mobility values.

Quantitative analysis of the ambipolar transistors and unipolar MoS_2 transistors on untreated 100 nm-thick silicon oxide revealed subthreshold slopes of 2,400 $mVdec^{-1}$ to 1,000 $mVdec^{-1}$. At room temperature, the subthreshold slope can be as steep as 60 mV over a decade of drain current. Any significant deviation from this ideal behavior towards higher values indicates local interface states. Passivating the interface states of the aluminum oxide in unipolar organic nanosheet transistors with chemically bonded self-assembly monolayers (SAM) allowed us to achieve steeper subthreshold slopes. However, the wetting problems of SAM with lithography chemicals prevented the use of this oxide passivation in the fabrication of ambipolar transistors and unipolar MoS_2 transistors. To resolve this issue, we introduced a new lithography-compatible interface state passivation by an ultrathin polymer. We observed that the charge transport was dominated by hopping in dangling bond-induced deep trap states for transistors on untreated oxides, resulting in poor subthreshold performance. In addition, the deep trap state hopping of charges made it impossible to determine the proper transistor characteristics. Contrarily, the transistors on passivated 100 nm-thick oxide demonstrated

hopping transport in tail states a few k_BT below the conduction band and substantially steeper subthreshold slopes of 189 $mVdec^{-1}$. Although the passivation reduced the required drain voltages to 5 V to establish the saturation region conditions, the MoS_2 transistors exhibited non-ideal saturation characteristics.

Non-ideal saturation characteristics of the transistors on passivated 100 nm-thick silicon oxide indicated the need for further improvement of the subthreshold slope to eliminate the domination of interface states' over the intrinsic properties of the semiconductor. We adopted a local gate architecture, used patterned aluminum as gate metal, and enhanced its oxide by oxygen plasma to produce high-quality ultrathin aluminum oxide. Aluminum oxide enabled using chemically bonded SAMs as an interface state passivation. By decreasing the passivation area through the local gate architecture, we could eliminate the wetting problems that had previously occurred for such SAM surfaces. The capacitance of the plasma-enhanced oxide increased by 20 times compared to the passivated 100 nm-thick silicon oxide. As a result, the gate voltage range was lowered to ±0.75 V, enabling saturation conditions to occur at drain voltages of 1 V. MoS_2 transistors on such ultrathin gate oxides exhibited textbook thin-film transistor characteristics; low operation voltages, steep subthreshold slopes of 61.6 $mVdec^{-1}$, and mobilities around 5 $cm^2V^{-1}s^{-1}$.

The results emphasize that efficient nanosheet transistor fabrication is possible with atomically thin semiconductors on ultrathin oxides if the surface properties are carefully adjusted. This work pushed the electronic properties of single transistor device characteristics, encouraging building of more complex organic/inorganic ambipolar transistors and integrated circuits.

Contents

"Dinlenmemek üzere yürümeye karar verenler, asla ve asla yorulmazlar."
"Those who decide to walk without resting, never and never get tired."

— Mustafa Kemal Atatürk

1

Introduction

"I would like to start by emphasizing the importance of surfaces. It is at a surface where many of our most interesting and useful phenomena occur. We live for example on the surface of a planet. It is at a surface where the catalysis of chemical reactions occur. It is essentially at a surface of a plant that sunlight is converted to a sugar. In electronics, most if not all active circuit elements involve non-equilibrium phenomena occurring at surfaces."

— Walter H. Brattain

The Nanosheet Transistor Era

The demand for high-performance and low-power electronics has driven technology for decades. Modern processors utilize billions of silicon (Si) metal-oxide-semiconductor field-effect transistors (MOSFET) as their primary building blocks. Following Moore's Law [1] over the past 50 years has resulted in not only cheaper and faster but also smaller and more densely packed MOSFETs. The Si MOSFET is remarkable not only because it is one of the smallest electronic switches but also because it represents the pinnacle of technological mastery over silicon. The single crystal wafers can be grown in sizes up to 300 mm in a controlled fashion, such as their doping, roughness, defect density, and crystal orientation. Fabrication of MOSFETs on high-quality Si wafers then enables the absolute control of charge transport, for instance, which led to the groundbreaking discovery of the quantum Hall effect in the 1990s [2]. The development of MOSFET has also influenced the fabrication of laboratory-scale single transistors

through ideas such as strain-enhanced mobility in atomically thin transistors [3, 4]. As a result, understanding the physics of MOSFETs and their fabrication is crucial for studying solid-state physics.

The renowned Si MOSFET was designed to bring critical elements into a two-dimensional (2D) plane known as "planar" geometry (Figure 1.1). Planar geometry was required due to the surface states of Si, which could only be passivated by thermal oxidation (SiO_2) to enable the field effect [6]. The first fabricated MOSFET had an oxide thickness of 100 nm, a channel length of 45 µm, and a channel width of 635 µm [7]. At that point, the never-ending process of scaling transistors down had already begun. In 35 years, channel lengths have decreased from 10 µm (1972) to 30 nm (32 nm node, 2009) [8]. At the same time, the oxide thickness was scaled down from 100 nm to 1.2 nm to lower the operation voltages.

As every benefit has a drawback, this aggressive scaling introduced two fundamental electrostatic limits: leakage currents (charge tunneling over the gate oxide) and short channel effects (depletion zone overlapping due to proximity of contacts). On the one hand, replacing

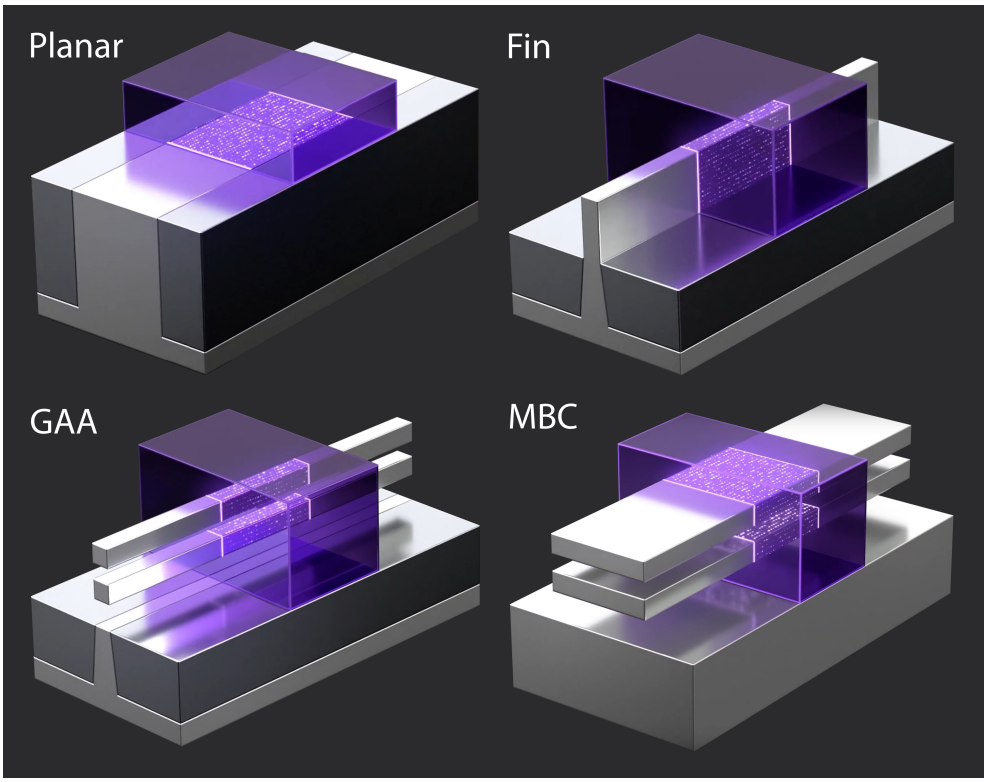

Figure 1.1: "Evolution" of the MOSFET: Planar, fin, gate-all-around (GAA), and multiple-bridge-channel field-effect transistors. The purple region represents the gate oxide, and the dotted region represents the transistor channel. Adapted from [5].

silicon oxide with oxides having higher dielectric constants (high-k) enabled the suppression of leakage currents by using thicker oxide layers to achieve the same capacitance as SiO_2. The measured high-k dielectric capacitance was equivalent to 0.9 nm-thick SiO_2. On the other hand, the solution to the short-channel effect required advanced fabrication techniques. The transistor design changed from planar (2D) to three-dimensional (3D) and was named FinFET. Here, the channel resembled a shark fin and got longer as it followed the fin, as depicted in Figure 1.1. A further benefit of this design was that the gate stack covered the channel from three surfaces compared to one. FinFETs had a considerably shorter lifetime than planar FETs, lasting from 2011 (at the 22 nm node) to the present day.

Despite their short lifetime, FinFETs successfully demonstrated that covering the channel with the gate oxide dramatically reduced operation voltages. In order to reduce operating voltages even further, gate-all-around (GAA) FETs were introduced to enclose the channel by the gate (Figure 1.1). Nevertheless, nanowires increased the fabrication complexity of GAA FETs. Samsung then introduced multi-bridge-channel™ (MBC) FETs based on Si nanosheets instead of nanowires to benefit from GAA while reducing fabrication complexity. IBM then realized this [9], as depicted in Figure 1.2, and the era of nanosheet MOSFETs began.

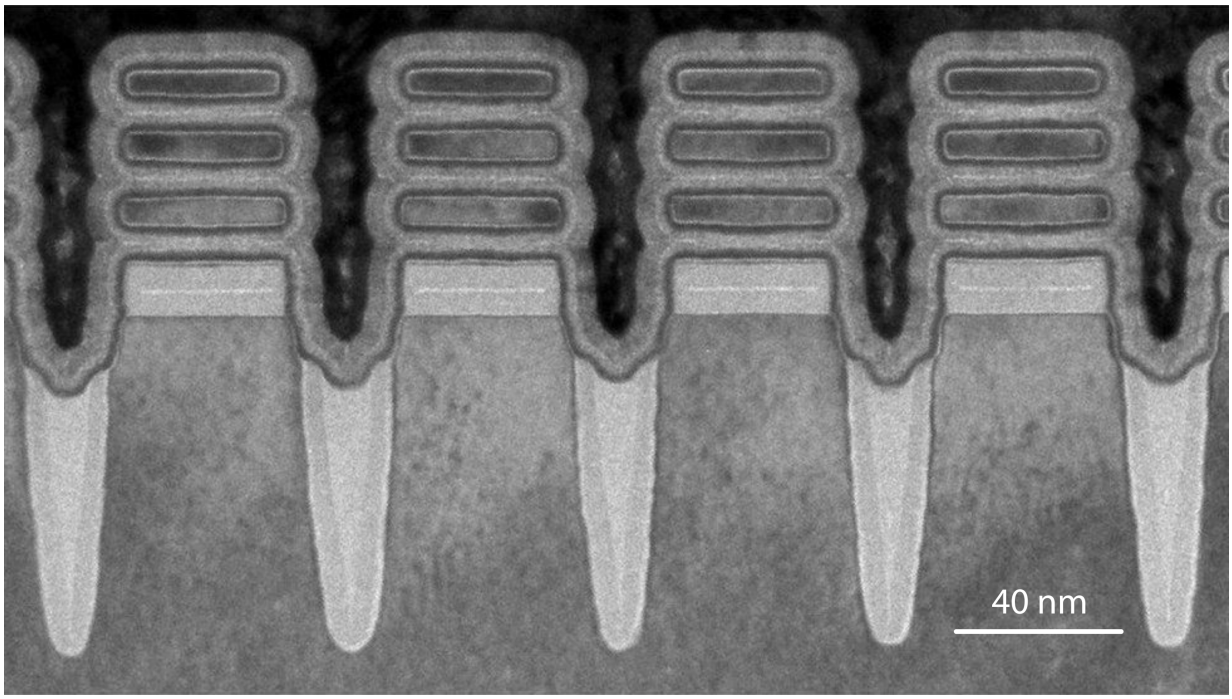

Figure 1.2: The nanosheet FETs. Taken from [9].

van der Waals Solids and Heterostructures

Physicists and material scientists entered the nanosheet era with the isolation of graphite nanosheets (graphene) from bulk graphite using standard adhesive tape in 2004 [10]. These naturally inorganic nanosheets now include metals (graphene), insulators (h-BN), and semiconductors (transition metal dichalcogenides, TMD). The key feature of inorganic nanosheets is their covalent in-plane and van der Waals (vdW) out-of-plane bond structure. The vdW bonds can easily be broken, even with adhesive tape, and sheets can be deposited on any surface. Individual nanosheets can be employed to investigate their fundamental features or be stacked to investigate novel vdW heterojunctions (Figure 1.3) [11].

After discovering atomically thin materials, many groups investigated the fundamental properties of these nanosheets. For instance, the mobility value of the suspended graphene reached up to 200,000 $cm^2V^{-1}s^{-1}$ [12], while the top-gated monolayer semiconductor molybdenum disulfide (MoS_2) exhibited a mobility value of 200 $cm^2V^{-1}s^{-1}$ [13]. In addition, MoS_2 became a direct band gap semiconductor in the monolayer limit, substantially increasing its photoluminescence [14]. Later, inorganic nanosheets were stacked into vdW heterostructures to benefit from individual layers in one stack. For example, strongly correlated phases such as unconventional superconductivity were observed in precisely stacked two graphene nanosheets

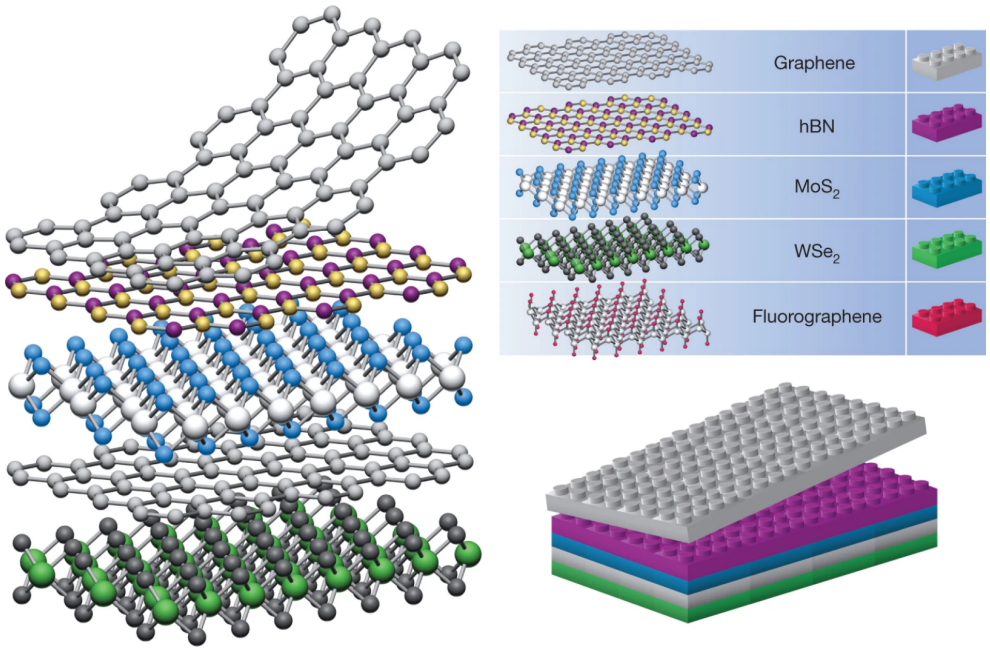

Figure 1.3: Illustration of inorganic nanosheet stacking for building van der Waals heterostructures. Taken from [11].

with an angle of 1.1°[15]. Furthermore, two TMD nanosheets were stacked for light-emitting transistors [16], and a TMD nanosheet was sandwiched between h-BN nanosheets to fabricate ultraclean atomically thin transistors [17].

However, creating vdW heterostructures by stacking 2D nanosheets is only one of many methods. Additionally, organic semiconductors (OSC) consist of small molecules that are zero-dimensional (0D) or long polymer chains that are one-dimensional (1D). The OSC can be utilized as individual molecules (the red and yellow blocks), fibers (the green block), or thin-films, as shown in Figure 1.4 [18]. The OSC thin-films are formed not only by out-of-plane vdW bonds but also in-plane. Therefore, this in-plane vdW interaction enables freedom in molecular design and makes them attractive for light-emitting diodes [19], solar cells [20, 21], transistors [22, 23, 24], and even light-emitting transistors [25, 26]. Furthermore, many novel devices, such as gate-tunable p-n junctions, can be fabricated by stacking inorganic nanosheets with organic thin-films [27, 28, 29, 30]. Last but not least, isolated molecules can be utilized for molecular doping or opening a band gap of 2D nanosheets [31, 32, 33].

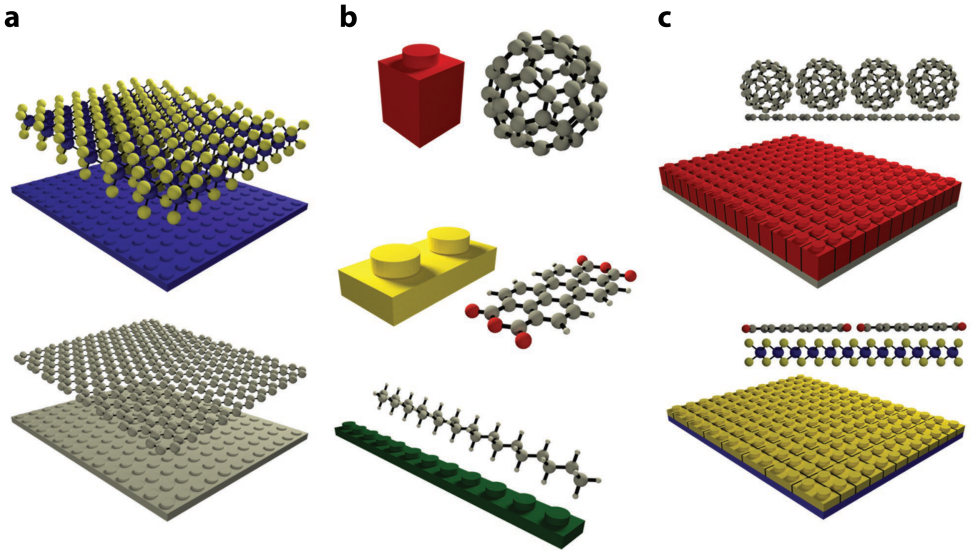

Figure 1.4: Illustration of inorganic nanosheet stacking with organic molecules for building van der Waals heterostructures. **a** Inorganic nanosheets. The blue and gray blocks represent MoS_2 and graphene, respectively. **b** Organic 0D and 1D small molecules. The red and yellow blocks represent buckminsterfullerene and perylenetetracarboxylic dianhydride, and the green block represents docosane. **c** Organic/inorganic van der Waals heterostructures. Adapted from [18].

Outline of the Dissertation

Transferable organic/inorganic nanosheet transistors, either as individual nanosheets or as heterojunctions, will be investigated in this Dissertation. In Chapter 2, the fundamentals of the van der Waals solids, thin-film transistors, and non-ideal transistor characteristics will be reviewed in detail. Starting with the necessity of transferable organic nanosheets, their realization, structural and electrical characterization, and organic/inorganic van der Waals heterojunction transistors will be represented in Chapter 3. After revealing the impact of the interface states in the heterojunction transistors, a lithography-compatible method for interface state passivation will be introduced in Chapter 4. The charge transport in heterojunction and inorganic nanosheet transistors on passivated oxides will then be investigated. The non-ideal characteristics in the saturation region of inorganic nanosheet transistors will compel the utilization of ultrathin oxides. Therefore, a novel plasma-enhanced gate stack will be adapted for inorganic nanosheet transistor fabrication to reveal their potential by pushing the single transistor limits. In conclusion, the summary and future perspectives will be discussed in Chapter 6.

2

Fundamentals of van der Waals Solids and Thin-Film Transistors

"It will be perfectly clear that in all my studies I was quite convinced of the real existence of molecules, that I never regarded them as a figment of my imagination, nor even as mere centres of force effects."

— Johannes Diderik van der Waals

2.1 Mixed Dimensional van der Waals Solids

2.1.1 0D - Small Molecule Organic Semiconductors

Small molecule OSCs are the 0D representative of the van der Waals solids. The molecules are formed through sp^2 hybridization of carbon atoms that leads to the delocalization of π-electrons throughout the molecule by overlapping π-bonds (Figure 2.1) [34]. Chemical synthesis of organic molecules provides a significant degree of freedom for molecular design, resulting in various molecular crystals. This chemical tunability gives rise to increased molecular stability, tunable absorption spectrum, and improved electronic properties [24, 35].

Single crystals, polycrystalline and amorphous films can be grown using small molecules. Forming the solid by vdW bonds brings several advantages, like being mechanically softer materials and having lower melting points (crucial for flexible electronics). However, vdW bonds

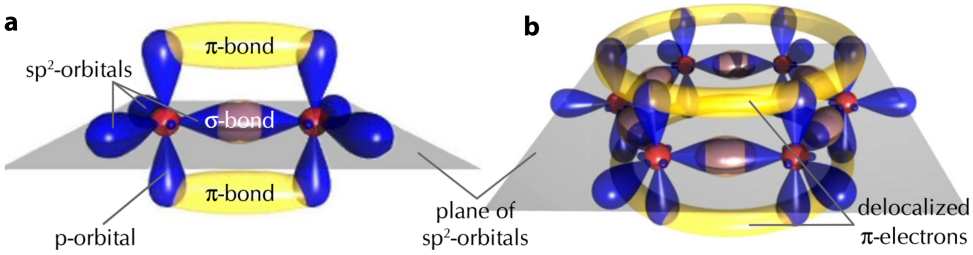

Figure 2.1: Representation of orbitals and bonds for **a** two (ethylene molecule) and **b** six (benzene molecule) sp^2-hybridized carbon atoms. Red spheres represent carbon atoms. Overlapping of π-bonds promotes the delocalization of π-electrons throughout the molecule. Taken from [34].

also bring stronger localization of electronic work function due to the weaker intermolecular interaction. The localization limits the mobilities of OSCs to 25 $cm^2V^{-1}s^{-1}$, even for single crystals [36].

Since single crystals are not scalable, polycrystalline films are technologically more relevant. The vacuum deposition of polycrystalline films enables scalability with precise thickness control. The molecular thin-film transistors (TFT) exhibit mobilities around 1 $cm^2V^{-1}s^{-1}$, which can compete with amorphous Si TFTs [39]. The purity and grain size of the polycrystalline film depend on the evaporation conditions, the purity of the source, surface properties, and packing motifs. The latter is crucial for improving mobility in polycrystalline films. The highest mobilities were achieved by rod-like molecules, for example pentacene and dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) (Figure 2.2a). Thus, the favorable packing motif is when its long axis is perpendicular to the surface (Figure 2.2b). This orientation promotes the delocalization of the electron wavefunctions by tighter in-plane molecular packing.

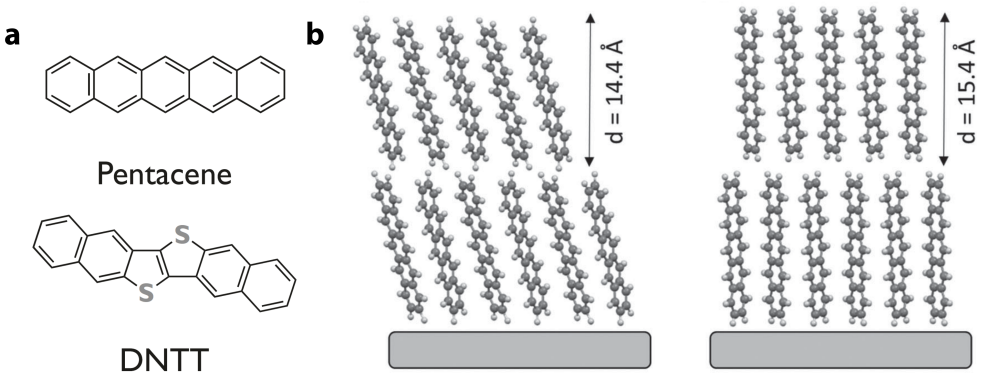

Figure 2.2: Molecular structure and packing motifs of small molecules. **a** Molecular structure of pentacene and DNTT. **b** Packing motifs of pentacene molecules. Left: Campbell bulk-phase with a molecular tilt of 21°. Right: Thin-film phase with a molecular tilt of 3°. The length of the pentacene molecule is 15.5 Å. Adapted from [37, 38].

2.1.2 2D - Atomically Thin Inorganic Semiconductors

Atomically thin semiconductors consist of a few atomic layers. The crystals are formed by covalent bonds in-plane, but van der Waals bonds out-of-plane, allowing their exfoliation down to the monolayer limit, in contrast to molecular solids. The main family of atomically thin semiconductors consists of TMDs [41]. TMDs have one atomic layer (M) sandwiched between two atomic layers (X) and form MX_2, where M is Mo or W, and X is S or Se (inset of Figure 1.3).

Isolating TMD sheets results in novel electrical and optical properties distinct from those of the bulk form. An indirect-to-direct band gap transition is one of the examples. TMDs are indirect band gap semiconductors in bulk, however, Mak et al. showed that they become direct band gap semiconductors in the monolayer limit as shown in Figure 2.3a [14]. Moreover, the band gap increases up to 2 eV as the layer number decreases. Since graphene is semimetal despite possessing extremely high mobilities, having a band gap is crucial for low power consumption in off-state of a transistor [42]. Additionally, Cui et al. confirmed the n-conductor behavior in MoS_2 crystals, exhibiting mobility values of up to 1,000 $cm^2V^{-1}s^{-1}$ for the monolayer and 34,000 $cm^2V^{-1}s^{-1}$ for six-layer MoS_2 after h-BN encapsulation at low temperatures (Figure 2.3b) [40].

Unlike Si, which is subject to surface states, atomically thin semiconductors benefit from the absence of dangling bonds owing to van der Waals out-of-plane bonds. However, the deposition of TMD crystals gives rise to several benefits and drawbacks that vary with the method used. One of the most popular approaches is mechanical exfoliation, in which individual layers are isolated from the bulk crystal using an adhesive tape [43]. After the adhesive

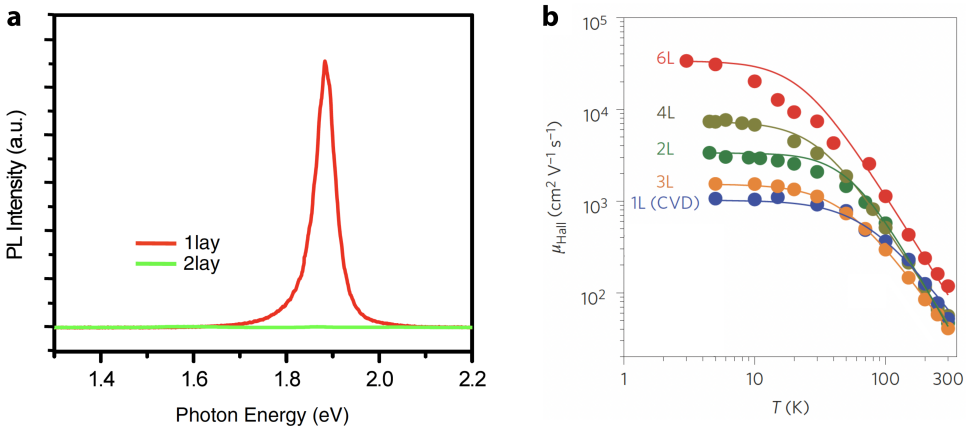

Figure 2.3: Layer number dependent **a** photoluminescence and **b** Hall mobility of MoS_2 crystals. Adapted from [14, 40].

tape has been placed on the substrate and peeled away, crystals of varying sizes and orientations are deposited on the substrate (Figure 2.4a). The method allows depositing the cleanest TMD crystals, but layer number and size cannot be controlled. Several research groups have attempted to solve this issue by employing a bottom-up strategy involving the chemical vapor deposition (CVD) of TMD crystals. The CVD method involves decomposing the precursors (like MoO_2 and sulfur) in a heated glass tube [44]. An inert gas like argon is then used to transport the precursor vapor on the substrate. With this method, the crystal formation can be precisely controlled; the achieved monolayer crystal sizes can be larger than 100 µm in a triangular form (Figure 2.4b). Then, the crystals are transferred to target substrates using wet or dry transfer methods [45]. The trade-off, however, is that sulfur vacancies can lead to unintentional doping [46], or the transfer process can cause cracks.

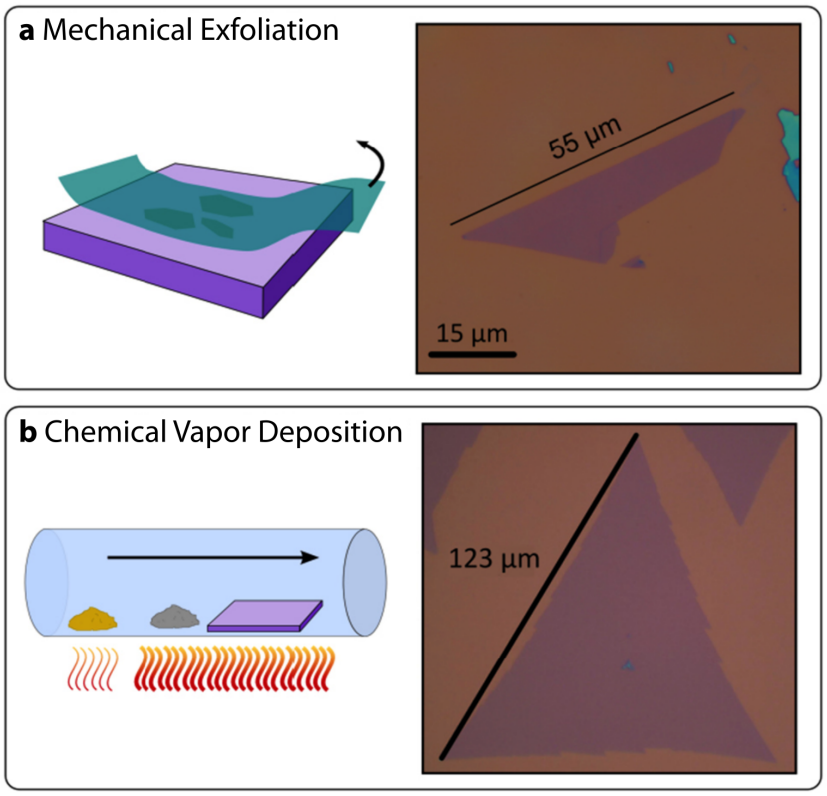

Figure 2.4: Top-down and bottom-up deposition methods of MoS_2 crystals. **a** Optical microscopy image of MoS_2 crystals deposited by mechanical exfoliation. The blue sheet represents the adhesive tape. **b** Optical microscopy image of MoS_2 crystals deposited by CVD method. An inert gas carries the heated precursors (black arrow) for deposition on the substrate. Adapted from [47, 48].

2.1.3 Charge Transport Models in Semiconductors

Depending on the purity of a semiconductor, charge transport conforms to one of the three principal models, as summarized in Figure 2.5 [49]. For semiconductors with a low disorder (such as single crystals), the charge transport model is known as band transport (or band-like transport for OSC). The conductivity is described by Drude model. In single crystals, the typical mobility values are in the order of 10^3 $cm^2V^{-1}s^{-1}$ for Si and 10^1 $cm^2V^{-1}s^{-1}$ for small molecule OSC.

Polycrystalline films typically have a higher density of trap states due to imperfections such as grain boundaries. Trap states within the band gap can be defined as shallow or deep, depending on their relative energetic positions according to the thermionic energy (k_BT): The states that are a few k_BT away from the band edge are referred to as shallow trap states, while those that are further away are referred to as deep trap states (Figure 2.5). An external stimulus, such as an electric field, or thermal energy, can release a charge from shallow trap states into the band states. This charge transport model is known as multiple trap and release. Here, the mobilities are closer to the single crystal mobilities since the charges could still be released partly to the band states.

In the case of a higher density of trap states in the band gap, the charges are continuously trapped and released in trap states and cannot reach the band states. This type of charge transport method is known as hopping transport, indicated by orange arrows in Figure 2.5.

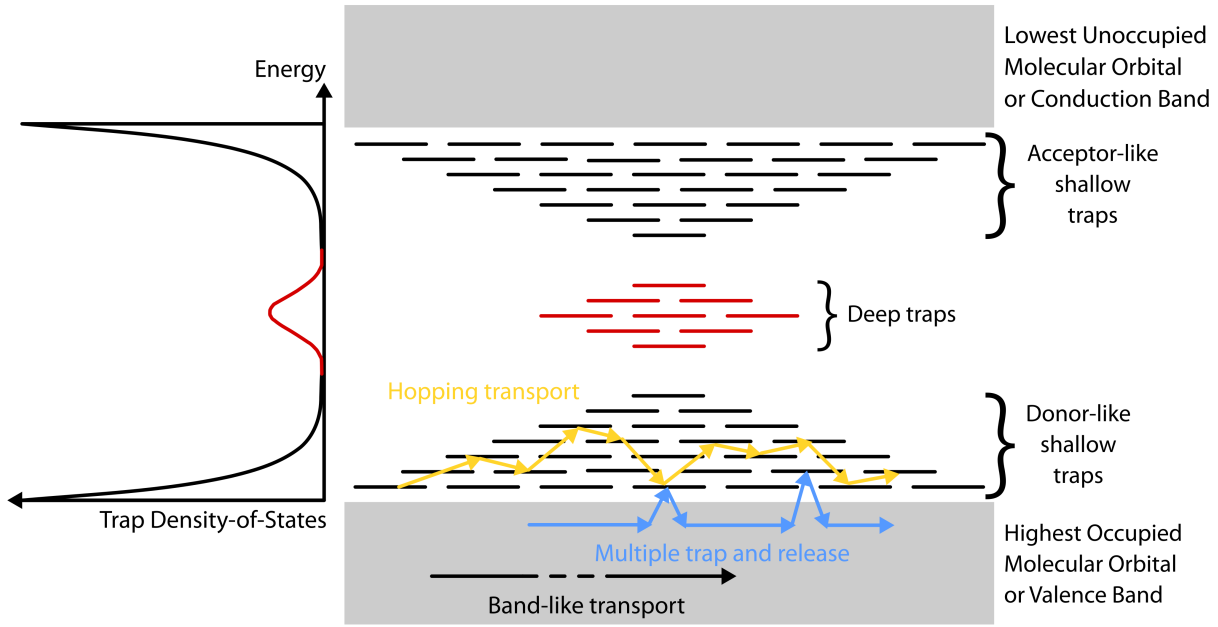

Figure 2.5: Illustration of charge transport models in semiconductors. Adapted from [49].

Here, the carrier mobility is strongly dependent on the hopping depth, the carrier density and the temperature. This transport model is the most common model among the thin films. Therefore, comprehending the connection between the trap states and field-effect charge density is essential in thin-film TFTs, which will be discussed in detail in the following sections.

2.2 Thin-Film Transistors (TFT)

As a device architecture, transistors are essential for studying charge transport in semiconductors since they provide direct access to charge-carrier mobility through field-effect doping. A well-known utilization of this concept is hydrogenated amorphous silicon (a-Si:H) as a TFT. Since thin films are mostly intrinsic semiconductors, a TFT differs from the MOSFET in conducting channel formation, where it is formed in accumulation mode in contrast to inversion mode. A schematic of a TFT is shown in Figure 2.6. W and L are the width and length of the transistor channel, where V_D and V_G are drain and gate potentials, respectively. In a TFT, on one side, the in-plane source and drain electrodes are responsible for charge injection/extraction and for the drift field. On the other side, the vertical metal-insulator-semiconductor (MIS) junction regulates the charge carrier density in the semiconductor like a parallel plate capacitor [50]:

$$Q(x) = C_{ox}\left(V_G - V(x)\right) \tag{2.1}$$

where Q(x) is charge density, C_{ox} is oxide capacitance, V_G is gate potential and V(x) is local channel potential. The C_{ox} can be written as,

$$C_{ox} = \varepsilon_0 \varepsilon_{ox} / d_{ox} \tag{2.2}$$

where ε_{ox} is relative dielectric constant of the oxide and d_{ox} is oxide thickness. According to the sign of the gate bias, either holes or electrons are accumulated in the semiconductor.

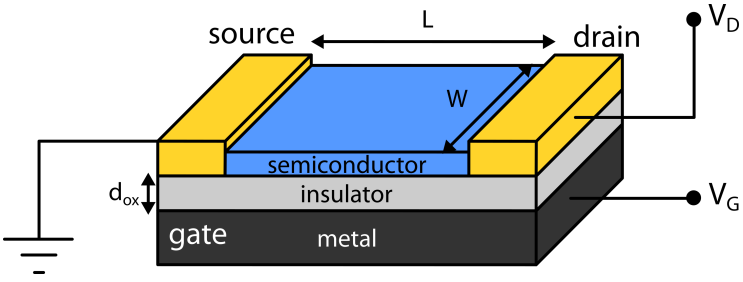

Figure 2.6: Illustration of a thin-film transistor. Source and drain represent the contacts, W and L represent channel width and length, and d_{ox} represents the oxide thickness. V_D and V_G represent the drain and gate voltages with respect to the source, which is always grounded. Adapted from [50].

A TFT can be fabricated in four different configurations, as sketched in Figure 2.7. The configuration mostly depends on the application or the fabrication restrictions. For example, the bottom-gate TFT configuration is advantageous to fabricate since metal/insulator gate stacks such as Si/SiO_2 are easily accessible in high quality. In contrast, contact configuration can be more complicated. For example, the TMD crystals are randomly placed on the oxide after transfer, and thus the top-contact (TC) configuration is more beneficial. Contrarily, OSCs are incompatible with lithography techniques, so it is necessary to fabricate OSC TFTs in the bottom-contact (BC) configuration in the case of lithography. This thesis will focus on bottom-gate transistors with either top or bottom contacts.

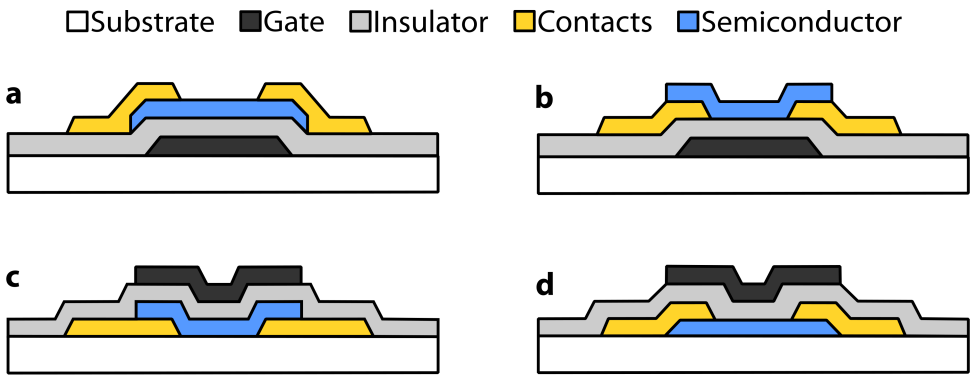

Figure 2.7: Thin-film transistor configurations. **a** Bottom-gate top-contact, **b** bottom-gate bottom-contact, **c** top-gate bottom-contact, **d** top-gate top contact.

2.3 Essential Concepts of TFTs

Being a field-effect device encourages comprehending and modifying the standard MOSFET definitions for TFTs. Despite its apparent simplicity, this adaptation can be challenging. TFTs can easily accommodate MOSFETs' operation regions due to the close relationship between the operation regions and the applied biases. However, essential MOSFET parameters, such as threshold voltage, contrast with the TFT due to its definition [50]. In this section, we review and extend these ideas further for TFTs.

2.3.1 Linear and Saturation Regions

Identifying the TFT operation regions is critical for several reasons. The saturation region plays a crucial role in integrated circuits by stabilizing the circuit against drain voltage fluctuations since the drain current is independent of the drain voltage in the saturation region. In contrast, an accurate contact resistance study can only be conducted in linear region where field-effect charges uniformly dope the semiconductor.

When the drain and source electrodes are connected to the ground, a TFT becomes an MIS diode. Field-effect charges are injected into the semiconductor in response to the gate bias (Figure 2.8a). Since MIS can be modeled as a parallel-plate capacitor, the field-effect charge density depends on the gate bias and the insulator's capacitance (Equation 2.1). Then, a small voltage applied to the drain contact would cause the charges to drift by the electric field. Here, the gate potential drops near the drain contact due to the applied drain bias (Figure 2.8b). This region is known as the linear region. The transistor acts like a resistor with the drain current proportional to the drain bias [51, 52]:

$$V_D << V_G - V_{Th}, I_D = \left(\frac{W}{L}\right) \mu_{lin} C_{ox} (V_G - V_{Th}) V_D \tag{2.3}$$

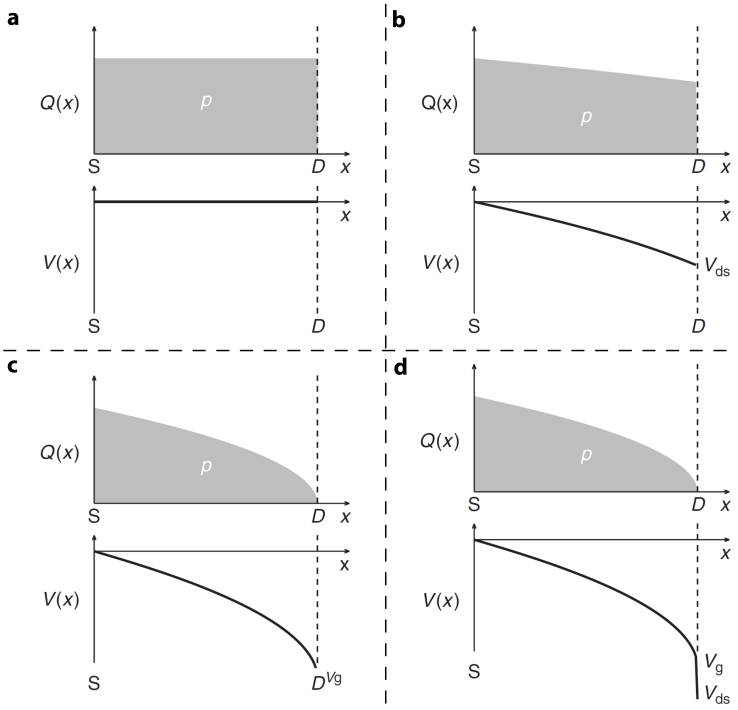

Figure 2.8: Distribution of field-effect charge density Q(x) and channel potential V(x) along the channel as a parameter of drain bias for p-channel TFT. **a** $V_D = 0$ V, **b** $V_D << V_G$, **c** $V_D = V_G$, and **d** $V_D > V_G$. S and D indicate source and drain electrodes, respectively. Adapted from [50].

V_{Th} is threshold voltage. Then, the linear mobility can be written as,

$$\mu_{lin} = g_m \left(\frac{L}{WC_{ox}}\right)\left(\frac{1}{V_D}\right) \tag{2.4}$$

where g_m is called as transconductance,

$$g_m = \left(\frac{\partial I_D}{\partial V_G}\right) \tag{2.5}$$

The gate potential drops more near the drain contact as the drain bias increases. Once they balance out, the channel pinches off at the drain contact, and the drain current saturates (Figure 2.8c):

$$V_D \geq V_G - V_{Th}, I_D = \left(\frac{W}{2L}\right)\mu_{sat}C_{ox}(V_G - V_{Th})^2 \tag{2.6}$$

and the saturation mobility,

$$\mu_{sat} = \left(\frac{\partial\sqrt{I_D}}{\partial V_G}\right)^2\left(\frac{2L}{WC_{ox}}\right) \tag{2.7}$$

Due to the saturation, a further increase in the drain bias would not increase the drain current (Figure 2.8d). In an ideal transistor, the saturation and linear mobility values must be comparable.

After introducing the operation regions, we now evaluate the current-voltage (IV) characteristics. A typical TFT characterization includes two distinct IV measurements: I_DV_D for constant V_G and I_DV_G for constant V_D. The former is referred to as the output curve and the latter as the transfer curve. Figure 2.9a shows a typical output curve exhibiting the linear and saturation regions. At low drain biases, the drain current increases linearly by the drain bias. This region is the linear region. At higher drain biases, the drain current saturates due to pinch-off, and this region is the saturation region.

However, output curve does not reveal crucial parameters like the onset and threshold voltages. We therefore focus on transfer curves to address this issue. We plot the transfer curve in three different scales, one for each set of parameters we wish to extract:

1. I_D on linear scale.

2. I_D on semi-logarithmic scale.

3. I_D on square-root scale.

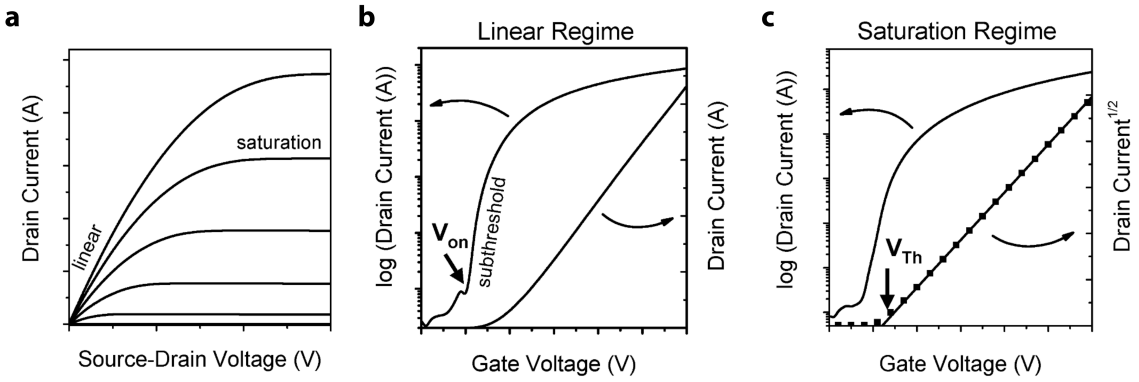

Figure 2.9: Determination of transistor regions and their related parameters. **a** Output curve for various gate voltages. The saturation region gets narrower with the increase in the gate voltage. **b** Transfer curve on semi-logarithmic and linear scales for the left and right y-axes, respectively. Arrow indicates the onset voltage (V_{on}). **c** Transfer curve on semi-logarithmic and square-root scales for the left and right y-axes, respectively. The threshold voltage is determined by the extrapolation of saturation current and indicated by the arrow (V_{Th}). Taken from [51].

The linear scale allows us to reveal the linear region from the slope of the drain current. Nonetheless, it is only possible to estimate the onset voltage (the voltage when the drain current reaches approximately 10 pA) and the subthreshold slope on a semi-logarithmic scale (Figure 2.9b). The latter allows us to reveal the saturation region from the slope of the saturation current and the threshold voltage from its extrapolation (Figure 2.9c). Due to the close relationship between the drain current on square-root scale and the saturation region, the current shown on this scale is defined as the saturation current.

2.3.2 Onset and Threshold Voltages

Once the gate metal is in contact with the semiconductor over the gate insulator, a band bending occurs due to a mismatch between the metal's work function and the semiconductor's Fermi level. This bending can be compensated by an external voltage, which is known as flatband voltage. For an ideal MIS diode, charge accumulation would begin right after the flatband voltage. However, the imperfections in MIS diodes, such as fixed charges, add to the flatband voltage. Consequently, the voltage after these contributions is known as the onset voltage. As depicted in Figure 2.9b, the onset voltage is the characteristic voltage that indicates when the injection of field-effect charges into the semiconductor starts, and the drain current increases rapidly after the off-state region. Since the drain current is relatively small around the onset voltage, the onset voltage must be determined on semi-logarithmic scale.

Compared to the onset voltage, the definition of the threshold voltage is more complex. Since TFTs operate in accumulation mode, we cannot refer to a balance between minority carriers at the interface and majority carriers in bulk, as we do for MOSFET in inversion mode. Therefore, the threshold voltage of a perfect TFT would be zero, but in practice, this is rarely the case. Amorphous silicon (a-Si) TFTs are where the concept of threshold voltage was first discussed by Shur and Hack [53] (sec. 4-12). Its amorphous nature gives rise to disorder and hence trap states. For an a-Si TFT, the threshold voltage was defined as the voltage to shift the Fermi level from the deep trap states into the tail states. Since the a-Si TFTs were dominated by dangling bonds, the hopping in deep trap states dominated the charge transport, resulting in a superlinear increase in saturation current. From this point of view, Horowitz et al. investigated the threshold voltage in organic TFTs, where the organic films were more refined than the a-Si [54]. The authors fabricated two organic dihexyl-sexithiophene (DH6T) TFTs. One of the transistors was left at ambient (Figure 2.10a), while the other was in vacuum (Figure 2.10b). The authors then compared the saturation current characteristics between the two TFTs. They found that the TFT exposed to ambient showed a saturation current with constant slope due to oxygen doping, while the TFT in vacuum showed a superlinearly increasing saturation current. According to Shur's definition, the authors estimated the threshold voltage for the TFT in which the saturation current was increasing superlinearly. As a result, a new parameter, called "zero voltage," was introduced for the TFT that exhibited a constant slope in saturation current.

Over time, researchers paid closer attention to the definition of the threshold voltage in TFTs. Hydrogenation of the a-Si (a-Si:H) significantly reduced its dangling bonds, and the results of a-Si:H TFTs led to a "redefinition" of the threshold voltage. Reduced dangling bonds

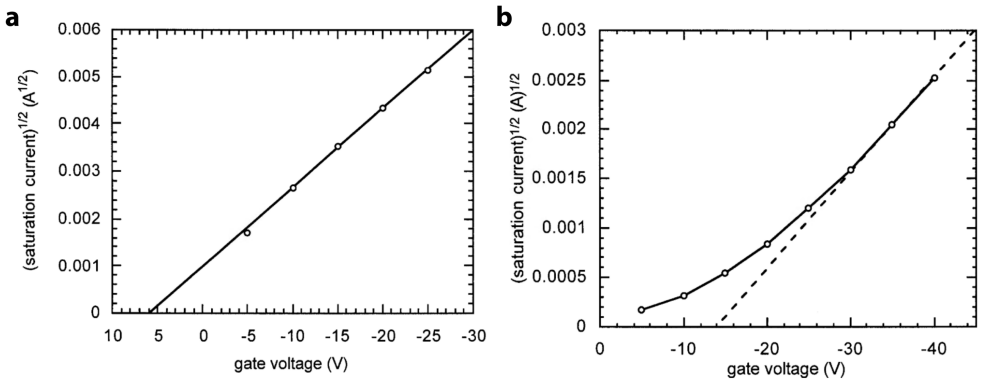

Figure 2.10: Characteristics of DH6T TFTs in ambient and in vacuum. **a** DH6T TFT kept and measured in ambient. The solid line indicates the extrapolation of the saturation current. **b** DH6T TFT kept and measured in vacuum. The dashed line indicates the extrapolation of the saturation current. Adapted from [54].

lowered the deep localized states in the band gap, which reduced the required field-effect charge density to shift the Fermi level to the tail states [55]. A-Si:H TFT characteristics were similar to Horowitz's TFTs in ambient; hydrogenation suppressed the superlinear increase of the saturation current (Figure 2.11). After the findings, Horowitz's "zero voltage" term has finally replaced the "threshold voltage" for TFTs.

After the a-Si:H results, Kalb and Batlogg also confirmed similar behavior for single-crystal organic FET with low disorder [56]. The authors pointed out that the saturation conditions were met in a pentacene single-crystal FET due to the constant slope of the saturation current, allowing the proper estimation of threshold voltage (Figure 2.12a). In contrast, the saturation conditions could not be met in its thin-film form since the slope of the saturation current was not constant (Figure 2.12b). They then claimed that using Shockley equations for mobility calculation was only valid if the threshold voltage could be precisely estimated as shown in Figure 2.12a. In light of these findings, the threshold voltage is now confirmed as the voltage required to establish the transistor regions by shifting the Fermi level from the deep states into the tail states, as suggested by Shur and Hack. This definition is powerful because establishing the operation regions does not require the shift of the Fermi level into the band (extended) states, however, the mobility in tail states would be lower than the band states. Furthermore, one can anticipate a temperature-dependent threshold voltage, as the energetic position of the tail states is significantly dependent on temperature. Consequently, establishing operation regions at lower temperatures would require more gate voltage.

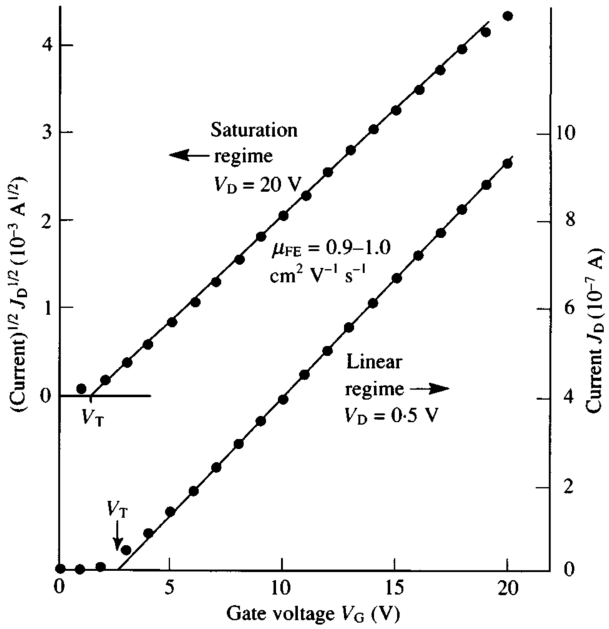

Figure 2.11: Determination of linear and saturation regions in a-Si:H TFT. The transfer curve on the square-root and linear scales are represented on the left and right y-axes, respectively. The estimated threshold voltages are indicated by V_T. Adapted from [55].

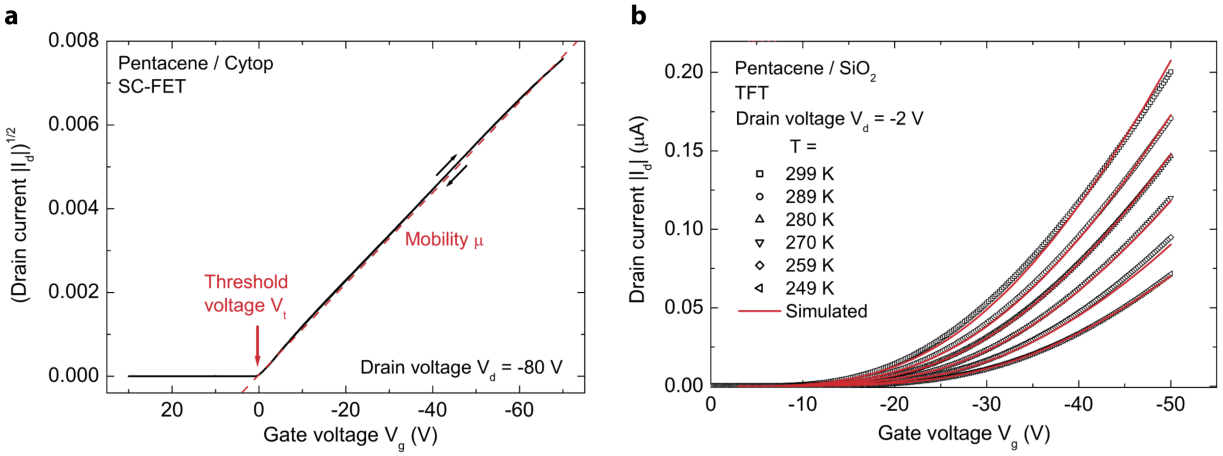

Figure 2.12: Transistor characteristics of pentacene single crystal and thin-film transistors. **a** Square-root plot of the transfer curve of pentacene single-crystal FET on CYTOP dielectric at room temperature. The red dashed line indicates the extrapolation of saturation current. **b** Linear plot of the transfer curve of pentacene TFT on SiO_2 for various temperatures. Adapted from [56].

2.3.3 Subthreshold Region

The subthreshold region covers below the threshold voltage, where field-effect charges fill deeper traps (several k_BT). In this region, a relatively low amount of charges can reach the tail states at room temperature. Consequently, the subthreshold region links the off-state region of a transistor to its saturation region. As depicted in Figure 2.9b, the subthreshold region is determined by the slope of the drain current on a semi-logarithmic scale. The characteristic parameter of the subthreshold region -the subthreshold slope- is defined as the gate voltage required to increase the drain current ten-fold (a decade). The subthreshold slope can be expressed as follows:

$$S = (ln10)\left(\frac{k_BT}{q}\right)\left(1+\frac{C_{int}}{C_{ox}}\right) \tag{2.8}$$

where C_{int} represents the capacitance of the interface states. The term comes from the similarity of a-Si dangling bonds and silicon oxide surface dangling bonds, where both led to the superlinear increase of saturation current, contributing to the subthreshold slope.

Due to the disordered nature of thin films, any disorder-related deep states can also contribute to total deep trap DOS. Therefore, Kalb and Batlogg added the capacitance of the bulk (material) deep states to the expression [56],

$$S = (ln10)\left(\frac{k_BT}{q}\right)\left(1+\frac{C_{int}+C_{bulk}}{C_{ox}}\right) \tag{2.9}$$

The thermionic limit of the subthreshold slope is approximately 60 mVdec^{-1} (at room temperature). Either by increasing the oxide capacitance or decreasing the interface/bulk states capacitance or by doing both, the thermionic limit can be achieved. We could quantify the capacitance of deep trap DOS by calculating any deviation from the thermionic limit. Although it does not provide information about the relative energetic positions distinctly, Equation 2.9 is still powerful; once the transistor is fabricated, we have an estimation of the deep trap DOS capacitance.

2.4 Role of Gate Capacitance in TFTs

As discussed, transistors can be improved by removing the deep states or by increasing the oxide capacitance. The former requires improvements on material and interface quality, the latter is a fabrication-based approach. This section examines the need for a higher oxide capacitance over various examples.

Gutierrez et al. recently emphasized the significance of oxide capacitance for the electronic band gap determination of TMD nanosheets from their TFT characteristics [57]. In this novel method, the authors fabricated TMD ($MoTe_2$) TFTs in which either electrons or holes could be accumulated, controlled by the gate voltage (Figure 2.13a). Three different gate stacks (300 nm SiO_2, 20 nm SiO_2, and ionic electrolyte) were utilized in the fabrication of the TFTs, yielding gate capacitances of 12 nFcm^{-2}, 170 nFcm^{-2}, and 50,000 nFcm^{-2}. The band gap of the semiconductor was determined by measuring the transconductance gap between electron and hole accumulations. The estimated band gaps of $MoTe_2$ were 50 V, 2.8 V, and 0.85 V for transistors gated by thick oxide, thin oxide, and ionic electrolyte, respectively, while the theoretical estimation for the band gap was around 0.85 V. The results indicated that the ionic electrolyte gated TFT matched with the expected band gap, where its subthreshold slope was also the steepest (135 mVdec^{-1}). Therefore, higher capacitance not only lowered the gate operation range by decreasing the subthreshold slope but also improved the reliability of the electrical characteristics.

The authors concluded that the relation between the applied gate potential and the Fermi level was the key to understanding the observed phenomena. Equation 2.10 represents the relationship between the gate potential (V_G), Fermi level (E_F), and electrostatic potential (ϕ):

$$e\Delta V_G = \Delta E_F + e\Delta\phi = \Delta E_F + \left(\frac{e^2\Delta n}{C_{ox}}\right) \tag{2.10}$$

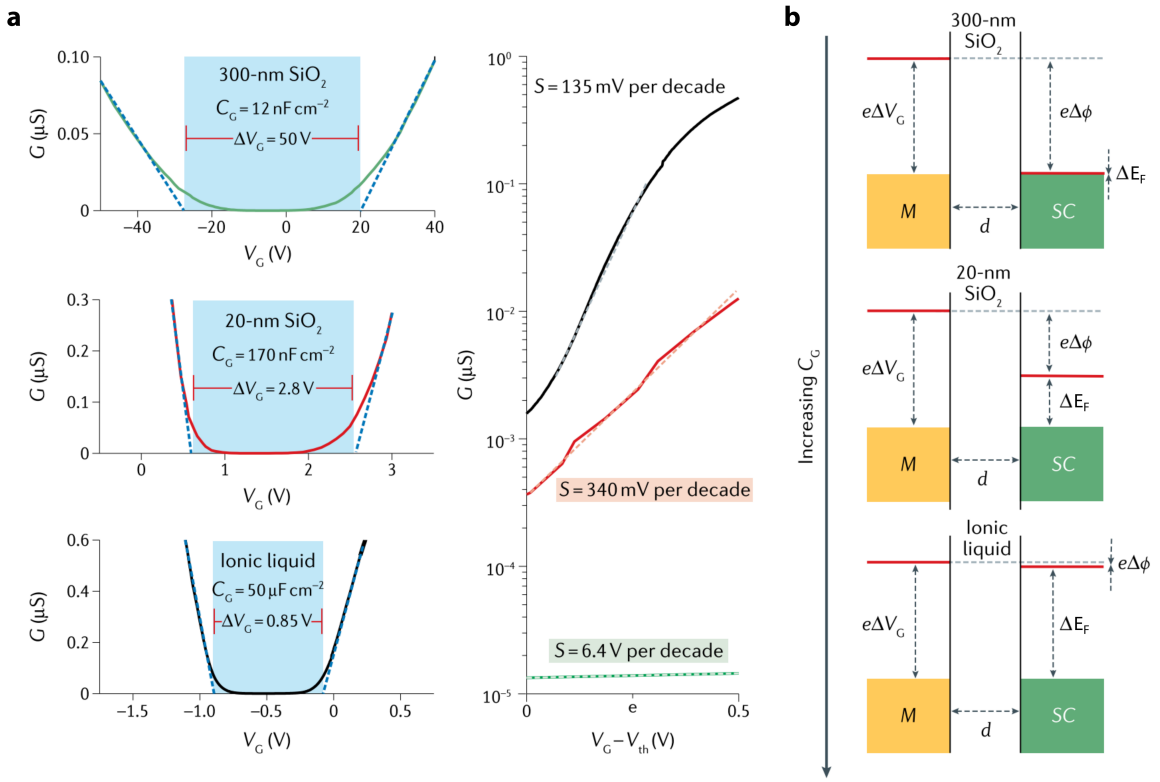

Figure 2.13: Effect of oxide capacitance on the band gap determination of $MoTe_2$ crystals. **a** Left: Determination of the transconductance gap from the extrapolations of electron and hole transconductances. The black, red, and green lines represent the highest to lowest capacitance (C_G). The dashed lines indicate the extrapolation. Right: Subthreshold slopes (S) of electrons as a function of oxide capacitance. **b** The effect of gate potential (V_G) on the Fermi level (E_F) in the presence of electrostatic potential (ϕ). M and SC indicate the contact metal and the semiconductor, respectively. Adapted from [57].

The latter represents the trap states (Δn). Ideally, there should be no trap states in the band gap, and the electrostatic potential is zero. As a result, any change in gate voltage would entirely shift the Fermi level. However, in the presence of trap states, Δn and hence the electrostatic potential is no longer zero. Therefore, the change in gate voltage only partially reflects the shift in the Fermi level since the field-effect charges start filling the trap states. The Fermi level is then pinned [53, 58] until the trap states get filled. The pinning strength depends on how high the trap DOS is, compared to the field-effect charge density. Delocalization might occur only at very high gate voltages in the case of low oxide capacitance.

Nevertheless, higher oxide capacitance gives rise to higher field-effect charge density, so the trap DOS can be filled even at lower gate voltages, which diminishes the electrostatic potential (Figure 2.13b). Then, the shift in gate voltage reflects the shift in chemical potential again, even in presence of the trap DOS. As a consequence, the contest between the trap DOS

and the field-effect charge density yields the same outcome as the subthreshold slope: To improve the effect of gate voltage, either the trap DOS must be reduced or the field-effect charges must overcome the trap DOS.

In addition, Shur and Hack investigated the role of gate voltage in a-Si:H TFTs for a fixed oxide capacitance. For an a-Si:H TFT, right after the onset voltage, the Fermi level is almost pinned because all field-effect charges start filling the deep trap states. Increasing the gate voltage increases the field-effect charges, filling the deep trap states, thereby shifting the Fermi level toward the tail states. The Fermi level would continue to shift as the gate voltage increases, and once it reaches the tail states, the transistor operation regions are established. Through thermally activated hopping, a small percentage of charges would reach the conduction band in this case. In the extreme limit, however, bandlike transport is also achievable, if the field-effect charges would be able to fill all the trap states under the extended states (band edge). Under this condition the charges do not need thermal activation to reach the conduction band any further. When this condition is met, the Fermi level would be positioned within the conduction band. Since the shallow trap states increases with proximity to the band edge, a relatively high density of field-effect charges is required to shift the Fermi level inside the tail states. Therefore, to achieve bandlike transport in a-Si:H TFTs, gate voltages of 50 V to 100 V are necessary for 100 nm-thick silicon oxide, which has a capacitance of 31 $nFcm^{-2}$. The transition from tail states to extended states is known as the Anderson transition (also known as the trap-free limit in diodes), and it has been observed in a-Si:H by Leroux and Chenevas-Paule [59], around predicted voltages by Shur and Hack, as depicted in Figure 2.14. Free carrier motion in a-Si:H TFT was only reported in that article, and other sources have not confirmed it yet [55].

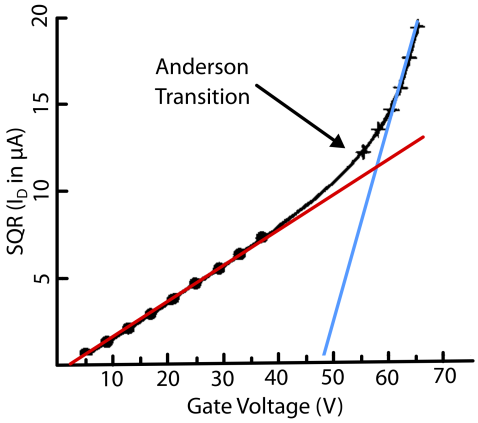

Figure 2.14: Square-root plot of the transfer curve of a-Si:H TFT on 100 nm-thick SiO_2 with low volume and interface trap states. Red and blue lines indicate the extrapolation of the saturation current before and after the Anderson transition, respectively. Adapted from [59].

2.5 Non-Ideal Characteristics in TFTs

While the TFT is a powerful device to study the charge transport in semiconductors, it is still limited by the trap states and contact effects, both of which lead to non-ideal characteristics and hence inaccurate mobility values. In this subsection, we discuss the origins of non-ideal characteristics in TFTs. As OSCs tend to be more disordered, many of the concepts were initially developed for organic TFTs; however, the conclusions from organic TFTs can be applied to inorganic TFTs under similar conditions.

In their commentary, Choi et al. investigated the challenges for accurate mobility estimation under several non-idealities [52], as shown in Figure 2.15. The authors focused on both linear and saturation regions, which are interchangeable. However, our focus here is on the saturation region for two reasons. First, all operation regions can be revealed on the square-root scale. Second, the saturation current provides information about the threshold voltage; the proper estimation of the threshold voltage is a requirement for the saturation condition, as discussed.

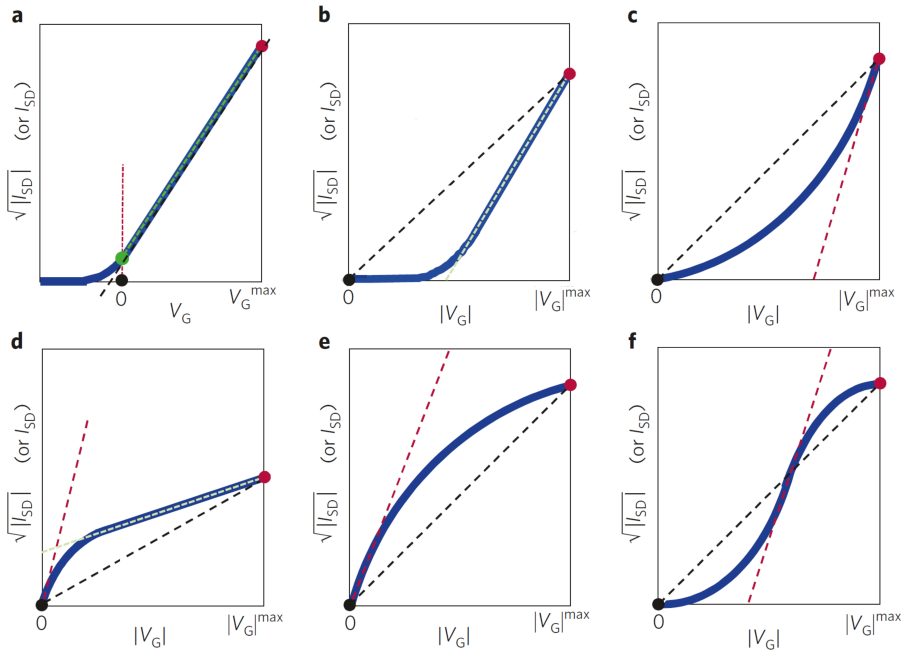

Figure 2.15: Mobility determination in the presence of non-ideal transistor characteristics. **a** Ideal transistor characteristics, **b** close-to-ideal transistor characteristics with shifted threshold voltage, **c** transistor characteristics exhibiting superlinearly increasing current, **d** transistor characteristics exhibiting contact hump curve, **e** transistor characteristics exhibiting parabolic curve, and **f** transistor characteristics exhibiting S-shaped curve. The red and green dashed lines indicate possible extrapolations of the saturation current, wherein the black dashed line indicates ideal extrapolation. Adapted from [52].

The authors noted that contact effects, trap states, or short channel effects could give rise to various non-ideal characteristics. Starting from the ideal conditions, we now reveal some of the non-ideal characteristics. Figure 2.15a represents the ideal TFT characteristics under saturation conditions. The slope of the saturation current was constant, and its extrapolation indicated zero threshold voltage. In this case, an accurate estimation of the saturation mobility was possible for any gate voltage. Figure 2.15b represents the second case; the threshold voltage was shifted, but the subthreshold region was still negligible. The slope of the saturation current was also constant, providing an accurate estimation of the threshold voltage. Nonetheless, mobility must be corrected due to the threshold shift.

The subthreshold region was no longer negligible once the TFT suffered from deep trap states (Figure 2.15c). Due to the difficulty in maintaining a constant slope for the saturation current, the threshold voltage could not be determined, and thus the saturation region could not be achieved.

As the quality of the semiconductors improved and the trap states were lowered, contact effects become more evident [60]. Figure 2.15d represents a typical non-ideality caused by the contact effects. In this particular case, the slope of the saturation current became constant after a "hump". According to Brittle et al., this hump was caused by the competition between the channel and contact resistances; the gate bias electrostatically promoted thermionic emission after the hump, establishing the proper saturation region [60].

Another type of contact effect is shown in Figure 2.15e, where the saturation current increased in a parabolic fashion. Parabolic behavior might occur if the drain potential was "resistively" dropped on the contacts rather than the channel. Consequently, TFT operated in the linear region instead of the saturation region. In the presence of a pronounced subthreshold region, the TFT's behavior would even exhibit an S curve, as shown in Figure 2.15f.

The commentary was based on the proper estimation of mobility under the non-ideal conditions, so the focus was on mobility correction factor. A more quantitative study was carried out by Liu et al. by using 2D calculations as summarized in Figure 2.16 [61]. The authors used 10 $nFcm^{-2}$ as oxide capacitance, channel length as 80 µm with a semiconductor thickness of 40 nm, as shown in Figure 2.16a. The authors investigated the sources of non-idealities in light of contact effects and disorder, separately and in combination. The contact effect was represented by the work function offset with the valence band (or HOMO for OSC) limiting hole injection (Figure 2.16b), while disorder was represented by the tail states (Figure 2.16c). μ_{int} and μ_{sat} indicate the initial and saturation mobilities, respectively.

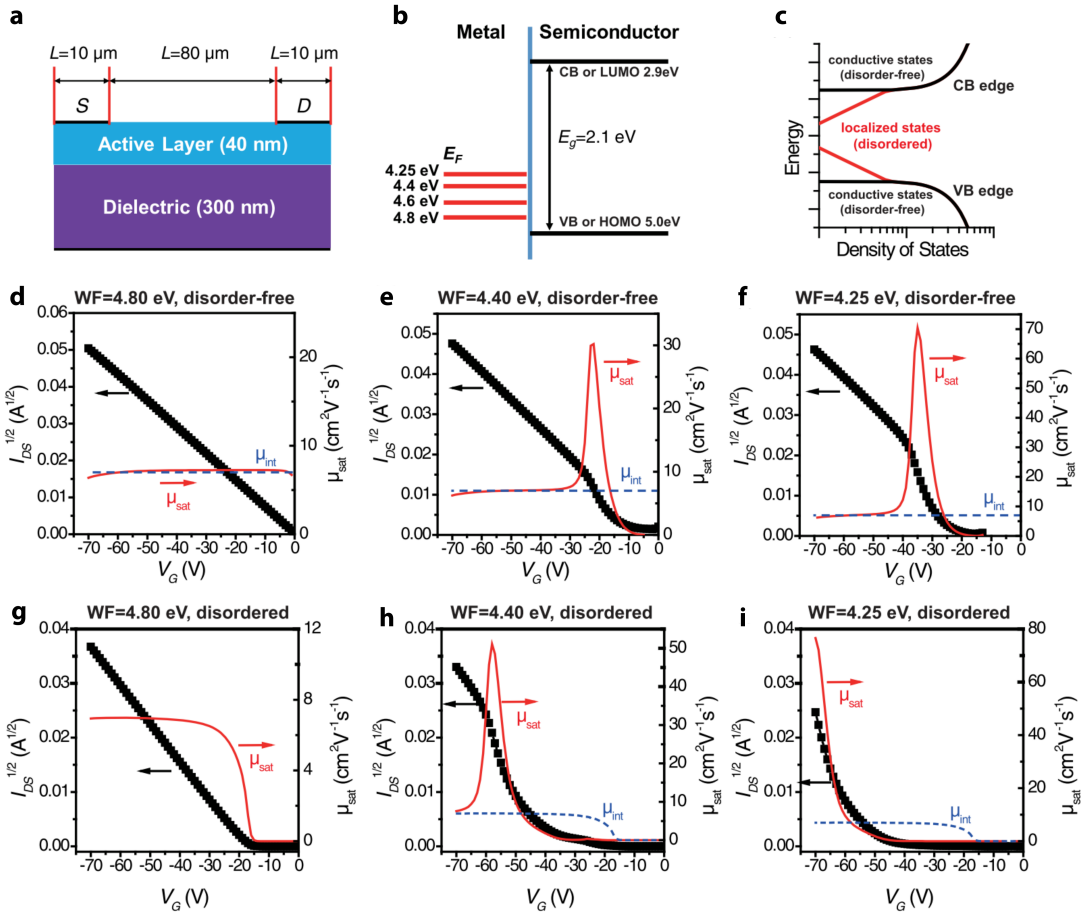

Figure 2.16: Quantitative calculations of non-ideal transistor characteristics in the presence of contact barrier and disorder. **a** Illustration of the transistor. **b** Illustration of the Schottky barrier contacts with various metal work functions. **c** Illustration of the disorder. **d-i** Saturation current and mobility characteristics under various contact and disorder conditions. μ_{int} and μ_{sat} indicate the initial and saturation mobilities, respectively. Adapted from [61].

Figure 2.16d shows the ideal characteristics of a saturation current. The ideal saturation conditions were met when the work function of the metal and the valence band were well-matched. Although the threshold voltage was shifted to negative voltages when tail states were introduced (Figure 2.16g), the calculated mobility value was still very close to that under ideal conditions, which contradicted to the assumptions of the previous commentary. In the case of higher mismatch by the increase in the metal work function, the charge injection became limited by the contact (Figure 2.16e). This limited injection gave rise to a distinct superlinear increase of saturation current like in the subthreshold region but in the absence of disorder. Nevertheless, once the gate bias promoted thermionic emission, the saturation current regained its constant slope. The point of promoted thermionic emission was called

the contact hump and caused a mobility peak. However, accurate calculation of mobility was still possible in the mobility plateau that followed the peak. In the presence of disorder, the subthreshold-like region shifted the hump further because deeper states were needed to be filled first, while the injection was limited by contact (Figure 2.16h).

In the presence of localized states with the highest mismatch, it was possible to reach the extreme limit (Figure 2.16i). Here, mobility did not exhibit a plateau, furthermore, not even the peak of mobility was ever reached. There was no way of estimating mobility accurately for given conditions, not even by applying the correction factor. The results again pointed out that the proper threshold voltage estimation is necessary for discussion on any mobility value.

2.6 Advanced Transistor Architectures: Ambipolar Transistors

Ambipolar transistors are a novel type of TFT in which electrons and holes accumulate in the semiconductor separately or simultaneously. Because of this, they are very appealing from a technological standpoint. Firstly, ambipolar transport is compatible with complementary metal-oxide-semiconductor (CMOS) technology, as it can be operated as either n-type or p-type. In addition, the transistor can be operated as a light-emitting field-effect transistor (LEFET) because both charges can accumulate in the semiconductor simultaneously. Moreover, ambipolar transistors allow us to investigate the charge transport of both carriers in a single transistor.

Ambipolar TFTs can be fabricated in a variety of ways. The most prevalent method is to employ an ambipolar semiconductor, where both charges are injected into the same semiconductor. For the fabrication of an ambipolar transistor with an ambipolar semiconductor, there are two possible approaches:

1. Employing a small band gap semiconductor and utilizing the same contact material for electron and hole injection.

2. Employing a large band gap semiconductor and utilizing asymmetric contact material to separate electron and hole injection.

Separated electron and hole injection by asymmetric contacts led to a development of a new method. In this third method, individual electron and hole conductors are combined for the ambipolar conduction. There are benefits and drawbacks to each of these methods, but their discussion goes beyond this dissertation.

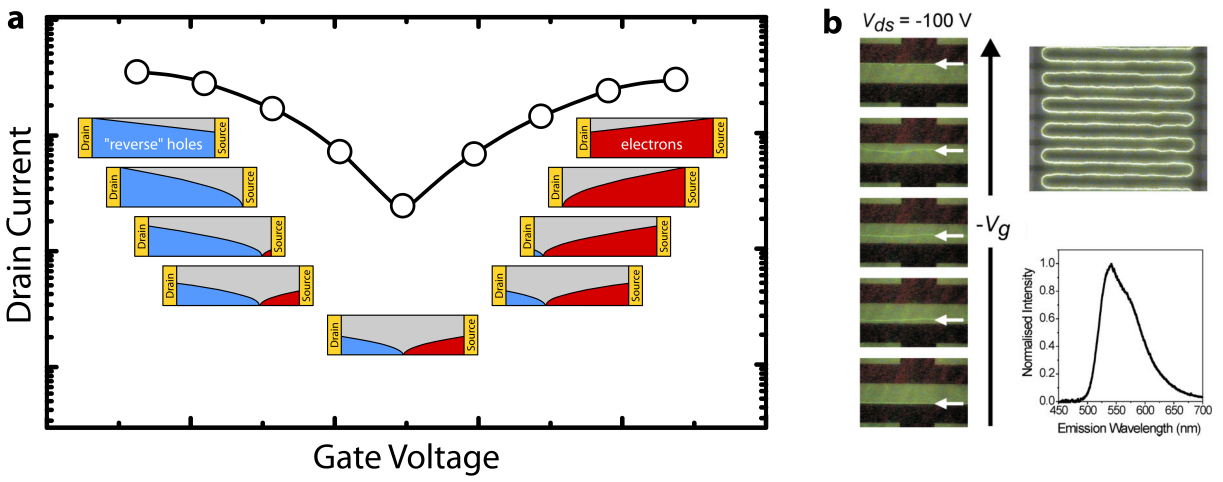

Figure 2.17: Illustration and investigation of charge transport in ambipolar transistors as a function of gate bias. **a** Illustration of gate bias-dependent charge distribution in an ambipolar semiconductor. **b** F8BT light-emitting field-effect transistor. The white arrow represents the recombination zone as a parameter of gate bias. Adapted from [25].

The ambipolar behavior is easier to comprehend if we begin with a unipolar transistor and then extend it to ambipolar transistor (sketched in Figure 2.17). If the drain bias for an n-conductor TFT is sufficiently less than the gate bias, then the transistor operates in the linear region. A decrease in gate bias would result in electron saturation. Further decrease in the gate bias would only move the pinch-off point toward the channel since contacts prevent hole injection. At this point, holes are injected into the semiconductor from the "drain" contact in an ambipolar transistor. Considering that electrons are saturated, holes would also be saturated. Therefore, if one charge goes beyond saturation, ambipolar transport no longer exists. Since both charges accumulate within the semiconductor, light emission can be observed in ambipolar TFTs. Therefore, for electroluminescent semiconductors, the term "recombination zone" (RZ) replaces the pinch-off point. For example, Zaumseil et al. demonstrated a F8BT (Poly[(9,9-dioctylfluorenyl-2,7-diyl)-alt-(benzo[2,1,3]thiadiazol-4,7-diyl)]) LEFET with precise control of RZ from one contact to the other, tuned by the gate voltage (Figure 2.17b) [25].

Since ambipolar TFTs differ significantly from unipolar TFTs, their electrostatics must be revised. Figure 2.18 depicts the sketch and the saturation current characteristics of a unipolar DNTT TFT. The initial bias conditions (negative drain and gate voltages) were setted up for regular hole accumulation. Typically, in case of reverse polarity for drain bias, the electric field

could no longer drift holes. In practice, however, the hole transport took place according to the equivalent circuit: holes became injected from the drain electrode and extracted from the source electrode. This equivalent circuit is therefore known as ”reverse” electrostatics.

The illustration represents the initial conditions as drain voltage was -3 V and V_G - V_{Th} was -1 V. In case of reverse polarity, holes would experience the equivalent circuit where the source contact being -3 V. As a result, the “effective” V_G - V_{Th} became +2 V. Figure 2.18b represents the saturation current characteristics under regular and reverse polarity. The change in the polarity of the drain bias shifted the threshold voltage by the as much drain bias. Consequently, the reverse charges in the ambipolar transistor would always exhibit a drain bias-dependent threshold voltage shift, which is the most essential feature of the ambipolar transistor.

Now, we investigate the threshold voltage shift in an ambipolar transistor. Since we can adjust the threshold voltage of the reverse charges by drain bias, we can adjust the crossing point of the electron and hole threshold voltages. Therefore, the ambipolar current dip and its value becomes a function of the drain bias (for reversed holes) according to,

$$I_D = \left(\frac{W}{2L}\right) C_{ox}(\mu_{sat,e}(V_G - V_{Th,e})^2 + \mu_{sat,h}(V_D - (V_G - V_{Th,h}))^2) \tag{2.11}$$

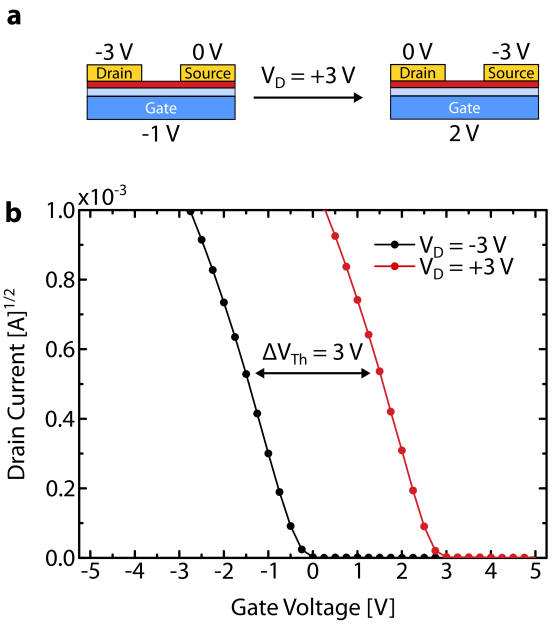

Figure 2.18: Illustration and investigation the polarity-dependent saturation current characteristics of the DNTT TFT. **a** Illustration of the proper (left) and the equivalent (right) circuit depending on the drain bias polarity. Red and light blue regions represent the semiconductor and the gate oxide, respectively. **b** Saturation current characteristics of DNTT TFT under positive and negative drain bias. Threshold voltage shift is indicated as ΔV_G.

where $\mu_{sat,e}$ and $\mu_{sat,h}$ are electron and hole saturation mobilies, $V_{Th,e}$ and $V_{Th,h}$ are electron and hole threshold voltages, respectively. Figure 2.19 depicts the transfer curve of a quinoidal biselenophene (QBS) organic ambipolar transistor on semi-logarithmic scale under various drain biases [62]. The left and right sides of the graph represent negative and positive drain biases, respectively.

The ambipolar dip followed the trend of the drain current by the increase in negative drain bias. Here, the electrons were reverse charges, and an increase in drain bias effectively changed the electron threshold voltage. This increased the intersection between the electron and hole threshold voltages, and the ambipolar current increased. We observed similar results for positive drain biases; here, the reverse charges were holes, so the ambipolar dip shifted towards right, following the drain current trend.

The characteristics of black curve is also worthy of discussion since it represents the ambipolar transistor at low drain bias limit. We noticed that the ambipolar dip current was comparable to the background noise level. Here we reached the limit where neither holes nor "reverse" electrons could be saturated under the current gate bias interval. Consequently, this condition was referred as the off-state of the ambipolar TFT. An important conclusion followed from this observation: ambipolar conduction only occurs when the drain bias is larger than the difference in threshold voltage between holes and electrons.

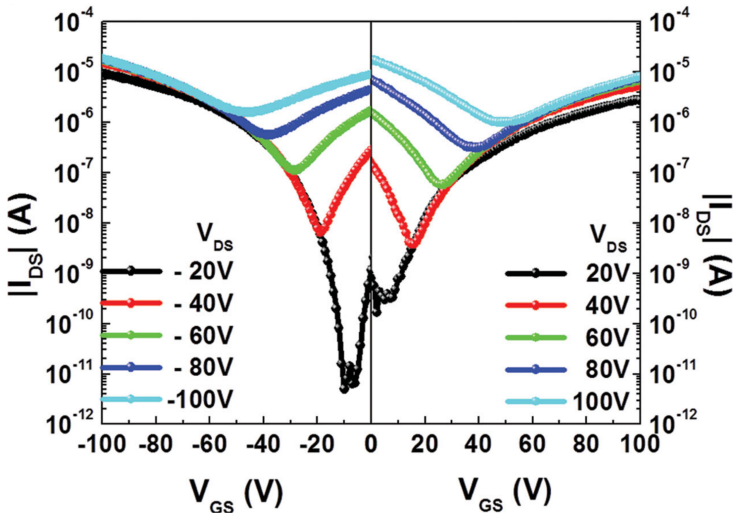

Figure 2.19: Drain bias-dependent ambipolar current behavior in QBS TFT. The left and right sides of the graph represent negative and positive drain biases, respectively. Taken from [62].

3

Transferable Organic Semiconductor (OSC) Nanosheets

"Semiconductor research and the Nobel prize in physics seem to be contradictory since one may come to the conclusion that such a complicated system like a semiconductor is not useful for very fundamental discoveries. Indeed, most of the experimental data in solid state physics are analyzed on the basis of simplified theories, and very often the properties of a semiconductor device is described by empirical formulas since the microscopic details are too complicated."

— Klaus von Klitzing

3.1 The Need for Transferable OSC Nanosheets

Crystallization of organic small molecules on well-defined surfaces

Small molecule OSCs are utterly advantageous for transistors owing to their low deposition and substrate temperatures, scalability, and thickness control. Nonetheless, the crystallization of small molecules is highly surface-dependent in terms of grain size, and molecular orientation as shown in Figure 3.1. These variations led to a significant barrier for the fabrication

of organic TFTs in the BC configuration [63]. Researchers examined this issue from a variety of angles, and the most successful approach today is the modification of gold surface with self-assembled monolayers (SAM).

Employing the SAM modification brought many advantages. For instance, the gold surface is vulnerable to environmental contamination, although it is a noble metal. These contaminations alter the work function of gold surface once it is exposed to ambient [64]. Here, SAM passivates the gold surface chemically. In addition, SAM molecules are fluorine- or hydrogen-terminated, which reduces surface energy of gold. Lower surface energy is crucial for promoting the crystallization of small molecules into highly ordered organic films (Figure 3.1).

Furthermore, SAM can tune the work function of gold. By using different SAM molecules, the work function can be adjusted within a range of about 1.5 eV [65]. This tunability of the work function allows for a better match between the highest occupied molecular orbital levels of organic semiconductors. Utilizing the optimal combination of SAM (as PFBT) and a small molecule OSC (as DPh-DNTT), Borchert et al. achieved record-low contact resistance for BC transistors, outperforming even TC transistors [66].

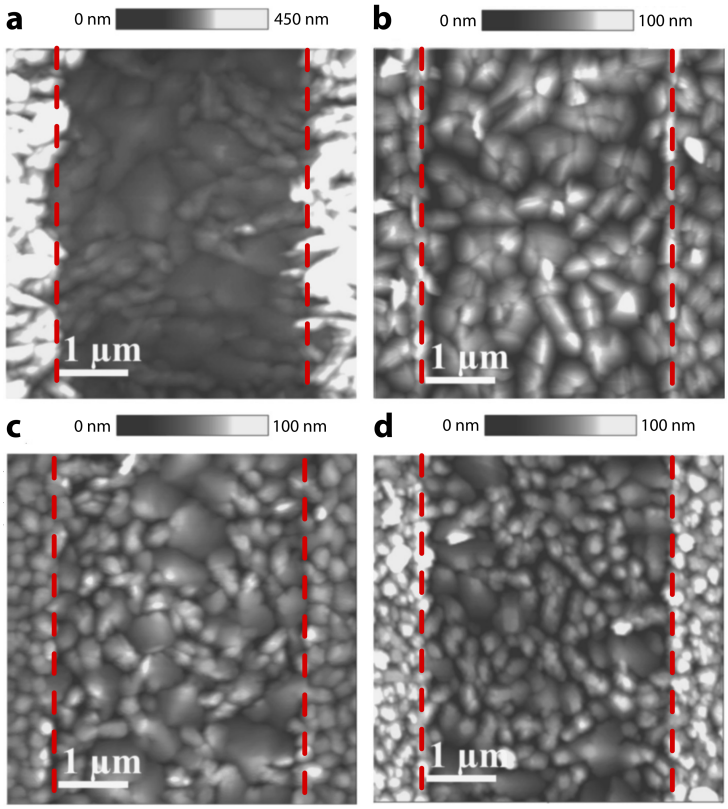

Figure 3.1: Crystallization of pentacene on untreated and SAM passivated gold revealed by AFM. **a** untreated gold, **b** C_7-SAM passivated gold, **c** C_{12}-SAM passivated gold, and **d** AnT-SAM passivated gold. Red dashed lines indicate gold/oxide intersections. Adapted from [63].

Crystallization of organic small molecules on 2D materials

Although SAM promotes the crystallization and hence the performance of BC organic TFTs on well-defined surfaces, the method cannot be generalized beyond this point as it is. Two seminal studies, one from each TFT architecture, illustrate the small molecule growth problem on 2D materials in striking detail. In the first article, Lee et al. fabricated BC pentacene TFTs, but with graphene contact in place of the traditional metal contacts [67]. The authors focused on the effect of graphene's cleanliness on the crystallization of pentacene and thus fabricated two distinct transistors. For the first transistor, graphene was utilized as-fabricated, whereas for the second transistor, graphene was annealed to remove PMMA residues prior to pentacene deposition (Figure 3.2). Surprisingly, the performance of the TFT with annealed graphene contacts was inferior. Using atomic force microscopy (AFM) for morphology inves-

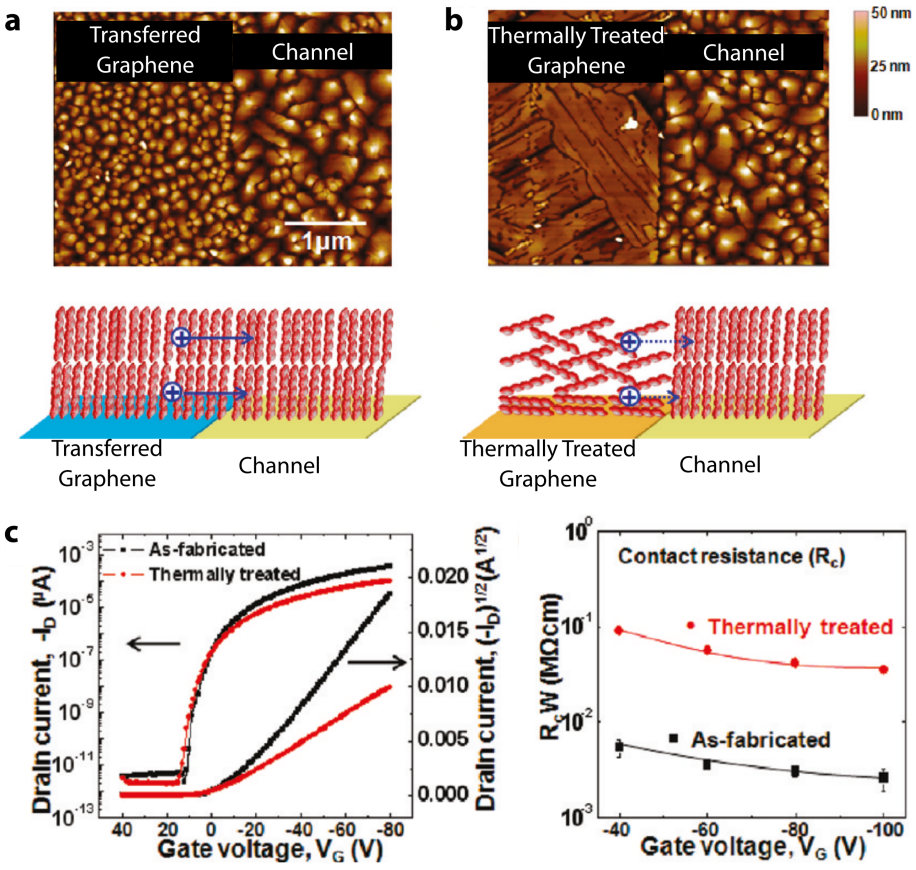

Figure 3.2: Untreated and thermally treated graphene bottom contact for pentacene TFT. Atomic force micrographs of pentacene thin film on **a** untreated and **b** thermally treated graphene contacts with corresponding illustrations of pentacene packing motifs. **c** Transistor characteristics of pentacene TFTs with untreated and thermally treated graphene bottom contacts. Left: Transfer curves on a semi-logarithmic scale. Right: Contact resistance analysis of the transistors. Adapted from [67].

tigation, the authors demonstrated that as-fabricated graphene promoted the crystallization of pentacene (Figure 3.2a). In contrast, the morphology of pentacene on annealed graphene exhibited needle-like packing motif (lying-down phase) as shown in Figure 3.2b, similar to untreated gold. The conclusion was that the PMMA residues promoted nucleation, enabling comparable morphology between the contacts and transistor channel. As a result of the lowered contact resistance, the transistor performance was improved (Figure 3.2c).

In the second study [30], Jariwala et al. demonstrated a gate-tunable vdW p-n junction by stacking pentacene with MoS_2. Here, the transistor consisted of three distinct surfaces—gold as the contact, SiO_2 as the transistor channel, and MoS_2 as the vdW heterojunction. As Figure 3.3 depicts, pentacene crystallized differently on each surface, limiting the device performance. One particular question arises after all these investigations: Is it possible to "transfer" these small molecule films to produce stable, highly ordered films to make them independent of surface properties? In this chapter, we address this question by realizing the transferable small molecule OSC nanosheets, including investigating their structural and electrical characteristics. Some of the findings in this chapter are published and patented [68].

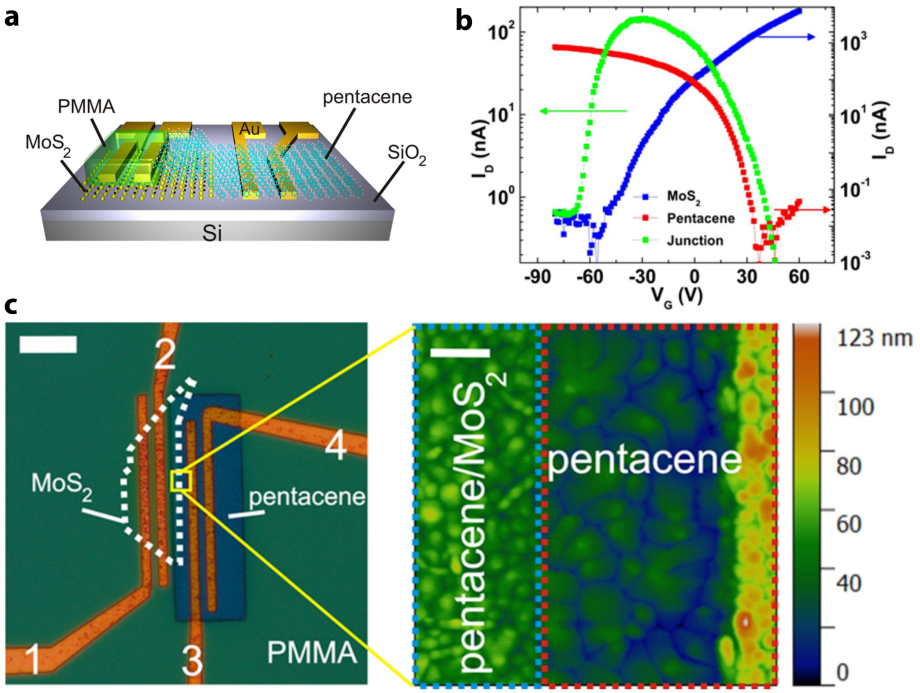

Figure 3.3: Gate tunable MoS_2/pentacene p-n heterojunction. **a** Illustration of the transistor. **b** Transfer curves of the unipolar pentacene transistor, unipolar MoS_2 transistor, and the p-n heterojunction on a semi-logarithmic scale. **c** Optical microscopy image with a close-up atomic force micrograph of the p-n heterojunction, demonstrating crystallization of the pentacene on the MoS_2 surface, gate oxide, and gold electrode, from left to right. Adapted from [30].

3.2 Realization of the OSC Transfer Method

3.2.1 Releasing the Nanosheets

The PMMA-assisted transfer method developed for 2D materials was inspirational for small molecule OSC films. However, a direct adaptation of the method for OSCs was challenging for the following reasons: First, acetone is incompatible with OSC, which is necessary for removing the PMMA after transfer. In addition, the OSC decomposition temperatures precluded using a subsequent annealing step to remove the residues, as was possible for the graphene. Second, the chemicals used to etch the oxide layers would harm the OSC film. To address these points, we revised the method for OSCs:

- Using water-soluble polymer as a sacrificial layer would allow us to release the film with water, which is harmless for OSC.
- Immersing the substrate to control the dissolving process to skip using the supporting layer.

First attempt: Immersion

We started by spin-coating polyvinyl alcohol (PVA), a well-known water-soluble polymer, on a Si substrate. We evaporated 50 nm-thick pentacene film on the PVA. We then immersed the substrate in water (Figure 3.4a) to release the pentacene film. While the proof-of-concept was successful, the method had low reproducibility. The poor solubility of PVA in water increased the release time, hence the risk of rupturing the nanosheet. We substituted PVA with poly-

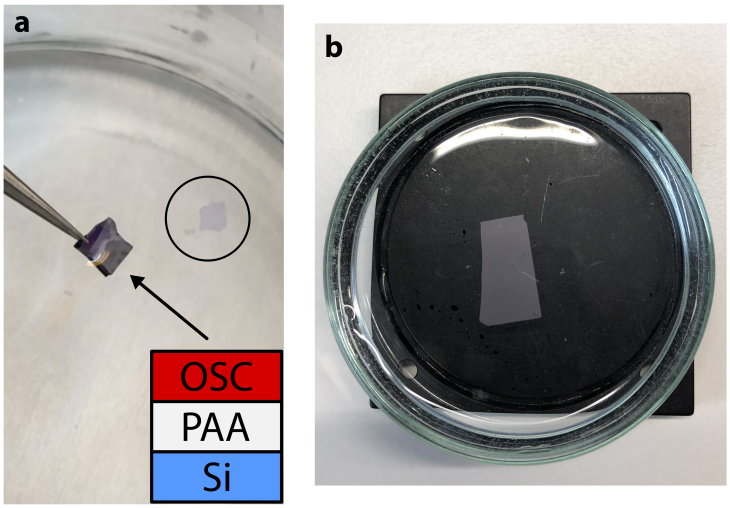

Figure 3.4: Nanosheet release by immersion to water. **a** Picture of the sample during immersion. Free floating nanosheet (approximately 16 mm^2) is encircled by a black circle . The inset represents the illustration of the substrate (not to scale). **b** Free floating nanosheet in sizes of 7 mm x 15 mm.

acrylic acid (PAA), which had higher solubility. This replacement accelerated the release and stabilized the immersion. Releasing the nanosheet from its substrate at a 1:1 ratio was possible (Figure 3.4b), however, reproducibility was still poor. In addition, this method did not work for other small molecules like DNTT. The preliminary results indicated that the approach was promising, but there was still room for improvement.

Second attempt: Dropping to water

In our second attempt, the main objective was to avoid immersion. In order to achieve this, we dropped the samples on the water in a beaker. This method increased stability compared to immersion but became sensitive to the dropping height and substrate's weight. The substrates were hydrophilic due to the oxygen plasma treatment for uniform PAA coating. Therefore, the substrate tended to sink after being dropped on the water, which was the driving force for dissolving PAA. Nonetheless, the nanosheet tended to float on the surface of the water due to its hydrophobic nature [69]. In order to continue the release, the substrate's weight needed to be compensated by the floating nanosheet as sketched in Figure 3.5a. This compensation caused stress on the nanosheet, increasing continuously as the substrate submerges. In addition, dissolving from both sides generated additional stress centers at the merging points depicted in Figure 3.5a.

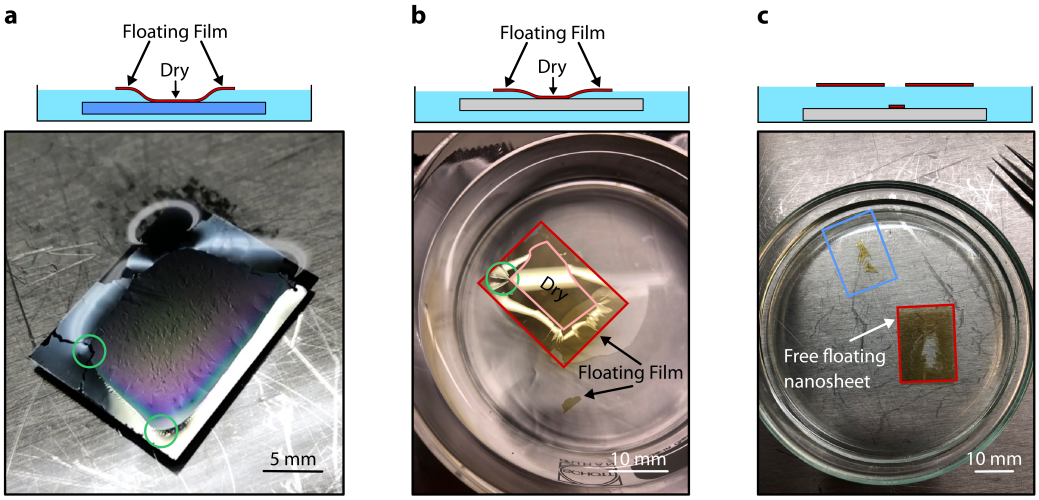

Figure 3.5: Nanosheet release by dropping to water. **a** Illustration and picture of Si substrate (blue) dropped on the water. The green circles indicate stress points. **b** Illustration and picture of borosilicate substrate (gray) dropped on the water. The tan line indicates the dissolving border. **c** Illustration and picture of a free floating C_{60} nanosheet, broken from its center during release. The blue and red rectangles represent the substrate and the nanosheet, respectively.

The increased stress during the release forced the nanosheet to crack through the middle, sinking the remaining film with the substrate. To lessen the weight and thus the bending of the nanosheet, we substituted silicon wafers with ultrathin borosilicate glass (Figure 3.5b). This substitution allowed us to reduce the weight and hence reproducible patches of nanosheets, even enabling the release of C_{60}. However, as shown in Figure 3.5c, we could not eliminate the nanosheet cracking in the substrate's center. In summary, we increased the reproducibility, the patch size, and the family of transferable small molecules but still needed to catch up in demonstrating more brittle films like DNTT in 1:1 size with the substrate for the generalization of the method.

Third attempt: Side injection of water

Carrying the substrate was the crucial step overlooked on the second try. We made several attempts, like introducing a beaker with a post inside to hold the substrate from sinking. Even with this, we could not release the nanosheet in a controlled fashion. Therefore, we opted for driving water from the side while placing the substrate on a glass carrier (Figure 3.6a). In this way, we could regulate the nanosheet's bending during the release by the amount of water reservoir. We then contacted the substrate and the water reservoir to start the dissolution. Water wetted towards the hydrophilic substrate with an advancing angle, and the nanosheet was gently released (Figure 3.6b). After the first two attempts, the procedure was significantly improved that any small molecule, including DNTT, could be released in 1:1 size with the substrate. In the case of pentacene, the largest releases reached 3 inches (1:1) in diameter while remaining only 20 nm thick. It was even possible to transfer bilayer stacks, like C_{60} on pentacene (Figure B.1).

We investigated wetting geometry in order to optimize the release process. The contact angles for substrate, glass carrier, and OSC film were <7°, 50°, and 80° [69], respectively (Figure B.2). The contact angle difference between the glass and the substrate created the surface tension gradient force [70]. This force drove the water to advance on the substrate once the water reservoir and the sample were in contact (Figure 3.6b). Release of the nanosheet proceeded until the PAA was entirely dissolved and the nanosheet floated freely on the water (Figure 3.6c).

Since the contact angle difference between the glass carrier and the substrate drove the process, the glass carrier played an important role. If the carrier would be more hydrophobic (by using a plastic carrier instead of glass carrier), the bending would increase due to a higher gradient force and cause the film to rupture. In contrast, if the carrier would be less hy-

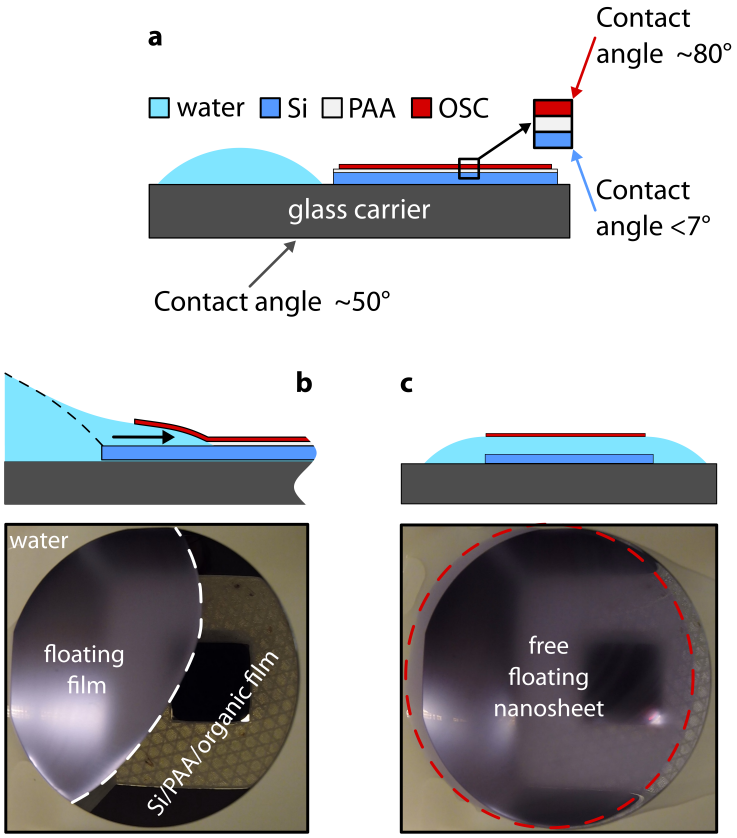

Figure 3.6: Nanosheet release by side injection. **a** Illustration of the wetting geometry before contact. **b** Illustration and picture of the release process during dissolving. The white dashed line indicates the border of the floating nanosheet. The black arrow represents the advancing direction. **c** Illustration and picture of the free floating nanosheet. The red dashed circle indicates the border of the free floating nanosheet.

drophobic, the dissolution of PAA could cease before releasing the nanosheet entirely since the advancing angle would decrease by the weaker gradient force during wetting (compare the dashed line with the advancing angle sketch in Figure 3.6b). The dissolving speed would diminish if the advancing angle became less than the critical contact angle. We measured this critical contact angle for wetting on the PAA layer by contact angle measurements. The water stopped wetting once the advancing angle was around 12° (Figure B.2).

3.2.2 Depositing the Nanosheets

Since water is the key for the entire process, the pick-up step has to be performed with extreme care. We first moved the glass carrier to a beaker for a better pick-up experience (Figure 3.7a). We noticed that the conventional pick-up technique (picking up the layer parallel to the water surface) for 2D materials results in several issues for OSC pick-up:

- The tweezer could damage the nanosheet if the nanosheet size exceeded the target substrate.
- The residual water on the tweezer could re-wet the substrate after pick-up.
- Wrinkles could form on the nanosheet after pick-up.

In addition, the nanosheet size was larger than the substrate size due to the captured water drop under the nanosheet after pick-up, and thus the nanosheet mostly formed wrinkles to fit the substrate during lamination. To address these issues, we modified the pick-up procedures as follows:

- We avoided contacting the sample surface or edges using a wafer tweezer (typically bent). We mounted the substrates with double-sided tape to the tweezer (Figure 3.7b).
- The pick-up angle must be slightly tilted against the nanosheet. This angle allowed the drainage of excess water from the substrate while pick-up. Using a wafer tweezer was also helpful in this regard.
- The sample must lie on a block nearly perpendicularly. This placement prevented visible wrinkles, as the remaining water followed gravity during drying (Figure 3.8).

It is important to mention an additional pick-up obstacle. Water is essential for the transfer process but also the primary limitation. The quality of the nanosheet transfer is highly dependent on the hydrophobicity of the target substrate. On the one hand, if the substrate was hydrophilic, it was relatively simple to pick-up the nanosheet because the substrate wetted the water. No capillary force acted on the nanosheet during the pick-up, and even small patches were transferable. In addition, the small patches could be repositioned on the substrate until the water evaporated. On the other hand, a hydrophobic substrate made it challenging to pick the nanosheet up. Capillary forces would cause the capillary repulsion on the substrate since water did not wet the substrate. This repulsion would forcefully propel the film away, causing

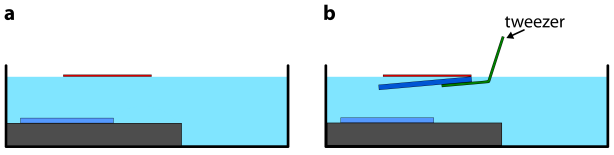

Figure 3.7: Illustrations of nanosheet pick-up. **a** The free floating nanosheet in beaker. **b** The nanosheet pick-up.

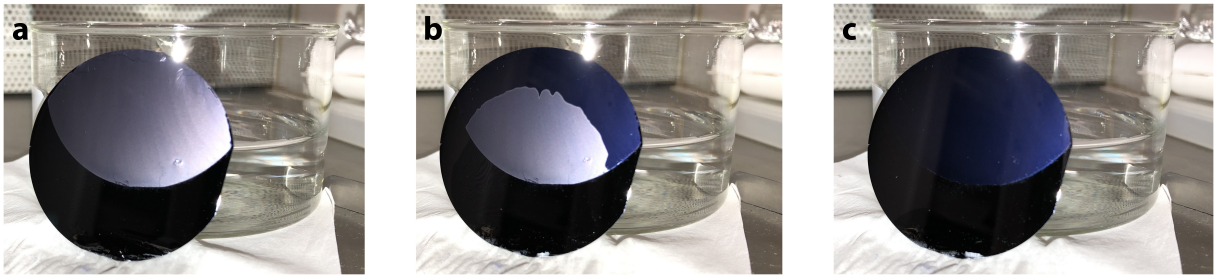

Figure 3.8: Pictures of organic nanosheets during lamination. **a** After pick-up, **b** half-laminated, and **c** completely laminated.

the film to fracture. Physical contact between the substrate and nanosheet eliminated this issue prior to pick-up (Figure 3.7b). Accordingly, it is always preferable to have a nanosheet larger than the substrate for hydrophobic substrates.

3.3 Characterization of the Transferred OSC Nanosheets

3.3.1 Structural Characterization

After optimizing the release and transfer of nanosheets, we examined the morphology and crystallinity of the 50 nm-thick pentacene and DNTT nanosheets by AFM and X-ray diffraction (XRD). The atomic force micrographs revealed that PAA promoted crystallization of pentacene. We determined the characteristic signatures of the polycrystalline film with grain sizes up to 5 µm. Compared to crystallization on oxide and TMD (Figure 3.1, 3.2, and 3.3), the grain sizes were considerably larger on the PAA (Figure 3.9a). We then investigated the morphology of pentacene nanosheet after transfer. We did not observe any noticeable change between the micrographs of before and after the transfer (Figure 3.9a-b). Similar results were achieved for DNTT nanosheets, with grain sizes up to 3 µm and no noticeable change in grain sizes after the transfer, as shown in Figure 3.9d-e.

Afterwards, we examined the crystallinity of the nanosheets by XRD. The pentacene film on PAA exhibited Bragg peaks up to the fifth order with a single molecular orientation comprising a standing-up (thin-film) phase (Figure 3.9c). However, the nanosheet exhibited significant polymorphism in the form of the Campbell-bulk phase, coexisting with the thin-film phase after transfer. This phase transition was evidence of induced stress on the pentacene nanosheet that occurred by the transfer process. During the nanosheet release, the nanosheet experienced stress by capillary repulsion while water was advancing on the substrate, causing

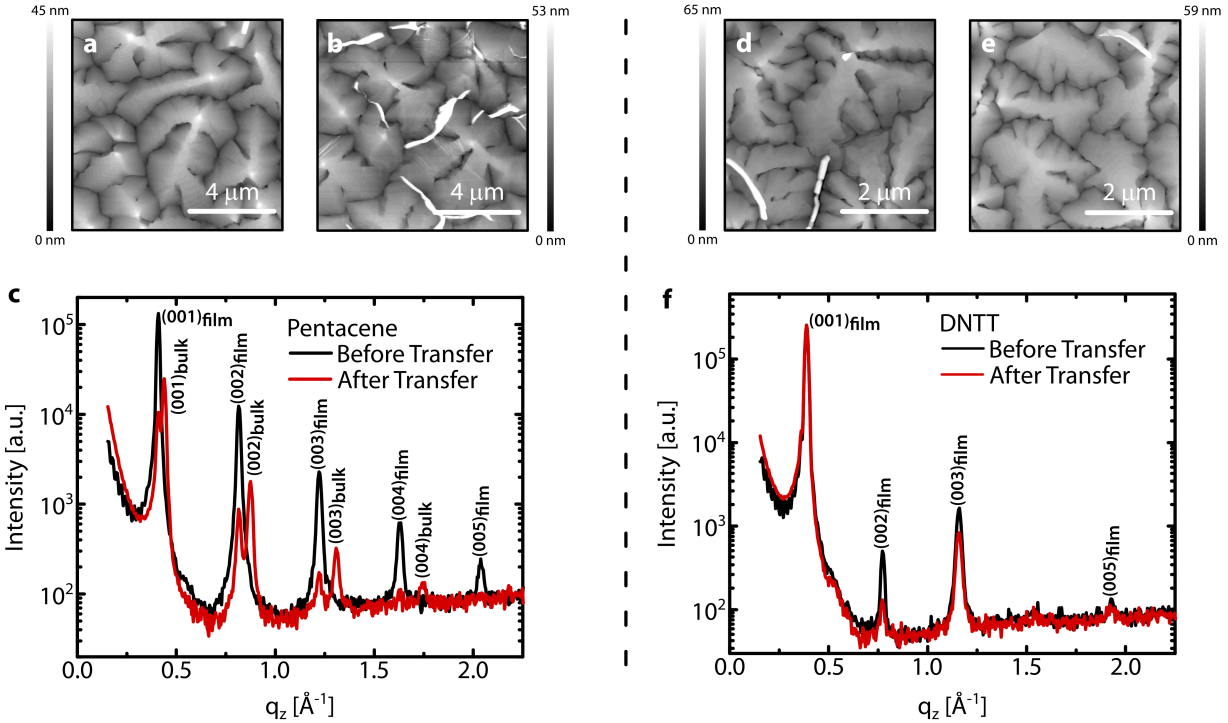

Figure 3.9: Morphology and crystallinity of 50 nm-thick pentacene and DNTT nanosheets before and after transfer. Atomic force micrographs of pentacene film **a** before and **b** after transfer. **c** X-ray diffraction measurements on pentacene film before and after transfer. Film and bulk indicate the packing motif of pentacene. Atomic force micrographs of DNTT film **d** before and **e** after transfer. **f** X-ray diffraction measurements on DNTT film before and after transfer.

the film to stretch. The visible creases on the nanosheet made it possible to see the stretching even with the naked eye. This stretch likely resulted in an expansion of the unit cell, thereby promoting molecular tilt. In the case of DNTT nanosheets, no phase transition occurred after transfer (Figure 3.9f). Nevertheless, DNTT nanosheets tended to fracture into stripes during nanosheet release due to the lack of polymorphism. The typical width of stripes was between 1 mm and 3 mm.

3.3.2 Electrical Characterization

The results of the structural characterization have demonstrated that nanosheets are functional and promising for electronic devices. In order to investigate their electrical properties in-depth, we fabricated nanosheet TFTs in various configurations. Nanosheets TFTs have the following properties in general:

- Nanosheets were approximately 50 nm thick.
- Evaporation rate was approximately 0.1 $Å s^{-1}$.
- Substrates were held at room temperature for pentacene and at 60 °C for DNTT during evaporation.
- Si/Al_2O_3 (33 nm)/SAM (C_{14}-phosphonic acid) gate stack was used in the fabrication of all organic TFTs unless stated else.
- Transistors were patterned by shadow masks with respective channel width and length of 200 µm and 100 µm (W/L = 2). Individual transistors are scribed with a pin after OSC deposition.
- Applied drain voltage was -5 V.
- All measurements were carried in under dark ambient conditions.

Comparison of as-evaporated pentacene TFTs on SAM and PAA

TFT performance can be affected by a wide variety of factors, including but not limited to interface quality and crystallization on particular surfaces. Therefore, we compared the performance of TC as-evaporated pentacene TFTs on the PAA to the SAM as a preliminary test since the as-evaporated films on SAM exhibit the highest mobility for organic transistors (Figure 3.10) [39]. With its low onset (-0.34 V) and threshold voltages (-1.71 V), the TFT on the SAM exhibited exceptional performance. The subthreshold slope was approximately 600 $mVdec^{-1}$ (Figure 3.10a). Unfortunately, the performance of TFT on PAA was inferior. We measured a

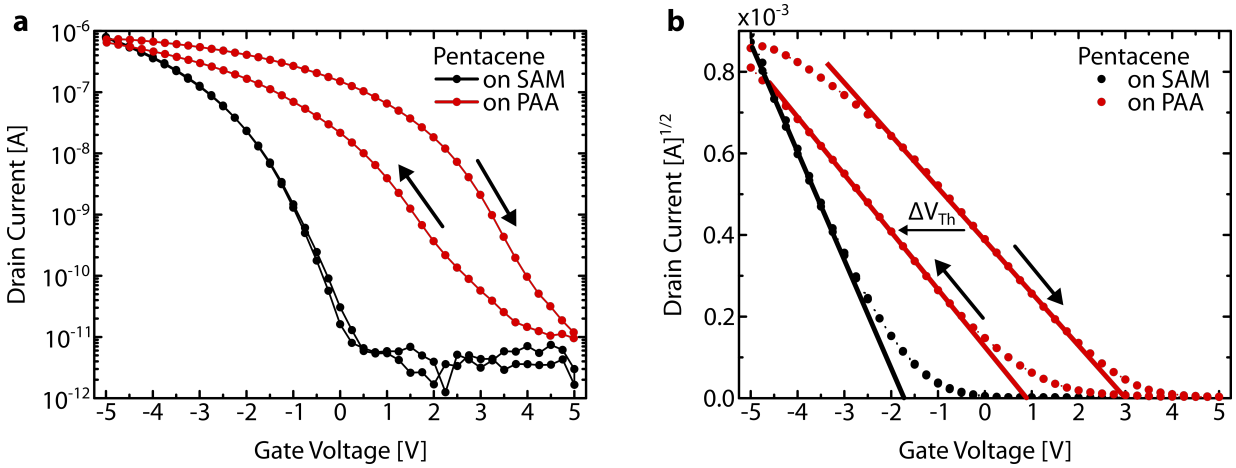

Figure 3.10: Characteristics of TC as-evaporated pentacene TFTs on SAM and PAA. Transfer curves of pentacene TFTs on **a** semi-logarithmic and **b** square-root scales. The black and red solid lines represent the extrapolations of saturation currents. The saturation current characteristics are for BW sweep direction.

significant threshold voltage shift of 1.65 V between forward (FW, negative-to-positive) and backward (BW, positive-to-negative) gate voltage sweeps (known as hysteresis, Figure 3.10b), even though the highest drain current was comparable to that of TFT on the SAM within the gate voltage range. Thus, we could only turn off the TFT at the high gate voltage limit in the FW sweep. The transistor characteristics was similar to TFTs on untreated SiO_2, where the interface states dominated the charge transport [71]. We concluded that the PAA surface impeded examining the intrinsic properties of as-evaporated organic films prior to their transfer, thereby obscuring their true potential.

Comparison of as-evaporated and transferred pentacene and DNTT TFTs

We begin by discussing the characteristics of transferred pentacene TFTs. We fabricated a benchmark TC as-evaporated pentacene TFT to use as a comparison standard. Then, we fabricated two transferred pentacene TFTs in BC and TC configurations. Figure 3.11 compares the results of as-evaporated and transferred TFTs. The parameters of the benchmark TFT were an onset voltage of 0.9 V, a threshold voltage of -0.67 V and no significant hysteresis (Figure 3.11a). The maximum drain current measured was 420 nA. In contrast, both transferred TFTs had comparable drain currents of approximately 70 nA. Therefore, we concluded at first glance that the performance of transferred TFTs was approximately seven times lower than the benchmark TFT. We observed a similar hysteresis value of 0.69 V for both TFTs, which was considerably lower than that on the PAA. The onset voltage of the TC transferred TFT was shifted

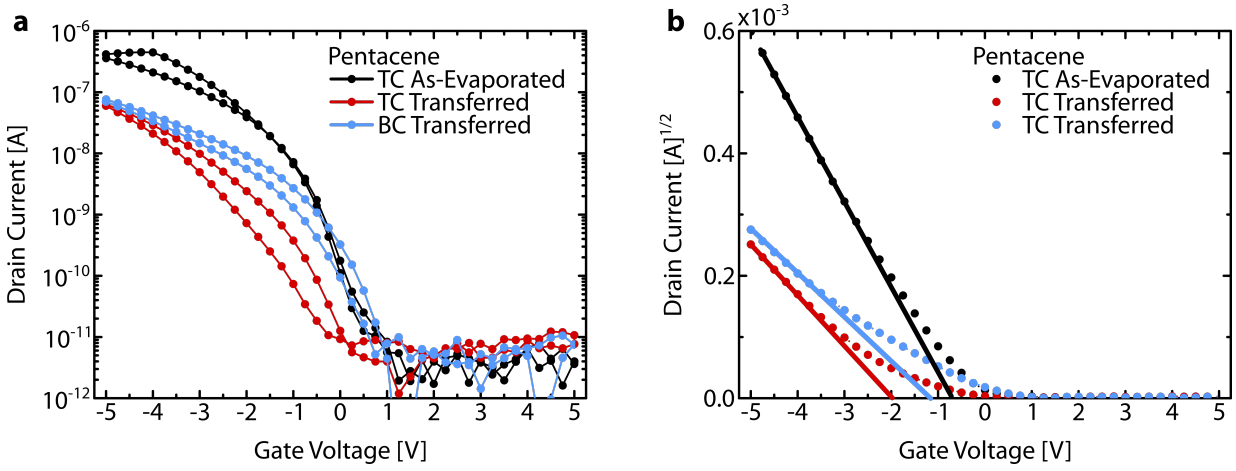

Figure 3.11: Characteristics of transferred pentacene TFTs in various configurations. Transfer curves of benchmark (TC as-evaporated) pentacene TFT and TC/BC transferred pentacene TFTs on **a** semi-logarithmic and **b** square-root scales. The black, red, and blue solid lines represent the extrapolations of saturation currents. The saturation current characteristics are for BW sweep direction.

to negative gate voltages, while the onset voltage of the BC transferred TFT was similar to the benchmark TFT. In addition, as presented in Figure 3.11b, transferred TFTs exhibited a pronounced subthreshold region, however, the subthreshold region of benchmark TFT was also not negligible. As a result, even with the most promising fabrication techniques, the disorder was still present in pentacene thin films.

DNTT TFTs in all possible configurations are shown in Figure 3.12, for a comprehensive comparison. The characteristics of the benchmark (TC as-evaporated) TFT was remarkable. We observed no hysteresis, with almost 0 V threshold voltage. The saturation current exhibited a slight contact hump, indicating that the contact problems were not negligible. We estimated the second threshold voltage of around 0.85 V. However, we found no apparent subthreshold-like region since the subthreshold slope was steep as 125 $mVdec^{-1}$.

The drain current performance of the transferred DNTT TFTs (around 380 nA) was almost an order of magnitude less than that of the benchmark TFT (3.76 µA). In contrast to transferred pentacene TFT, transferred DNTT TFTs exhibited no significant hysteresis. The TC transferred TFT exhibited a small subthreshold region, whereas the BC transferred TFT showed nearly none. The subthreshold slopes for TC and BC transferred DNTT TFTs were 281 $mVdec^{-1}$ and 187 $mVdec^{-1}$, respectively. For BC transferred TFT, we observed the saturation-to-linear transition point on the square-root scale, as the threshold voltage was approximately 0.53 V. Thus, linear region conditions were met at the highest gate bias. The threshold voltage of the TC transferred TFT was -0.74 V.

The most important outcome was the contrast between BC as-evaporated and transferred DNTT TFTs. As anticipated, the morphologic differences led to a significant reduction in performance of the BC as-evaporated TFT: a prominent superlinearly increasing saturation current, a substantial subthreshold slope (approximately 500 $mVdec^{-1}$), and a threshold voltage (-1.18 V). Astoundingly, the BC transferred TFT performed almost 15-fold better than the BC as-evaporated TFT.

Figure 3.12c represents the estimated mobilities in order to compare the transistor performances. The mobility value of the benchmark TFT was the highest. However, it showed a mobility peak of around 1.2 $cm^2V^{-1}s^{-1}$ before stabilizing at 0.7 $cm^2V^{-1}s^{-1}$ due to the contact hump. Though the mobility values of transferred TFTs were consistent regardless of the configuration, the BC transferred transistor exhibited a long mobility plateau, a hallmark of proper saturation characteristics independent of gate bias. In contrast, the BC as-evaporated transistor exhibited the lowest mobility, as expected.

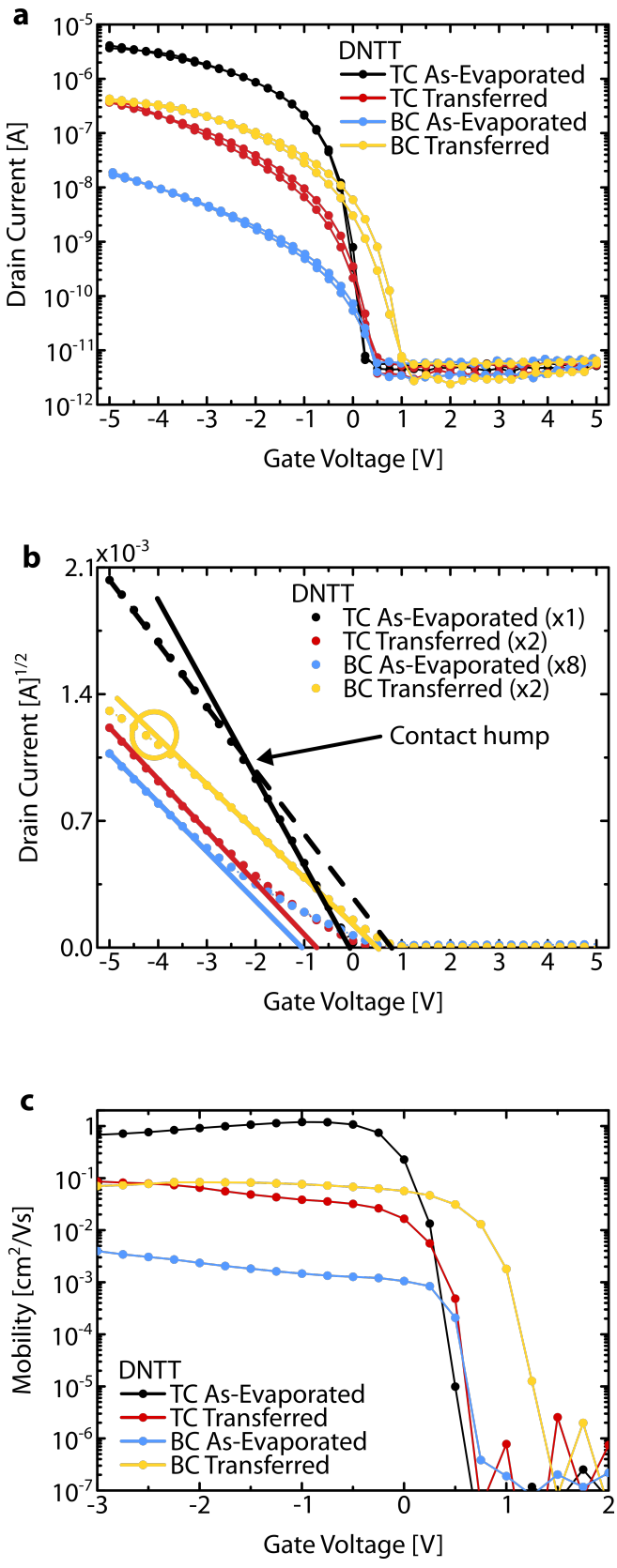

Figure 3.12: Characteristics of transferred DNTT TFTs in various configurations. Transfer curves of TC/BC as-evaporated and TC/BC transferred DNTT TFTs on **a** semi-logarithmic and **b** square-root scales. The black, red, blue, and yellow solid lines represent the extrapolations of saturation currents. The black dashed line represents the extrapolation of saturation current for above contact hump. The yellow circle indicates the saturation-to-linear transition point. The saturation current characteristics are for BW sweep direction. **c** Mobility characteristics of the TFTs for BW sweep direction.

Comparison of TC transferred pentacene TFTs: Contact patterning before or after transfer

After our investigations, we demonstrated the necessity of transferable nanosheets, especially in BC configuration. However, we could still not point out the reason for nearly an order of magnitude lower performance compared to benchmark transistors. Unfortunately, we could not extract the initial potential of the as-evaporated films on PAA because the transistor characteristics on the PAA performed inferiorly. To address this issue, we focused on identifying the possible injection problems by fabricating transferable pentacene TFTs with a different approach. On the one TFT, the fabrication steps were analogous to those of a TC transferred pentacene TFT. On the other TFT, the contacts were patterned prior to nanosheet transfer. Although this method was not as reproducible as a conventional nanosheet transfer, we could still fabricate a functional TFT for comparison, as depicted in Figure 3.13.

Contact patterning prior to transfer showed significant benefits: lower hysteresis, almost zero threshold voltage, and negligible subthreshold region. However, the saturation current revealed parabolic behavior toward the high gate bias end. This behavior indicated that the contacts were ohmic but resistive, so most of the voltage was dropped at the contacts. Thus, we observed a saturation-to-linear transition point even though the V_G-V_{Th} was similar to the applied drain bias. The transition point indicates that the "effective" drain voltage was lower in the channel. Based on this comparison, we concluded that pre-patterning the contacts promoted charge injection, narrowed the subthreshold region, and caused resistive contacts.

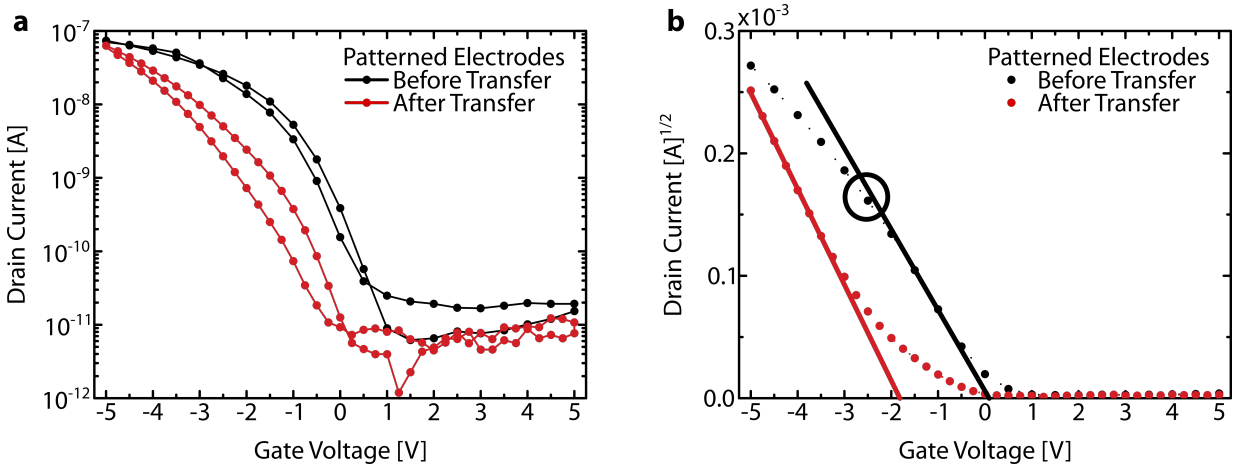

Figure 3.13: Characteristics of TC transferred pentacene TFTs with contact patterning before or after transfer. Transfer curves of pentacene TFTs on **a** semi-logarithmic and **b** square-root scales. The black, and red solid lines represent the extrapolations of saturation current. The black circle indicates the saturation-to-linear transition point. The saturation current characteristics are for BW sweep direction.

3.4 Ambipolar Organic/Inorganic Nanosheet Transistors

The promising performance of the transferred nanosheet TFTs motivated us to take a step forward for van der Waals heterojunctions. Here, the fabrication complexity increases with the integration of the TMD crystals. The main reason is that the TMD crystals are randomly positioned on the gate oxide. Therefore, patterning the contacts with shadow masks is no longer feasible. We utilized photolithography for TMD transistor fabrication since TMD crystals were compatible with lithography chemicals in contrast to OSCs. For the ambipolar transistor, we first fabricated a TC TMD transistor. Afterward, we transferred the OSC nanosheet for a BC organic TFT using the contacts of the TMD transistor. Since the OSC nanosheet could be transferred in any size and performed adequately in BC configuration, this was the optimized ambipolar transistor architecture.

Substituting shadow masks with photolithography led to another fabrication challenge; incompatibility of SAM passivation with lithography chemicals. We passivated the gate oxide by hydrophobic SAM for unipolar OSC transistors to reduce the interface states. Unfortunately, the SAM-passivated substrates were hydrophobic to lithography solvents. Consequently, we used untreated Si/SiO_2 (90 nm) gate stack for the ambipolar transistors.

After stacking the monolayer (ML) MoS_2 crystals that accumulated electrons with the DNTT nanosheet that accumulated holes, we anticipated achieving ambipolar behavior. Figure 3.14 illustrates the characteristic "V" shape of ambipolar charge transport in MoS_2/DNTT vdW heterojunction transistor. The dip of the ambipolar current shifted by the polarity of the drain

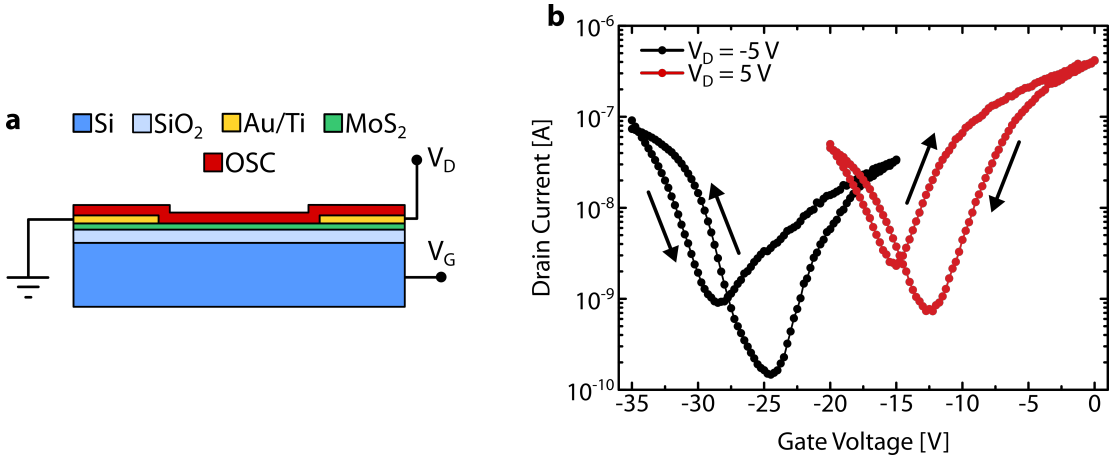

Figure 3.14: Characteristics of ambipolar MoS_2/DNTT transistors on 90 nm-thick silicon oxide for ±5 V drain voltage. The arrows indicate the sweep directions.

bias. Comparable drain currents indicated that the mobilities of both charge types were balanced. The on/off ratio of ambipolar transistor was around three orders of magnitude, and the ambipolar transistor exhibited hysteresis as high as 6 V.

The crucial point of an ideal ambipolar transistor is to achieve saturation conditions for both carriers as described in 2.6. Figure 3.15 represents the saturation current characteristics of the ambipolar transistor for $V_D = \pm 5$ V. We separated the FW and BW sweeps due to the presence of hysteresis.

Since the threshold voltages shifted between FW and BW sweeps, the ambipolar current and its position were also shifted. For $V_D = -5$ V in the FW sweep, the ambipolar dip voltage was -28.5 V, and the threshold voltage difference was 1.4 V ($V_{Th,h} = -30.3$ V, $V_{Th,e} = -28.9$ V). In the BW direction, the ambipolar dip voltage shifted to -24.5 V, and the threshold voltage difference increased to 3.7 V ($V_{Th,h} = -27.5$ V, $V_{Th,e} = -23.8$ V).Therefore, the ambipolar current in the FW sweep was higher (900 nA) than in the BW sweep (146 nA) because the threshold voltage difference was lower. We observed similar behavior for $V_D = +5$ V, the difference in threshold voltages for the FW sweep were only 0.2 V, with the ambipolar dip occurring at -15 V. The ambipolar dip shifted to -12.5 V, and the difference increased to 3.1 V during the BW sweep. Consequently, the ambipolar currents were consistently higher in the FW sweeps than in the BW sweeps, regardless of the drain bias sign.

For a comprehensive understanding of ambipolar behavior, we conducted drain bias-dependent measurements. We concentrated on the FW sweeps as the threshold voltage difference was smaller (Figure 3.16). For both signs of drain bias, the TFT operated as two unipolar TFTs separated by a distinct off-state region when the drain bias was low. The ambipolar tran-

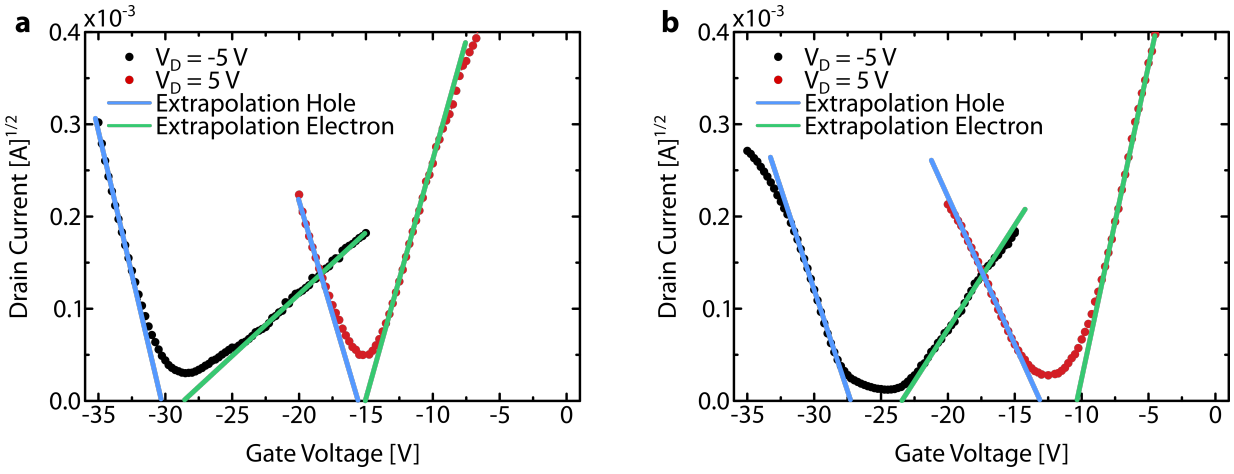

Figure 3.15: Transfer curves of ambipolar MoS_2/DNTT transistors on a square-root scale for ±5 V drain voltage in **a** FW and **a** BW sweeps.

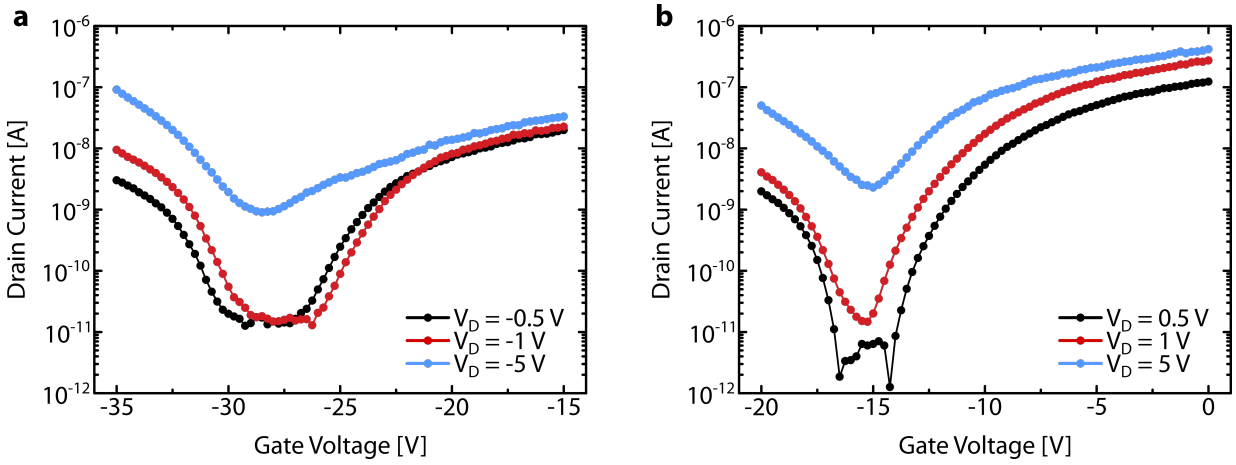

Figure 3.16: Transfer curves of ambipolar MoS_2/DNTT transistors on a semi-logarithmic scale under various **a** negative and **b** positive drain biases in FW sweep.

sistor's on/off ratio increased as a consequence of achieving off-state region. This result was reasonable at low drain biases, as ambipolar current was highly dependent on the intersection of the threshold voltages of both charges. Since the threshold voltages of our transistors were initially high, increasing the threshold voltage intersection required higher drain biases. At a drain bias of -5 V, we observed ambipolar operation due to a greater intersection of threshold voltages. We observed similar behavior for a +5 V drain bias. However, in this case, the ambipolar behavior was attained at merely +1 V. Increasing the drain bias further only increased the intersection.

Although we increased the ambipolar current by increasing the drain bias, the ambipolar current trend still needs to be realized. As discussed, for appropriate ambipolar behavior, the dip of the ambipolar must shift with drain bias. The shift could be towards more negative or positive gate voltages while the ambipolar current increases, depending on the polarity of the drain bias (Figure 2.18 and 2.19). Drain bias-dependent measurements showed the fact that the measured current was not a true ambipolar current (Figure 3.16). However, there should be no ambipolar current if the threshold voltages do not intersect.

We must consider the operation of unipolar TFTs in order to comprehend the observed ambipolar current. In an unipolar TFT, the subthreshold region separates the saturation and off-state regions. An ambipolar transistor then requires two distinct subthreshold slopes, for electrons and holes. We began our evaluation by fitting the curve according to saturation conditions (the red solid line in Figure 3.17) on a square-root scale. The ideal saturation conditions revealed that the threshold voltages did not intersect according to the applied gate and drain biases. This lack of intersection caused the ambipolar current to vanish under ideal conditions.

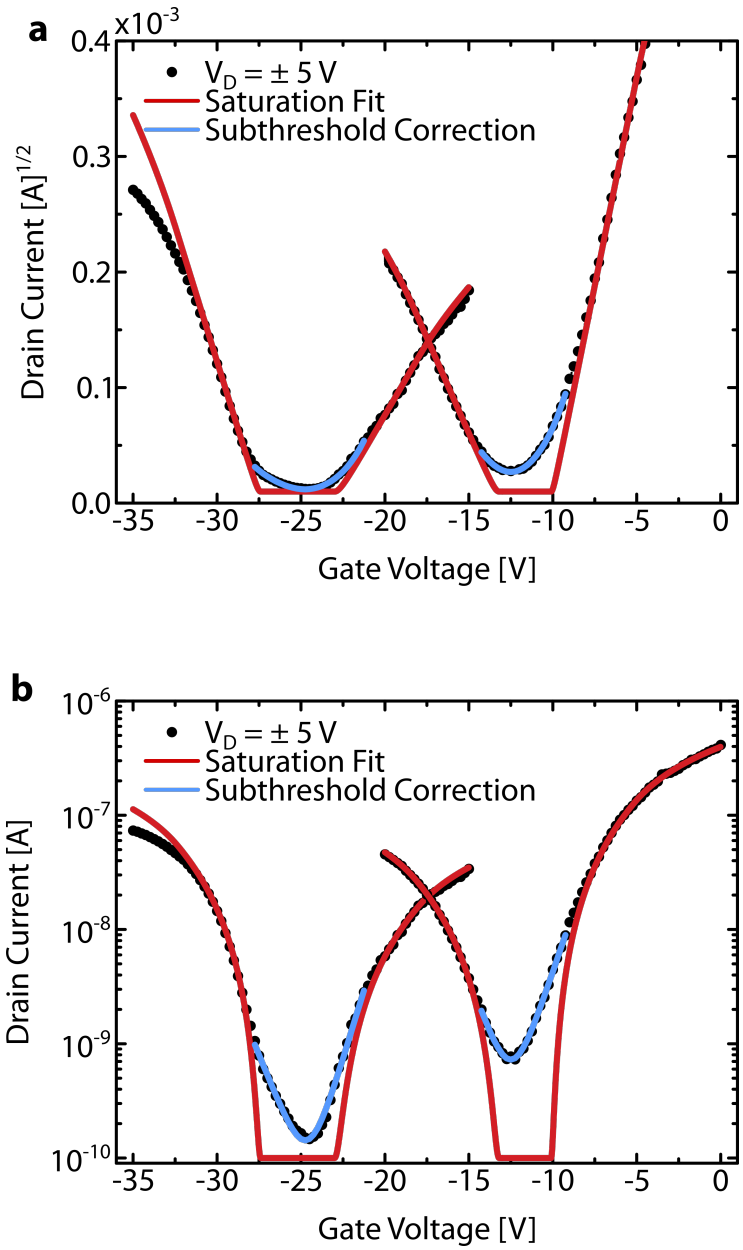

Figure 3.17: Revealed saturation and subthreshold regions of ambipolar MoS_2/DNTT transistor for ± 5 V drain biases. Transfer curves of the ambipolar transistor on **a** square-root and on **b** semi-logarithmic scales in BW sweep. The red and blue solid lines represent saturation and subthreshold regions, respectively.

In order to explain the finite current, we extended the saturation region by subthreshold region (the blue solid line in Figure 3.17). We plotted the transfer curve on a semi-logarithmic scale to evaluate the fitting. As expected, we could explain the finite current by the intersection of the subthreshold slopes of both charges. The results were similar to the positive drain bias; only the subthreshold slopes slightly differed. Typical subthreshold slopes were around 2,800 $mVdec^{-1}$, corresponding to a total trap density of 1.1×10^{13} $cm^{-2}eV^{-1}$.

As a result, we deduced that the ambipolar current results from intersection of subthreshold slopes rather than threshold voltages. The ambipolar dip shift, therefore, did not conform to the ambipolar current trend. We must reduce the contribution of subthreshold slopes to address this challenge. Since we know that the subthreshold slope is influenced by interface states (Equation 2.9), finding a lithography compatible interface passivation method is essential for enhancing the ambipolar transistors, which is the main topic of the following chapter.

4

Lithography Compatible Oxide Passivation for Nanosheet TFTs

"... the amorphous material has more defects and imperfections than in single-crystalline semiconductors, resulting in more complicated transport processes in the TFT. To improve device performance, reproducibility, and reliability, the bulk and interface trap densities must be reduced to reasonable levels."

— Simon M. Sze

4.1 The Need for Lithography Compatible Oxide Passivation

In Chapter 3, we observed that the interface states caused enormous onset and threshold voltage shifts, giving rise to a substantial subthreshold slope as high as 2,400 $mVdec^{-1}$ in ambipolar transistors on untreated silicon oxide. Sections 2.3 and 2.4 discussed the importance of the interface states and the oxide capacitance; low interface trap DOS and/or high oxide capacitances are necessary to establish operation regions properly. Several groups focused on improving transistors by introducing ultra-thin gate oxides through atomic layer deposition (ALD) [72, 73, 74] or encapsulating by h-BN [17]. However, the ALD and exfoliation techniques increase the fabrication's complexity by involving several fabrication steps. On the one hand, the ALD-deposited oxide surface would still contribute to interface trap states. On the other

hand, the exfoliation method is not scalable. Therefore, surface state passivation of the gate oxide is necessary to improve the characteristics of the transistors where lithography has to be employed. The incompatibility of SAM passivation with lithography chemicals leads us to polymer-based oxide passivation alternatives. Since the lithography solvents limit the category of polymers, here we propose cyclic olefin copolymer (COC). COC, a glass-clear amorphous polymer, was developed for transparent moldings such as lenses. In addition, COC is resistant to alcohols and ketones with short chain lengths and is hydrophobic [75]. As a result of its scalability and simple implementation to the existing fabrication, COC is a promising alternative. The versatility of COC signifies that it can be applied to a wide variety of oxides, including SiO_2, increasing its potential for CMOS technology. In this chapter, we investigate the promise of COC as an oxide surface passivator for MoS_2 nanosheet-based transistors. Some of the findings in this chapter are published and patented [76].

4.2 Compatibility of the Oxide Passivation with Lithography Solvents

4.2.1 Calculation of Hansen Solubility Parameter Distance

Hansen solubility parameter (HSP) distance is the simplest method for finding the good and poor solvents of a solid [77]. The method relies on a space with the dispersion force (δd), the dipolar intermolecular force (δp), and the hydrogen bond (δh) energies as its dimensions. The HSP sphere of a solid is determined by comparing its solubility with more than 50 solvents. After calculating the critical radius (R_0) over the sphere, the HSP distance (R_a) between the solid and the solvent can be determined using:

$$R_a^2 = \left(4 \cdot (\delta d_2 - \delta d_1)^2 + (\delta p_2 - \delta p_1)^2 + (\delta h_2 - \delta h_1)^2\right) \tag{4.1}$$

Relative energy difference (RED) is determined using the ratio of R_a/R_0. If the RED value is less than one, the solvent is good, and vice versa. If RED = 1, then partial dissolution occurs.

The HSP and HSP sphere of COC was investigated by different groups. The HSP of the COC are δd = 18 $MPa^{1/2}$, δp = 3 $MPa^{1/2}$, and δh = 2 $MPa^{1/2}$. According to the measurements from Ref. [78, 79], COC has an R_0 of roughly 6.67. We used the HSP distance between COC and toluene as an example since toluene is the main solvent of COC. We calculated R_a to be 1.6, so RED is less than 1, as expected. Next, we determined the HSP distance between COC and lithog-

raphy chemicals. Here, acetone was the lift-off solvent, and MIBK:2-propanol (MIBK:IPA, 1:3) was the developer. Solvents for polymethyl methacrylate (PMMA, lithography resist) include anisole and chlorobenzene. COC and acetone, MIBK:IPA, anisole, and chlorobenzene had respective R_a values of 10.24, 12.63, 5.11, and 2.39. These R_a values indicated that anisole and chlorobenzene were good solvents for COC, while acetone and MIBK:IPA were poor solvents. During lithography, the sample was typically overexposed to acetone (between 3 hours to 6 hours), followed by MIBK:IPA for 50 seconds to 60 seconds, and spin-coating of PMMA dissolved in anisole. The results anticipated that the film would withstand exposure to acetone and MIBK:IPA.

4.2.2 Chemical Stability of the Passivation

Figure 4.1 presents atomic force micrographs of untreated and solvent-exposed COC films. As shown in Figure 4.1a, the COC film was uniformly coated, exhibiting an root-mean-square (RMS) roughness of 0.27 nm before exposure. Figure 4.1b-c depicts the COC film exposed to acetone for 19 hours and MIBK for 1 minute. The only noticeable change in the exposed films was a slight increase in their RMS roughness: 0.30 nm after acetone and 0.42 nm after MIBK exposures.

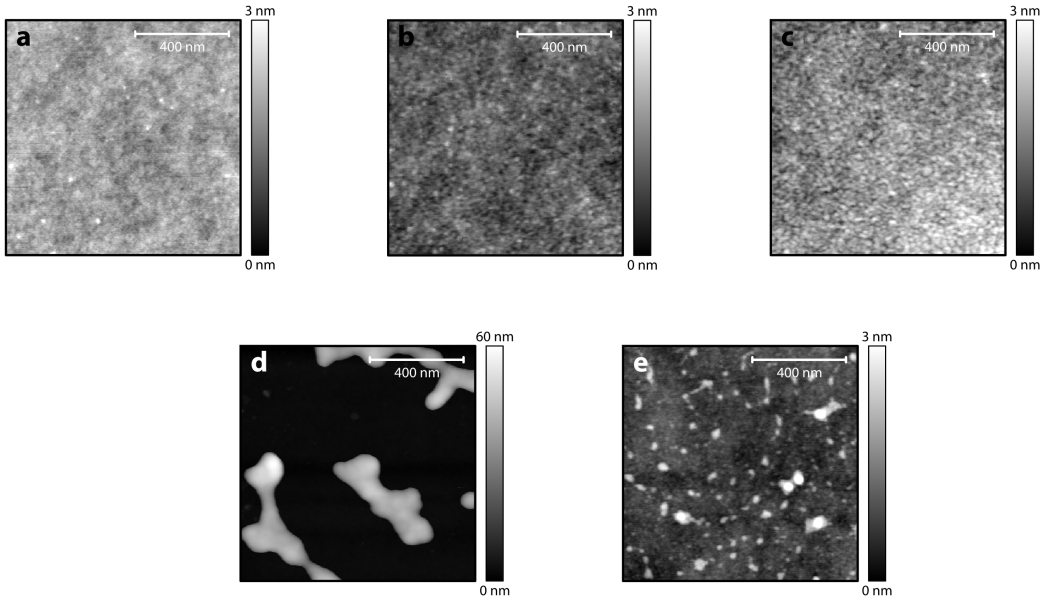

Figure 4.1: Morphology of ultrathin COC films after solvent exposure: **a** untreated COC film, **b** COC film after 19 h acetone exposure, **c** COC film after 1 min MIBK exposure, **d** COC film after 1 min anisole exposure, and **e** COC film after 1 min chlorobenzene exposure.

In contrast, anisole and chlorobenzene significantly damaged the COC film after a minute exposure. When exposed to anisole, the COC film became piled up and formed dense clusters, while chlorobenzene dissolved the COC as seen in Figure 4.1d-e. We anticipated that the COC film would remain stable despite its brief exposure to anisole during spin-coating. Nonetheless, spin-coating must be performed immediately after the drop-casting.

We also performed AFM to characterize a COC-encapsulated MoS_2 transistors to investigate the morphology of the COC film (Figure 4.2). During encapsulated transistor fabrication, the COC film was subjected to two spin-coating steps: PMMA (in anisole) and COC (in toluene). The line profile over COC/MoS_2/COC demonstrated that the MoS_2 crystal functioned as a hard mask, protecting the COC film beneath from all involved solvents. Consequently, we proved that the COC film would withstand the lithography processes.

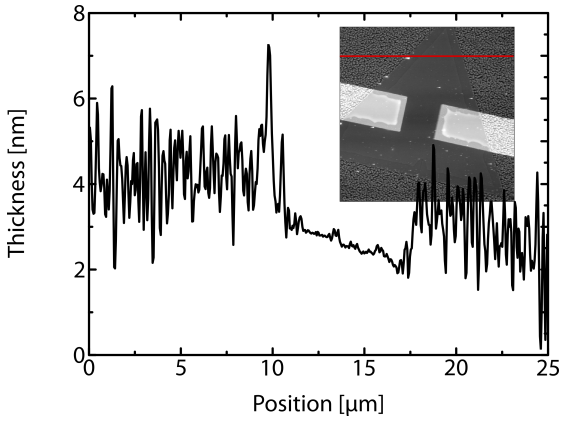

Figure 4.2: Determination of surface roughness of a COC-encapsulated MoS_2 transistor by AFM. The red solid line represents the line profile.

4.3 Thickness Determination of the Ultrathin Oxide Passivation

The COC film needs to be as thin as possible since the COC film acts as a second capacitor, connected in series with the SiO_2. Here, the relative dielectric constant of the COC is less than the SiO_2 (2.35 for COC [75] and 3.9 for SiO_2). Therefore, the COC film reduces the total capacitance of oxide stack as following,

$$\frac{1}{C_{stack}} = \frac{1}{C_{ox}} + \frac{1}{C_{coc}} \tag{4.2}$$

We opted for 5 nm as the optimal thickness because it was sufficient for uniform coating while still being negligible capacitance. The thickness of the ultrathin COC film was 5.7 nm, as verified by AFM in Figure 4.3.

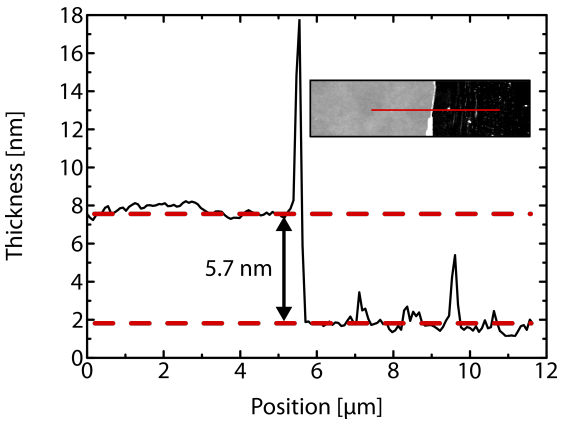

Figure 4.3: Determination of thickness of an ultra-thin COC film by AFM. The red solid line represents the line profile.

4.4 Ambipolar Nanosheet Transistors on Passivated Oxide

After confirming the lithography compatibility of COC films, we fabricated ambipolar transistors on COC-passivated 90 nm-thick silicon oxide. Figure 4.4 depicts transfer curves of ambipolar MoS_2/ DNTT transistor on passivated oxide on a semi-logarithmic scale. Passivation of the interface states dramatically reduced the applied gate voltages, hence the ambipolar dip down to -5 V (from -30 V) for V_D = -5 V and to 0 V from -15 V for V_D = 5 V (compared to Figure 3.16). As a result of the suppression of interface trap states, hysteresis was also lowered (from 5 V to 1.4 V). Accordingly, the ambipolar current and its position became independent of the sweep direction. However, ambipolar TFTs' electron and hole mobilities on passivated oxide were unbalanced. We explained this by the improved performance of MoS_2 on the passivated oxide.

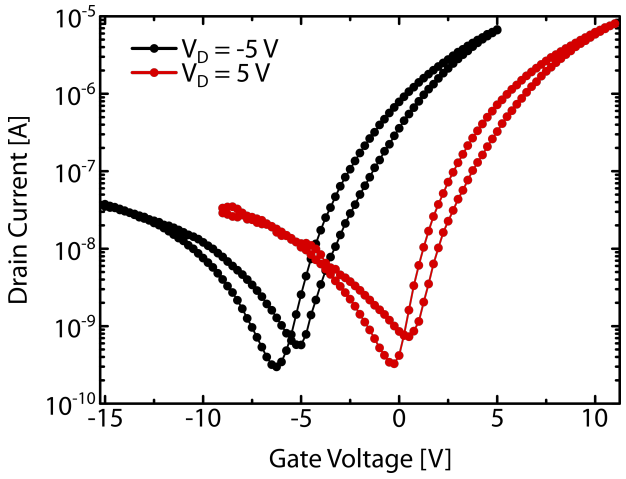

Figure 4.4: Characteristics of ambipolar MoS_2/DNTT transistors on passivated 90 nm-thick oxide for ±5 V drain voltage.

As discussed in the previous chapter, we distinguish the subthreshold slope intersection from threshold voltage intersection by observing the ambipolar current response as a function of drain bias. Figure 4.5 represents drain bias-dependent characteristics of ambipolar transistors on COC-passivated oxide on a semi-logarithmic scale. Interface state suppression enabled the true ambipolar dip shift, following the drain current trend with increasing negative drain bias (Figure 4.5a). The shift was nearly proportional to the increase in the drain voltage up to -6 V, indicating that the saturation conditions were met. Then, the shift decreased to 1 V per 2 V increase in drain voltage. For the lowest drain bias, the transistor was nearly turned off. The corresponding ambipolar current was 10^{-11} A, with an electron on/off ratio of about 10^4. There was three orders of magnitude increase in ambipolar current by the increase in drain bias to -10 V. Remarkably, BW sweep exhibited a similar performance (Figure 4.5b).

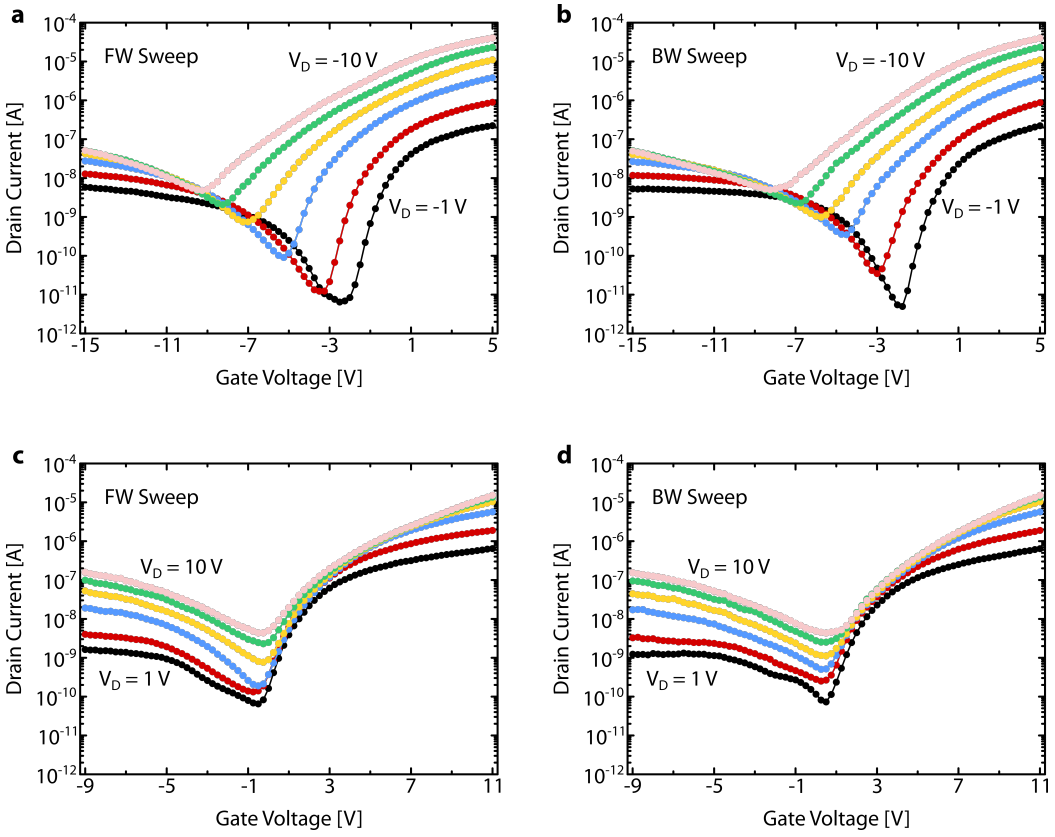

Figure 4.5: Semi-logarithmic plot of transfer curves of MoS_2/DNTT ambipolar transistors on passivated 90 nm-thick oxide under various drain biases for **a** FW and **b** BW sweep directions for negative drain voltages. **c** FW and **d** BW sweep directions for positive drain voltages.

In contrast, the ambipolar dip shift did not follow the drain current trend for positive drain biases (Figure 4.5c-d). As the drain bias increased, ambipolar current exhibited an increasing trend, though it was not as clear as when the drain bias is negative. Moreover, for the lowest drain voltage (1 V), the ambipolar current was as low as 10^{-10} A, which was an order of magnitude higher than the ambipolar current at V_D = -1 V. According to these unexpected characteristics, we concluded that the ambipolar transistor had problems in electron accumulation.

We revealed the saturation and subthreshold regions of the ambipolar TFT through saturation fitting. Figure 4.6 compares the transfer curves on semi-logarithmic and square-root scales for moderate (V_D = ±4 V) and high (V_D = ±10 V) voltages. We observed that the n-conductor's subthreshold slope contributed significantly to the ambipolar behavior. Furthermore, the electron threshold voltage was drain bias-dependent; increasing the drain bias shifted the electron threshold voltage (from 2 V to 5.25 V). For V_D = 10 V, the n-conductor's sub-

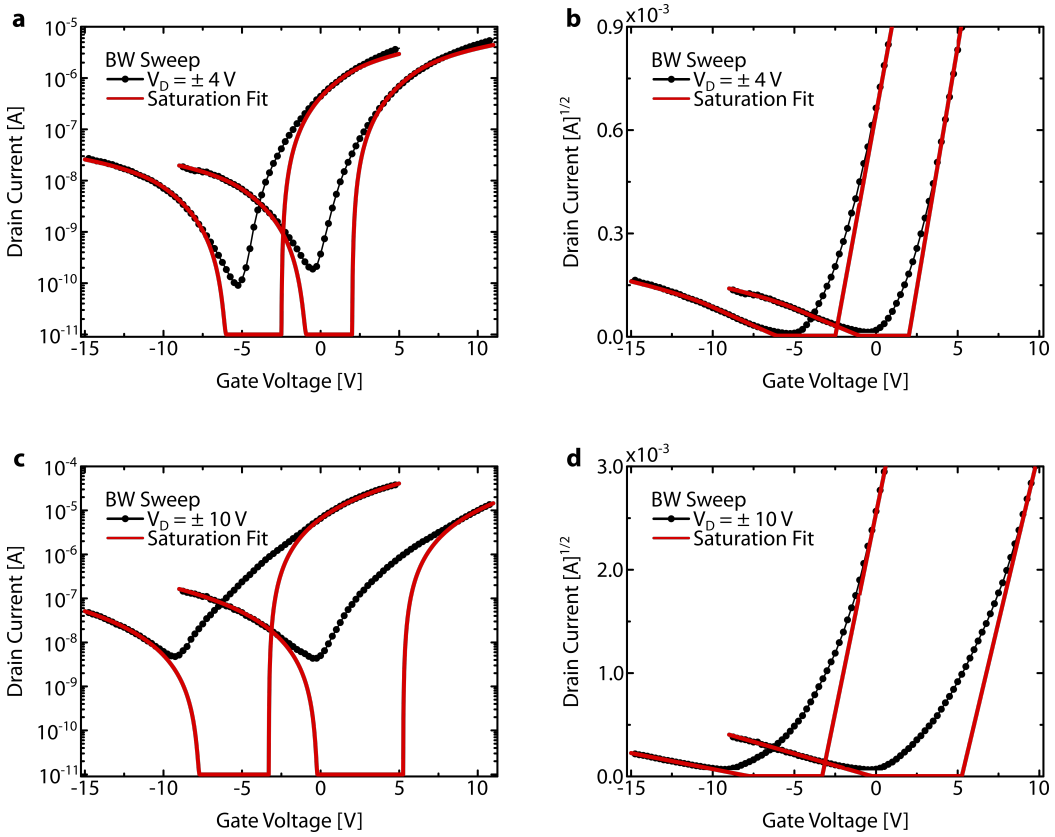

Figure 4.6: Revealed saturation regions of ambipolar MoS_2/DNTT transistors on passivated oxide under high drain biases. Transfer curve of the ambipolar transistors on passivated 90 nm-thick oxide for drain voltages of ±4 V and ±10 V, on **a, c** semi-logarithmic and **b, d** square-root scales. The red solid lines represent the electron and hole saturation regions.

threshold region completely dominated the drain current. In contrast, the saturation conditions were met for any drain bias for p-conductor. The results pointed out that the MoS_2 crystals performed poorly under high drain biases and thus required further investigation.

4.5 MoS_2 Nanosheet Transistors on Passivated Oxide

4.5.1 Impact of the Passivation and Oxide Capacitance

To examine the impact of the passivation and oxide capacitance on the transistor characteristics of unipolar MoS_2 transistors, we fabricated four substrates in four configurations, as summarized below:

- Four TFTs on **untreated 300 nm-thick SiO_2** (Figure 4.7a). 300 nm is a standard SiO_2 thickness that has been widely utilized [80, 81, 82, 83, 84].
- Four TFTs on **untreated 100 nm-thick SiO_2** to study the effect of oxide capacitance (Figure 4.7b).
- Four TFTs on **COC-passivated 300 nm-thick SiO_2** to study the effect of the passivation (Figure 4.7c).
- Four TFTs on **COC-passivated 100 nm-thick SiO_2** to study the effect of the passivation together with the oxide capacitance (Figure 4.7d).

The estimated oxide capacitances are also summarized in Table 4.1.

At first glance, we observed that the operating range of the transistors on different substrates varied considerably. The distribution of onset voltages for TFTs on untreated 300 nm-thick oxide varied between -20 V and -8 V. TFTs had significantly poor subthreshold slopes, averaging at 1,570 ± 460 $mVdec^{-1}$. These values confirmed that the interface trap states were enormously high and heterogeneous. Comparing the characteristics of the transistors with the highest (the black dotted line) and lowest (the yellow dotted line) onset voltages showed substantial differences. For instance, the transistor that showed the highest onset voltage exhibited a subthreshold slope of approximately 2,390 $mVdec^{-1}$ and hysteresis of 0.98 V. In contrary, the transistor that showed the lowest onset voltage exhibited a subthreshold slope approximately 1,160 $mVdec^{-1}$, and hysteresis of 0.3 V. The variations in subthreshold slope and hysteresis indicated that the TFT with a lower onset voltage was less affected by the interface trap states.

As a result of increased capacitance, the TFTs on untreated 100 nm-thick oxide performed better than TFTs on untreated 300 nm-thick oxides. As shown in Figure 4.7b, the transistors exhibited lower onset voltages (−4.3 ± 1.3 V) and steeper subthreshold slopes (1002 ± 208 $mVdec^{-1}$). As expected, increase in oxide capacitance reduced the influence of the interface trap states, resulting in reduced gate bias range. However, TFTs exhibited higher hysteresis (1475 ± 225 mV).

Contrarily, the COC passivation stabilized all TFTs, regardless of the oxide thickness. The operating range of the transistors was as low as ±5 V after COC passivation. Onset voltages of TFTs on passivated 300 nm and 100 nm-thick oxides were −0.9 ± 0.5 V and −1.1 ± 0.5 V, while hysteresis values were 595 ± 45 mV and 125 ± 105 mV, respectively. Most importantly, the subthreshold slopes were substantially steeper; the estimated values were 484 ± 133 $mVdec^{-1}$ for TFTs on COC-passivated 300 nm-thick oxide and 189 ± 54 $mVdec^{-1}$ for TFTs on COC-passivated 100 nm-thick oxide.

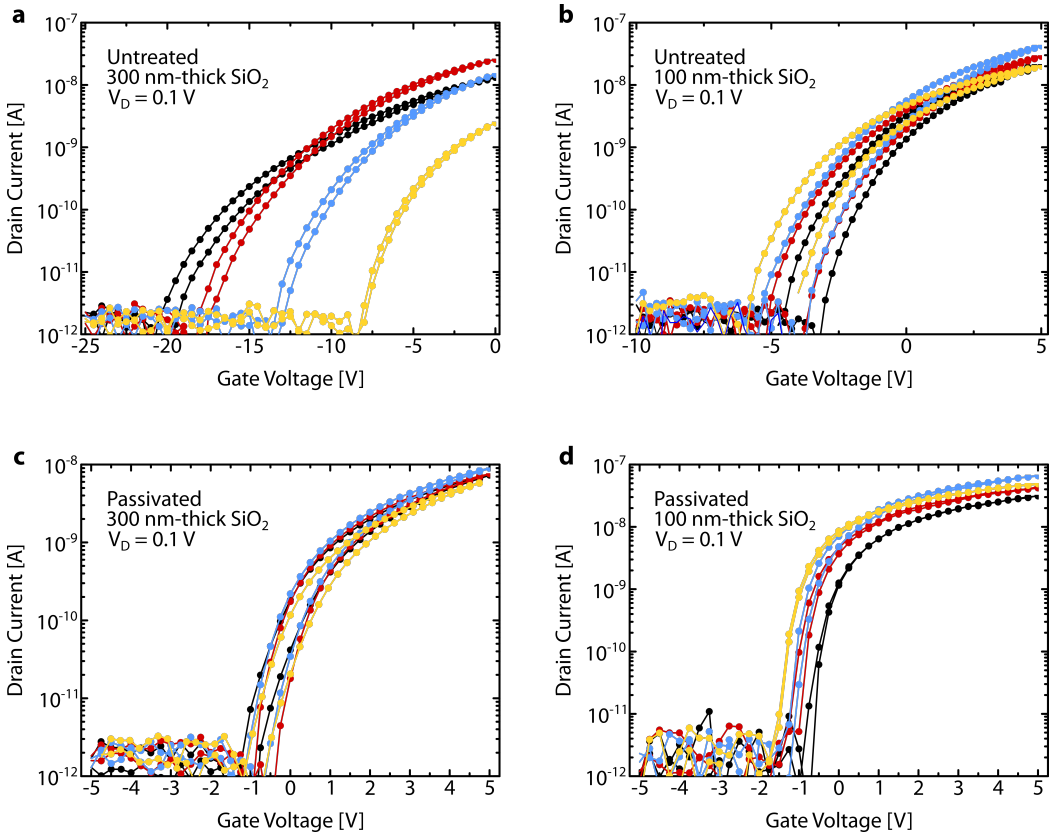

Figure 4.7: Characteristics of MoS_2 TFTs on untreated and passivated oxides as a parameter of oxide thickness under V_D = 0.1 V. Semi-logarithmic plot of the transfer curve of MoS_2 TFTs on **a** untreated 300 nm-thick SiO_2, **b** untreated 100 nm-thick SiO_2, **c** passivated 300 nm-thick SiO_2, and **d** passivated 100 nm-thick SiO_2.

Table 4.1: Onset voltage, subthreshold slope, interface trap state density, and hysteresis values of the TFTs on untreated and passivated SiO_2 as a parameter of oxide thickness.

	untreated 300 nm SiO_2 (11.5 nFcm^{-2})	untreated 100 nm SiO_2 (34.5 nFcm^{-2})	passivated 300 nm SiO_2 (11.2 nFcm^{-2})	passivated 100 nm SiO_2 (31.9 nFcm^{-2})
Onset voltage [V]	-15 ± 6	-4.3 ± 1.3	-0.9 ± 0.5	-1.1 ± 0.5
Subthreshold slope [mVdec^{-1}]	$1{,}566 \pm 460$	$1{,}002 \pm 208$	484 ± 133	189 ± 54
Interface trap DOS [cm^{-2}eV^{-1}]	1.88×10^{12}	3.45×10^{12}	5.05×10^{11}	4.40×10^{11}
Hysteresis [mV]	725 ± 375	1475 ± 225	595 ± 45	125 ± 105

Next, we used Equation 2.9 to calculate the interface trap DOS from the subthreshold slopes. Here we used the interface trap DOS as the main parameter affecting the subthreshold slope since we controlled it through passivation. Table 4.1 summarizes the respective interface trap DOS. The results demonstrated that the interface trap DOS for the untreated oxides were high and heterogeneous but substantially stabilized after COC passivation. Because of interface trap state inhomogeneities, the subthreshold slope did not linearly follow the capacitance as predicted by the Equation 2.9. Since COC passivation reliably stabilized TFT performance, we also realized the scaling behavior (Figure B.7).

4.5.2 Investigation of Transistor Operation Regions

Having proved the potential benefits of interface trap state passivation, we now focus on revealing the transistor operation regions. To this point, we present the transconductance plot along with the transfer curve on a square-root scale. This combined graph enables us to reveal the linear region from the transconductance plot, and from the square-root scale, we reveal the saturation and subthreshold regions. We use the transconductance here instead of transfer curve on a linear scale. The reason is that the transconductance (derivative of the drain current) is more responsive and must provide a transconductance plateau if the drain current has a constant slope on a linear scale. We then extrapolate the saturation current on a square-root scale to determine the threshold voltage.

Figure 4.8a-b compare the transistors with the highest drain current from the previous measurements on untreated 300 nm and 100 nm-thick oxides, respectively. First, TFT characteristics were similar regardless of the oxide thickness. The main difference was that TFT on thinner oxide needed lower operating voltages in agreement with the semi-logarithmic plot. In both transistors, no transconductance plateau was observed even though the applied drain voltage was substantially less than the gate voltage range. Contrarily, transconductance was increasing with the gate bias. These results confirmed that the transistors were not operat-

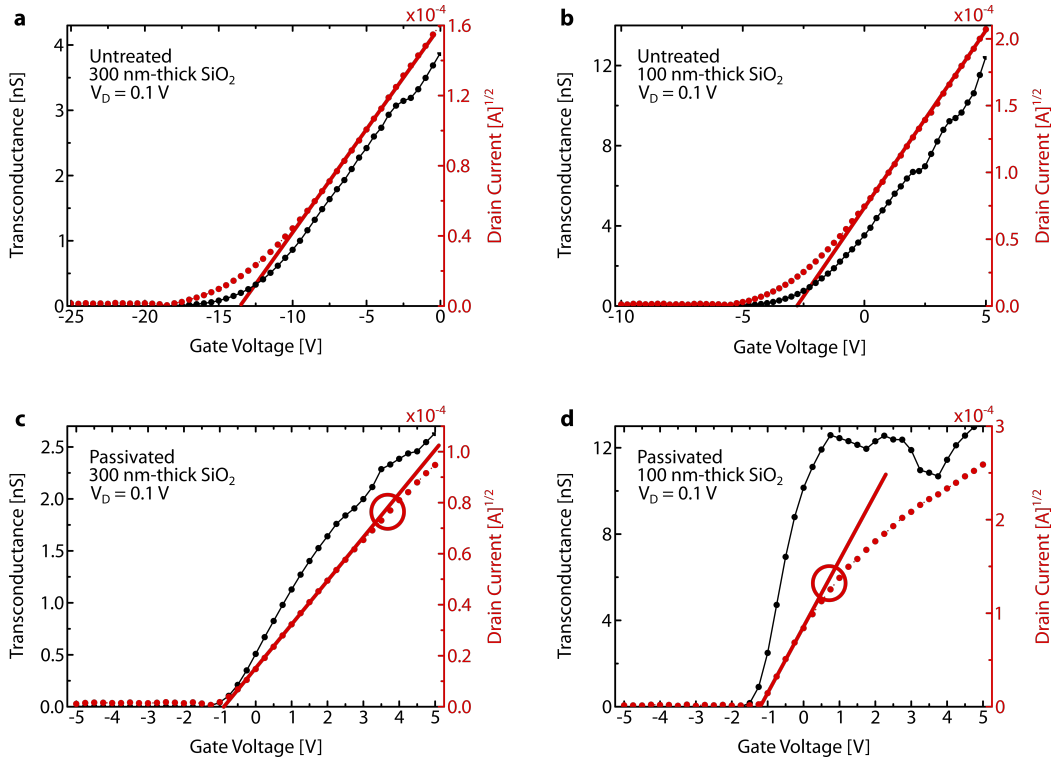

Figure 4.8: Revealing operation regions of MoS_2 TFTs on untreated and passivated oxides for various oxide thicknesses for V_D = 0.1 V. Transconductance curve and square-root plot of the transfer curve of MoS_2 TFTs on **a** untreated 300 nm-thick oxide, **b** untreated 100 nm-thick oxide, **c** passivated 300 nm-thick oxide, and **d** passivated 100 nm-thick oxide. The black and red y-axes represent transconductance curve and transfer curve on a square-root scale, respectively. The red solid lines indicate the extrapolations of saturation currents, the red circles indicate the saturation-to-linear transition point.

ing in the linear region. Instead, we observed a substantial subthreshold region. Therefore, it is evident that if interface trap states dominate the transistor, any estimation for operation regions (consequently, mobility) would be inaccurate.

Figure 4.8c-d compare the TFT characteristics on passivated 300 nm and 100 nm-thick oxides. On the square-root scale, it was evident that COC passivation significantly suppressed the subthreshold region, even for TFTs on 300 nm-thick oxide. The estimated threshold voltage was approximately -0.85 V. Additionally, the increase of transconductance was significantly more rapid than the TFT on untreated 300 nm-thick oxide; the latter required nearly 10 V for a 2 nS increase in transconductance, whereas the former required only 3.5 V for the same increase (Figure 4.8c). Although we cannot achieve a distinct transconductance plateau yet, to some extent, we observed a saturation-to-linear transition point toward the high gate bias limit at around V_G = 3.5 V on the square-root scale.

The TFT on passivated 100 nm-thick oxide performed exceptionally well. A rapid increase in transconductance followed by a plateau around 12 nS. We also observed a clear saturation-to-linear transition point at the gate voltage where the transconductance plateau started. The estimated threshold voltage was -1.19 V. After evaluating all the results, we concluded that the operation regions could only be revealed by interface passivation and increasing the oxide capacitance.

Comparison of transistors shown in Figure 4.8 shed light on the contest between the interface trap DOS and the density of field-effect charges, affecting charge transport dramatically. On the one edge, low capacitance and high interface trap states (untreated 300 nm-thick oxide) caused Fermi level pinning in deep states and hence deep level hopping transport. As a result, the transconductance strongly depended on the density of the field-effect charges. On the other edge, high capacitance and low interface trap states (passivated 100 nm-thick oxide) allowed the Fermi level shift into the tail states by the applied gate bias. Here, only a limited fraction of field-effect charges could enter the conduction band, with the remainder going into the tail states like in multiple trap and release model. However, this was enough to establish the operation regions similar to a-Si:H transistors (Figure 2.11).

4.5.3 Effect of Drain Bias on the Operation Regions

The results clarified that COC-passivated 100 nm-thick oxide is suitable for further characterization. We now concentrate on the drain bias dependence of the TFT to uncover its saturation region. We measured the transistor under various drain voltages (0.1 V, 1 V, and 5 V) for a gate voltage range of ±5 V. The left and right y-axes of the graphs are now semi-logarithmic and square-root scales. Here, we can extract all the necessary parameters, the off-state region, the onset voltage, the subthreshold region and its slope, the threshold voltage, the saturation region, and the linear region. In Figure 4.9, the blue dashed lines represent the onset voltage (when the current reaches 10^{-11} A), while the blue solid lines represent the subthreshold slope. The red solid lines represent the extrapolation of the saturation current, while the red dashed lines represent the threshold voltage. The voltage gaps between the onset and the threshold voltages are indicated at the top of the graph.

The transistor demonstrated nearly ideal performance at $V_D = 0.1$ V (Figure 4.9a). We estimated an onset voltage of -2 V and a threshold voltage of -1.77 V. Subthreshold slope linked off-state region to saturation region, as predicted by the ideal transistor characteristics. With the increase of the drain bias to 1 V (Figure 4.9b), the onset and threshold voltages were slightly

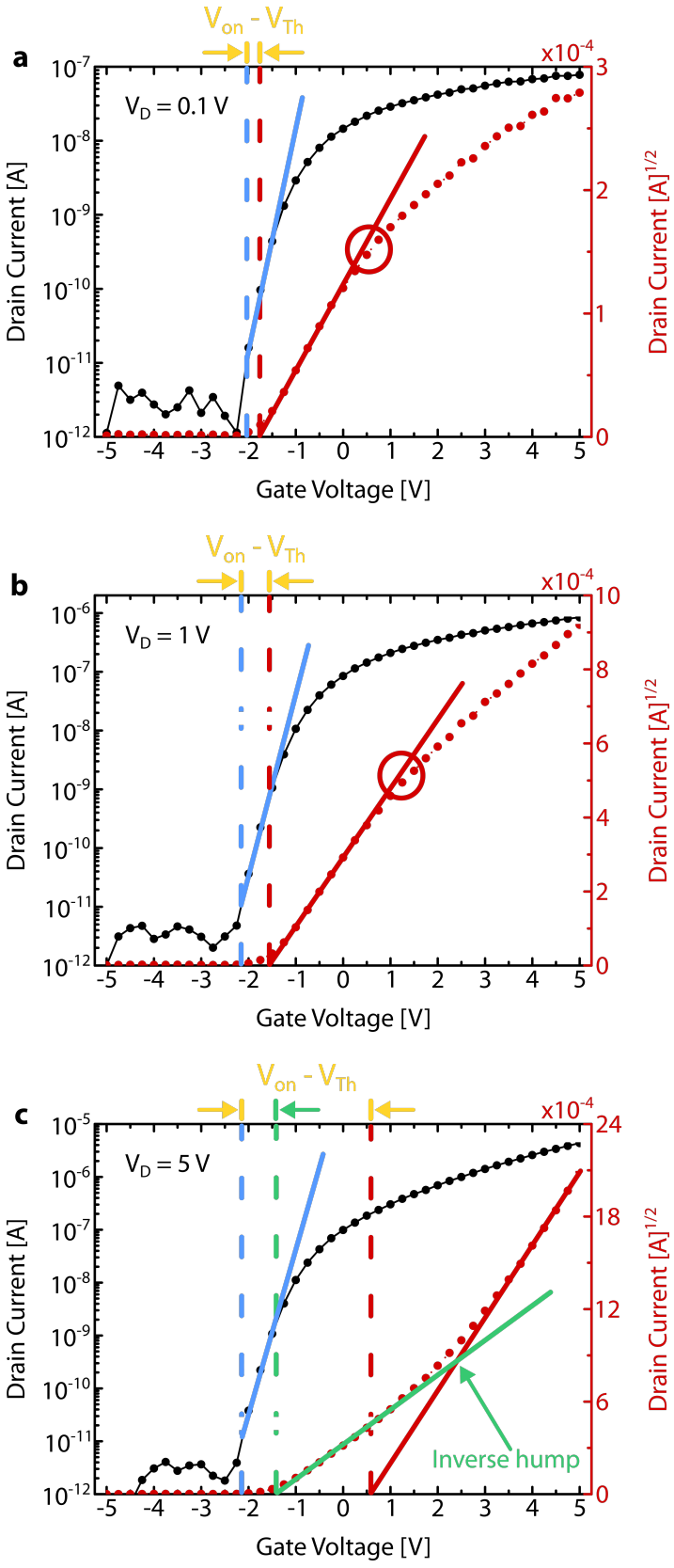

Figure 4.9: Characteristics of MoS_2 TFTs on passivated 100 nm-thick oxide for **a** V_D = 0.1 V, **b** V_D = 1 V, and **c** V_D = 5 V. The black and red y-axes represent transfer curves on the semi-logarithmic and square-root scales, respectively. The red circle indicates the saturation-to-linear transition point. The red and blue solid lines represent the extrapolations of saturation currents and the subthreshold slopes. The red and blue dashed lines represent the estimated onset and the threshold voltages. The green solid line indicates the estimation of the second threshold voltage.

shifted to -2.16 V and -1.55 V, respectively. Although these shifts gave rise to 0.6 V gap between the onset and threshold voltages, the subthreshold slope still linked the off-state region to the saturation region.

The increase of the drain voltage to 5 V caused a dramatic change in transistor characteristics (Figure 4.9c). The drain bias did not affect the onset voltage while significantly affecting the threshold voltage. The voltage gap between the onset and threshold voltages increased to 1.55 V. Typically, this gap denotes a significant subthreshold slope. The subthreshold slope, however, remained unchanged between 0.1 V (373 $mVdec^{-1}$) and 5 V (346 $mVdec^{-1}$). In addition, the saturation current exhibited a straight increase rather than a superlinear increase. In light of these indications, we extrapolated this region (represented by green solid line) and the extrapolation of the saturation current at low gate bias region brought a new threshold voltage of -1.39 V, which was very close to the threshold voltage for a 1 V drain bias (-1.55 V). Once we introduced this voltage as the new threshold voltage, the subthreshold slope could even link the off-state and saturation regions.

We called this behavior an "inverse" hump; here, the hump is inwards instead of outwards, as in the contact hump. The saturation current characteristics in the presence of the inverse hump exhibited similarities to the a-Si:H TFT, where the authors claimed the observation of Anderson transition (Figure 2.14). According to their measurements, the a-Si:H TFT exhibited a sharp increase in the saturation current after the Anderson transition, similar to our results. However, the inverse hump in MoS_2 TFTs occurred at lower voltages, possibly due to the weaker disordered nature of the MoS_2 crystals. In addition, we could only observe the inverse hump at high drain biases. Nonetheless, temperature-dependent measurements, like those performed by Pepper in a Si MOSFET, are required to prove the existence of the Anderson transition [85].

Comparison of MoS_2 crystals from different providers

Up to this point, the MoS_2 crystals were grown and provided by the group of Prof. Turchanin (FSU). However, the quality of CVD growth of MoS_2 crystals can vary from method to method, so we fabricated and investigated MoS_2 crystals grown by the group Prof. Högele (LMU) to compare the possible differences in MoS_2 transistors. From now on, we indicate the FSU-grown MoS_2 crystals as FSU MoS_2 transistors and LMU-grown MoS_2 crystals as LMU MoS_2 transistors. We followed the same fabrication steps as we did for the FSU MoS_2 transistors. Figure 4.10 depicts the characteristics of LMU MoS_2 TFT as a function of drain bias. At first glance, we

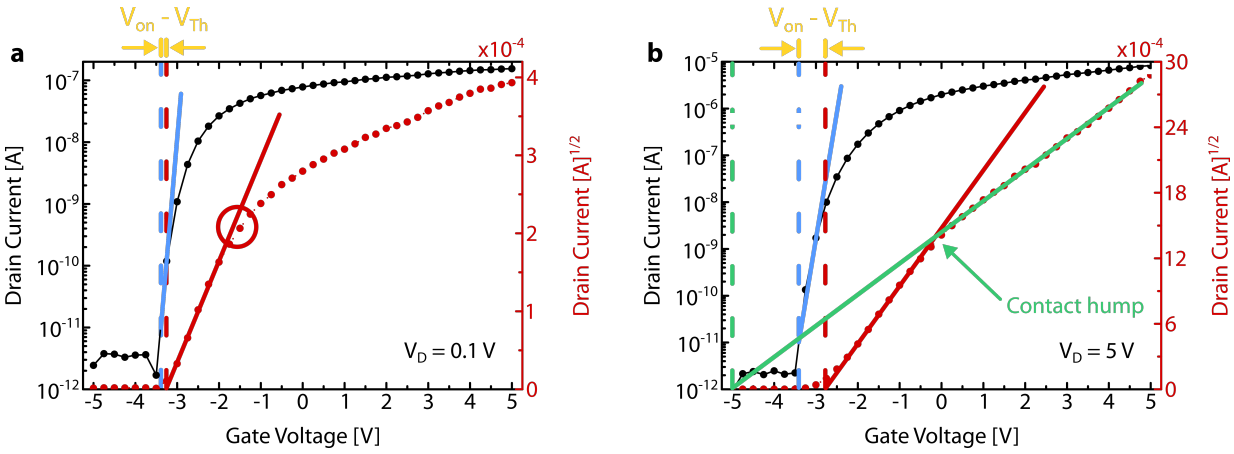

Figure 4.10: Characteristics of MoS_2 TFTs (crystals provided by group of Prof. Högele) on passivated 100 nm-thick oxide for **a** V_D = 0.1 V, and **b** V_D = 5 V. The black and red y-axes represent transfer curves on the semi-logarithmic and square-root scales, respectively. The red circle indicates the saturation-to-linear transition point. The red and blue solid lines represent the extrapolations of saturation currents and the subthreshold slopes. The red and blue dashed lines represent the estimated onset and the threshold voltages. The green solid line indicates the estimation of the second threshold voltage.

observed that the onset voltage shifted from -2 V to -3.4 V for V_D = 0.1 V. However, the voltage gap between the onset and threshold voltages was relatively small as 0.13 V compared to FSU MoS_2 TFTs (Figure 4.10a). Likewise, the gap corresponded to the subthreshold slope.

Figure 4.10b represents the transistor characteristics for V_D = 5 V. The onset voltage remained nearly constant while the threshold voltage increased by 0.47 V, but the subthreshold slope could still link the off-state region to the saturation region. We found, however, that the transistor exhibited a contact hump in the saturation current. The estimation of the threshold voltage after the hump (the green solid line) was approximately -5 V. This threshold voltage significantly exceeded the onset voltage. In addition, if the estimation would be accurate, the transistor must exhibit a saturation-to-linear transition point, due to the fact that the drain bias became lower than the V_G - V_{Th} at higher gate voltages, but it did not. Therefore, assuming the threshold voltage was more accurate after the contact hump is also not convincing.

In order to perform a quantitative analysis, we compared the mobility characteristics of both providers (Figure 4.11). We used the linear mobility equations (Equation 2.4) for low drain bias and the saturation mobility equations (Equation 2.7) for high drain bias conditions. FSU MoS_2 exhibited a clear mobility plateau at around 4.5 $cm^2V^{-1}s^{-1}$ for V_D = 0.1 V. Nonetheless, once we increased the drain voltage to 5 V, the mobility characteristics were drastically altered due to the inverse hump. Mobility tended to saturate until V_G = 2 V but then increased up to 15 $cm^2V^{-1}s^{-1}$ at V_G = 5 V. The point of rapid increase corresponded to the inverse hump. On

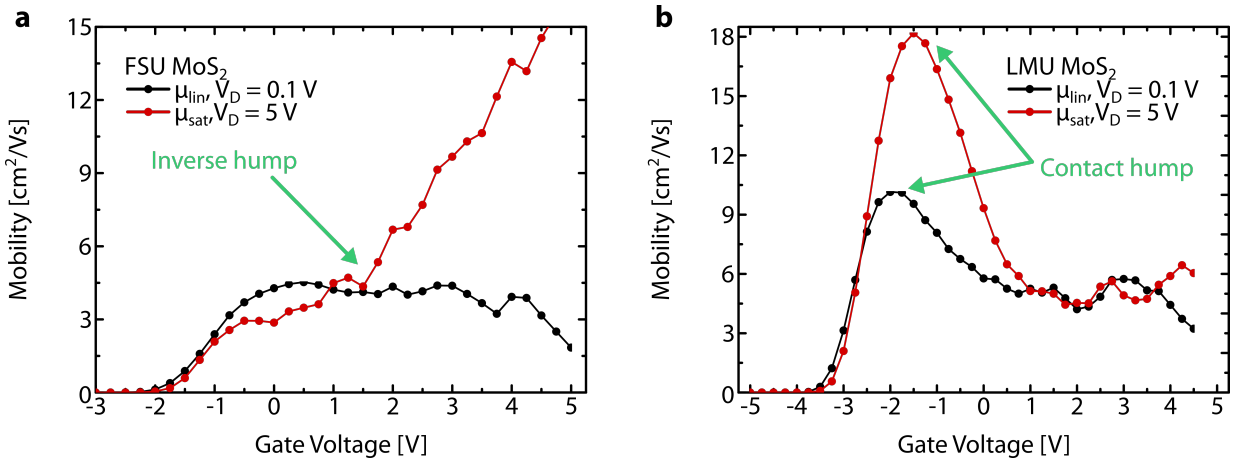

Figure 4.11: Mobility characteristics of **a** FSU MoS_2 TFTs, and **b** LMU MoS_2 TFTs for low and high drain biases. FSU and LMU indicates the provider of the MoS_2 crystals.

the other hand, LMU MoS_2 exhibited a mobility peak due to the contact hump for both drain biases. The mobility peak for V_D = 0.1 V was nearly two times higher than its plateau value, whereas the mobility peak for V_D = 5 V was nearly four times higher. However, the mobility became constant around 5 $cm^2V^{-1}s^{-1}$ beyond a gate voltage of 1 V, regardless of the drain bias.

When we compared the characteristics of the MoS_2 transistors from both groups:

- We did not observe significant differences in the mobility values, except the types of the humps.
- We later found that the onset voltage of the LMU MoS_2 TFT was also shifted to lower gate voltages after several days in the desiccator, became similar to the onset voltage of FSU MoS_2 TFT. This is an important outcome, indicating that the performance of the FSU MoS_2 TFT would always be lower due to the time spent on sample delivery.
- The puzzle of the different hump types between the crystals motivated for a new set of samples, which will be explained in the following subsection.

Transistor characteristics of LMU MoS_2 crystals on passivated 50 nm-thick oxide

We fabricated LMU MoS_2 TFTs on a passivated 50 nm-thick oxide to increase the oxide capacitance further. For the new gate stack, we predicted an oxide capacitance of 59.2 $nFcm^{-2}$. Figure 4.12a represents the characteristics of 10 MoS_2 TFTs for V_D = 0.1 V. The transistors exhibited onset voltages of around -1 V. While transconductances reached 100 nS, on/off ratios

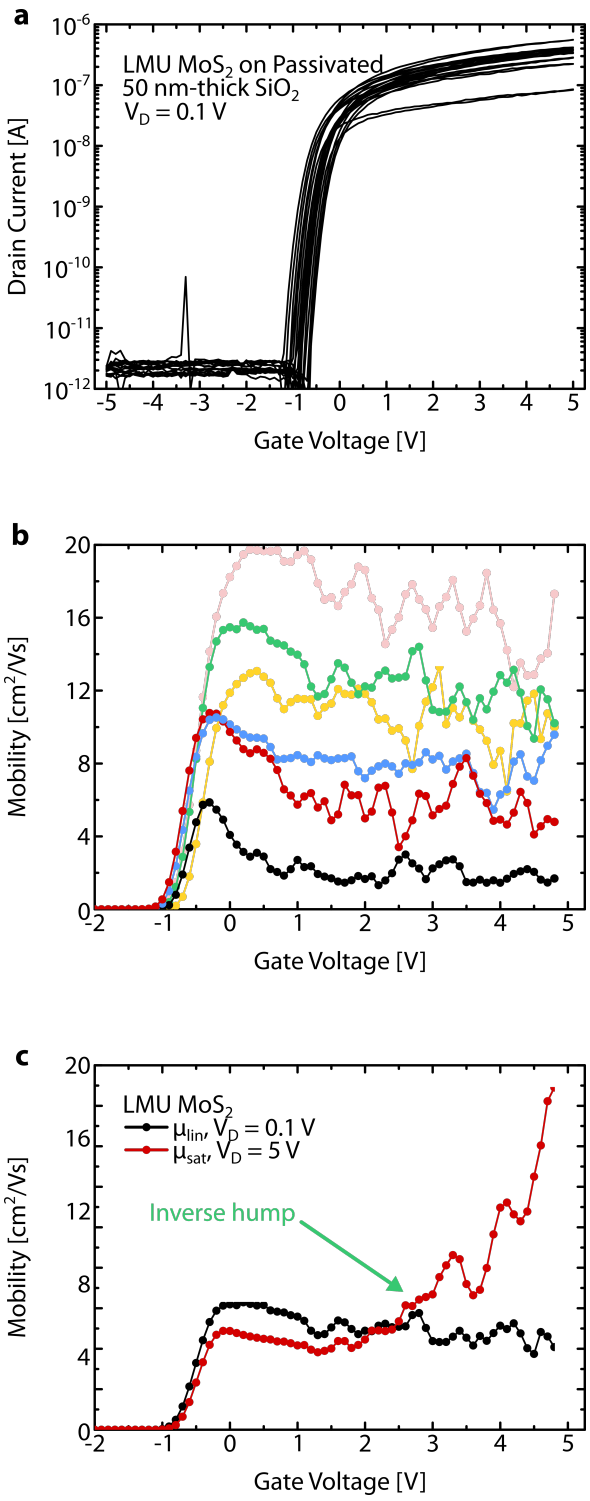

Figure 4.12: Characteristics of LMU MoS_2 TFTs on passivated 50 nm-thick oxide. **a** Transfer curves of 10 LMU MoS_2 transistors on a semi-logarithmic scale. **b** Linear mobility characteristics of the selected transistors. **c** Mobility characteristics of MoS_2 TFT under 0.1 V and 5 V dran bias.

reached up to 10^6. The performance of the transistors was promising, even though measurements were performed four days after fabrication, which lowered the overall performance of the transistors.

The transistor characteristics became clear when we examined the estimated mobility values of the chosen TFTs (Figure 4.12b). First, the mobility values exhibited a broad distribution. The transistor with the highest drain current naturally had the highest mobility, around 17 $cm^2V^{-1}s^{-1}$ with no sign of contact hump. However, the transistor with the lowest drain current exhibited a contact hump and a mobility value as low as 2 $cm^2V^{-1}s^{-1}$ in the mobility plateau. The subthreshold slopes of transistors did not differ significantly in-between (133 $mVdec^{-1}$ to 143 $mVdec^{-1}$). The most striking aspect was that the TFT with the lowest mobility exhibited a mobility peak, while the TFT with the highest mobility did not. Comparing all TFTs, it was evident that the TFTs that exhibited a mobility peak later exhibited a poor mobility plateau value. In contrast, TFTs without mobility peaks consistently exhibited higher mobility plateau values. Since all TFTs were on the same substrate and fabricated identically, we deduced that the mobility peak was not related to Schottky barriers but rather to poor contacts. Scanning photocurrent microscopy micrographs revealed that the contact quality of the transistors on the same substrate, even within the same transistor, can be uneven (Figure B.9).

We finally performed high drain bias measurements and compared the mobility characteristics for low and high drain biases for one of the selected transistors (Figure 4.12c). We surprisingly observed the signs of inverse hump in mobility trend for $V_D = 5$ V. Consequently, we confirmed that the LMU MoS_2 TFT also exhibited inverse hump, similar to FSU MoS_2 TFT. The comprehensive investigation reveals that the contact humps are related to poor contacts, and the inverse humps can be observed in MoS_2 TFTs regardless of the growth.

5

Plasma-Enhanced Ultrathin Oxides for Nanosheet Transistors

"Localization was a different matter: very few believed it at the time, and even fewer saw its importance; among those who failed to fully understand it at first was certainly its author."

— Philip W. Anderson

5.1 The Need for Ultrathin Oxides for Low-Voltage Electronics

A groundbreaking paper on the fabrication of low-power OSC complementary circuits was published by Klauk et al. in 2007 [39]. In this study, the organic TFTs were fabricated through a novel gate stack architecture. The authors employed aluminum as the gate electrode, which naturally oxidizes up to 1.6 nm. Then, the native aluminum oxide was subjected to a "plasma-enhanced oxidation" process. Performing the oxidation step in a reactive ion etching (RIE) chamber under pure oxygen gas increased the thickness of the native aluminum oxide up to 3.6 nm. Specifically, RIE was necessary for this enhancement due to anisotropic acceleration of oxygen ions, where the ions could penetrate the material deeper and thus enhance oxidation.

Nonetheless, tested for a 100 µm by 100 µm capacitor area (patterned with shadow masks), 3.6 nm-thick aluminum oxide was not sufficient to operate the capacitors within an acceptable voltage range (±3 V, Figure 5.1). Further reduction of leakage currents was then enabled by SAM passivation. After being subjected to plasma-enhanced oxidation, the oxide surface was

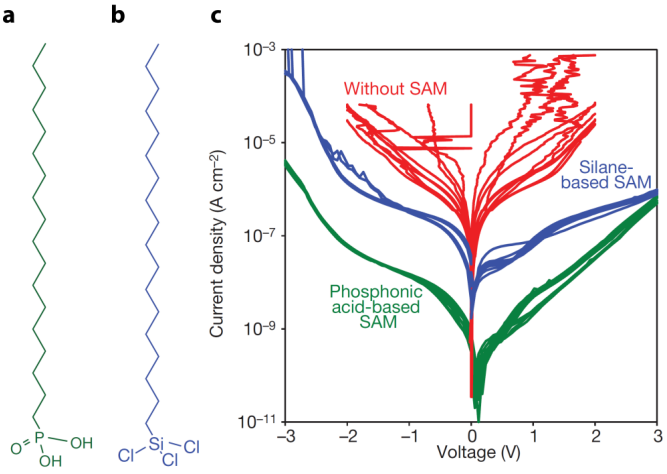

Figure 5.1: Molecular structures of SAMs and leakage current characteristics of untreated and SAM-passivated plasma-enhanced oxide. Illustration of the molecular structure of **a** n-octadecylphosphonic acid, and **b** n-octadecyltrichlorosilane. **c** Leakage current characteristics of the untreated, silane-based SAM-passivated, and phosphonic acid-based SAM-passivated capacitors. Adapted from [39].

already primed for strong chemical bonding with SAM. Even though silane-based SAM (Figure 5.1a) reduced leakage currents to below 10^{-3} Acm^{-2}, phosphonic acid-based SAM (Figure 5.1b) also met the leakage currents of modern electronics by reducing them to below 10^{-5} Acm^{-2} as shown in Figure 5.1c.

Then, p- and n-conductor OSCs were evaporated for TC transistor fabrication (inset of Figure 5.2a). Figure 5.2a-b represents the performance of pentacene and F_{16}CuPc TFTs. On the one hand, the pentacene TFT demonstrated excellent performance, including an on/off ratio of seven orders of magnitude and mobility value of 0.6 cm^{2}V^{-1}s^{-1} within an operation range of only 3 V. On the other hand, F_{16}CuPc TFT showed similar performance characteristics, except

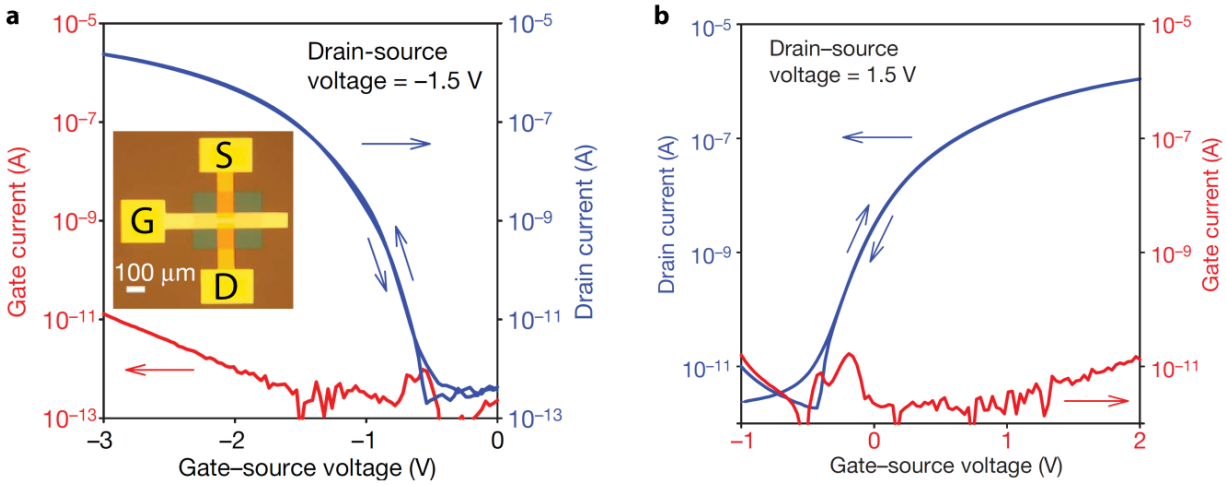

Figure 5.2: Low-voltage pentacene and F_{16}CuPc transistors on passivated plasma-enhanced aluminum oxide. **a** Drain and gate currents of pentacene TFT on a semi-logarithmic scale. Inset represents the optical microscopy image of the transistor. **b** Drain and gate currents of F_{16}CuPc TFT on a semi-logarithmic scale. Adapted from [39].

for its lower mobility of 0.02 $cm^2V^{-1}s^{-1}$. Nonetheless, to compensate the low mobility geometrically, the channel width of the $F_{16}CuPc$ TFT was increased to 1,000 µm, whereas the channel width of the pentacene TFT was only 100 µm. Each TFT had a channel length of 30 µm.

Before this groundbreaking study, organic TFTs typically required operation voltages in the tenths of a volt due to thick gate insulators (soft (polymer) or hard (SiO_2)), resulting in low capacitances of around (10 to 30) $nFcm^{-2}$ [86]. Therefore, a new era for low-voltage organic transistors was ushered by realization of this novel gate stack. For example, use of a double gate stack allowed Sekitani et al. to fabricate nonvolatile floating gate memory arrays on flexible substrates (Figure 5.3) [87]. In a floating gate transistor, one gate stack (control gate) was used to operate the transistor, and the other gate stack (floating gate) was used to trap charge to shift the threshold voltage in a controlled fashion. Sze provided a concise overview of floating gate transistors (p.352, 3rd Ed). The authors first performed multiple gate voltage sweeps in a double capacitor teststructure to examine the stability of the double gate stack. Up to 100 measurements, at a maximum applied voltage of 6 V for a capacitor area of 3×10^{-4} cm^2, the leakage currents were consistent (Figure 5.3a). A pentacene floating gate transistor was subsequently fabricated to investigate memory operation further (Figure 5.3b). The threshold voltage window (2 V) and device-to-device uniformity were adequate for clear read-out if the transistor was programmed at -6 V and erased at +3 V, as demonstrated by the gate voltage difference between two read-out operations.

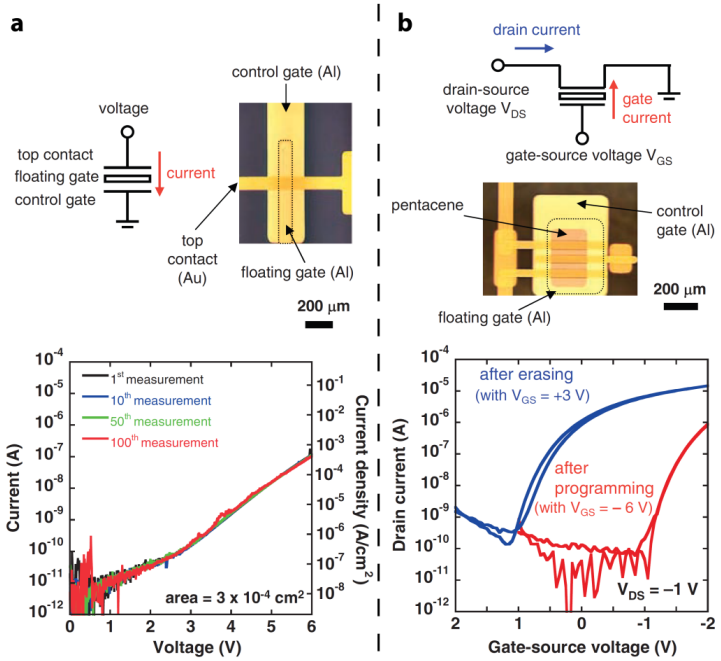

Figure 5.3: Characteristics of the floating-gate memory transistors. **a** Top: Illustration and the optical microscopy image of the floating-gate capacitor. Bottom: Leakage current characteristics of the floating-gate capacitor over 100 sweep cycles. **b** Top: Illustration and the optical microscopy image of the floating-gate transistor. Bottom: Characteristics of the floating-gate transistor. Programming and erasing read-outs exhibited a memory window of 2 V. Adapted from [87].

Even though OSCs have a mobility disadvantage, they are promising for utilization in flexible electronics. To this point, organic electronics on a five-Euro note was realized by Zschieschang et al. by this novel gate stack [88]. Figure 5.4a depicts the picture of the complementary circuit on the banknote and a close-up microscopy image of a single transistor. Even on a banknote, the p-conductor DNTT TFTs exhibited impressive characteristics such as a mobility value of 0.2 $cm^2V^{-1}s^{-1}$ and a subthreshold slope of 100 $mVdec^{-1}$ with a 92 % working transistor yield (Figure 5.4c). For the n-conductor $F_{16}CuPc$, the authors compensated the mobility mismatch geometrically, as they did for transistors on the glass substrate (Figure 5.4d). Although the transistors exhibited higher leakage currents, the authors could still achieve impressive results: a supply voltage of about 3 V, static power consumption of 1 nW, and a small-signal gain of about 100 on a five-Euro note.

Geiger et al. then performed a more systematic work toward optimizing plasma-enhanced oxidation [89]. The impact of plasma conditions on the aluminum oxide thickness and, by extension, leakage current, and transistor characteristics was investigated in this article. As measured by transmission electron microscope cross-section image, Figure 5.5a represents aluminum oxide thicknesses as a function of plasma power and duration. Controlling the plasma conditions allowed the authors to achieve a range of oxide thicknesses from 4.3 nm to 7.3 nm.

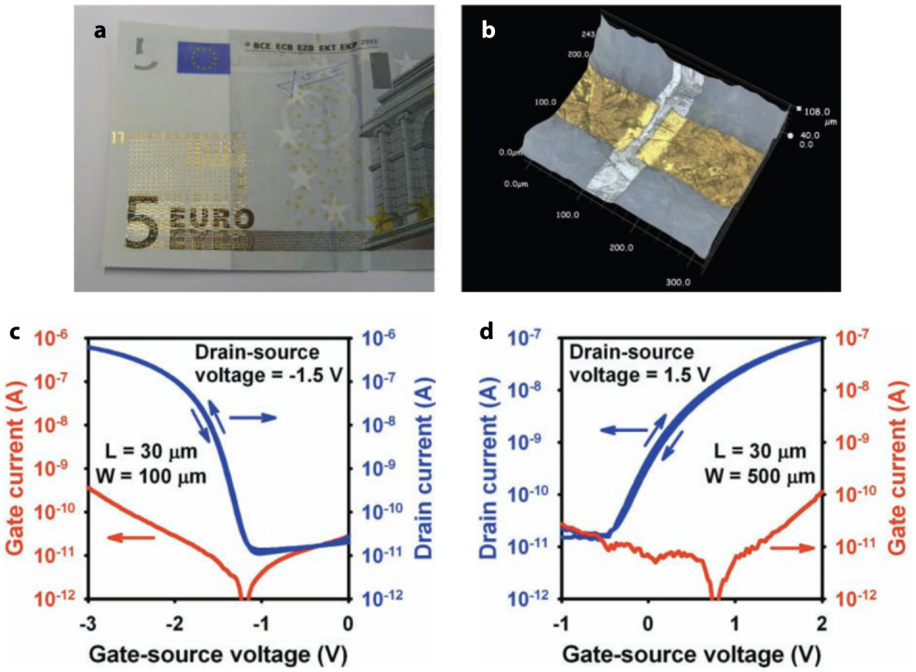

Figure 5.4: Organic electronics on 5-Euro note. **a** Picture of the organic complementary circuit on 5-Euro note. **b** Optical microscopy image of an individual organic transistor on banknote. **c** Characteristics of DNTT transistor on banknote. **d** Characteristics of $F_{16}CuPc$ transistor on banknote. Adapted from [88].

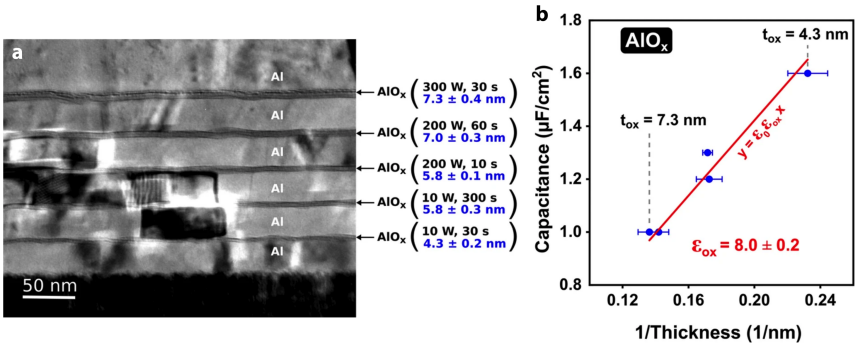

Figure 5.5: Determination of the thickness of plasma-enhanced aluminum oxides for various plasma parameters. **a** Cross section TEM image of several gate stacks for various plasma powers and duration. **b** Capacitance-thickness curve of the plasma-enhanced aluminum oxide for the determination of relative dielectric constant. Adapted from [89].

Combining the measured capacitances and the corresponding thicknesses, the authors determined the relative dielectric constant of the plasma-enhanced aluminum oxide as 8.0 (Figure 5.5b).

The leakage current performance of untreated and SAM passivated aluminum oxides under different plasma conditions was then studied in capacitor test structures (Figure 5.6). The capacitor performed like a resistor after a 10 W 30 s oxygen plasma, but after 300 W 30 s, the leakage currents were significantly suppressed. Consequently, the plasma power significantly improved the leakage characteristics for a fixed plasma duration. In contrast, the leakage current almost reached saturation after 60 s for a constant 200 W plasma power, suggesting that the plasma-enhanced oxidation was a self-limiting process. In the case of SAM passivation,

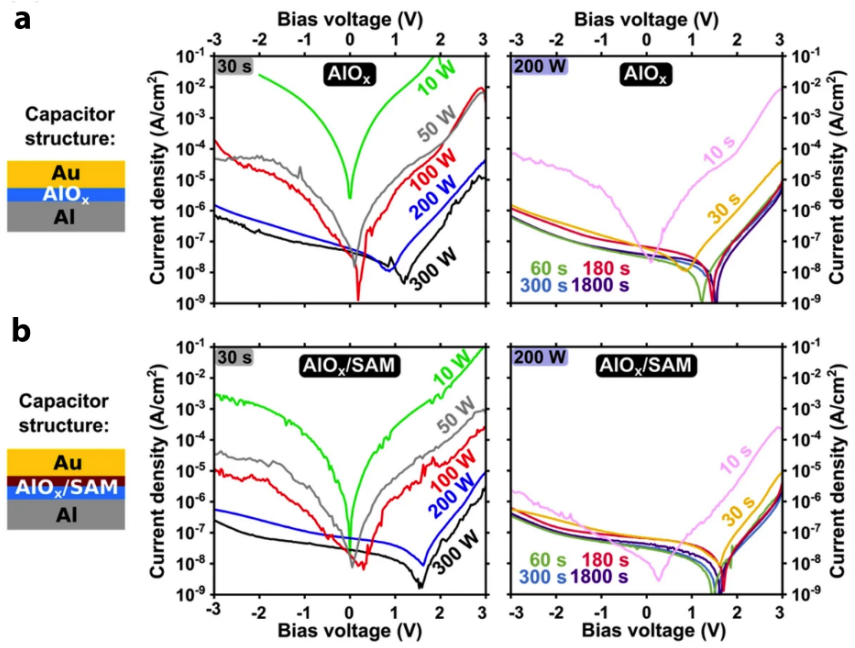

Figure 5.6: Leakage current characteristics of untreated and SAM-passivated plasma-enhanced aluminum oxide for various plasma parameters for **a** untreated oxide, and **b** SAM-passivated oxide. Adapted from [89].

the leakage currents were lower, but they did not improve further for plasma durations longer than 60 seconds for 200 W plasma power as well. In this chapter, we utilize this novel gate stack to fabricate MoS_2 nanosheet TFTs to meet the saturation conditions at lower drain voltages to investigate the non-ideal saturation characteristics further.

5.2 Producing Plasma-Enhanced Aluminum Oxide

5.2.1 Deposition of Aluminum Film

Despite the technique's apparent simplicity, we encountered several challenges when putting into practice. The roughness of the aluminum film was the first problem to solve. The electron beam evaporation is the most efficient method for metal deposition. This method, however, became a bottleneck in producing high-quality aluminum films. The surface roughness of the electron beam evaporated 30 nm-thick aluminum film with an evaporation rate of 1 $Å s^{-1}$ is shown in Figure 5.7a. Here, droplets appeared on the aluminum film, adding significantly to its roughness (4 nm in RMS). Such roughness values were unacceptable for a gate stack. Therefore, our electron beam evaporator's current configuration did not enable the production of smooth aluminum films.

We then introduced the thermal evaporation method, based on melting metals in an evaporation boat using ohmic (Joule) heating. Unfortunately, the thermal evaporation of aluminum did not solve the problems at once. Since molten aluminum has a low surface tension, it quickly wetted the boat and caused spilling during the evaporation. Additionally, aluminum

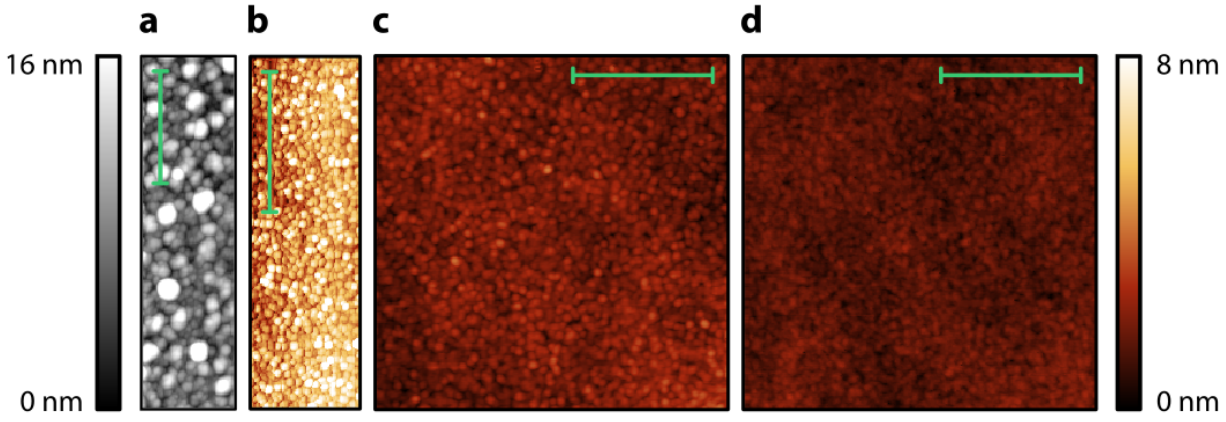

Figure 5.7: Determination of the roughness of 30 nm-thick aluminum films by AFM. **a** Electron-beam evaporated, and **b** thermally evaporated aluminum films. Thermally evaporated aluminum film **c** after 1 min, and **d** after 5 min plasma oxidation. Scale bars are 400 nm for all micrographs.

formed an alloy with the boat after melting, significantly altering the boat's resistance. These changes caused rate instabilities, affecting the smoothness of the aluminum film. Kurt Lesker's innovative boat design helped us overcome this obstacle. This design separates the titanium boride crucible (EVC9INTSPL01) from the tungsten heater (EVCH10). The separation prevents the alloy problem and, consequently, rate fluctuations. Not only that but the crucible towers above the heater socket. This area is known as the "cold lip," in which aluminum condenses during evaporation due to a significant temperature drop and preventing spilling. Using this specialized pot, we could bring the RMS roughness down to 1.5 nm with stable evaporation rates (Figure 5.7b).

As was also observed by Geiger et al., oxidation made it possible to reduce the roughness further. Figure 5.7c represents the morphology of the aluminum film following oxidation (300 W, 60 s). The oxygen ion bombardment enabled a drastic decrease in RMS roughness to 0.45 nm. With an increase in the plasma duration to 5 minutes, we achieved the RMS roughness as low as 0.34 nm (Figure 5.7d).

5.2.2 Optimizing the Oxidation Process

Aluminum corrosion after oxidation

RIE systems are commonly employed in dry etching processes. For this reason, many different gas compositions, such as SF_6 and Cl_2, are involved in etching recipes. Since chlorine is corrosive to aluminum, the latter posed a significant problem to the oxidation process. Figure 5.8 represents the optical microscope image of the chlorine-associated corrosion in aluminum film after oxidation. Extending the time of the chamber cleaning procedure and then performing a longer (at least 15 min) preconditioning step before processing the sample prevented the corrosion.

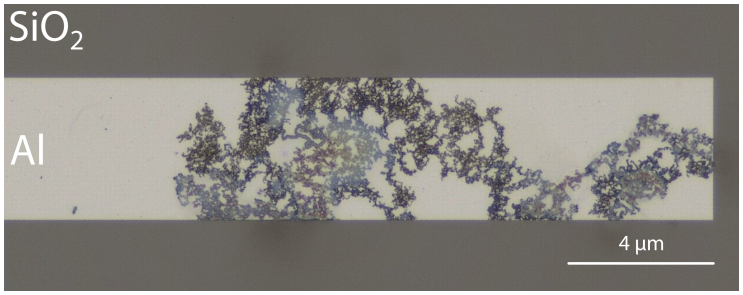

Figure 5.8: Chlorine-associated aluminum corrosion after plasma oxidation.

Aluminum blistering after oxidation

The plasma-enhanced oxidation occurs under very intense plasma conditions, such as a plasma power of 300 W. Therefore, substrates experience a significant temperature increase due to the oxygen ion bombardment. As shown in Figure 5.9, this can cause aluminum blistering. The generated heat could sometimes be high enough that blistering can occur within a minute. Using synthetic oils such as fomblin improves the heat dissipation of the substrate. However, the oil must be thoroughly cleaned with acetone after oxidation. Otherwise, it can potentially contaminate the sample surface during the lift-off.

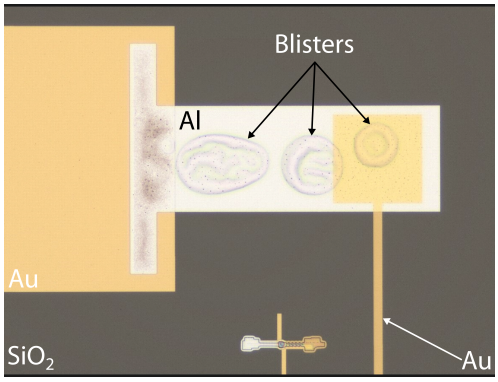

Figure 5.9: Plasma-associated aluminum blistering after oxidation.

Effect of evaporation rate on the aluminum edge quality

We discovered that the aluminum's evaporation rate significantly affected the gate stack's edge quality after lift-off. On the one hand, higher deposition rates lead to smoother aluminum films [90]. On the other hand, in the case of lithography patterning, higher deposition rates (25 $Å s^{-1}$) caused rougher edges, as depicted in Figure 5.10. We found that the 15 $Å s^{-1}$ is the optimum evaporation rate for film smoothness and edge sharpness.

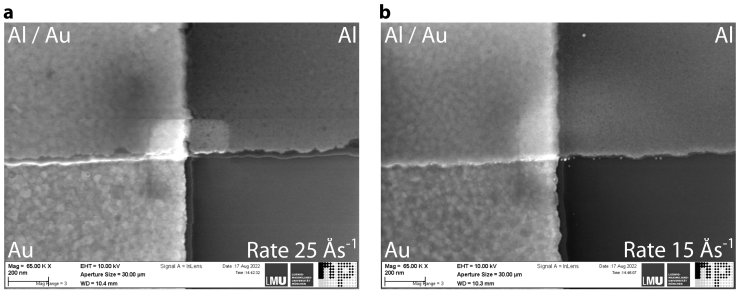

Figure 5.10: Effect of aluminum evaporation rate on the edge quality of the gate stack. **a** 25 $Å s^{-1}$. **b** 15 $Å s^{-1}$.

Strong adhesion of PMMA after oxidation

We noticed significant residues on the gate electrode while we fabricated the capacitor test structures. Scanning electron microscopy (SEM) image of the capacitor intersection and a darkfield optical microscopy image of the fabricated capacitor are shown in Figure 5.11a-b, respectively. According to the images, the aluminum surface exhibited residues, while silicon oxide and gold surfaces were clean. We then realized that the reason was the high surface energy of the aluminum film after oxidation, which promoted the adhesion of the PMMA. To avoid PMMA residues, we passivated the primed surface with SAM, which reduced the surface energy and, consequently, the adhesion of PMMA (Figure 5.11c). Unlike the SAM passivation on the Si gate stack, the SAM passivation on the patterned aluminum oxide enabled the performing the subsequent lithography steps due to the optimized wetting geometry.

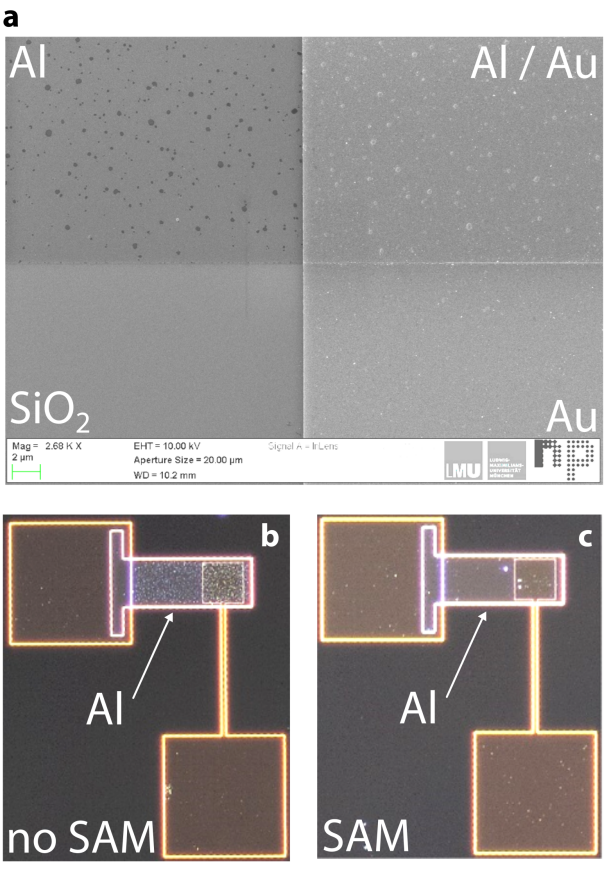

Figure 5.11: Plasma-associated PMMA contamination on the aluminum film. **a** SEM image of the capacitor intersection. Optical microscopy images of the **b** untreated, and **c** SAM-passivated oxides for capacitor test structures.

5.3 Optimization of Transistor Fabrication on Plasma-Enhanced Gate Stack

5.3.1 Capacitor Test Structures

Using the optimized deposition and oxidation parameters, we aimed for the lowest leakage possible for capacitor test structures. We defined the capacitor area as 50 µm to 50 µm and performed the oxidation at 300 W, the highest power available, for 60 s. We also tried 200 W, but our leakage currents were higher than those reported by Geiger et al. The variations in RIE systems might account for the deviation. Whereas Geiger et al. used a conventional RIE, we used an inductively coupled plasma (ICP) RIE for the oxidation process. In conventional RIE, there are two parallel plates, while in ICP-RIE, the top plate is replaced by an ICP tube. Since the plasma in an ICP tube is controlled independently, the latter provides superior plasma control. Nonetheless, this might have reduced the acceleration of the ions during oxidation, resulting in higher leakage currents.

Figure 5.12 represents the effect of patterning techniques and contact material on the leakage current characteristics of the capacitor test structures. In conventional single-layer PMMA resist, the PMMA profile is a step-like pattern. However, with a double-layer PMMA resists, the PMMA profile exhibits an undercut pattern, which allows a better lift-off experience. Therefore, in the case of an undercut pattern, we anticipated that the oxidation of the edges might be improved. Figure 5.12a compares the leakage current characteristics of single-layer and double-layer PMMA resists for patterning the capacitor test structures. Optimization of

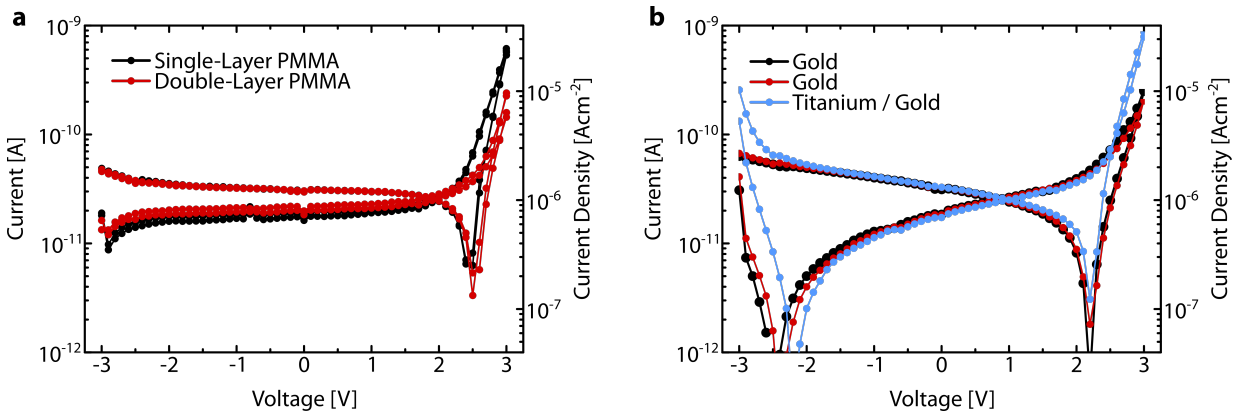

Figure 5.12: Leakage current characteristics of the capacitors with plasma-enhanced aluminum oxide as dielectric. Impact of **a** resist undercut, and **b** contact material.

the lithography steps led to a nearly five-fold reduction in leakage currents at +3 V. It is worth noting that no leakage current contribution from the gate edges was observed, as confirmed by measurements taken on various overlapping gates (Figure B.10).

Until now, we utilized gold contacts for the capacitor test structures. For MoS_2 nanosheet TFTs, however, we shall use titanium as the contact material. To address the differences, we fabricated capacitor test structures on three substrates: two with gold contacts for the substrate to substrate reliability and one with titanium/gold contacts (Figure 5.12b). Due to the oxidation process's uniformity, we obtained similar leakage current values from gold-contacted capacitors on different substrates. However, the leakage current values for titanium contacts increased from 200 pA to 1 nA. This increase implied that MoS_2 TFTs would have a narrower gate voltage range.

5.3.2 Transistor Layout

For the transistor geometry, we fabricated the transistors in two different contact layouts. For the first contact layout, we patterned the contacts so that the transistor channel was parallel to the local gate stack. Contrarily, for the second contact layout, we patterned the contacts so that the transistor channel was perpendicular to the local gate stack. Surprisingly, we could not turn off the transistors in the former layout (Figure 5.13a).

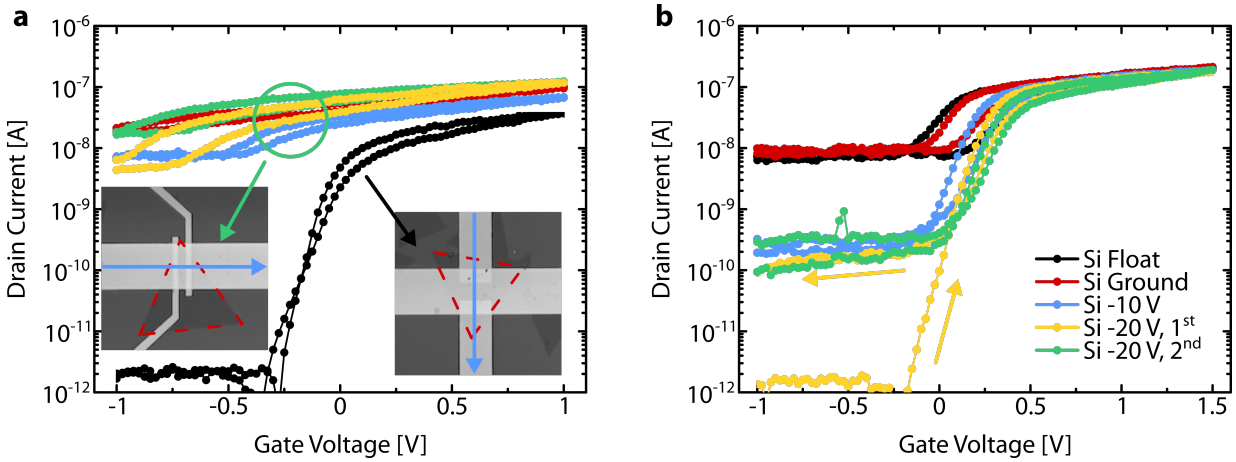

Figure 5.13: Role of transistor layout on the characteristics of MoS_2 TFTs on plasma-enhanced gate stack. **a** Transistor layout in parallel and perpendicular to the gate stack. The black dotted transfer curve represents the layout where the channel is perpendicular to the gate stack (black arrow indicates the corresponding inset). The colored dotted transfer curves represent the layout where the channel is parallel to the gate stack (green arrow indicates the corresponding inset). The blue arrows indicate the channel direction, and the red dashed triangle indicates the MoS_2 crystal. **b** Effect of Si back gate bias on the transistor characteristics. The yellow arrow indicates the sweep direction of the gate voltage.

In the first contact layout, the MoS_2 crystal outside the local gate stack (excess layer) played a critical role. Since we could not completely cover the crystals with the local gate, we could not entirely deplete the semiconductor with the local gate. These excess charges then contributed to the transistor current as a background because both contacts were connected over the excess layer (Figure 5.13a colored dotted lines). We applied bias to the Si back gate to deplete the excess charges to prove this idea. Figure 5.13b shows the transfer curve characteristics of MoS_2 TFTs on a semi-logarithmic scale as a function of the back gate bias. We observed a significantly high off-state current when the back gate was floating or grounded. Applying -10 V to the back gate reduced the off-state current to nearly 200 pA. An increase in the back gate bias (-20 V) helped to turn the transistor off during the FW sweep; however, once the transistor was turned on, the off-state current stabilized at 200 pA again in the BW sweep. Furthermore, the off-current was permanently stabilized; we could never turn the transistor off by a second sweep while the back gate bias was -20 V. A back gate electrode did not play any role in the background current; we obtained similar results for transistors on glass substrates. The results demonstrated that the MoS_2 crystals already exhibited a finite charge carrier density. Therefore, this layout is inappropriate for fabricating transistors in the presence of an excess layer.

Nonetheless, the transistor could be turned off once the channel was perpendicular to the local gate, as shown in Figure 5.13a (the black dotted line). The excess charges were blocked in this layout because the transistor channel was entirely on the local gate stack. This layout simplifies the transistor fabrication because etching the excess MoS_2 crystal is not necessary to diminish the effect of excess charges.

5.4 MoS_2 Nanosheet TFTs on Plasma-Enhanced Gate Stack

Using optimized fabrication steps, we fabricated the MoS_2 nanosheet transistor on the plasma-enhanced gate stack. Figure 5.14 represents the transfer curve characteristics of the transistor on semi-logarithmic and square-root scales. In Figure 5.14a, we observed that the high capacitance of the plasma-enhanced gate stack significantly reduced the applied gate biases. The transistor could be operated within a gate voltage range of ±0.75 V, which enabled low voltage operation conditions owing to the astonishingly steep subthreshold slope of 61.6 $mVdec^{-1}$ verified by a linear fit over two decades of current (Figure 5.15a). The transistor exhibited no

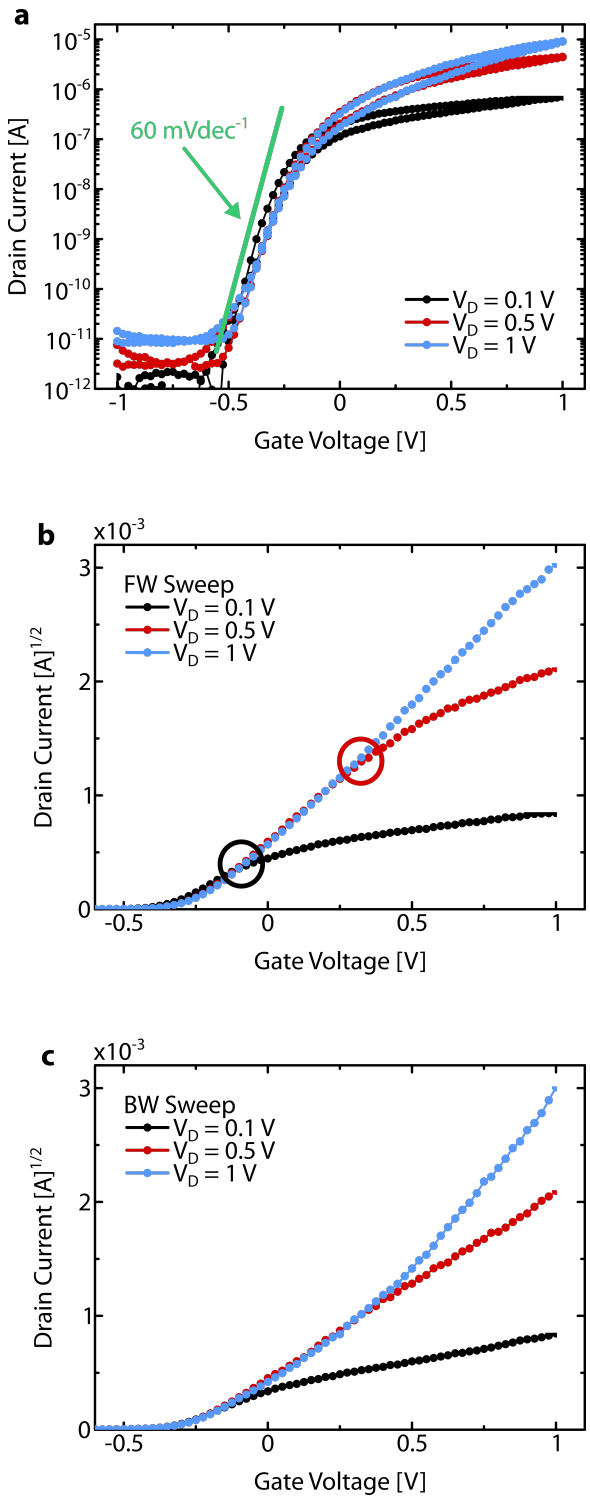

Figure 5.14: Low-voltage transistor characteristics of MoS_2 nanosheets on plasma-enhanced gate stack. **a** Transfer curves of the MoS_2 TFTs on a semi-logarithmic scale. The green solid line indicates the thermionic limit of subthreshold slope as 60 $mVdec^{-1}$. **b** Saturation current characteristics of the MoS_2 TFT for FW sweep direction. The black and red circles indicate the saturation-to-linear transition points for V_D = 0.1 V and 0.5 V, respectively. **c** Saturation current characteristics of the MoS_2 TFT for BW sweep direction.

leakage current; thus, we achieved on/off ratios of around 10^6. The transistor exhibited negligible hysteresis regardless of the drain bias. The decrease in the applied gate biases also enabled the lowering of the required drain biases to fulfill the saturation conditions.

Next, we investigated the saturation current characteristics. Figure 5.14b-c represent the transfer curve on the square-root scale for FW and BW sweeps. The transistor regions were well-established in the FW sweep (Figure 5.14b). For example, from V_D = 0.1 V to 0.5 V, the shift in the saturation-to-linear transition point was precisely 0.4 V. Moreover, for V_D = 1 V, the saturation current exhibited a constant slope over the gate voltage range, suggesting a well-established saturation region. We estimated the threshold voltage accordingly as -0.23 V. In contrast, the BW sweep (Figure 5.14c) exhibited an inverse hump at around V_G = 0.45 V for V_D = 1 V.

To investigate the inverse hump, we performed separate linear fittings for the saturation current in FW and BW sweeps (Figure 5.15b). The saturation current in the FW sweep agreed well with the linear fit (the red solid line). In contrast, we observed two distinct saturation current slopes in BW sweeps, causing the inverse hump. We estimated the threshold voltages as -0.24 V and 0.06 V below and above the inverse hump. Since the high oxide capacitance enabled lower gate and drain biases, the inverse hump occurred at lower gate voltages than the inverse hump of the transistor on passivated 100 nm-thick oxide.

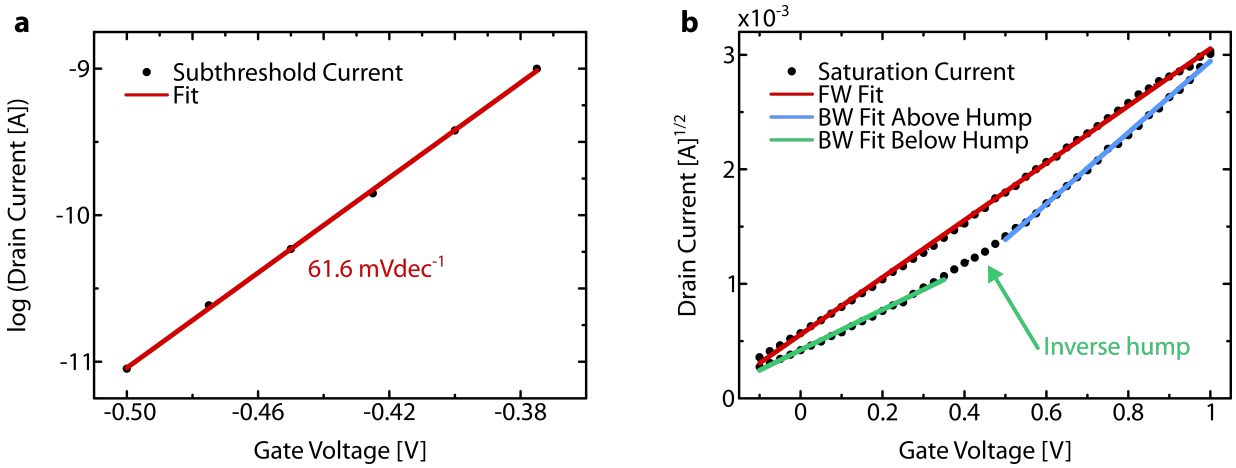

Figure 5.15: Linear fittings for subthreshold slope and saturation currents. **a** Subthreshold slope fit over two decades of current for 0.1 V drain bias. The corresponding subthreshold slope is 61.6 $mVdec^{-1}$. The corresponding R^2 value of the linear fit is 0.9996. **b** Saturation current fit for FW (the red solid line) and BW (the blue and green solid lines) sweep directions. Due to the presence of the inverse hump, the saturation current exhibits<s two distinct slope. The corresponding R^2 values of the linear fits are 0.9993, 0.9980, and 0.9955 for FW, BW above hump, and BW below hump, respectively.

We investigated the mobility characteristics in FW, and BW sweeps for a comprehensive analysis. Assuming an oxide thickness of 8 nm, we estimated a gate capacitance of 527 $nFcm^{-2}$. Figure 5.16a-b represent the mobility as a parameter of drain bias for FW and BW sweep directions, respectively. At first glance, the mobility for $V_D = 0.1$ V decreased slightly over the gate voltage and exhibited a mobility plateau of around 2 $cm^2V^{-1}s^{-1}$. At $V_D = 0.5$ V, we found mobility complementary between saturation and linear mobilities; since the applied drain bias was moderate relative to the gate voltage range, we calculated both linear and saturation mobilities for $V_D = 0.5$ V. We observed that the saturation mobility exhibited a plateau at approximately 4 $cm^2V^{-1}s^{-1}$ up to $V_G = 0.2$ V and then decreased after the transition point. At the same time, linear mobility began to exhibit a mobility plateau at 4 $cm^2V^{-1}s^{-1}$ after $V_G = 0.2$ V, as evidence of an established linear region. The complementary mobility between saturation and linear mobilities indicated almost ideal conditions for the transistor in the FW sweep. Furthermore, the mobility plateau value was around 5 $cm^2V^{-1}s^{-1}$ for $V_D = 1$ V.

The inverse hump modified the mobility characteristics in the BW sweep. At low drain bias, we observed similar mobility behavior to the FW sweep direction. At $V_D = 0.5$ V, the saturation mobility did not exhibit any decrease over the gate voltage, instead, it exhibited a plateau at 2 $cm^2V^{-1}s^{-1}$. Additionally, the linear mobility increased with the gate bias. The most significant change was observed at $V_D = 1$ V, where mobility rapidly increased due to the inverse hump. However, we could still achieve a mobility plateau for at least 11 data points at the high gate bias limit, at around 7 $cm^2V^{-1}s^{-1}$.

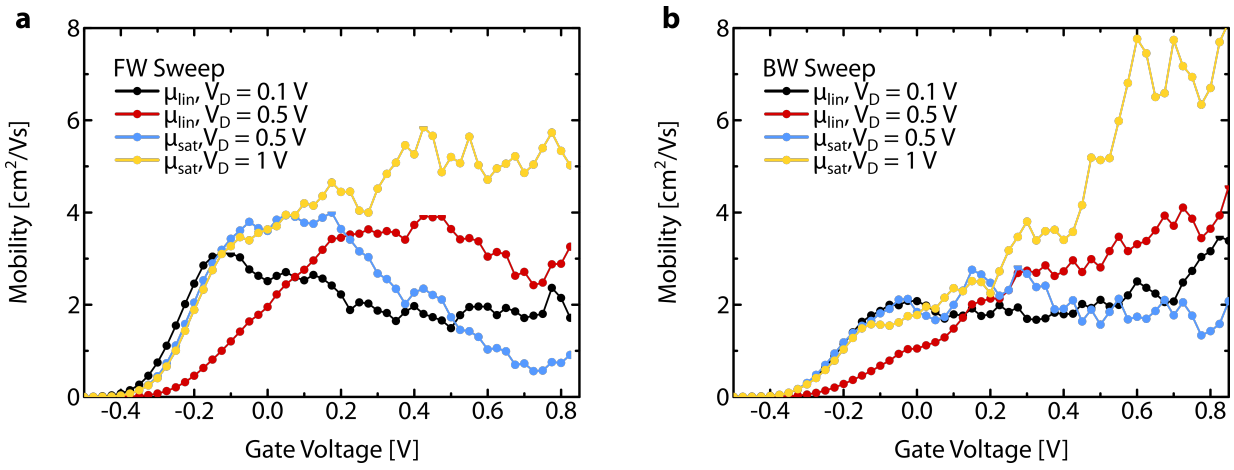

Figure 5.16: Mobility characteristics of low voltage MoS_2 TFTs on plasma-enhanced gate stack for various drain biases.

As a final remark, the increase in the oxide capacitance and the SAM passivation enabled textbook transistor characteristics for MoS_2 nanosheet transistors. We pushed the boundaries of MoS_2 nanosheets at a single transistor limit, which serves as a solid base for building van der Waals ambipolar transistors. The novel electronic properties of the stacked transistors can now be revealed due to the complete suppression of the interface states. Since the plasma-enhanced gate architecture is scalable, lithography compatible, and suitable for MoS_2 nanosheet transistor fabrication, the approach is extended from organic nanosheet electronics to inorganic nanosheet electronics. Fundamentally, the mystery of crystal mobility remains; if the Anderson transition exists, the mobilities are still underestimated. If the Anderson transition does not exist, we at least prove that fabricating transistors with high oxide capacitances brings a better base for mobility calculation, as the mobility values are still reasonable compared to transistors on 100 nm-thick passivated oxide due to establishing saturation conditions at much lower drain biases.

6

Summary and Outlook

"God made the bulk; surfaces were invented by the devil."

— Wolfgang Pauli

We have investigated the charge transport in transferable van der Waals nanosheets, either as individual nanosheets or as heterojunctions. First, we established a method to make the transfer of organic nanosheets possible. Showing that the nanosheets preserved their crystallinity after the transfer, we compared the as-evaporated and transferred nanosheet transistors in the bottom-contact configuration. We demonstrated that resolving crystallization problems in as-evaporated films by transfer improved the transistor performance by 15-fold. Then, we stacked the transferable organic nanosheets with inorganic nanosheets to build van der Waals heterojunctions. We observed the ambipolar behavior where both charge carriers were accumulated in the transistor simultaneously. Nonetheless, the dangling bond-induced surface states of the oxide caused excessive onset and threshold voltage shifts and a pronounced subthreshold region. While the thermionic limit is only 60 $mVdec^{-1}$ for the subthreshold slope, the ambipolar and unipolar MoS_2 transistors exhibited subthreshold slopes of more than 1,500 $mVdec^{-1}$. We introduced COC to passivate the interface states and investigated its compatibility with lithography chemicals. In the case of unipolar MoS_2 transistors, the subthreshold slope became 480 $mVdec^{-1}$ after passivation and even steeper (189 $mVdec^{-1}$) after increasing the passivated oxide capacitance. The steep subthreshold slopes enabled the lowering of the operation voltages of the transistors to ±5 V, however, the non-ideal saturation conditions compelled the lowering of the subthreshold slope to the thermionic limit and

hence lower the operation voltages further. To increase the oxide capacitance, we introduced an ultrathin high-k aluminum oxide, which was produced by plasma-enhanced oxidation of aluminum. The transistors on plasma-enhanced oxide exhibited subthreshold slopes as steep as 61.6 $mVdec^{-1}$, forming a solid base for future unipolar and ambipolar electronics in terms of scalability, low voltage, and high performance. This last chapter will review the significant results of the dissertation with final remarks to pave the path for future experiments.

Transferable organic nanosheets could become a standard as atomically thin semiconductors. Although their limited mobility compared to their inorganic counterpart, organic nanosheets offer adequate performance, especially where the crystallization of small molecules cannot be controlled. Many well-known small molecules, such as pentacene, DNTT, C_{60}, and rubrene, are now transferable. In addition, Moritz Waibel showed in his bachelor's thesis that the molecular derivatives of DNTT and BTBT are also transferable. Here, DPh-DNTT is promising since it exhibits the highest mobility among small molecules. Utilizing DPh-DNTT nanosheets may lower the contact resistances in organic transistors -especially when the lithography is involved in fabrication- to stretch the limits toward gigahertz organic transistors. Furthermore, the bilayer nanosheets, for instance, pentacene and C_{60}, can enable the fabrication of transferable p-n heterojunctions (Figure B.1). Substituting a non-hazardous chemical with water can also expand the range of applications, especially where a glove box is necessary.

We still need to address some questions to reveal the potential of transferable organic nanosheets, for example, why their mobility values are lower than those of benchmark transistors. In order to approach this question thoroughly, we also examined the crystallinity of the nanosheets during this dissertation. For instance, we optimized the transfer process using the stress-induced polymorphism in pentacene nanosheets. By evaluating the thin-film-to-bulk phase ratio as a stress indicator, Veronika Reisner demonstrated in her master's thesis that utilizing thinner nanosheets increased the ratio, indicating that the stress was managed mechanically [91]. In addition, she also demonstrated that the hydrophobicity of the target substrate significantly affected the crystallinity. The total XRD intensity decreased in the case of a hydrophobic target substrate, which is inevitable to suppress the interface states. Furthermore, having larger grains can also be a limitation. In a previous XRD study, Nickel et al. investigated how surface conditions affected the crystallinity of pentacene thin films. The authors found that, contrary to expectations, the dislocation density increased with grain size, lead-

ing to a more rapid decrease in XRD intensity along the Bragg peaks [92]. When we compared the XRD of as-evaporated DNTT on PAA and SAM, we made the preliminary observation that the decrease over the first five peaks was more rapid for a 50 nm-thick DNTT film on PAA than on SAM (Figure B.12). Therefore, the intrinsic mobility of the transferable organic nanosheets can be enhanced with an in-depth study of the impact of different water-soluble films on the crystallinity of the nanosheets.

During the dissertation, we studied the exciton dynamics in MoS_2/pentacene, WS_2/pentacene [93], and MoS_2/DNTT (in preparation) van der Waals heterojunctions in collaboration with the group of Prof. de Jong (Uni. Twente) and the groups of Prof. Turchanin and Prof. Dietzek (Uni. Jena). Since both nanosheets have relatively high exciton binding energies [94], the vdW heterojunction is expected to facilitate exciton dissociation at the interface. We indeed observed ultrafast exciton dissociation by the vdW interface, furthermore, a coupling between the organic and inorganic nanosheets. However, the experiments were conducted on heterojunctions transferred on gold/aluminum coated substrates (for reflection geometry) or glass (for transmission geometry), where we know now that dangling bonds play a crucial role. Therefore, similar experiments on passivated substrates can reveal novel exciton dynamics in the heterojunctions, guiding future ambipolar transistors.

Ambient conditions strongly influenced the transistor characteristics of organic and inorganic nanosheets in different ways. On the one hand, the performance of transferred DNTT transistors improved after being exposed to ambient conditions (Figure B.4). After two days in ambient, not only did the drain current improve dramatically (from 23 nA to 500 nA), but so did the subthreshold slope (from 373 $mVdec^{-1}$ to 280 $mVdec^{-1}$). The doping of the organic thin films under ambient conditions was also observed by Horowitz [54] and Ante [95]. On the other hand, the performance of the MoS_2 transistors decreased despite being stored in a desiccator. We observed a two-fold lower mobility and an onset voltage shift from -3.4 V to -2 V after four days (Figure B.5). While the van der Waals heterojunction transistors can be left exposed to ambient conditions for an extended period to balance the mobility mismatch between nanosheets, the stability of unipolar TMD transistors can be enhanced by incorporating a second COC layer for encapsulation. By using MIBK instead of anisole to prepare the PMMA solution, any potential damage to the bottom COC layer can be prevented, ensuring complete

encapsulation. It would therefore be beneficial to investigate the wetting properties of MIBK on TMD surfaces and determine the optimum COC thickness.

The connection between the dangling bond-induced interface states and oxide capacitance confirmed several crucial facts. Firstly, it is clarified that the interface states would dominate the charge transport by compelling deep-state hopping in the transistors on untreated oxides. This results in a pronounced subthreshold region, masking the intrinsic trap states of the material. Therefore, the dangling bond passivation is essential to study the intrinsic characteristics of the materials. Quantifying the passivated surface state density in a MOS diode could provide valuable information to compare different passivation methods. Secondly, we proved that the transistor operation regions only be comprised if the Fermi level is shifted into the shallow trap (tail) states. To fulfill this condition in the CVD-grown MoS_2 transistor within a ±5 V gate voltage range, we need a minimum oxide capacitance of around 30 $nFcm^{-2}$ after passivation. Furthermore, the capability to shift the Fermi level into the tail states enhanced the sensitivity of the transistors to both the density and distribution of the tail states. We could now quantify the quality of MoS_2 crystals by using the transistor parameters. For instance, the photoluminescence (PL) spectrum of different MoS_2 crystals on the same substrate revealed that the PL signals were red- or blue-shifted, indicating that the tail DOS distribution varied (Figure B.13, in collaboration with the group of Prof. Urban, Uni. Munich). A possible correlation between the PL and the transistor characteristics could provide crucial information on the tail state distribution to optimize the inorganic nanosheet growth and transfer. Thirdly, the interface passivation also revealed the intrinsic optoelectronic characteristics of the MoS_2 transistors. Najafidehaghani et al. observed that the MoS_2 transistors on untreated oxide exhibited positive photoconductivity. In contrast, by passivation, our MoS_2 transistors exhibited negative photoconductivity due to well-balanced trap states [96], which boosted their photoresponsivity to world-high.

One of the unusual features of MoS_2 transistors on passivated oxides was the observation of the inverse hump (or maybe an Anderson transition compared to Figure 2.14) at the high drain bias limit. Since the Anderson transition was first observed in a single-crystal Si MOSFET [85], the Anderson transition in single-crystal MoS_2 can also be expected. However, reviewing a few parameters for exploring the Anderson transition in MoS_2 transistors is crucial. First, we know the effect of ambient conditions on the transistor characteristics of MoS_2 nanosheet TFTs. Therefore, the encapsulation of MoS_2 crystals by h-BN nanosheets is necessary. In addi-

tion, the contact problems must either be improved or eliminated; graphene contacts for the former or the van der Pauw design (four-probe measurements) can be utilized for the latter. Furthermore, the Anderson transition is not only field-effect carrier density-dependent but also temperature-dependent, therefore, the transition must be proved at cryogenic temperatures as well. Demonstrating a room-temperature Anderson transition would be a significant achievement since its existence could improve the performance of any electronic circuit based on the MoS_2 transistors with higher mobilities after optimizing the circuit according to the Anderson transition conditions.

The textbook-like characteristics of MoS_2 nanosheet transistors on the plasma-enhanced gate stack could inspire further studies. Firstly, this new architecture can be utilized in other inorganic nanosheets to investigate novel charge transport properties. At this point, tungsten disulfide (WS_2) and molybdenum ditelluride ($MoTe_2$) are conspicuous. It has been shown that these inorganic nanosheets are ambipolar materials, furthermore, electroluminescent [97, 98]. Therefore, fabricating WS_2 or $MoTe_2$ ambipolar transistors on plasma-enhanced gate stack can lead to low-voltage light-emitting transistors with high luminescence yields due to the high field-effect charge density by the high oxide capacitance. Secondly, a unique layout of the ambipolar transistor, known as split-gate architecture, can be fabricated. Instead of a single gate that accumulates both charge carriers, this architecture consists of two gates separated by a narrow gap—typically around 1 μm or less. While one of the gates accumulates one charge type, the other gate accumulates the counter charge, like a field-effect doped p-n junction. This promotes the recombination between the gates like forward biased p-n diode. Lastly, aggressively scaled organic nanosheet transistors can also be fabricated. A transistor channel width and length of less than 750 nm allows for the realization of single-grain transistors, which may improve charge transport by eliminating the grain boundaries.

Our detailed investigation of the MoS_2 nanosheet transistors proved that contact quality limits the ultimate performance, even though some transistors exhibited textbook-like features. We surprisingly observed that the transistors on the same substrate with the same contact material exhibited disparate mobility characteristics; on the one hand, the transistor that exhibited low mobility plateau values (2 $cm^2V^{-1}s^{-1}$) also exhibited a mobility peak. On the other hand, mobility plateau values were around 17 $cm^2V^{-1}s^{-1}$ for the transistors that exhibited no mobility peak. It was claimed in the literature that the mobility peak indicates a possible Schottky barrier, however, the contrast of the mobility characteristics between the

transistors having the same contact material pointed out that a Schottky barrier does not directly limit the mobility. At this point, diffraction-limited scanning photocurrent microscopy was the best method for revealing contact homogeneities. To that extent, we comprehended from the photocurrent maps that contacts were not necessarily poor as both but rather were uneven, which caused a non-balanced charge injection. This result does not mean that there is no Schottky barrier since the same photocurrent maps exhibited a finite and uniform photocurrent on the good injection contact, which indicates a non-negligible Schottky barrier exists between Ti and MoS_2. Therefore, to achieve the true potential of the MoS_2 crystals, the contact non-idealities should be improved by additional steps like annealing the MoS_2 crystals [44] or cleaning residues with contact mode AFM [99], and the Schottky barrier should be lowered by utilizing other contact materials like bismuth [100].

A

List of Publications and Patents

List of Publications

1. "Wafer Scale Synthesis of Organic Semiconductor Nanosheets for van der Waals Heterojunction Devices"

   Sirri Batuhan Kalkan, Emad Najafidehaghani, Ziyang Gan, Fabian Alexander Christian Apfelbeck, Uwe Hübner, Antony George, Andrey Turchanin, Bert Nickel, npj 2D Materials and Applications 5, 92 (2021).

   My Contribution: Pursuing the growth and transfer of organic nanosheets including their characterization, fabrication of unipolar organic transistors and organic/inorganic ambipolar transistors including their characterization, analyzing the transistor characteristics and writing the manuscript including the preparation of all figures.

2. "High-Performance Monolayer MoS_2 Field-Effect Transistors on Cyclic Olefin Copolymer Passivated SiO_2 Gate Dielectric"

   Sirri Batuhan Kalkan, Emad Najafidehaghani, Ziyang Gan, Jan Drewniok, Michael F. Lichtenegger, Uwe Hübner, Alexander S. Urban, Antony George, Andrey Turchanin, Bert Nickel, Advanced Optical Materials 11, 2201653 (2023).

   My Contribution: Utilizing the interface passivation, fabrication of all untreated and passivated TFTs including their electrical characterization, analyzing the transistor characteristics, fabrication of passivated TFT for optoelectronic measurements, writing the manuscript including the preparation of all figures.

3. "Exciton Dynamics in MoS_2-Pentacene and WSe_2-Pentacene Heterojunctions"

   Pavel A. Markeev, Emad Najafidehaghani, Gergely F. Samu, Krisztina Sarosi, Sirri Batuhan Kalkan, Ziyang Gan, Antony George, Veronika Reisner, Karoly Mogyorosi, Viktor Chikan, Bert Nickel, Andrey Turchanin, Michel P. de Jong, ACS Nano 16(10), 16668-16676 (2022).

   My Contribution: Fabrication of the MoS_2-Pentacene and WSe_2-Pentacene Heterojunctions.

List of Patents

1. Method of Transfer of Organic Semiconductor Films to a Substrate and Electronic Devices Made therefrom, WO2022EP57304.

   Antony George, Sirri Batuhan Kalkan, Bert Nickel, Andrey Turchanin

2. Electronic and Optoelectronic Devices with Interface Passivation, recently filed.

   Antony George, Sirri Batuhan Kalkan, Emad Najafidehaghani, Bert Nickel, Andrey Turchanin

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ARTICLE OPEN

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Wafer scale synthesis of organic semiconductor nanosheets for van der Waals heterojunction devices

Sirri Batuhan Kalkan[1,4], Emad Najafidehaghani[2,4], Ziyang Gan[2], Fabian Alexander Christian Apfelbeck[1], Uwe Hübner[3], Antony George[2], Andrey Turchanin[2]✉ and Bert Nickel[1]✉

Organic semiconductors (OSC) are widely used for consumer electronic products owing to their attractive properties such as flexibility and low production cost. Atomically thin transition metal dichalcogenides (TMDs) are another class of emerging materials with superior electronic and optical properties. Integrating them into van der Waals (vdW) heterostructures provides an opportunity to harness the advantages of both material systems. However, building such heterojunctions by conventional physical vapor deposition (PVD) of OSCs is challenging, since the growth is disrupted due to limited diffusion of the molecules on the TMD surface. Here we report wafer-scale (3-inch) fabrication of transferable OSC nanosheets with thickness down to 15 nm, which enable the realization of heterojunction devices. By controlled dissolution of a poly(acrylic acid) film, on which the OSC films were grown by PVD, they can be released and transferred onto arbitrary substrates. OSC crystal quality and optical anisotropy are preserved during the transfer process. By transferring OSC nanosheets (p-type) onto prefabricated electrodes and TMD monolayers (n-type), we fabricate and characterize various electronic devices including unipolar, ambipolar and antiambipolar field-effect transistors. Such vdW p-n heterojunction devices open up a wide range of possible applications ranging from ultrafast photodetectors to conformal electronics.

npj 2D Materials and Applications (2021)5:92 ; https://doi.org/10.1038/s41699-021-00270-9

INTRODUCTION

Heterojunctions based on organic semiconductors (OSCs) and monolayer transition metal dichalcogenides (ML TMDs), exploiting the advantages of both material systems, attract interest in the engineering of electronic, photonic and optoelectronic devices[1–3]. OSC exhibit excellent electronic properties which can outperform or act complementary to inorganic semiconductors[4–6]. OSC based electronic and optoelectronic devices such as organic light-emitting diodes (OLED)[7] are already used as constituents of several consumer products widely, especially in displays of television sets and mobile phones. ML TMDs are known for their superior electronic transport properties and have been identified as promising candidates for ultrathin device technologies[8,9]. The combination of OSCs and high-performance ML TMDs provides novel opportunities for complementary metal–oxide–semiconductor (CMOS) technology[10,11]. However, integration of OSCs and TMDs into the heterojunction devices via physical vapor deposition (PVD) of OSCs onto the TMD surfaces is challenging, since the low diffusion and ordering of the organic molecules limits functional properties of the formed OSC films[12,13]. Here we report a methodology for fabrication of highly crystalline ultrathin (down to 15 nm) OSC nanosheets with lateral dimensions up to 3-inch and their transfer onto arbitrary substrates. We employ this methodology for the assembly of van der Waals (vdW) heterostructures with two-dimensional (2D) materials. As an example for 2D materials, we chose ML TMDs. In brief, water-soluble polyacrylic acid (PAA) thin films on silicon wafers were used as growth substrates to form highly crystalline OSC films of pentacene or dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) via PVD. We show that these films can be controllably released as mechanically stable nanosheets from the growth substrate by the dissolution of the water-soluble PAA substrate and transferred onto arbitrary substrates. We apply various characterization techniques such as atomic force microscopy (AFM), X-ray diffraction and confocal microscopy to demonstrate the high crystallinity and therewith optical anisotropy of the OSC nanosheets before and after transfer. We use the OSC nanosheets to fabricate field-effect transistors (FETs) and to study their performance. To this end, the nanosheets were transferred onto prefabricated electrodes to realize wafer-scale bottom-contact FET arrays and their properties were compared with OSC films directly grown on the wafer by PVD. Besides that, the p-type OSC nanosheets were transferred onto prefabricated n-type MoS_2 device structures to realize high-performance ambipolar and antiambipolar FETs.

RESULTS AND DISCUSSION

Release and transfer of organic nanosheets

First, we describe the transfer method. We spin coat a water-soluble PAA thin film on an oxygen plasma-treated 3-inch Si wafer. The PAA layer acts as the growth substrate for PVD of highly ordered pentacene or DNTT films with thicknesses ranging from 15 to 50 nm. We found out that a controlled release of the OSC films is possible by a water-assisted transfer technique, see Fig. 1. We place a Si wafer with the OSC film next to the water droplet, see Fig. 1a and Supplementary Fig. 1, and establish a contact between the wafer and the droplet, see Fig. 1b. The surface tension difference between the untreated glass plate and the plasma-treated Si wafer drives the water towards the Si[14]; the water intrudes between the substrate and the OSC film, which results in its release from the substrate and formation of a free-standing OSC nanosheet. Due to the hydrophobic nature of the OSC[15], the released nanosheet floats on the water meniscus.

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RESEARCH ARTICLE

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High-Performance Monolayer MoS_2 Field-Effect Transistors on Cyclic Olefin Copolymer-Passivated SiO_2 Gate Dielectric

Sirri Batuhan Kalkan, Emad Najafidehaghani, Ziyang Gan, Jan Drewniok, Michael F. Lichtenegger, Uwe Hübner, Alexander S. Urban, Antony George, Andrey Turchanin, and Bert Nickel**

Trap states of the semiconductor/gate dielectric interface give rise to a pronounced subthreshold behavior in field-effect transistors (FETs) diminishing and masking intrinsic properties of 2D materials. To reduce the well-known detrimental effect of SiO_2 surface traps, this work spin-coated an ultrathin (≈5 nm) cyclic olefin copolymer (COC) layer onto the oxide and this hydrophobic layer acts as a surface passivator. The chemical resistance of COC allows to fabricate monolayer MoS_2 FETs on SiO_2 by standard cleanroom processes. This way, the interface trap density is lowered and stabilized almost fivefold, to around 5×10^{11} cm^{-2} eV^{-1}, which enables low-voltage FETs even on 300 nm thick SiO_2. In addition to this superior electrical performance, the photoresponsivity of the MoS_2 devices on passivated oxide is also enhanced by four orders of magnitude compared to nonpassivated MoS_2 FETs. Under these conditions, negative photoconductivity and a photoresponsivity of 3×10^7 A W^{-1} is observed which is a new highest value for MoS_2. These findings indicate that the ultrathin COC passivation of the gate dielectric enables to probe exciting properties of the atomically thin 2D semiconductor, rather than interface trap dominated effects.

1. Introduction

Owing to their atomic scale thickness, 2D materials are promising candidates for next generation beyond Moore nanoelectronics.[1,2] However, in contrast to conventional metal oxide semiconductor (MOS) fabrication steps where buried oxide interfaces are employed, here the SiO_2 surface is exposed to ambient conditions and organic solvent during the transfer steps of the 2D materials via the poly(methyl methacrylate) (PMMA) assisted transfer method.[3,4] As a result, the oxide surface is a source of trap states, giving rise to dominant nonidealities in output and transfer characteristics.[5–9] This obstructs the fundamental investigations of 2D materials on SiO_2/Si wafers[10,11] tremendously; and their integration in complementary metal oxide semiconductor (CMOS) technologies[12] is an ongoing challenge.

The amount of these trap states can be quantified by extending Shockley's equations for ideal linear and saturation field effect transistor (FET) regimes by a pronounced subthreshold regime.[13] Here, the subthreshold swing, S, is the gate voltage difference that is required to increase the FET drain current by one decade. An ideal device at room temperature shows a subthreshold swing of around 60 mV $decade^{-1}$ known as the thermionic limit.[14] In presence of traps and depletion effects, the subthreshold swing increases according to,[14]

$$S = \left(60 \text{ mV decade}^{-1}\right) \times [1+\alpha] \quad (1)$$

Here, α is a correction to account for depletion of the semiconductor and for interface traps at the semiconductor/gate dielectric interface. For ultrathin FETs, usually interface traps dominate the correction.[15] Then the equation for S reads,[16]

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ARTICLE

Exciton Dynamics in MoS_2-Pentacene and WSe_2-Pentacene Heterojunctions

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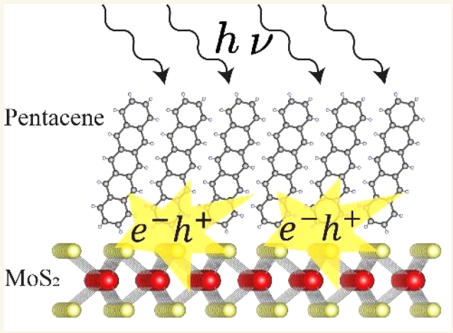
ABSTRACT: We measured the exciton dynamics in van der Waals heterojunctions of transition metal dichalcogenides (TMDCs) and organic semiconductors (OSs). TMDCs and OSs are semiconducting materials with rich and highly diverse optical and electronic properties. Their heterostructures, exhibiting van der Waals bonding at their interfaces, can be utilized in the field of optoelectronics and photovoltaics. Two types of heterojunctions, MoS_2-pentacene and WSe_2-pentacene, were prepared by layer transfer of 20 nm pentacene thin films as well as MoS_2 and WSe_2 monolayer crystals onto Au surfaces. The samples were studied by means of transient absorption spectroscopy in the reflectance mode. We found that A-exciton decay by hole transfer from MoS_2 to pentacene occurs with a characteristic time of 21 ± 3 ps. This is slow compared to previously reported hole transfer times of 6.7 ps in MoS_2-pentacene junctions formed by vapor deposition of pentacene molecules onto MoS_2 on SiO_2. The B-exciton decay in WSe_2 shows faster hole transfer rates for WSe_2-pentacene heterojunctions, with a characteristic time of 7 ± 1 ps. The A-exciton in WSe_2 also decays faster due to the presence of a pentacene overlayer; however, fitting the decay traces did not allow for the unambiguous assignment of the associated decay time. Our work provides important insights into excitonic dynamics in the growing field of TMDC-OS heterojunctions.



KEYWORDS: *transition metal dichalcogenides, organic semiconductors, pentacene, exciton dynamics, transient reflection spectroscopy, MoS_2, WSe_2*

1. INTRODUCTION

The study of van der Waals heterojunctions based on transition metal dichalcogenides (TMDCs) and organic semiconductor (OS) thin films has been ongoing for several years; however, there are still many fascinating avenues for researchers to explore.[1] The TMDCs themselves exhibit fascinating physical phenomena such as exceptionally large exciton binding energies,[2,3] spin-valley locking,[4] and the exciton Hall effect.[5] TMDCs and organic semiconductors are highly dissimilar nonconventional semiconductors that share the characteristic of interlayer bonding via van der Waals interactions. Forming heterojunctions of these materials offers interesting opportunities for combining diverse (opto-)electronic properties. An important step for the technological development of such structures has been taken recently, in the demonstration by some of us of devices fabricated by layer transfer of TMCDs as well as organic semiconductor thin films.[6] A strong advantage of this approach is that the organic semiconductors can be grown on a suitable substrate for obtaining high quality crystalline layers, avoiding molecular disorder that occurs upon direct deposition on TMCD substrates.

The wide variety of devices that have been constructed in the field so far include light emitting diodes,[7] tunneling transistors,[8] and photovoltaic cells.[9,10] Arguably, one of the most promising applications out of these possibilities is photovoltaics, and the present work is carried out in its context, focusing on exciton dynamics at TMDC/OS interfaces. Some of the aforementioned heterojunctions have been studied previously in various combinations and conditions by similar ultrafast pump probe spectroscopic techniques.[10−16] Most of these previous studies focused on 2D TMDCs grown on quartz and SiO_2/Si wafers, which were then

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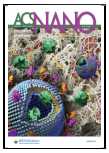

https://doi.org/10.1021/acsnano.2c06144
ACS Nano 2022, 16, 16668–16676

B

Supporting Graphs

Transferable p-n heterojunction

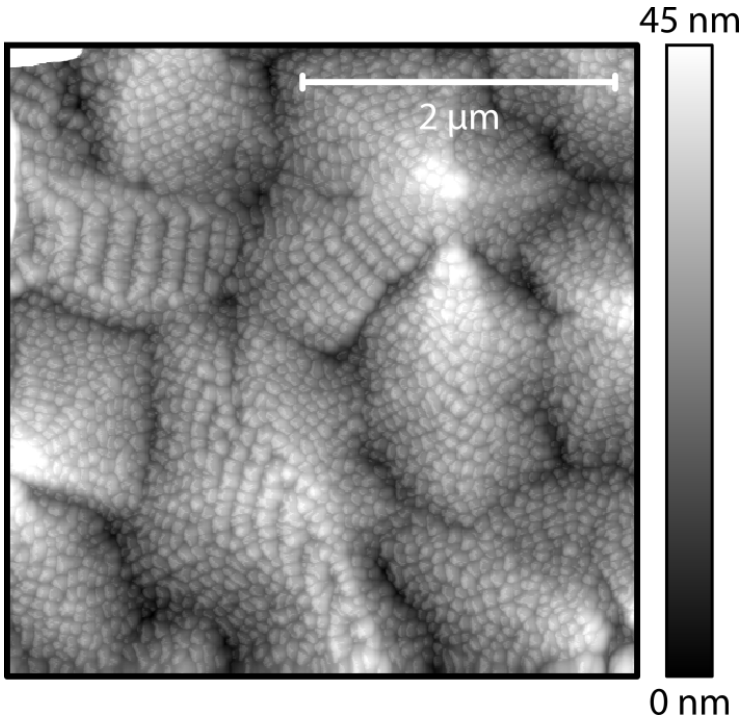

Figure B.1: Transferable pentacene/C_{60} heterojunction.

Contact angle measurements

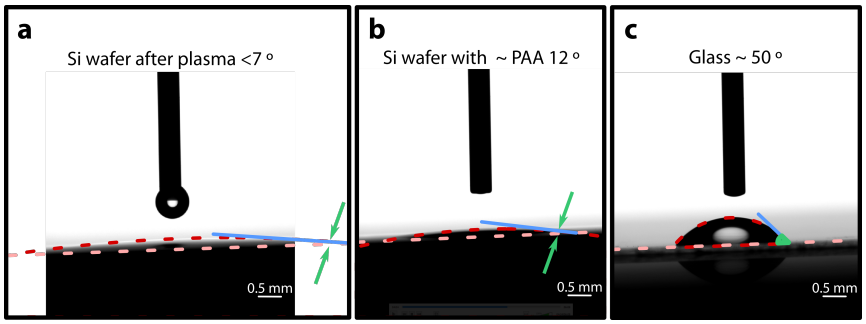

Figure B.2: Contact angle measurements of the substrate, PAA, and the glass carrier.

Device Images

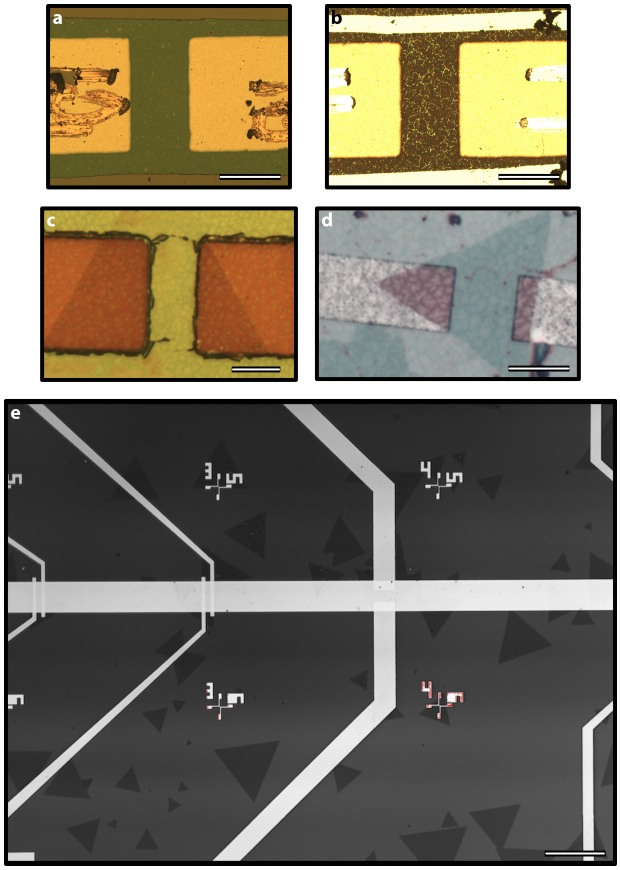

Figure B.3: Typical device images of unipolar/ambipolar nanosheet TFTs. **a** Unipolar DNTT (scalebar is 100 µm), **b** unipolar pentacene (scalebar is 100 µm), **c** ambipolar MoS_2/DNTT photolithograpily patterned, **d** ambipolar MoS_2/DNTT electron beam lithographically patterned, and **e** unipolar MoS_2 on plasma-enhanced oxide. Scale bars are 100 µm for **a** and **b**, 10 µm for the others.

Stability of Transferred DNTT TFTs under ambient conditions

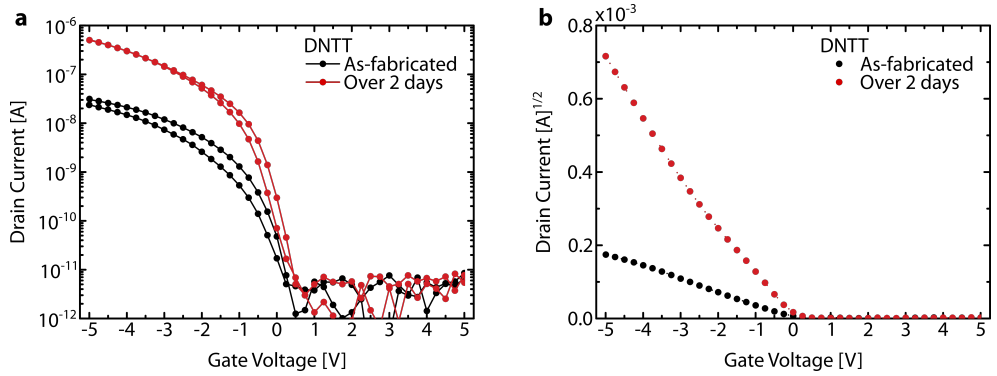

Figure B.4: The comparison of transistor characteristics of BC transferred DNTT TFTs as-fabricated and over days. **a** Semi-logarithmic and **b** square-root plots of transfer curves of transferred DNTT TFTs measured as-fabricated (black dotted line) and over the weekend (red dotted line).

Stability of MoS_2 TFTs under ambient conditions

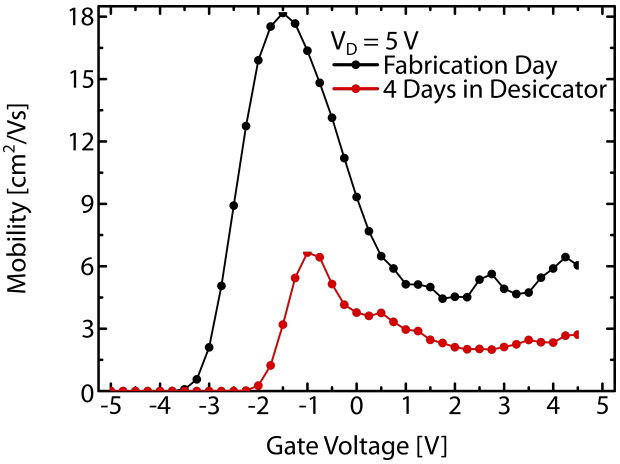

Figure B.5: Effect of ambient conditions on the mobility of the TFTs over days.

Reproducibility of COC passivation on various substrates

As shown in Figure B.6, we began with the reproducibility of the COC application by fabricating two chips containing multiple transistors. 12 unipolar MoS_2 TFTs, fabricated on COC-passivated oxide are shown in Figure B.6a. First, the operation range of TFTs was as low as 3 V due to low onset voltages, which vary within a 1 V gate voltage. The on/off ratios were approximately 10^5, and the output currents were of the same magnitude. They exhibited almost no hysteresis, and their characteristics were comparable. The second chip showed similar results as well (Figure B.6b). These results demonstrated that the COC passivation was uniform and reproducible.

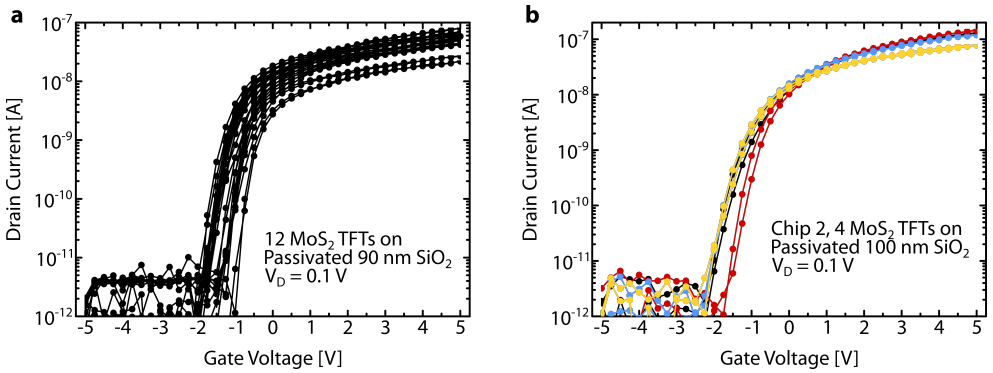

Figure B.6: Reproducibility of MoS_2 TFTs on COC-passivated oxide. Semi-logarithmic plot of the transfer curve of **a** 12 MoS_2 TFTs on passivated 90 nm oxide (Chip 1), **b** 4 MoS_2 TFTs on passivated 100 nm oxide (Chip 2).

Subthreshold slopes of MoS_2 TFTs on various substrates

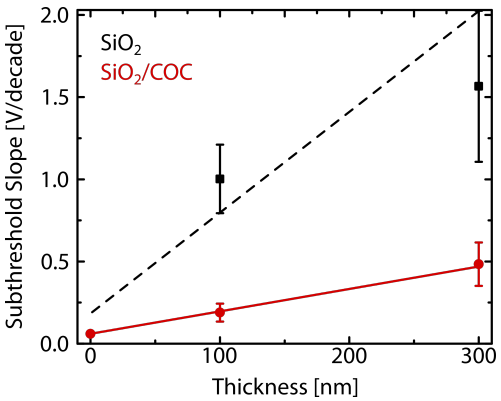

Figure B.7: Subthreshold slopes of MoS_2 TFTs on various substrates. The black dashed line indicates the best fit according to the thermionic limit for TFTs on untreated oxides. The red solid line indicates the best fit according to the thermionic limit for TFTs on passivated oxides.

Bonding of TFTs on Global Gate Oxides

Wirebonding the transistors posed a challenging issue during the photocurrent spectroscopy experiments. We started with optimizing the bonding parameters for $Si/SiO_2/Ti/Au$ capacitors, with Ti used as an adhesion layer (6 nm-thick). Before delving into the bonding results, it is crucial to discuss the bonding conditions. First, it is necessary to have a minimum thickness of 60 nanometers for the gold layer to guarantee the mechanical stiffness. Secondly, the gold pad must be free of any residue and thoroughly cleaned beneath the pad (i.e. COC must be etched). Lastly, heating the substrate proves to be beneficial, with a minimum temperature of 60 degrees yielding observable improvements in adhesion. The UniTemp WB-200 was used as the bonder for ball/wedge bonding of the sample/chip carrier. During the bonding process, we kept all other bonding parameters fixed except the power:

1. Bonding time 10 ms
2. Bonding force 0.15 N

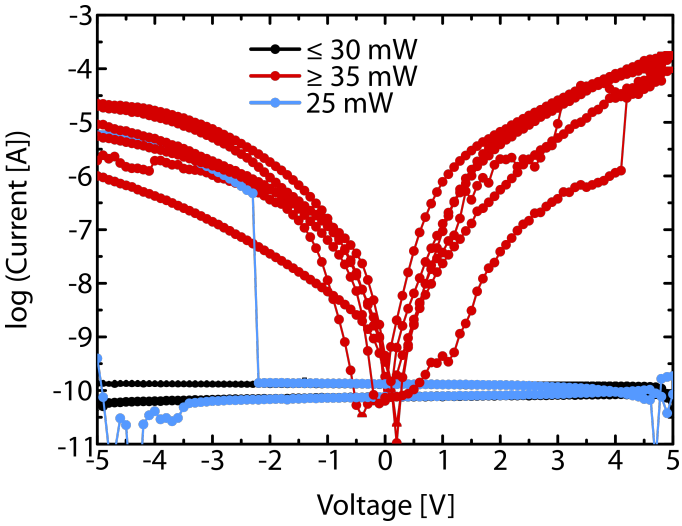

Figure B.8: Leakage current measurements of $Si/SiO_2/Ti/Au$ capacitors as a parameter of bonding power.

Based on the findings, we conclude that the gate oxide can withstand up to 30 mW (with a coincidence at 25 mW). It is worth noting that if the substrate temperature is increased, the bonding power can be further decreased.

Scanning Photocurrent Microscopy on the MoS_2 TFT

Scanning photocurrent microscopy was used to investigate the influence of contacts with a diffraction-limited laser spot. In this method, the sample is illuminated by a laser beam and the transistor is scanned by the piezo motors. The parameters of the piezo motors were 26 V and 100 Hz to achieve a step size of about 300 nm. In addition, a lock-in amplifier time constant of 20 ms, a laser frequency of 2 kHz and a power density of 0.4 μWcm^{-2} were used. More details on the confocal microscopy setup can be found in Appendix D.

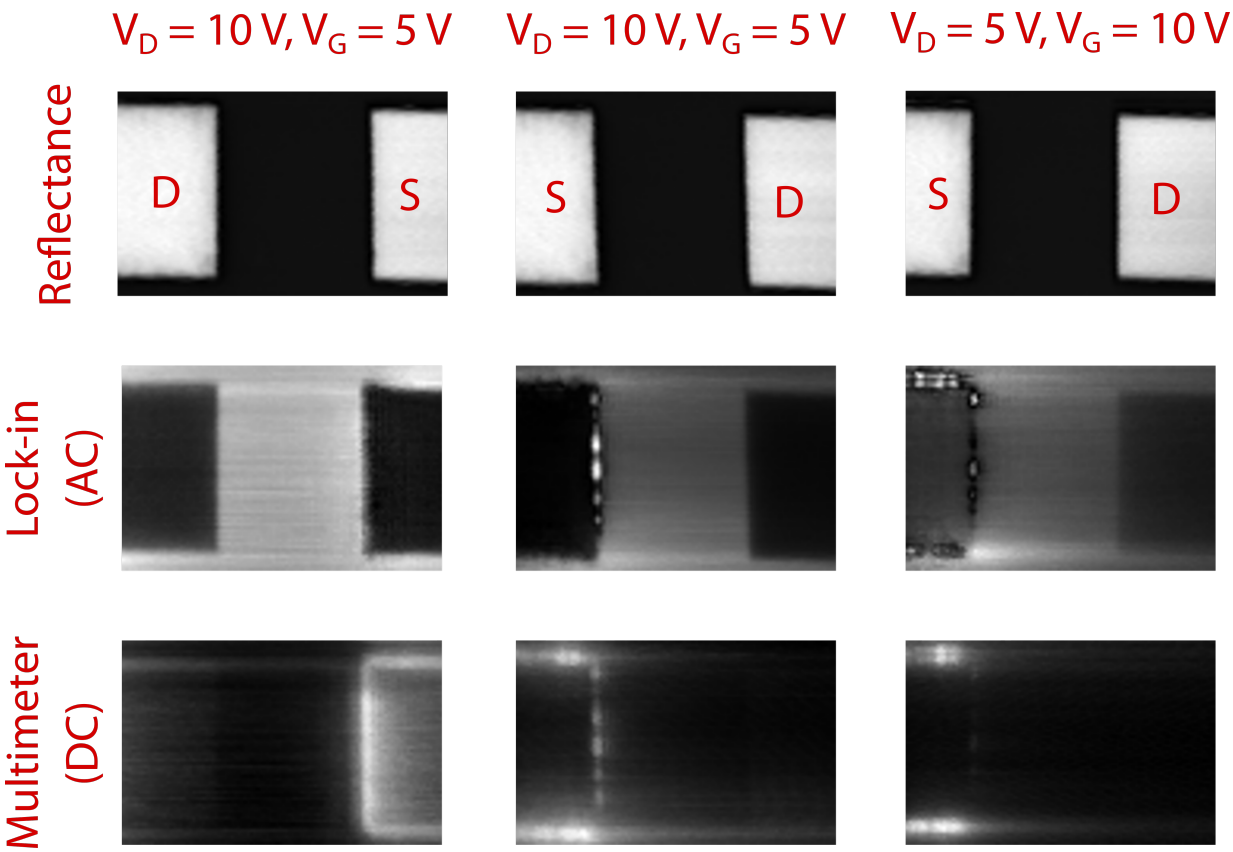

Figure B.9: Reflectance, AC (measured by lock-in amplifier) and DC (measured by digital multimeter) current photocurrent micrographs of MoS_2 TFTs with different bias and contact conditions. S and D represent source and drain, respectively. The diode laser was operated at 2 kHz with a laser power of 0.4 μWcm^{-2}.

Effects of the Gate Electrode Edges on Leakage

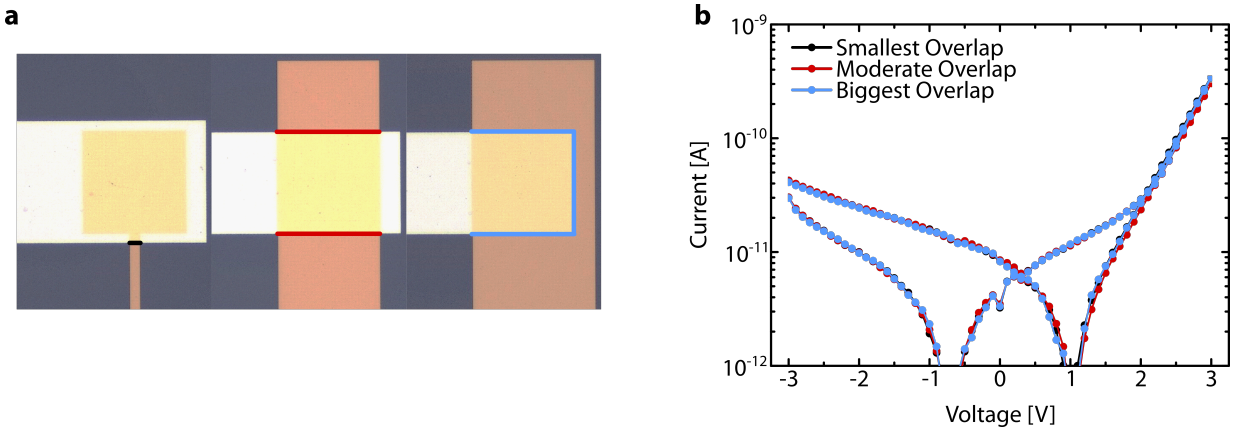

Figure B.10: Reflectance, AC (measured by lock-in amplifier) and DC (measured by digital multimeter) current photocurrent micrographs of MoS_2 TFTs with different bias and contact conditions. S and D represent source and drain, respectively. The diode laser was operated at 2 kHz with a laser power of 0.4 μWcm^{-2}.

Mobility Calculation with Savitzky-Golay Filter

During calculations of mobility, contact-related fluctuations inhibited overall behavior. To address this issue, mobilities are calculated using 2nd order Savitzky-Golay filtering. Here, smoothening is optimized over five data points to minimize fluctuations while preserving the underlying behavior. A clear comparison between the raw data and the filtered data for a single transistor is presented below.

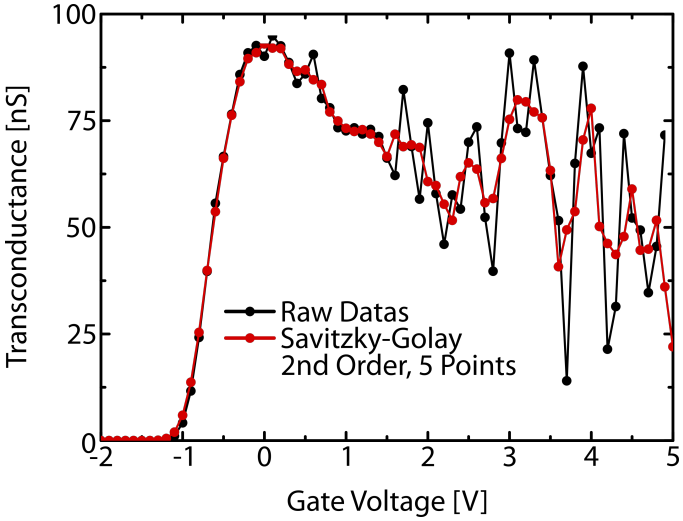

Figure B.11: Comparison of with and without Savitzky-Golay filtering for transconductance of MoS_2 TFT.

XRD of as-evaporated polycrystalline DNTT films on PAA and SAM

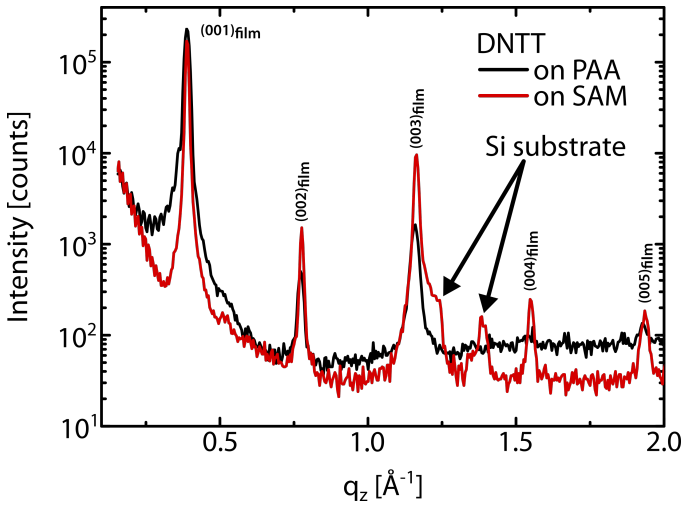

Figure B.12: XRD of as-evaporated polycrystalline DNTT films on PAA and SAM.

Photoluminescence of different MoS_2 crystals on the same substrate

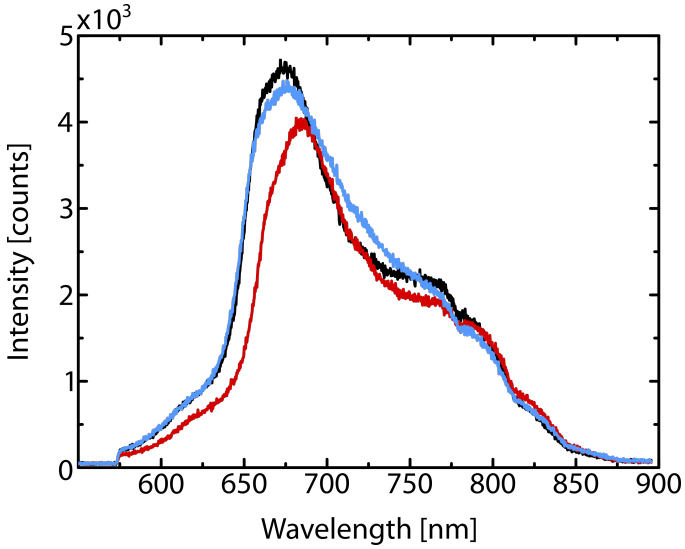

Figure B.13: Photoluminescence of different MoS_2 crystals on the same substrate.

C

Fabrication of van der Waals Transistors

Improvements on TFT fabrication in the group

We began by substituting the gate insulator. Si/SiO_2/COC was the common bilayer gate insulator for organic TFTs ([101, 102, 103, 104]) in earlier studies. Liewald also tried bilayer oxide stacks based on electrochemically oxidized aluminum oxide and tetratetracontane (TTC) with a total dielectric thickness of 66 nm ([104, 105]). These gate insulators are inadequate for fabricating cutting-edge organic TFTs from various aspects. First, the typical thickness of silicon oxide was 100 nm, and its capacitance was approximately 34.5 nFcm^{-2}. We, therefore, substituted the SiO_2 with Al_2O_3 grown by ALD. Thin enough for high capacitance yet thick enough not to leak during measurements, we chose 33 nm as the optimal thickness. The approximate capacitance of 33 nm thick Al_2O_3 was 241 nFcm^{-2}. Moreover, we changed from COC passiva-

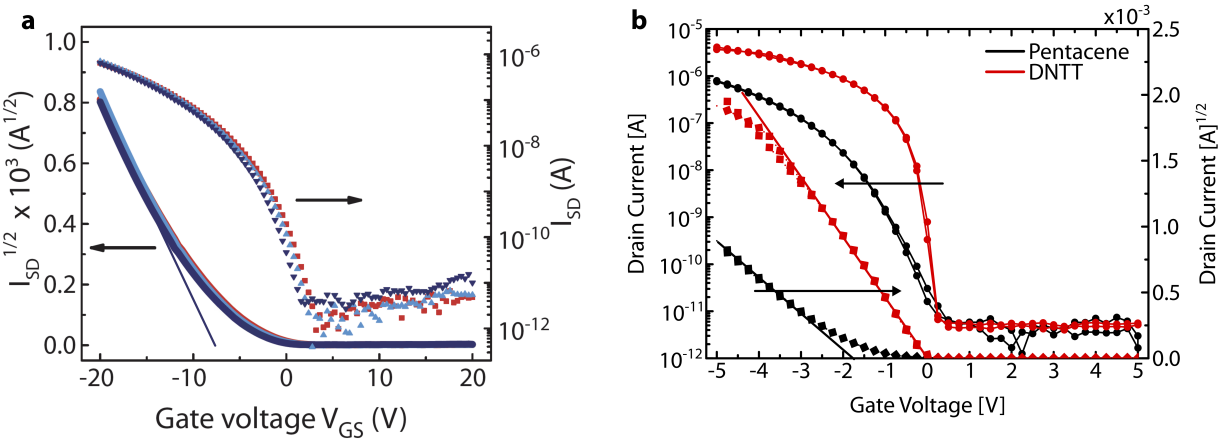

Figure C.1: Transistor characteristics of organic TFTs with previous and the new oxide stack. **a** Pentacene TFT on SiO_2/COC gate stack. **b** Pentacene and DNTT TFTs on Al_2O_3/SAM gate stack.

tion to SAM passivation by the substitute. Through this modification, the hydrophobicity had increased from approximately 90 ° to 105 °, and physical polymer-based passivation was replaced with chemical molecular-based passivation. Second, we revised the geometry of the TFT. In earlier studies, the typical transistor channel widths (W) and lengths (L) were 2 mm and 20 µm, respectively (W/L = 100). It is well-known that these high width-to-length ratios in channel dimensions result in high contact resistance [95]. Therefore, we decreased the width-to-length ratios with new shadow masks to achieve proper transistor characteristics. Cadilac Laser GmbH manifactured polyimide masks with a fixed width of 200 µm and lengths of 100 µm, 50 µm, and 20 µm. Unless otherwise specified, the geometry of the subsequent measurements will be 200 µm to 100 µm (W/L = 2). Figure C.1 presents the comparison of the new pentacene and DNTT TFTs to earlier TFTs. We reduced the applied gate and drain voltages from 20 V to 5 V by the improvements. Furthermore, we achieved similar output currents for pentacene TFTs, although we reduced the W/L 50 times (Equation 2.11). The results proved that the new fabrication method brings state-of-the-art TFTs, so the quality of growth, interface, and electrical contacts were excellent.

Substrate Cleaning

Standard cleaning of the growth substrates:

- Sonication in acetone for 10 min at 60 °C for full power.
- Sonication in IPA for 10 min at 60 °C for full power.
- Sonication in DI-water for 10 min at 60 °C for full power.
- Blow dry air.

Standard cleaning of the transistor substrates without photoresist protection:

- Sonication in acetone for 10 min at 60 °C for full power.
- Sonication in IPA for 10 min at 60 °C for full power.
- Blow dry air.

Standard cleaning of the transistor substrates with photoresist protection:

- Soaking in acetone for 30 min.
- Rinsing in IPA for 30 min.
- Blow dry air.

Use separate beakers for each solvent. In case of a necessity for surface activation, such as PAA coating or SAM passivation, an additional oxygen plasma step was carried for 5 min at 50 W under 10 sccm oxygen flow. Do not spend time between the plasma treatment and deposi-

tion/functionalization.

PAA deposition:

- Typical concentration is 2.5 % w/w, filtered from solution right before coating by 0.22 µm pore-sized syringe filter.
- Spin-coating for 60 s at 4,000 rpm without ramping (results in approximately 50 nm-thick PAA film).
- Loaded to the UHV chamber right after the spin-coating.

Further details of the PAA preparation is summarized in Veronika Reisner's master thesis.

SAM functionalization:

- Prepare a 5 ml of 20 mM stock solution by dissolving 27.8 mg n-tetradecylphosphonic acid in 5 ml IPA. Stir the stock solution for 30 min.
- Divide into two 2 ml Eppendorf tubes and centrifuge for at least 10 min at 15,000 rpm.
- Use the upper half for 1 ml centrifuged solution and mix it with 19 ml IPA to obtain 1 mM solution.
- Immerse the plasma treated substrates for 3 h to overnight. Overnight causes clusters of the SAM.
- Wash/sonicate (low power) the substrates with IPA.
- Bake at 130 °C for 3 min for solvent evaporation.

COC deposition:

- Typical concentration is 0.25 % w/w with TOPAS COC 6013-S04. Rinse the COC pellets rinsed with toluene by dropcasting from pipette. Rinse the bottle for the main COC solution before the preparation. Scale toluene **under fume hood.** For further information, please refer to C. Liewald's bachelor thesis.
- Each material that will be involved in the deposition process have to be rinsed with toluene, including Eppendorf tubes and the pippettes.
- Prepare three Eppendorf tubes, fill one of them with COC solution, the other with toluene. Centrifuge both at (8,000 to 10,000) rpm for 10 min.
- Use the upper half of the COC solution and fill the third tube. The solvent is ready for COC deposition.
- Spin-coating for 60 s at 6,000 rpm without ramping (results in approximately (5 to 6) nm-thick COC film). Bake the substrates for solvent evaporation at 100 °C for 3 min.

Single-layer PMMA lithography, mostly used for MoS_2 and ambipolar transistor patterning:

- Typical PMMA solvent for single-layer lithography was 950 K A4.
- Spin-coating for 40 s at 5,000 rpm with ramping for 1 s at 800 rpm for approximately 200 nm-thick PMMA layer. Bake the substrates for solvent evaporation at 180 °C for 2 min. In case of COC deposited substrates, bake at 100 °C for 10 min. TOPAS COC 6013-S04 has glass transition temperature around 130 °C.
- The dose factor is 0.95 for 10 kV and the developer time is 50 s after patterning. Rinse with IPA after.
- After metal deposition, lift-off at least for 3 h.

Double-layer PMMA lithography, mostly used for Ti/Au deposition for aluminum gates:

- Use PMMA 495K A4 (prepared in-house) as first layer.
- Spin-coating for 40 s at 5,000 rpm with ramping for 1 s at 800 rpm for approximately 120 nm-thick PMMA layer. Bake the substrates for solvent evaporation at 180 °C for 2 min. In case of COC deposited substrates, bake at 100 °C for 10 min. TOPAS COC 6013-S04 has glass transition temperature around 130 °C.
- Use PMMA 950K A4 as second layer.
- Spin-coating for 40 s at 5,000 rpm with ramping for 1 s at 800 rpm for approximately 200 nm-thick PMMA layer. Bake the substrates for solvent evaporation at 180 °C for 2 min. In case of COC deposited substrates, bake at 100 °C for 10 min. TOPAS COC 6013-S04 has glass transition temperature around 130 °C.
- The dose factor is 1.2 for 10 kV and the developer time is 62 s after patterning. Rinse with IPA after.
- After metal deposition, lift-off at least for 3 h.

Double-layer PMMA lithography for aluminum gates (Klauk group recipe):

- Use PMMA 150K A4.5 (prepared in-house) as first layer.
- Spin-coating for 40 s at 5,000 rpm with ramping for 1 s at 800 rpm for approximately 210 nm-thick PMMA layer. Bake the substrates for solvent evaporation at 150 °C for 3 min. In case of COC deposited substrates, bake at 100 °C for 10 min. TOPAS COC 6013-S04 has glass transition temperature around 130 °C.
- Use PMMA 950K A4 (prepared in-house) as second layer.
- Spin-coating for 40 s at 5,000 rpm with ramping for 1 s at 800 rpm for approximately 95 nm-thick PMMA layer. Bake the substrates for solvent evaporation at 150 °C for 3 min. In case of COC deposited substrates, bake at 100 °C for 10 min. TOPAS COC 6013-S04 has glass transition temperature around 130 °C.

- The dose factor is 2.5 for 20 kV and the developer time is 60 s after patterning. Rinse with IPA after.
- After metal deposition, lift-off at least for 3 h.

Plasma enhanced oxidation at LS Maier:

- Perform a standart cleaning recipe before you start due to the corrosion problems.
- Perform a pre-conditioning step for 15 min with the process parameters before loading the sample.
- Place the substrates on the oil drop on the wafer holder for better thermalization. The oil can wet pretty badly, use only enough.
- Perform the oxidation for 300 W for 60 s.
- Clean the back side of the substrates from oil and immerse it to phosphonic acid SAM.

Metal deposition:

- Typical thickness of titanium is 5 nm, evaporation rate 0.3 $Å s^{-1}$.
- Typical thickness of gold is 30 nm, evaporation rate 1 $Å s^{-1}$.
- Typical thickness of aluminum is 30 nm, evaporation rate 15 $Å s^{-1}$.

D

Scanning Confocal Microscopy Setup

This appendix summarizes the improvements in the former version of the microscope together with the low-temperature and high-vacuum compatible new version. Therefore, the appendix covers the technical details rather than the scientific discussion of the results. In his doctorate thesis, C. Westermeier explained in detail the former version of the microscope and the scientific background of the Davydov splitting (Figure D.1, D.2)[102]. Here, our first emphasis is on the missing points prevented from achieving the diffraction-limited resolution in the microscope. After completing the improvement in the former version of the microscope, we introduce the new microscope construction.

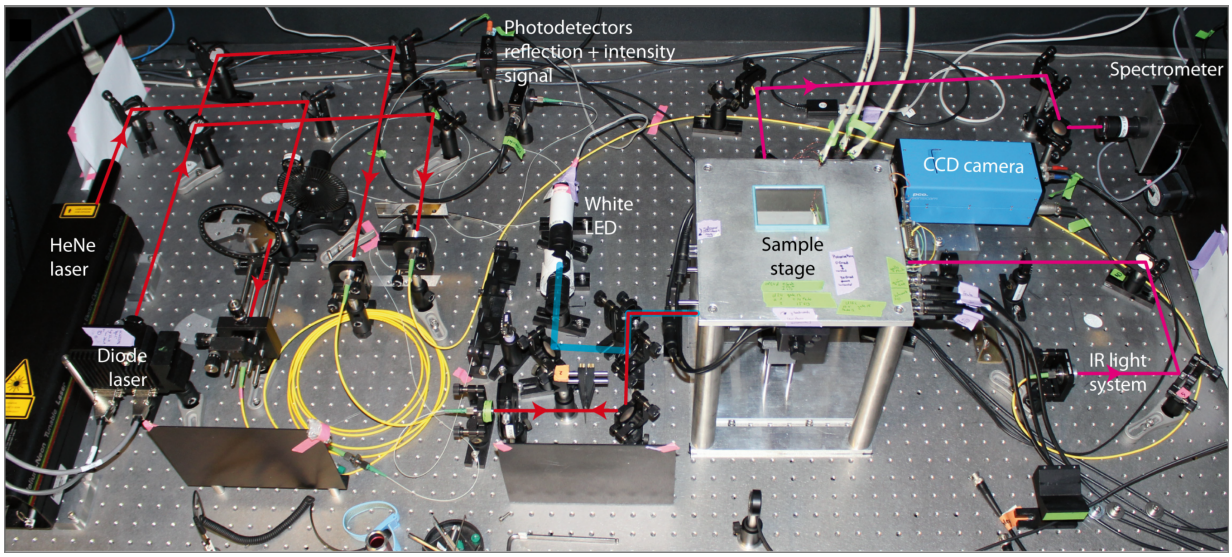

Figure D.1: The former microscope setup. Adapted from [102].

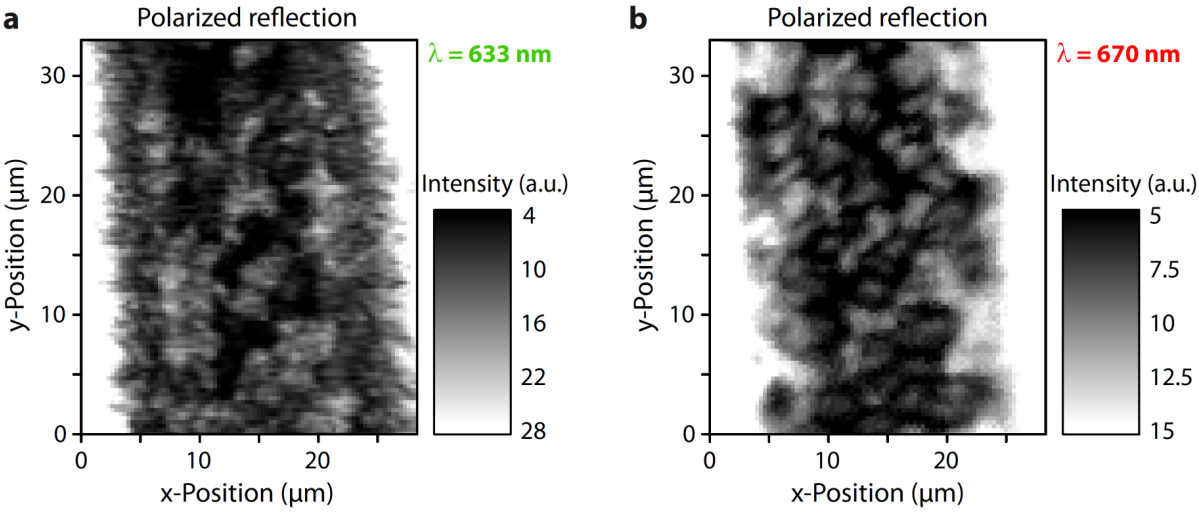

Figure D.2: Davydov splitting in pentacene thin film as a function of laser wavelength, measured by C. Westermeier. Adapted from [102].

Former Version of the Microscope

As discussed, the typical grain size of pentacene is around 4 µm in lateral. Therefore, the grains must be able to be revealed by a scanning confocal microscope in reflectance geometry as a function of wavelength and polarization. A typical reflection map of pentacene thin film acquired by C. Westermeier is shown in Figure D.2. Although the grain sizes are around 5 µm, the micrographs are far from sharpness, and the grain details are barely resolved. Two main reasons can cause the problem; either the beam is not in focus or the focused beam size is bigger than the diffraction limit. While the former is determined according to CCD cameras or lock-in amplifier, the latter is related to the precision of the beam alignment. We found out that the main reason was related to the focused beam size due to an improper beam alignment. The free beam was not straight in the objective since the beam path was not correctly aligned. After correcting the beam straightness on the beam path of the objective, we achieved drastically sharper images, also verifying the Davydov splitting in a higher resolution as shown in Figure D.3 [102, 106].

Then, we improved the laser sources of the microscope. The commonly used He-Ne gas laser had no TTL reference signal for the lock-in amplifier, therefore, using an additional optical chopper was required. However, the reference signal of the optical chopper was not as sharp as a laser diode reference signal due to the poor measurement sensitivity of the optical chopper. To address this issue, we added 405 nm and 515 nm laser diodes to existing 635 nm and 670 nm laser diodes. Since the microscope is built on single-mode fiber input, the beam pro-

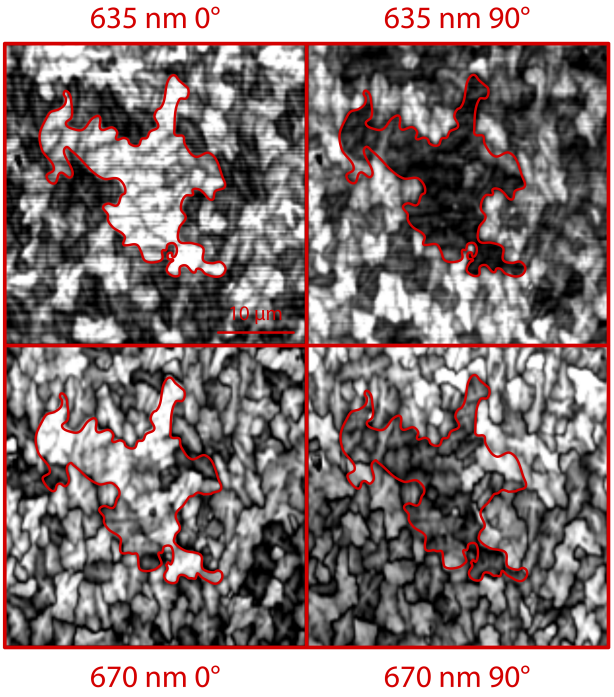

Figure D.3: High resolution Davydov splitting in pentacene thin film as a function of laser wavelength and polarization.

file of the laser source did not limit the using laser diodes. The reflectance maps of pentacene films by various wavelengths are shown in Figure D.4. First, we could reveal the pentacene grains by several wavelengths with similar sharpness. This indicated that the beam alignment was correct, regardless of wavelength. Second, the micrographs demonstrated that the contrast of the grains in reflectance geometry was different for different wavelengths. Third, the reflectance micrographs proved that the Davydov splitting could be revealed only by 635 nm or 670 nm. Consequently, we saw no polarization dependence reflection for the 515 nm and 405 nm lasers. Finally, we added two more lasers to the microscope, 443 nm (DNTT main absorption peak) and 488 nm wavelengths, to cover almost all the prominent colors in the visible range.

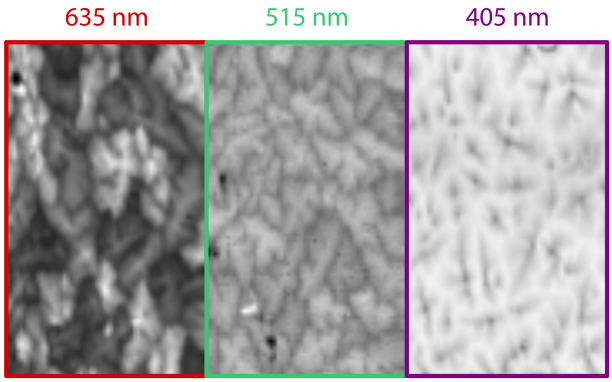

Figure D.4: Reflection micrographs of pentacene thin film under 635 nm, 515 nm and 405 nm laser wavelengths.

Although the microscope was improved drastically, the focus drift problem was still present. The former doctorate students performed a deep investigation on the focus drift. The results revealed that the construction of the microscope was the main reason for the focus drift: using 40 cm-long rods to hold the sample upside-down (Figure D.2). Due to the thermal expansion of the stainless steel, sub-degree changes in the laboratory temperature were enough to drift the focus over time (Figure D.5, see 405 nm map). For a 40 m^2 laboratory, keeping the temperature within a variety of 0.1 °C is unrealistic. In addition, the free-beam path of the spectrometer was also not optimum due to the height mismatch between the beam path and the spectrometer slit. To address these issues, we rebuilt the microscope as shown in Figure D.6a. The microscope became compatible with the vacuum and low-temperature measurements with the new construction. The new construction brought many additional benefits. First, the microscope was built using Thorlabs optical 30 mm cage system, allowing a more compact construction. Second, the free beam path was confined in the cage system, drastically eased the alignment procedure. More importantly, since the objective and the piezo motors were on the same construction (Figure D.6c), the drift problem was resolved (Figure D.5). Lastly, the photoluminescence path was coupled to a multimode (MM) fiber with a well-established,

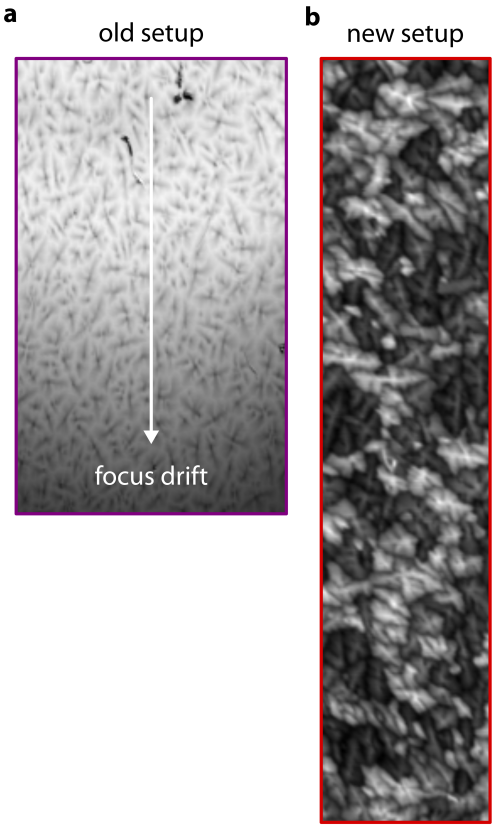

Figure D.5: Change in the reflection intensity during the mapping. **a** 405 nm former version. **b** 635 nm new version.

optimized beam path at the MM fiber end for the spectrometer height (Figure D.6b). Therefore, the microscope is fully operational for reflection, photoluminescence, and photocurrent mappings, with a diffraction-limited focus, without a focus drift.

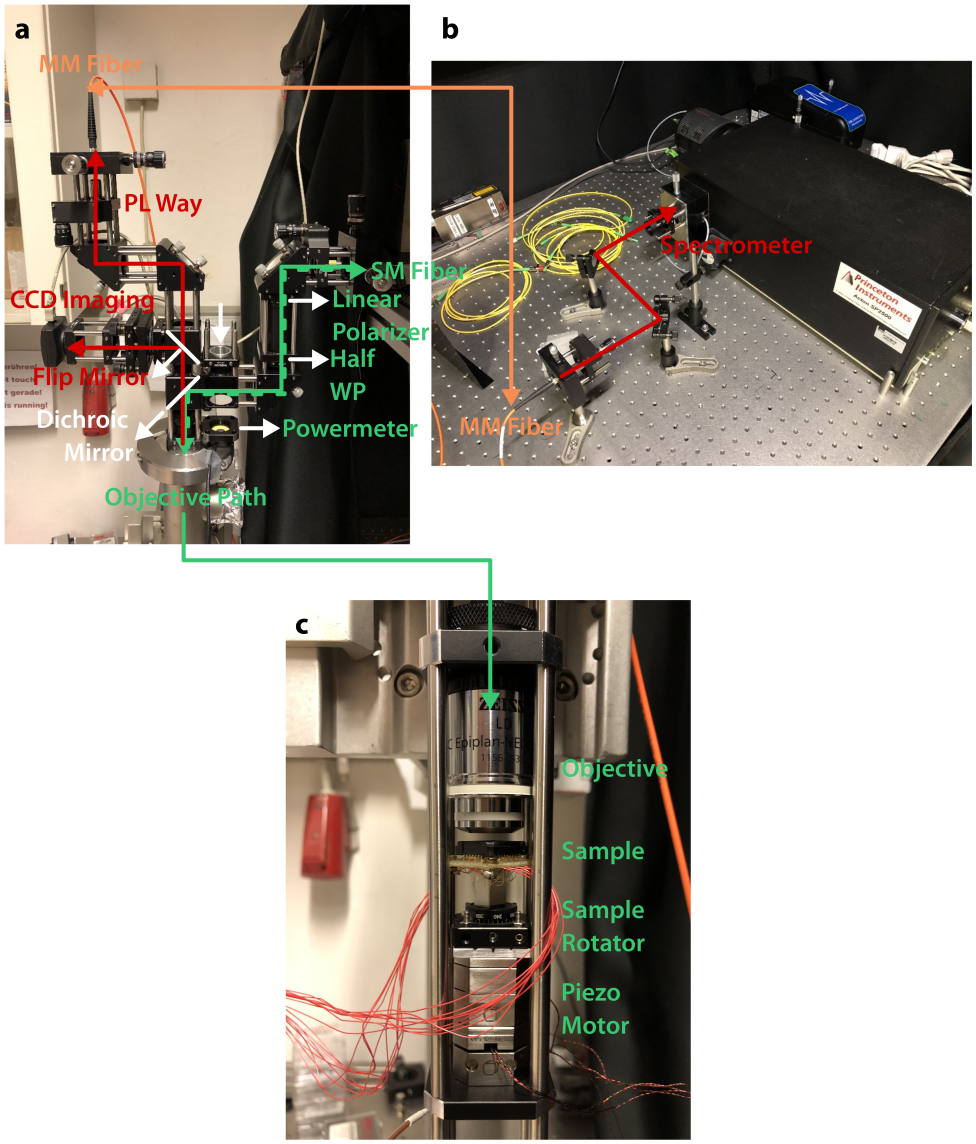

Figure D.6: The new microscope. **a** Optical construction of the microscope. **b** PL path of the microscope. **c** Position of the objective and the sample.

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List of Acronyms

0D Zero-Dimensional

1D One-Dimensional

2D Two-Dimensional

3D Three-Dimensional

AFM Atomic Force Microscopy

Al_2O_3 Aluminum Oxide

ALD Atomic Layer Deposition

AnT Anthracene-2-thiol

a-Si Amorphous Silicon

a-Si:H Hydrogenated Amorphous Silicon

BC Bottom-Contact

BW Backward

C_{60} Buckminsterfullerene

Cl_2 Chlorine Gas

CMOS Complementary-Metal-Oxide-Semiconductor

COC Cyclic Olefin Copolymer

CVD Chemical Vapor Deposition

DH6T Dihexyl-Sexithiophene

DNTT Dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene

DOS Density of States

DPh-DNTT diphenyl-dinaphtho[2,3-b:2′,3′-f]-thieno[3,2-b]thiophene

F_{16}CuPc Copper Hexadecafluorophthalocyanine

F_8BT Poly[(9,9-dioctylfluorenyl-2,7-diyl)-alt-(benzo[2,1,3]thiadiazol-4,7-diyl)]

FET Field-Effect Transistor

FW Forward

GAA Gate-All-Around

h-BN Hexagonal Boron Nitride

high-k High Relative Dielectric Constant

HOMO Highest Occupied Molecular Orbital

HSP Hansen Solubility Parameter

ICP Inductively Coupled Plasma

IPA Isopropanol

IV Current-Voltage

L Length

LEFET Light-Emitting Field-Effect Transistor

MBCFET Multiple-Bridge-Channel Field-Effect Transistor

MIBK Methyl Isobutyl Ketone

MIS Metal-Insulator-Semiconductor

ML Monolayer

Mo Molybdenum

MoO_2 Molybdenum Dioxide

MoS_2 Molybdenum Disulfide

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

$MoTe_2$ Molybdenum Ditelluride

OSC Organic Semiconductors

PAA Polyacrylic Acid

PFBT 2,3,4,5,6-Pentafluor-thiophenol

PMMA Poly(methyl methacrylate)

PVA Polyvinyl Alcohol

QBS Quinodial Biseleophene

RED Relative Energy Difference

RIE Reactive Ion Etching

RMS Root-Mean-Square

RZ Recombination Zone

S Sulfur

SAM Self-Assembled Monolayers

SC FET Single Crystal Field-Effect Transistor

Se Selenium

SEM Scanning Electron Microscopy

SF_6 Sulfur Hexafluoride

Si Silicon

SiO_2 Silicon Dioxide

TC Top-Contact

TFT Thin-Film Transistor

TMD Transition Metal Dichalcogenides

vdW van der Waals

W Width

XRD X-ray Diffraction

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