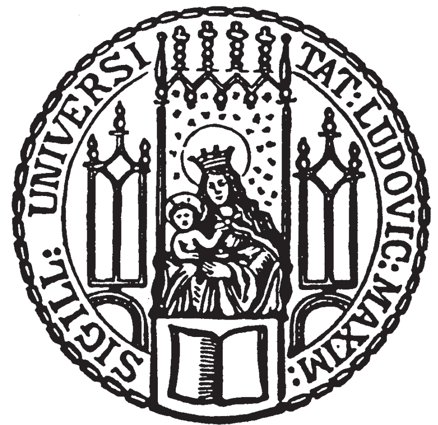
Production and Performance of Silicon Pixel Modules with Planar Sensors for the ATLAS ITk Upgrade

Dissertation by Šejla Hadžić



Production and Performance of Silicon Pixel Modules with Planar Sensors for the ATLAS ITk Upgrade

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Zusammenfassung

Für den High Luminosity Large Hadron Collider (HL-LHC) wird das derzeitige Spurendetektorsystem des ATLAS-Experiment durch ein Silizium-System namens Inner Tracker (ITk) ersetzt. Der Pixeldetektor, das Subsystem, das dem Kollisionspunkt am nächsten ist, besteht aus Modulen basierend auf den folgenden zwei Sensortechnologien: Ein-Chip-Module mit 3D Sensoren und Vier-Chip-Module (Quad) mit planaren Sensoren. Für die planaren Sensoren wurde die dünne n^{+}-in-p-Technologie gewählt, die Sensoren mit reduzierter Dicke und höherer Auslesegranularität im Vergleich zum ursprünglichen Pixeldetektor des ATLAS-Experiments implementiert.

Die nächste Phase des ITk-Pixel-Projekts ist die Montage und das Testen von Pixelmodulen. Der Fokus dieser Arbeit liegt auf dem Letzten. Dies lässt sich in Labor- und Teststrahlmessungen von montierten Quad-Modulen unterteilen. Für Ersteres wurde der Versuchsaufbau im Rahmen dieser Arbeit optimiert und zum Testen von aufgebauten Prototyp-Modulen verwendet.

Die Module, die mit Sensoren verschiedener Hersteller ausgestattet sind, werden vor und nach der Bestrahlung mit Teilchenstrahlen getestet. Um eine schnelle und reibungslose Datenrekonstruktion und -analyse zu gewährleisten, wurde im Rahmen dieser Arbeit die Umstellung auf das neue Analyse-Framework, Corryvreckan, durchgeführt. Vor der Auswahl dieses Frameworks als neuer Standard für die Analyse von ITk-Pixel-Teststrahldaten wurde seine Leistung mit der der früher verwendeten Softwarepaketen verglichen. Zusätzliche Funktionalitäten wurden implementiert, um der ungleichmäßigen Pixel Matrix der Quad-Sensoren gerecht zu werden. Das neue Framework wurde verwendet, um die Leistung von Quad-Modulen mit zwei Versionen von Auslese-Chips, dem Prototyp-RD53A-Chip und dem Vorproduktions-ITkPixV1.1-Chip, zu bewerten. Die Variablen wie Clustergröße, Residualverteilungen und Pixeleffizienz wurden für verschiedene Pixelgrößen der Quad-Module untersucht.

Im Rahmen der Vorproduktionsphase wurde die Charakterisierung von Sensoren aus einem 100 µm dicken Wafer durchgeführt. Damit lässt sich die Qualität der hergestellten Sensoren im Hinblick auf die ITk-Anforderungen bestimmen.

Abstract

For the High Luminosity Large Hadron Collider (HL-LHC) upgrade, the current tracking system of the ATLAS experiment will be replaced by an all-silicon system, called Inner Tracker (ITk). The closest to the collision point will be the Pixel Detector sub-system, instrumented with modules employing two sensor technologies: single-chip modules with 3D sensors and four-chip (quad) modules with planar sensors. For the planar sensors, the thin n^+-in-p technology was chosen, which implements sensors of reduced thickness and higher readout granularity with respect to the original pixel detector of the ATLAS experiment.

The next phase of the ITk pixel project is the production, assembly and testing of pixel modules. The main focus of this thesis is the performance evaluation of assembled quad modules, which can be divided into the laboratory and test-beam measurements. For the former, the experimental setup was adapted and optimized in the scope of this thesis and used for testing of first assembled prototype quad modules.

Assembled modules with sensors from different manufacturers will be tested with particle beams before and after irradiation. To ensure fast and smooth test-beam data reconstruction and analysis, the transition to the new framework, called Corryvreckan, was performed as a part of this thesis. Before choosing this framework as the standard tool for the analysis of ATLAS ITk pixel test-beam data, the validation was performed to compare its performance to that of previously used software packages. Additional functionalities were implemented to accommodate the non-uniform pixel matrix of the quad sensors. The framework as such was used to evaluate the performance of quad modules with two readout chip versions, the prototype RD53A chip and the pre-production ITkPixV1.1 chip. Quantities such as cluster size and residual distributions, as well as hit efficiency, were studied for various pixel sizes implemented for the quad modules.

As a part of the pre-production phase, the characterization of sensors from one 100 µm thick wafer was performed. This allows to determine the quality of manufactured sensors with respect to the ITk requirements.

For my beloved parents

Mojim dragim roditeljima

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Introduction

The experimental program at the Large Hadron Collider is a prominent example of the shared effort across countries to push the boundaries of human knowledge about the fundamental constituents of matter and the underlying laws of nature. The main aim of this program is to study the predictions of the Standard Model, a relativistic quantum field theory representing, for now, our best attempt to classify discovered elementary particles and describe three of four known interactions in the Universe between them. A great success of the LHC was achieved in 2012, when a theoretically predicted particle, the Higgs boson, was discovered by the ATLAS and CMS collaborations. The next operational phase for the LHC is the upcoming luminosity upgrade, which will result in an increase in the number of collisions per second and thus allow to perform precision measurements of Higgs boson properties. Increased luminosity will create a challenging environment, such that the present detector systems need to be upgraded or even partly replaced. This is also true for the ATLAS experiment, for which the upgrade of all of its subsystems is foreseen. In this context, the tracking system of the ATLAS experiment will be replaced with an all-silicon detector called the Inner Tracker (ITk), consisting of modules with pixel and strip sensors. The construction of this new detector is shared among multiple institutes over the world, including the Max-Planck-Institut für Physik (MPP), which contributed to the development of the n^+-in-p planar sensor technology chosen for most of the pixel modules.

The main focus of this thesis is the performance evaluation of new pixel modules with planar sensors for the ITk pixel detector. Each assembled module will undergo quality control testing in the laboratory, for which the experimental setup was adapted and optimized in the scope of this thesis. The second type of performance evaluation are measurements with particle beams. These test-beam measurements allow the operation of modules in conditions close to those expected in the final experiment, with external trigger signals and in synchronization with other detectors. An important aspect of the test-beam activities is the data analysis, for which a flexible software framework was needed. The Corryvreckan framework was recognized as suitable for this purpose. The transition to the new software framework for the test-beam data reconstruction and analysis and its further development for the needs of the ITk pixel test-beam group are performed within this thesis.

The thesis is structured as follows. In Chapter 1, the introduction to the LHC accelerator complex and the ATLAS experiment is given, together with the planned upgrades for both. Chapter 2 gives a theoretical background of semiconductors, in particular of silicon, as the chosen material for the ITk. In Chapter 3, the components of the ITk pixel modules, such as the sensor layout and developed readout chips are discussed, followed by the description of the module assembly procedure. Chapter 4 is dedicated to the experimental

setups and instrumentation used to evaluate the performance of the quad modules (four chips attached to one sensor). The electrical characterization of the prototype modules assembled at the MPP is discussed in Chapter 5. Chapter 6 is dedicated to the description of data reconstruction and analysis performed with the Corryvreckan framework. Here, the performance of this framework is compared with that of previously used software packages. In addition, the further software development needed to accommodate the geometry of the quad sensors is presented. Within this thesis first quad modules, assembled with two versions of the readout chip, are tested with particle beams. Results obtained from multiple test-beam campaigns are presented in Chapter 7. The characterization of 100 µm thick sensors from a pre-production is described in Chapter 8. In Chapter 9, a summary of the main results is given.

Throughout this thesis natural units $c = \hbar = 1$ are used, and therefore energy, momentum and mass are given in electron volt (eV).

1 The LHC and the ATLAS experiment

The primary tool of high energy physics to study elementary constituents of matter are particle collision experiments. The basic idea behind such experiments is to accelerate elementary or composite particles and bring them into collision. The collision products are afterwards studied to quantify parameters and investigate the limits of a theory. Designing and building such a machine requires knowledge from different fields of expertise, including civil and mechanical engineering, solid state physics, microelectronics, computer science and cryogenics, making particle accelerators among the most complex manmade machines. Over the last decades, the size of accelerators, and thus the collision energy, has been increased, allowing to explore new regimes and challenge theoretical predictions. The present largest and most powerful particle accelerator in the world is the Large Hadron Collider (LHC) [1], located at CERN[1] near Geneva, operating since September 2008, with the goal of investigating the structure of matter and pushing the frontier of human knowledge.

In Section 1.1 of this chapter, the main characteristics of the LHC complex and planned upgrades are described. The complete overview of the ATLAS experiment is given in Section 1.2. Section 1.3 of this chapter is dedicated to planned upgrades of the ATLAS experiment, with a focus on the tracking system upgrade.

1.1 The Large Hadron Collider

The Large Hadron Collider consists of a 27 km long underground tunnel, previously housing the Large Electron-Positron Collider (LEP) [2], hosting superconducting dipole magnets and accelerating structures to achieve the desired particle energy. Inside the accelerator, two high energy particle beams travel in opposite directions in separate beam pipes and collide at four Interaction Points (IPs) along the accelerator ring. The accelerator is designed for proton-proton collisions with a center-of-mass energy of $\sqrt{s} = 14$ TeV at a nominal instantaneous luminosity of 10^{34} cm^{-2}s^{-1} and lead ion collisions up to $\sqrt{s} = 1.15$ PeV at a nominal instantaneous luminosity of 10^{27} cm^{-2}s^{-1}. The collision products are detected and analyzed with detectors constructed around interaction points, each designed for specific scientific goals. Two of them, the ATLAS[2] [3] and CMS[3] [4] experiments are large multi-purpose detectors implementing complementary technologies. The ALICE[4] [5] experiment

[1] European Organization for Nuclear Research
[2] A Toroidal LHC Apparatus
[3] Compact Muon Solenoid
[4] A Large Ion Collider Experiment

is used to study the quark-gluon plasma in heavy-ion collisions and the LHCb[5] [6] detector is designed for investigating CP violations in the interactions of b-hadrons. Particles produced by proton-proton collisions in the LHC are detected and studied by additional smaller experiments designed for very specialized purposes.

1.1.1 Accelerator complex

The LHC accelerates protons using radiofrequency cavities, resulting in a bunched structure of the beam. Charged particles accelerated along the circular ring lose energy in form of synchrotron radiation, for which the energy loss is proportional to m^{-4}. Therefore, this effect is less severe when accelerating heavier particles, like protons, allowing to increase the energy accessible to an accelerator. The LHC accelerator complex is shown in Figure 1.1.

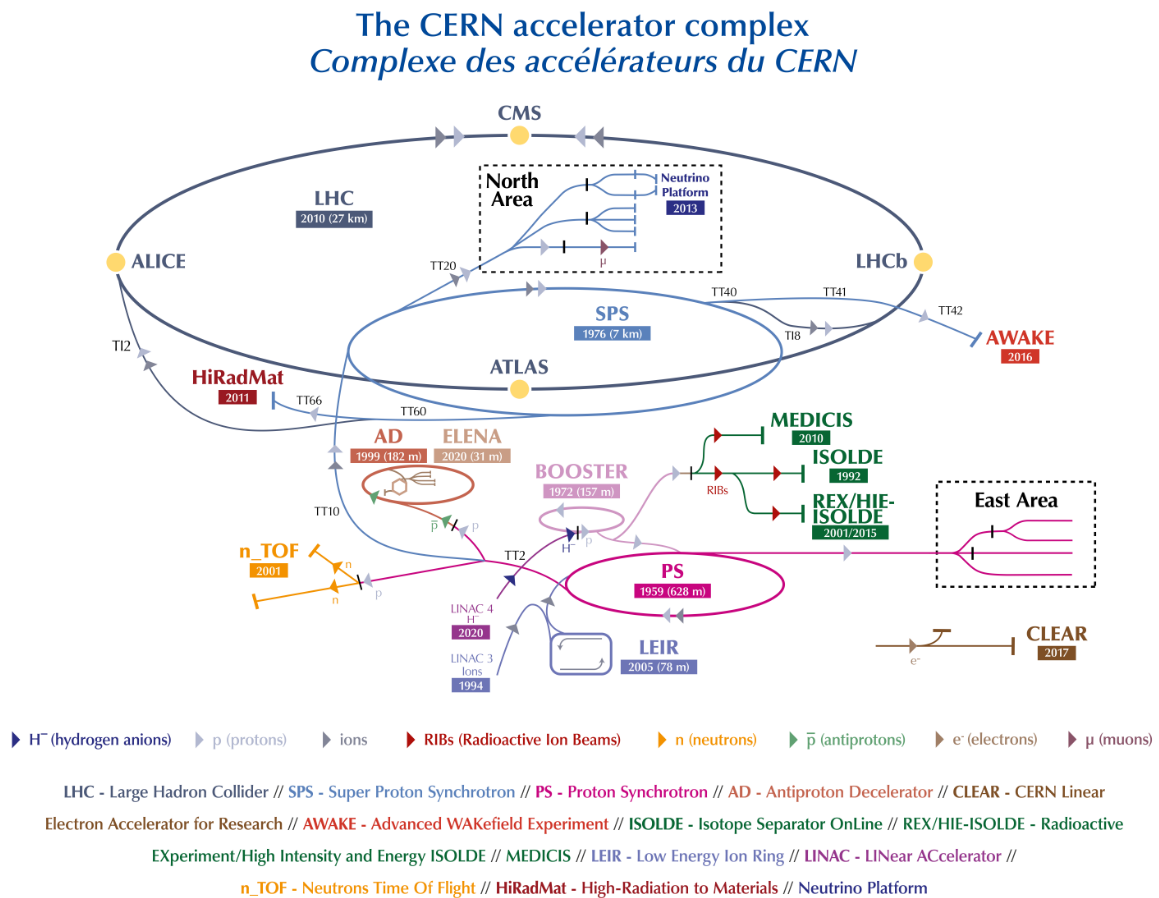


Figure 1.1: The LHC accelerator complex [7].

To reach the desired collision energy, particles are traveling through a series of preaccelerators before they are injected into the LHC ring. The acceleration process starts from

[5]Large Hadron Collider beauty

negative hydrogen ions (H^-, hydrogen atoms with an additional electron), which are accelerated to 160 MeV by the Linear Accelerator 4 (LINAC 4). Additional electrons are removed during the injection from the LINAC 4 to the Proton Synchrotron Booster (PSB), leaving only protons, which are accelerated to 2 GeV. These are injected into the Proton Synchrotron (PS), where they reach 25 GeV and afterwards transferred to the Super Proton Synchrotron (SPS) to be accelerated up to 450 GeV. This is followed by the final injection into the two opposite beam pipes of the LHC ring, where they are accelerated until they reach the collision energy. The beams are kept in stable orbits by superconducting dipole magnets and in focus by quadrupole magnets.

Luminosity

The two most important parameters of an accelerator are the achievable collision energy and luminosity. Higher energy in an accelerator can be achieved by building larger acceleration rings or using more powerful magnets. Instantaneous luminosity $\mathcal{L}$ determines the rate of particle interactions dN/dt occurring for a given process cross-section σ_{p}:

$$\frac{dN}{dt} = \mathcal{L} \cdot \sigma_{\mathrm{p}}. \tag{1.1}$$

In a collider, the luminosity is given by the beam intensity I per collision area A. Assuming a circular machine and Gaussian beam profiles of two identical beams, the luminosity can be expressed as [8]:

$$\mathcal{L} = \frac{I}{A} = \gamma \frac{N_{\mathrm{b}}^2 n_{\mathrm{b}} f_{\mathrm{rev}}}{4\pi \epsilon_{\mathrm{n}} \beta^*} R_{\phi}, \tag{1.2}$$

where γ represents the Lorentz factor, N_b is the number of particles per bunch, and n_b is the number of bunches per beam. Furthermore, f_{rev} represents the revolution frequency, ϵ_{n} is the transverse normalized emittance, and β^* is a beam geometry parameter describing the focal length at the collision point. The geometrical reduction factor of the luminosity is given by R_ϕ and depends on the crossing angle ϕ between colliding beams and σ, σ_{z} as the root mean square (RMS) of the beam sizes in the traverse and longitudinal directions [8]:

$$R_\phi = 1/\sqrt{1 + \frac{\phi \sigma_{\mathrm{z}}}{2\sigma}}. \tag{1.3}$$

The time-integral of the instantaneous luminosity is the integrated luminosity:

$$L = \int \mathcal{L} dt, \tag{1.4}$$

and represents the collected data size as an important value to characterize the performance of an accelerator.

The first larger dataset at the LHC was collected in 2010, at a center-of-mass energy of $\sqrt{s} = 7$ TeV. Since then all LHC beam parameters were improved. In 2018, collisions occurred at a center-of-mass energy of $\sqrt{s} = 13$ TeV with a maximum peak luminosity exceeding two times the design value.

Table 1.1: Comparison of beam parameters at the nominal LHC and the HL-LHC [8] for the 25 ns bunch spacing.

Name	Symbol	Unit	LHC	HL-LHC
Center-of-mass energy	$\sqrt{s}$	TeV	14	14
Number of bunches	N_b		2808	2808
Particles per bunch	n_b	10^{11}	1.15	2.2
Revolution frequency	f_{rev}	kHz	11.245	11.245
Normalized emittance	ϵ_n	µm	3.75	2.5
Beta function at the IP	β^*	m	0.55	0.15
Crossing angle	ϕ	µrad	285	590
RMS bunch length	σ_z	cm	7.55	7.15
RMS bunch beam size at the IP	σ	µm	16.7	13.6
Levelled luminosity	$\mathcal{L}_{lev}$	10^{34} cm^{-2}s^{-1}	1	5
Peak luminosity	$\mathcal{L}_{peak}$	10^{34} cm^{-2}s^{-1}	1	7.18
Collisions per bunch-crossing	$< \mu >$	events	19	200

1.1.2 The High Luminosity LHC

The High-Luminosity LHC (HL-LHC) project is the next phase of the LHC operation with the aim to strengthen the discovery potential of the LHC after 2030. To achieve this goal, a series of upgrades of the accelerating components is planned which will bring the collider to its nominal center of mass energy of $\sqrt{s} = 14$ TeV and an increase of the integrated luminosity of more than ten times the design value of the LHC [8]. All parameters of the initial LHC design as well as the HL-LHC upgrade are summarized in Table 1.1.

The operation of the LHC and the road towards the HL-LHC are divided into data taking periods: Run 1 (2010-2013), Run 2 (2015-2018), the present Run 3 (2022-2026) and Run 4 (from 2030) which marks the start of the HL-LHC. The data taking periods are separated by Long Shutdown (LS) periods for accelerator and detector maintenance and upgrades towards the HL-LHC. The upgrade roadmap is illustrated in Figure 1.2 and consists of the following activities on the accelerator complex per each of the LS periods:

- The **LS1** took place in the years 2013 to 2015, during which the consolidation of more than 10 000 interconnections between accelerator magnets, the addition of further magnet-protection systems, and the improvement and strengthening of cryogenic, vacuum and electronic systems took place.
- The **LS2** took place in the years 2019 to 2022 and was mainly dedicated to the LHC Injector Upgrade to increase the LHC peak luminosity to 2×10^{34} cm^{-2}s^{-1}, aiming of reaching an integrated luminosity of 450 fb^{-1} by the end of Run 3. In 2020, the LINAC 2 was replaced with LINAC 4. In addition, over the period of three years, 16 new collimators were installed in the accelerator complex.
- The **LS3** upgrade is scheduled to take place from 2026 to 2029, with the plan of installing new quadrupole magnets based on the niobium-tin (Nb_3Sn) superconducting compound, an innovative technology that will allow to achieve magnetic fields above

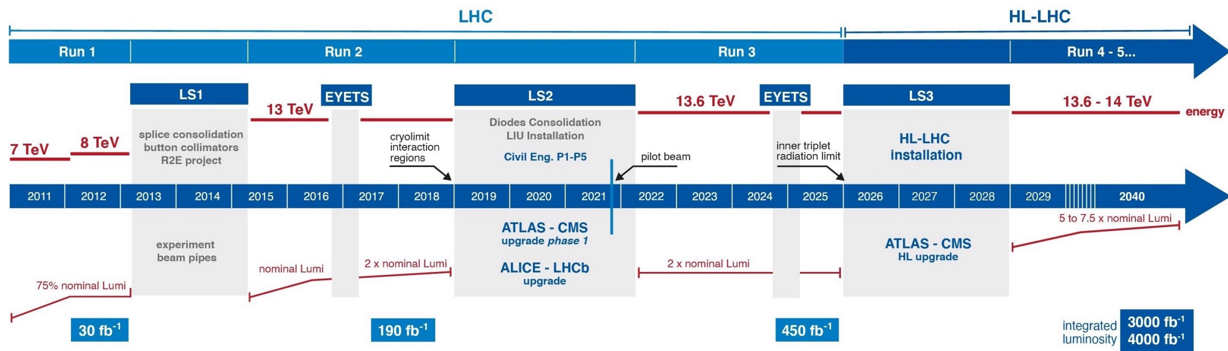


Figure 1.2: The upgrade schedule of the LHC as of February 2022 [9].

10 T, in comparison to the present magnets that achieve 8.3 T. The second major planned upgrade is the installation of 16 superconducting radio-frequency "crab" cavities, on either side of the ATLAS and CMS detectors. With this technology, it will be possible to enlarge the overlap area between the incoming bunches and thus increase the number of collisions per bunch crossing.

1.2 The ATLAS experiment

The ATLAS detector is one of the two general-purpose detectors at the Large Hadron Collider, with the same scientific goals but different technological solutions than the CMS detector. The main motivation behind the design of the ATLAS experiment was the search for the Higgs boson expected to be responsible for the symmetry breaking mechanism essential to explain the mass generation in the elementary particle physics. In 2012, the successful operation of the LHC (Run 1) was followed by the discovery of a new particle, which was confirmed to be the Higgs boson, with a mass of 125 GeV [10, 11]. Although designed with the goal to search for the Higgs boson, the ATLAS experiment is capable of a wide variety of measurements and searches, from precision measurements of the Standard Model (SM) parameters to the TeV scale search for new particles beyond the SM. This broad physics program is possible due to its key design aspects, such as the high charged-particle momentum resolution, good electron and photon identification, precise vertexing for jet flavor tagging and accurate jet and missing energy measurements as well as good muon identification and momentum resolution [3].

Most of the particles created in the proton-proton collisions at the LHC are heavy and decay shortly after their production. Their identification is obtained through the measurement of their final decay products. To detect all particles produced in the collisions, the experiment is designed with a hermetic structure of different detection subsystems layered around the interaction point, each dedicated to the measurement of some of the quantities such as the trajectory, momentum, or energy of particles.

With its length of 44 m, diameter of 25 m and weight of 7000 tonnes, ATLAS is the largest detector ever constructed for a particle accelerator. Figure 1.3 shows the ATLAS detector

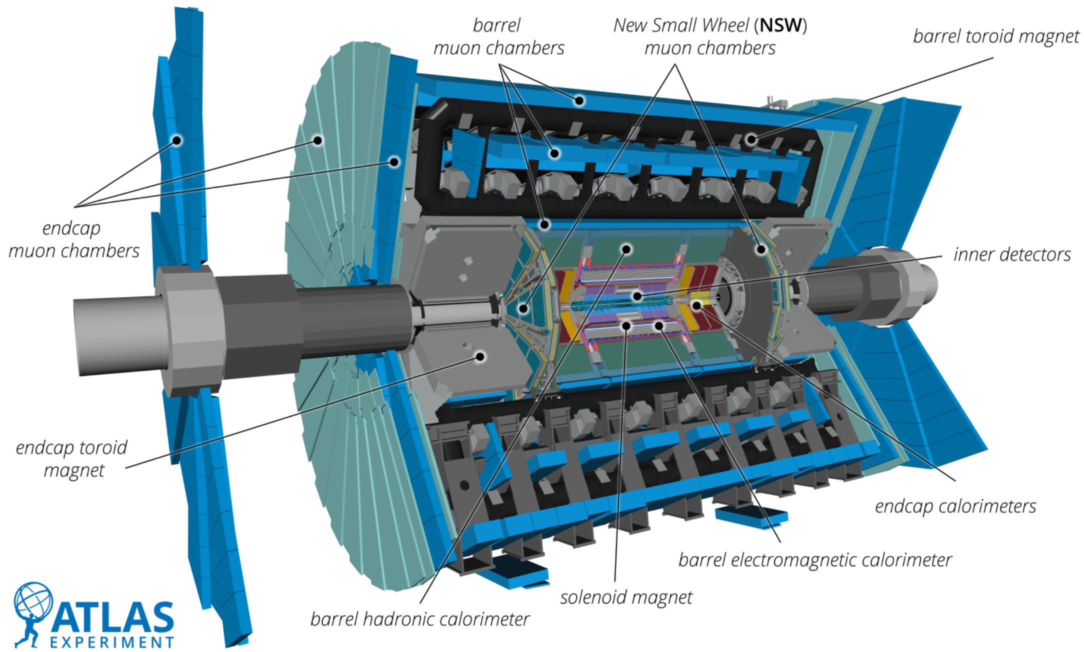


Figure 1.3: A complete view of the ATLAS detector [17].

with its subsystems grouped into three main categories:

- The Inner Detector (ID) [12, 13] is the innermost tracking system, surrounded by a solenoid. The ID measures the momentum of charged particles through the curvature of their trajectories bent by the magnetic field.
- The calorimeters, electromagnetic (ECAL) [14] and hadronic (HCAL) [15], measure the energy of the particles.
- The Muon Spectrometer (MS) [16], is the outermost tracking system with a toroidal magnet, dedicated to the momentum measurements of muons.

Each subsystem is divided into a central cylindrical part or barrel and a disk-shaped forward part on each side of the barrel referred to as end-caps.

Magnet system

As magnet system, the ATLAS detector uses two large superconducting magnets to bend the trajectory of charged particles and measure their momenta:

- the inner homogeneous 2 T magnetic field is created by the central solenoid magnet that surrounds the ID;
- the outer inhomogeneous magnetic field is produced by eight very large air-core superconducting barrel loops and two end-caps air toroidal magnets, situated within the MS.

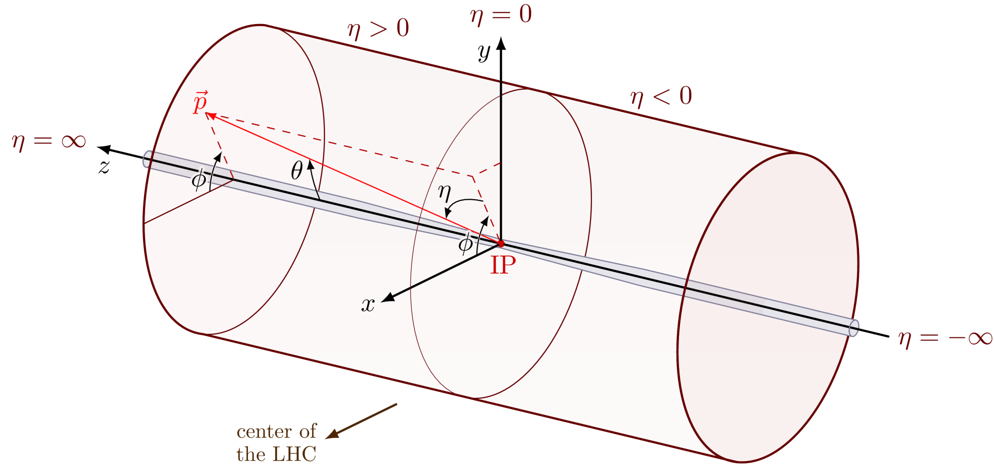


Figure 1.4: Visualization of the ATLAS coordinate system. This image is modified from Ref. [18].

To provide strong magnetic fields, the superconducting magnets are cooled with liquid helium to 4.5 K.

Coordinate system

The coordinate system of the ATLAS detector is defined in the cylindrical coordinates as illustrated in Figure 1.4, with its origin at the nominal IP in the center of the detector, such that the x-axis points to the center of the LHC, the y-axis points upwards, and the z-axis is defined by the counterclockwise beam direction. The quantity ϕ is the azimuthal angle around the beam line. The pseudorapidity is defined in terms of the polar angle θ measured from the positive z-axis as:

$$\eta = -\ln\left(\tan\frac{\theta}{2}\right) \tag{1.5}$$

For a particle emerging the IP perpendicular to the beam line $\eta = 0$, while $\eta = \infty$ indicates a particle parallel to the beam direction. Each detector subsystem is limited differently in its pseudorapidity coverage and combined they ensure the coverage over almost the entire rapidity. The two ends of the ATLAS detector are called the A-side and the C-side, with the former being along the positive z-axis.

Trigger and Data Acquisition System

The ATLAS experiments observes proton-proton collision events at a frequency of 40 MHz, where each event corresponds to a data size of around 1.5 MB, resulting in a data stream of 60 TB/s. Therefore, a dedicated Trigger and Data-Acquisition (TDAQ) system [19] is used to identify, select, and store only collisions interesting for the analysis, reducing the initial frequency of 40 MHz to 1 kHz of stored events. Events are selected using a two-stage trigger system. A fast first level trigger (L1) is hardware-based and relies on the data from the calorimeters and the muon spectrometer. Selecting the events with large electromagnetic

deposits or high p_{T} muon tracks, it reduces the initial event rate down to 100 kHz using custom-built electronics. The main new components for the Run 3 are new L1 calorimeter feature extraction modules to process finer granularity information from the calorimeter system for improved electron, photon, and tau selections. In addition, the signals from the New Small Wheel (NSW) system (Section 1.2.3) are included in the L1 muon end-cap trigger. This will significantly reduce the overall rate by rejecting a large fraction of fake triggers, which refer to particles created by interactions with the detector material in the region between the Small and Big Wheels. Events selected by the L1 trigger are passed to the software-based High Level Trigger (HLT), which performs an event reconstruction to further reduce the data rate down to 1 kHz.

1.2.1 The Inner Detector

The Inner Detector (ID) is the first sub-detector system that records collision products. It has the purpose of reconstructing the helical trajectories of charged particles through the application of tracking algorithms, and determining their charge and momenta. The ID is constructed as a combination of high-resolution semiconductor detectors in the inner part and straw tubes in the outer part, providing pattern recognition, momentum and vertex measurements, with high efficiency over the pseudorapidity range $|\eta| < 2.5$.

The Pixel Detector [20] is the innermost element of the ID. Designed with high granularity, it has a crucial role in the reconstruction and identification of primary and secondary vertices and provides excellent spatial resolution. The active area of the ATLAS Pixel Detector consists of four barrel layers, including the later added Insertable B-Layer (IBL) [21] and two identical end-cap systems, each with three disks. The original three layers of the pixel system are made of 1744 identical 250 µm thick planar n^+-in-n sensors with 50×400 µm^2 pixel cell size and FE-I3 readout chips [22]. The additional barrel layer, inserted during the Phase-0 upgrade, has two different sensor technologies implemented: planar n^+-in-n and 3D n^+-in-p sensors, where both employ the FE-I4 readout chip [23], with a larger area, reduced pixel size (50×250 µm^2) and an improved radiation hardness compared to the FE-I3 chip.

The middle section of the ID is the SemiConductor Tracker (SCT) [24] whose barrel consists of silicon strip modules arranged in four layers and nine end-cap disks per side. Each SCT module consists of a pair of sensors glued back-to-back at 40 mrad stereo angle. All sensors have a thickness of 285 µm and are constructed of high-resistivity p^+-in-n sensors with implants AC-coupled to the readout strips.

The outermost part of the ID is the Transition Radiation Tracker (TRT) [25], where the basic detector elements are 4 mm diameter thin-walled proportional drift tubes (straw tubes) filled with a gas mixture of 70% Xe, 27% CO_2 and 3% O_2 and a gold-plated tungsten wire as anode. The particle traversing a straw tube will cause the ionization of the gas. Created charges are collected on the anode by applying a strong potential difference between the wall and the wire. Transition radiation photons are emitted from ultra-relativistic particles when crossing the surface between two media of different dielectric constants and are

absorbed in the Xe-based gas mixture. Particle identification is possible using low- and high-level thresholds implemented in the front-end electronics. The low-level threshold is optimized to detect all hits, while the high-level threshold is used to detect large energy deposits. As the number of photons produced is proportional to the Lorentz factor γ, particle identification is based on the probability of a particle's signal to exceed the high level threshold, which is different for an electron or a much heavier hadron.

1.2.2 The Calorimeter System

The calorimeters located around the tracking system, are usually designed to stop traversing particles inside their volume and measure the energy they deposit via interaction with atoms. When passing through a calorimeter, an incoming particle generates a cascade of secondary particles, forming a shower. The secondary particles will contribute to the shower development until their energy is below the threshold for further interactions. Depending on the nature of the primary particle, the shower can be:

- electromagnetic, created by electrons, positrons or photons, that interact with matter via the electromagnetic force. Electrons and positrons lose energy mainly by ionization and Bremsstrahlung, and high energy photons via e^+e^- pair production.
- hadronic, created by hadrons that interact with matter via the strong nuclear force.

Electromagnetic showers are usually more compact and shorter than the hadronic ones. Therefore, in collider experiments, the calorimeter system is split into two: electromagnetic and hadronic calorimeter. They are constructed using different materials and designs and in different sizes, that reflect the dimensions of the shower they have to absorb.

The ATLAS electromagnetic calorimeter is a high granularity liquid Argon (LAr) detector with accordion-shaped Kapton electrodes and lead absorber plates, providing a coverage within $|\eta| < 3.2$. The ionization charge is collected on copper-clad Kapton electrodes. A presampler detector, consisting of an active LAr layer of 1 cm (0.5 cm) thickness in the barrel (end-cap) region, is used to correct for the energy loss by electrons and photons upstream of the calorimeter. For the Run 3, new trigger readout boards with higher granularity are implemented for the LAr system, which leads to an improvement in rejecting fake electron triggers.

The ATLAS hadronic calorimeter is divided into three subdetectors: tile, LAr hadronic end-cap (HEC) and forward (FCal) calorimeter, providing a coverage within $|\eta| < 4.9$. The tile calorimeter is a sampling calorimeter, with high lateral granularity, using steel as the absorber and scintillating tiles as the active material. On both sides, tile readout is done by photomultipliers via wavelength shifting fibers. The Hadronic End-cap Calorimeter is located directly behind the electromagnetic end-cap calorimeter. The liquid argon is chosen for this part of the hadronic calorimeter over scintillation tiles, due to higher radiation in the forward region. The forward calorimeter consists of three sections, the first made of copper absorbers, while the others use tungsten.

1.2.3 The Muon Spectrometer

Most of the particles created in collisions are absorbed in the calorimeter system, except for muons and neutrinos. Muons leave a signal in the ID, but pass through calorimeters almost undetected, as they do not generate extended electromagnetic or hadronic showers. Therefore, the outermost part of the ATLAS detector is the muon spectrometer, optimized for reconstruction and identification of muons with transverse momentum from a few GeV to several TeV, in the pseudorapidity range up to $|\eta| < 2.7$. The muon spectrometer is based on gas detectors, with different technologies in the precision-tracking and triggering chambers.

The barrel region is equipped with Monitored Drift Tube (MDT) chambers for precision-tracking. Resistive Plate Chambers (RPC) are used for triggering, due to their good time resolution and high rate capability. To suppress fake muon triggers in the transition region from the barrel to the end-caps, eight additional integrated Thin-Gap RPC and small-diameter Monitored Drift Tube (sMDT) chambers have been installed during the LS2, as part of the Phase-I upgrade of the ATLAS experiment.

In its original design, the end-cap regions are equipped with precision measurement Cathode Strip Chambers (CSC) and Thin Gap Chambers (TGC) for triggering purposes. To maintain the ATLAS muon momentum resolution in the high-background environment of the upgraded LHC, the major Phase-I upgrade of the muon spectrometer included the replacement of the original Small-Wheel (SW) with one New Small Wheel [26]. The NSW implements two new detector technologies: the small strips Thin Gap Chambers (sTGC) and the Micromegas (MM).

1.3 Phase-II upgrade of the ATLAS experiment

Increased instantaneous luminosity, and thus number of pile-up events per bunch crossing at the HL-LHC require the upgrade of some present detector technologies, electronics and data acquisition systems of the LHC experiments. The upgrade of all detector systems of the ATLAS detector was planned, with many improvements being completed during the past LS periods. This section gives an overview of the planned Phase-II upgrades of the ATLAS detector during the LS3, prior to the start of the HL-LHC era. Here the focus is on the upgrade of the ATLAS tracking system.

1.3.1 Upgraded detector components

The large increase of pile-up interactions is one of the main experimental challenges for the HL-LHC physics program. To distinguish between collisions occurring close in space, but well-separated in time, a novel High-Granularity Timing Detector (HGTD) is proposed to be installed in front of the LAr end-cap calorimeters [27]. The HGTD is based on a low-gain avalanche detector technology that provides high-precision timing information.

Due to the limited radiation tolerance of certain currently installed front-end components and incompatibility with the upgraded trigger system, the planned calorimetry upgrades are focused on the replacement of the readout electronics and LAr low-voltage powering system [28, 29].

The muon system will be significantly upgraded during the LS3 [30]. The trigger and readout electronics for the RPC, TGC, and MDT chambers will be replaced to make them compatible with the higher trigger rates and longer latencies necessary for the new level-0 (L0) trigger. To maintain high trigger efficiency, new RPC chambers with increased rate capability will be installed onto the inner MDT chambers of the barrel. Due to limited space in the small sector of the barrel, the present MDT chambers will be replaced with integrated RPC and sMDT stations that fit in the MDT envelope. In the barrel to end-cap transition region, currently installed TGC doublet chambers will be replaced with so-called triplet chambers with finer readout granularity. In addition, the low-voltage and high-voltage power system of the muon spectrometer will be replaced, to ensure safe and reliable operation through the full operation period of the HL-LHC.

1.3.2 The Inner Tracker

Due to expected sensor and front-end electronics performance degradation, the ATLAS tracking system will be completely replaced during the LS3. The new complete silicon tracking system, called Inner Tracker (ITk), will be composed of:

- the Pixel Detector [31], consisting of five barrel layers (L0-L4), starting at a radius of 3.4 cm (L0) from the beam line, and multiple inclined or vertical ring-shaped end-cap disks, extending the coverage to $|\eta| < 4.0$;
- the Strip Detector [32], consisting of four strip module layers in the barrel region starting at a radius of 40.0 cm from the beamline and six disks in the end-caps, covering a pseudorapidity of $|\eta| < 2.7$.

The schematic depiction of the ITk Layout is shown in Figure 1.5.

ITk Pixel Detector

The design of the ITk pixel detector was driven by requirements for the position resolution, channel occupancy and radiation hardness. The new pixel detector will have a total active surface of around 13 m^2, which is approximately one order of magnitude larger than the current pixel detector. The Max-Planck-Institut für Physik (Werner-Heisenberg-Institut), referred to as MPP, proposed the thin pixel sensor technology [34] and was one of the main drivers of its development [35]. This technology allows to overcome the problems that occur when operating thick detectors, as those of the current pixel detector, after the irradiation, such as the high full-depletion voltage and leakage current. Two n$^+$-in-p sensor technologies, with not only lower thickness, but also reduced pixel size compared to the current pixel detector, will be used for the ITk pixel modules:

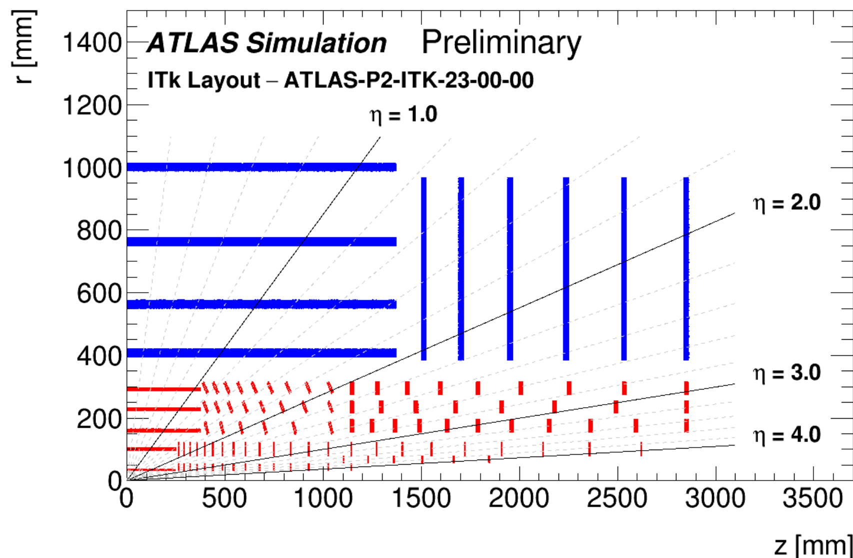


Figure 1.5: The layout of active elements in one half of the ITk detector in the r-z projection [33]. The pixel detector is shown in red and the strip detector in blue.

- Single-chip 3D sensors are chosen for the innermost layer (L0) due to their radiation tolerance. Each sensor is 2×2 cm^2 in size and has 150 µm active thickness with 100 µm support wafer. Two pixel layouts are chosen: 50×50 µm^2 and 25×100 µm^2, both with a single collection electrode in the center.
- Four-chip planar sensors are planned for L1-L4. Each of these quad sensors is 4×4 cm^2 in size, with a sensor thickness of 100 µm in L1 and 150 µm in all other layers. The chosen pixel layout is 50×50 µm^2 throughout.

Due to the high particle fluence up to $2{\cdot}10^{16}$ n_{eq}/cm^2, expressed in the unit of 1 MeV neutron equivalent (n_{eq}) fluence, and total ionizing dose (TID) of 10 MGy, the two innermost layers are designed to be replaceable. The readout chip is developed by the RD53 Collaboration as a common chip for the ATLAS and CMS pixel detectors, and it evolved from the prototype RD53A to the final ATLAS version called ITkPix.

An important aspect to be considered in the detector design is the material budget, which impacts the tracking performance. To minimize the material budget, the assembled modules in the detector will be attached to and supported by light-weight carbon-based structures which have high thermal conductivity. The cooling of the modules is done using CO_2 circulating through titanium tubes integrated into these carbon structures. The cable mass, as a major contributor to the material budget, is reduced using link sharing and a serial powering scheme to operate the pixel modules.

During the production, about 10 000 pixel modules will be assembled using custom-built tools. The MPP, will contribute to the production of the L1 modules. The details of the sensor and front-end electronics design, as well as the module assembly, are given in Chapter 3.

2 Semiconductor tracking devices

Particles created in the collisions have to be detected. The determination of their charge, momentum and energy allows particle identification. Modern collider experiments combine several detector types specialized for high-precision measurement of one or few particle properties as introduced for the ATLAS detector in Section 1.2.

Tracking detectors play a crucial role in any modern high energy physics experiment since they allow the determination of particle trajectories. With known particle trajectory, the information about their momentum, charge and origin can be deduced, allowing the identification of particles belonging to a single interaction. Therefore, the requirement for such detectors is to have a good spatial resolution. To minimize multiple scattering that impacts the measurement precision, these detectors should also have low material budget, i.e. the amount of material present in the detector expressed in fractions of radiation lengths.

There are two main types of tracking detectors, gaseous and semiconductor detectors, both based on the collection of the ionization charge. Both types are typically placed in a magnetic field which allows the measurement of the momentum by determining the curvature radius. In the transverse plane, the momentum of a particle can be determined as:

$$p_{\mathrm{T}}[\mathrm{GeV}] = 0.3 \cdot z \cdot B[\mathrm{T}] \cdot r[\mathrm{m}], \tag{2.1}$$

where B is the magnetic field, r is the radius of the curvature, and z is the charge of the particle expressed in the units of the elementary charge. Although more expensive compared to the gaseous tracking detectors, which are used in the muon systems of LHC experiments, semiconductor tracking detectors have several advantages which make them an ideal type of detector to be operated near the interaction point. These are the high granularity and radiation hardness, in combination with low average energy needed to create one electron-hole pair and high charge mobility that allows short collection times and thus fast readout.

In this chapter, the properties of semiconductor devices and their application in high energy physics experiments are presented. Section 2.1 gives an overview of the general properties of semiconductors, in particular, silicon as the preferred material for collider experiments. The silicon sensors, installed in the innermost layer of the LHC experiments are exposed to high radiation, which leads to severe damage in the sensor material. Taking this into account, sensors can be designed to withstand a high radiation dose. However, significant changes in their properties are observed. Therefore, Section 2.2 gives an overview of the effects introduced by radiation damage in silicon, as well as the changes of the sensor properties.

2.1 General properties

Based on the arrangement of their constituents, solid state materials can be divided into two categories: **amorphous**, with randomly placed atoms and **crystalline**, whose constituents are arranged in highly ordered microscopic structure, forming a crystal lattice that extends in all directions. Unlike free atoms with discrete energy levels, in lattice structures atomic orbitals of the constituents start overlapping resulting in the formation of the energy bands, that are used to describe the electrical properties of the material.

The probability of the occupancy of a specific energy state E in the band at thermodynamic equilibrium can be expressed using the Fermi-Dirac distribution:

$$f(E) = \frac{1}{e^{\frac{(E-E_\mathrm{f})}{k_\mathrm{B}T}} + 1}, \tag{2.2}$$

where k_B is the Boltzmann constant, T the absolute temperature and E_f the Fermi energy, at which the probability of occupancy is:

$$f(E = E_\mathrm{f}) = \frac{1}{2}. \tag{2.3}$$

All energy levels up to E_f are filled at the temperature of $T = 0$ K. At higher temperatures, electrons can occupy excited states above the Fermi level. The highest energy band completely filled with electrons at the absolute zero temperature is called the *valence band*, while the next energy band, partially filled with electrons is called the *conduction band*, since here electrons can move freely within the crystal lattice, contributing to the conductivity of the material. The Fermi energy level for materials without impurities lies in the middle between the valence E_v and conduction E_c bands:

$$E_\mathrm{f} \approx \frac{E_\mathrm{v} + E_\mathrm{c}}{2}. \tag{2.4}$$

The valence, conduction and Fermi levels have different configurations for conductors, semiconductors and insulators as illustrated in Figure 2.1. If the valence and conduction bands overlap, the material has free charge carriers even at $T = 0$ K and is called a conductor. If the Fermi level lies above the valence band and energy gap E_g (the difference between the energy of the conduction and valence band) is too large for electrons to be thermally excited into the conduction band even at higher temperatures, such a material is considered an insulator.

There is a third type of material, that is in the focus of this thesis, whose E_g is much smaller than those of insulators, allowing thermally excited electrons to jump from the valence into the conduction band, leaving a hole behind. Such materials are called **intrinsic semiconductors** and are characterized by equal concentrations of electrons and holes. The resistivity ρ of the material depends on the concentrations of the electrons (n) in the conduction bands and the holes (p) in the valence band as well as their respective mobilities $\mu_\mathrm{e,h}$:

$$\rho = \frac{1}{e(n\mu_\mathrm{e} + p\mu_\mathrm{h})}. \tag{2.5}$$

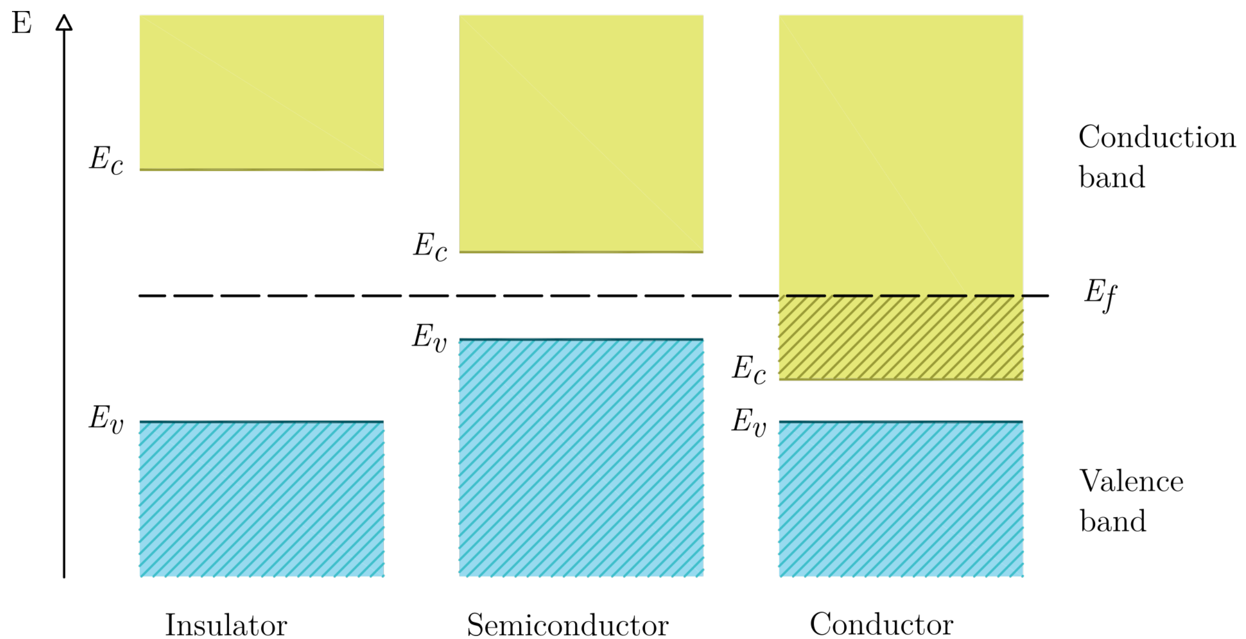


Figure 2.1: Energy band configuration for insulators, semiconductors and conductors.

The most commonly used semiconductor materials are silicon and germanium. Although the E_{g} for germanium ($E_{\mathrm{g}} = 0.74$ eV) is smaller than that of the silicon ($E_{\mathrm{g}} = 1.12$ eV) leading to the lower mean ionization energy, silicon is the preferred material in modern collider experiments. It is the most intensively studied semiconductor, whose electrical properties are well known, available in large quantities and has well-developed processing due to the progress in the microelectronics industry. Since the detector technology in the ITk is based on silicon, the following sections are discussing the properties of this material.

2.1.1 Extrinsic semiconductors

The electrical conductivity of the semiconductor can be modified by replacing the silicon atoms in the crystal lattice with the impurity elements in a process known as **doping**. Added elements create additional energy levels within the band gap, as shown in Figure 2.2.

By adding pentavalent impurities (like phosphorus) to the silicon, a new so-called donor energy level (E_{D}) is formed close to the conduction band. The energy difference between the newly formed energy level and the conduction band is smaller than that of intrinsic semiconductors (0.045 eV for phosphorus [36]), therefore electrons occupying this level can be easily excited into the conduction band. This type of material is referred to as n-type silicon with electrons as majority charge carriers.

Addition of the trivalent impurities (like boron) to the silicon results in the formation of an additional energy level known as the acceptor energy level (E_{A}) close to the valence band. These states can be easily occupied by the valence electrons, due to the small energy

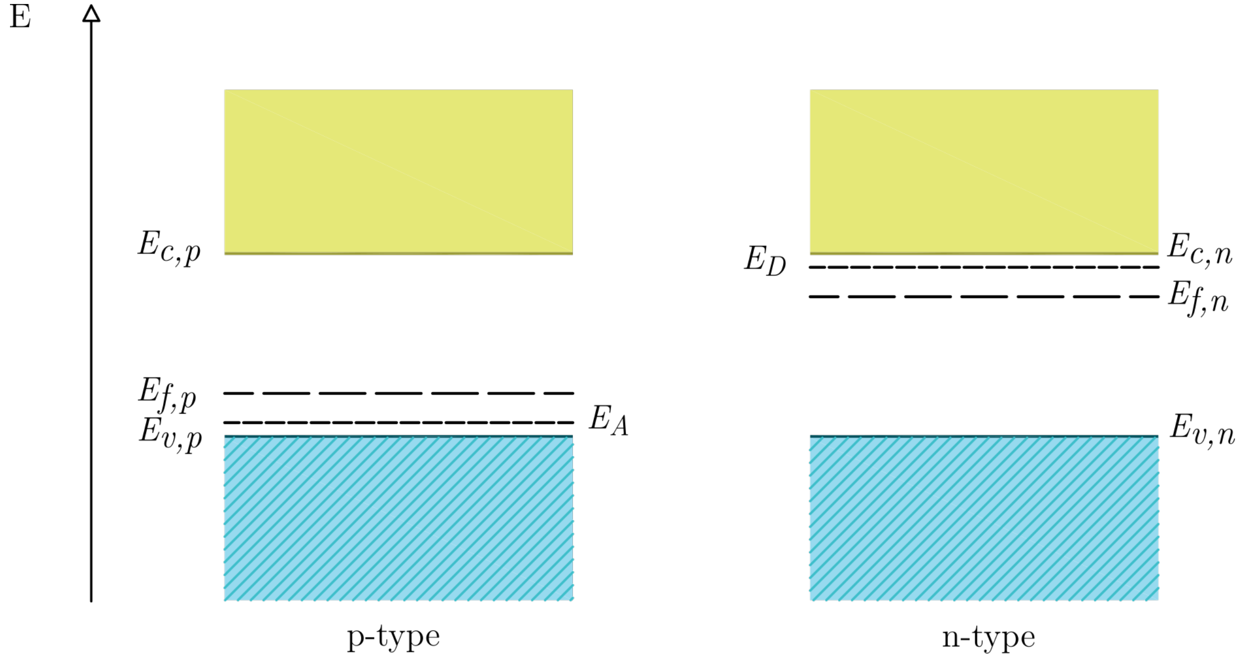


Figure 2.2: An illustration of the different energy levels in p-type and n-type silicon.

difference between two energy levels (0.045 eV for boron [36]). This process creates p-type silicon with holes as majority charge carriers.

The doping process alters the Fermi level, in a way that it is closer to the conduction band for n-type silicon and closer to the valence band for p-type silicon. The process of doping is an industrial method, that can be applied with different concentrations and a submicron precision, suitable for the sensor design.

2.1.2 The pn-junction

The pn-junction is formed when one piece of each p-type and n-type silicon are joined together as illustrated in Figure 2.3.

Free charge carriers of one type drift towards the location with the lower charge carrier concentration via diffusion, where they recombine with the charges of the opposite sign until the Fermi levels in differently doped regions are identical. Since the positive donor ions in the n-side and negative acceptor ions in the p-side are non-mobile, an electric field builds up preventing further charge carrier flow and equilibrium is established. The region where the electric field exists is known as the depletion region. The potential within the pn-junction can be calculated by solving the Poisson equation:

$$\Delta\phi = -\frac{\rho}{\epsilon_0\epsilon_{\mathrm{Si}}} = \frac{qN_{\mathrm{eff}}}{\epsilon_0\epsilon_{\mathrm{Si}}}, \quad N_{\mathrm{eff}} = N_{\mathrm{A}} - N_{\mathrm{D}} \tag{2.6}$$

where ρ is charge density, ϵ_0 is vacuum permittivity, and $\epsilon_{\mathrm{Si}} = 11.75$ is the dielectric constant for silicon. The effective doping concentration N_{eff} is defined as the difference of the acceptor and donor concentrations in respective regions.

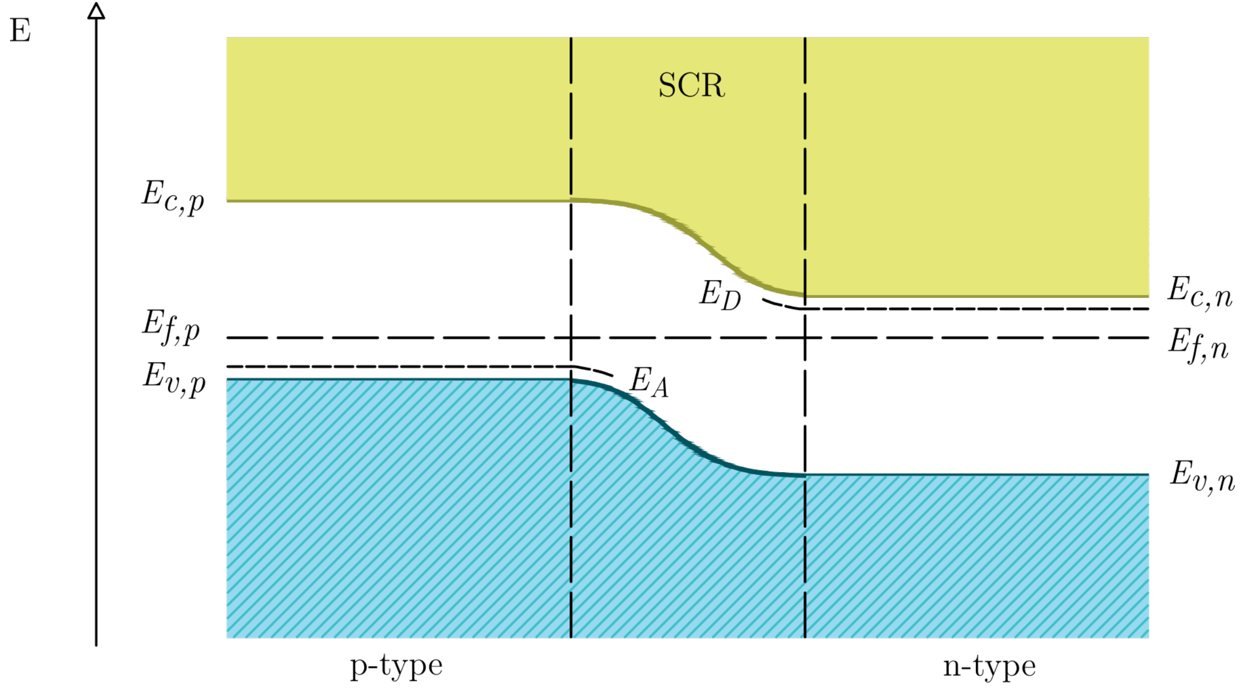


Figure 2.3: A schematics of a pn-junction with indicated different energy levels where p–type and n–type silicon states are indicated by the indices p and n.

The voltage corresponding to the potential difference is called built-in voltage V_{bi} and in the case of constant doping concentrations on both sides it can be written as [36]:

$$V_{\mathrm{bi}} = \frac{k_{\mathrm{B}}T}{\mathrm{e}} \ln\left(\frac{n_{0,\mathrm{n}} \cdot p_{0,\mathrm{p}}}{n_{\mathrm{i}}^2}\right) \approx \frac{k_{\mathrm{B}}T}{e} \ln\left(\frac{N_{\mathrm{D}} \cdot N_{\mathrm{A}}}{n_{\mathrm{i}}^2}\right) \tag{2.7}$$

where $n_{0,\mathrm{n}}$ is the electron concentration in the n-doped side, $p_{0,\mathrm{p}}$ is the hole concentration in the p-doped side, and n_{i} is the intrinsic concentration. If complete ionization of donors and acceptors is assumed, the electron and hole concentration can be replaced by the concentration of donors and acceptors. Typical built-in voltages are of the order of milivolts, creating a depletion region of only few microns thickness.

2.1.3 Depletion voltage and leakage current

The width of the depletion region can be altered by applying an external voltage. Applying the voltage in the same direction as the built-in voltage results in the removal of further charge carriers and therefore the depletion region extends. This operational mode is suitable for particle detectors since the current from free charge carriers is minimized, allowing to measure the signal created by the traversing particle. The depletion region serves as an ionization chamber for incoming particles that produce electron-hole pairs along their trajectories. The total width of the depletion region can be calculated under the same

assumptions used for Eq. 2.7 as [36]:

$$W = \sqrt{\frac{2\epsilon_0\epsilon_{\mathrm{Si}}}{e}\Big(\frac{1}{N_{\mathrm{D}}} + \frac{1}{N_{\mathrm{A}}}\Big)(V + V_{\mathrm{bi}})}, \tag{2.8}$$

where V is the externally applied voltage. For silicon sensors, the junction can be realized as a shallow and highly-doped implant in a low-doped bulk material. Therefore, the width of the depletion region, in this case, is expressed as:

$$W \approx \sqrt{\frac{2\epsilon_0\epsilon_{\mathrm{Si}}}{eN}V}, \tag{2.9}$$

where N is the dopant concentration of the low-doped side of the junction, and the typically low built-in voltage is neglected. For the sensor operation, it is beneficial for the depletion region to extend over the entire thickness of the sensor. The voltage required to achieve this is called full depletion voltage V_{fd} and is typically much larger than the built-in voltage.

For a reverse biased pn-junction, in the absence of radiation, there is always a **leakage** or **dark current** that can be divided into surface and bulk currents. The bulk current I_{b} is caused by the thermally generated charge carriers in the depletion region and therefore depends on its volume. The bulk current is also strongly dependent on the temperature T according to:

$$I_{\mathrm{b}} \propto T^2 e^{-E_{\mathrm{g}}/2k_{\mathrm{B}}T}. \tag{2.10}$$

The surface current contribution emerges when the depleted region reaches the wafer surface and is usually small compared to the bulk current. Increasing the bias voltage to very high values creates additional electron-hole pairs, leading to an avalanche process, due to which the leakage current exponentially increases resulting in a **breakdown** that defines an operational voltage limit for a device.

2.1.4 Charge generation

A charged particle traversing through a semiconductor creates electron-hole pairs along its trajectory. At 300 K the average energy needed for the creation of one such pair for silicon is 3.65 eV. At intermediate energies of incoming particles, the mean energy loss along the path of a charged particle traversing the material is described by the Bethe-Bloch formula [37]:

$$-\langle\frac{dE}{dx}\rangle = Kz^2\frac{Z}{A}\frac{1}{\beta^2}\Big[\frac{1}{2}\ln\frac{2m_{\mathrm{e}}c^2\beta^2\gamma^2T_{\mathrm{max}}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2}\Big], \tag{2.11}$$

with $K = 4\pi N_{\mathrm{A}} r_{\mathrm{e}}^2 m_{\mathrm{e}} c^2$. Here N_{A} is the Avogadro constant. For an absorber, the atomic number is represented with Z and the mass number with A (for silicon $Z_{\mathrm{Si}} = 14$ and $A_{\mathrm{Si}} = 28$). The term $m_{\mathrm{e}}c^2 = 0.511$ MeV is the rest energy of the electron, β is the velocity of the traversing particle in natural units and $\gamma = 1/\sqrt{(1-\beta^2)}$ is the Lorentz factor. The term $\delta(\beta\gamma)$ is the density effect correction to the ionization energy loss, and I is the mean excitation energy (173 eV for silicon). Since energy loss is a stochastic

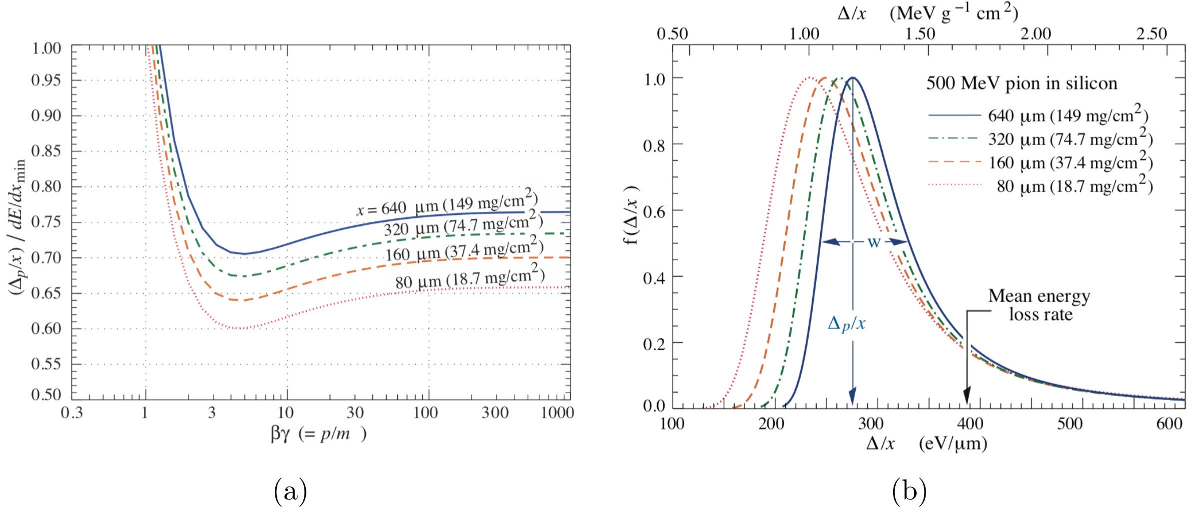


Figure 2.4: Figure a) shows the most probable energy loss in silicon scaled to the mean loss of a minimum ionizing particle of 388 eV/µm (1.66 MeVg^{-1}cm^2). Figure b) shows an example of the most probable energy loss of 500 MeV pions in silicon detectors of different sensor thicknesses, normalized to unity at the most probable value Δ_p/x. The quantity w is the full width at half maximum. Both images are taken from Ref. [37].

process, there is a non-zero probability that the incident particle will interact with an orbital electron of an atom and release an electron with a significant kinetic energy that can cause secondary ionizations, δ-electrons or δ-rays. The quantity T_max corresponds to the maximum energy transfer possible in a single collision. In high energy physics experiments, the signal generation for most of the charged particles is approximated by the one of a MIP (Minimum Ionizing Particle) corresponding to $\beta\gamma \approx 3-4$, which can pass through the full active thickness of a silicon tracking detector. Below this point the term $1/\beta^2$ dominates and the mean energy loss decreases with increased energy. Above this point, the logarithmic term leads to a slow rise. The example of the most probable energy loss scaled to the mean loss at minimum ionization for several silicon sensor thicknesses is shown in Figure 2.4a.

The energy loss is subject to large fluctuations. Therefore, for a sensor of thickness x, the probability distribution of energy loss is approximated by the Landau-Vavilov distribution with the Most Probable Value (MPV), denoted by Δ_p:

$$\Delta_\mathrm{p} = \xi\Big[\ln\frac{2m_\mathrm{e}\beta^2\gamma^2}{I} + \ln\frac{\xi}{I} + 0.200 - \beta^2 + \delta(\beta\gamma)\Big]. \tag{2.12}$$

Here ξ is the ratio of sensor thickness and β. The long tail of the Landau-Vavilov distribution is due to the generation of δ electrons, whose directions are typically perpendicular to the trajectory of the incoming particle. The emission of the δ electrons leads to the average energy loss higher than the most probable value Δ_p of the distribution, and contributes to the creation of large clusters and thus degrades the spatial resolution of the detector. The fluctuations around the maximum of this distribution are larger for thinner sensors [36].

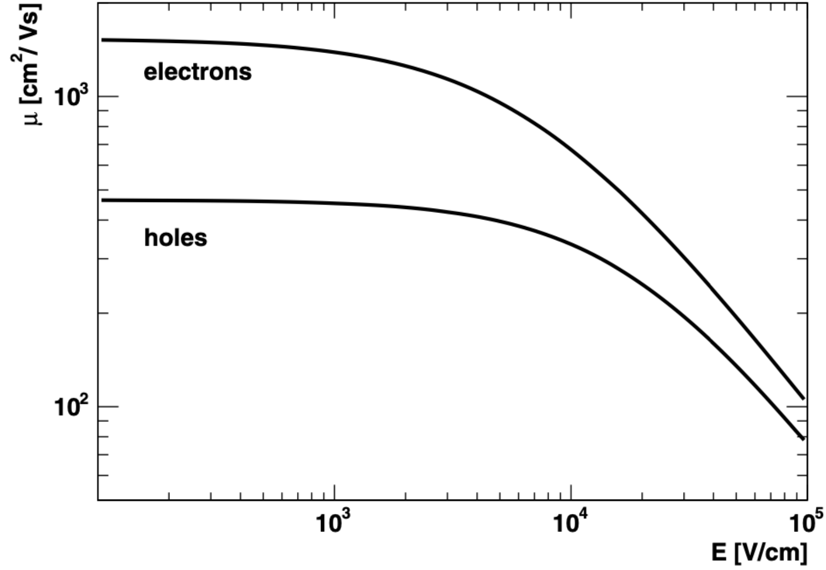


Figure 2.5: Mobility of electrons and holes as a function of an electric field. The image is taken from Ref. [36]

The examples for 500 MeV pions traversing thin silicon detectors of various thicknesses are shown in Figure 2.4b.

2.1.5 Signal formation

Applying the reverse bias voltage to the sensor creates an electric field $\vec{E}$ which causes the drift of the free charge, created by the passing particle, to the electrodes with the velocity:

$$\vec{v_{\mathrm{e,h}}} = \mu_{\mathrm{e,h}}\vec{E}. \tag{2.13}$$

This expression is true in regions of low electric fields. At higher fields, the drift velocity does no longer depend linearly on the electric field, but reaches a saturation value v_{s}. This effect, known as "mobility degradation", can be described by parametrizing the mobility as a function of the electric field [38]:

$$\mu = \frac{v_{\mathrm{s}}/E_{\mathrm{C}}}{[1 + (E/E_{\mathrm{C}})^{\beta}]^{1/\beta}}, \tag{2.14}$$

with E_{C} and β fitting parameters. The electron and hole mobilities resulting from Eq. 2.14 are shown in Figure 2.5. The mobility of electrons is three times that of holes, making holes more prone to trapping (Section 2.2.2), especially in the case of irradiated silicon sensors.

According to the Shockley-Ramo Theorem [39, 40], the movement of charges induces a current at the electrodes:

$$i = \mathrm{e}\vec{v} \cdot \vec{E_{\mathrm{W}}}, \tag{2.15}$$

where $\vec{E_{\mathrm{W}}}$ is the weighting field which can be obtained by applying a unit potential to the electrode of interest, while keeping all others at zero potential. The total induced charge Q is obtained by integrating the current over the collection time.

During the drift to the electrodes, electrons and holes are also subject to random movements, due to the gradients in the carrier concentrations within the material, which leads to the diffusion of the charge cloud. The lateral extent of this cloud after the total drift time t is given by:

$$l_{\mathrm{D}} = \sqrt{2Dt}, \tag{2.16}$$

where D is the diffusion constant related to the absolute temperature and mobility as:

$$D = \mu \frac{k_{\mathrm{B}} T}{e}. \tag{2.17}$$

This can cause the spread of the induced signal over several electrodes in the case of segmented semiconductors.

2.2 Radiation damage in silicon detectors

The high radiation doses, to which silicon detectors in the collider experiments are usually exposed to, induce considerable damage of the sensor and readout electronics. This damage is more severe at hadron colliders, like the LHC, than at electron-positron colliders due to the higher particle flux. As the final result, the detector performance is altered, which is why the radiation hardness is a vital parameter to be considered when designing a detector.

2.2.1 Sensor damage mechanisms

The energy and momentum transfer of highly energetic hadrons to the atoms of the sensor material are the main source of sensor damage, that can be divided into bulk and surface damage. Surface damage is caused by ionizing radiation and occurs at the interface layer between the bulk and silicon oxide layer (the details of the sensor layout are given in Section 3.1). Ionizing radiation generates electrons that will diffuse outside of the oxide layer with holes remaining due to their smaller mobility. This creates a positive charge density at the sensor surface which attracts the electrons, leading to a compensation of the doping concentration between the pixel implants.

Bulk damages are the main reason for the performance deterioration of silicon sensors in collider experiments. High energetic particles, predominately charged hadrons and neutrons, will not only interact with electron clouds, but also with the nuclei, resulting in crystal imperfections that can be electrically active and impact the electric properties of the material. Depending on the energy of the incoming particle, multiple types of point defects can occur, as illustrated in Figure 2.6. The momentum transfer of an incoming particle to a silicon nuclei can displace this atom from the crystal lattice, creating a vacancy.

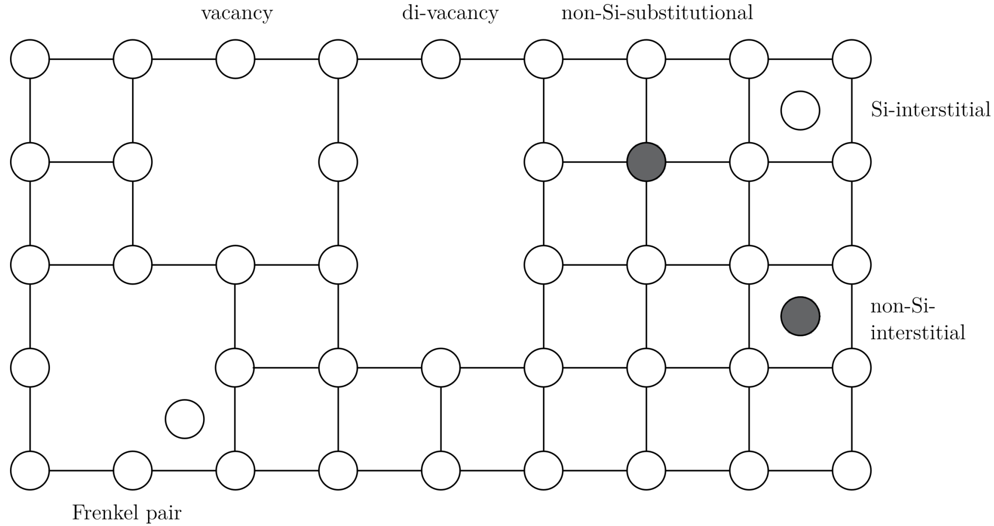


Figure 2.6: An illustration of different elementary defects in the silicon crystal lattice: vacancies, Frenkel pair, non-Si-substitutional, and interstitials of Si and non-Si type.

In the case of a high momentum transfer, the hit silicon atom can propagate through the lattice and cause more defects on its way. When it reaches the end of its path, this atom can get trapped between the lattice atoms (Si-interstitial), or close to a vacancy (Frenkel pair) for a low momentum transfer. In addition, the dopant atoms or atoms from other sensor parts can be dislocated, causing impurities in the lattice structure (non-Si-substitutional) or in-between the lattice atoms (non-Si-interstitial).

To compare the damages caused by particles of different types and energies, the radiation damage is scaled with the **Nonionizing energy loss (NIEL)**, where neutrons of 1 MeV are used as reference particles. The fluence of an arbitrary type of radiation Φ is expressed as an equivalent fluence of 1 MeV neutrons Φ_{eq} that would create the same damage:

$$\Phi_{\text{eq}} = \kappa\Phi, \tag{2.18}$$

where κ is the energy-dependent hardness factor of a certain type of particle.

2.2.2 Effects on sensor performance

The macroscopic properties of the silicon detectors are altered by the discussed radiation damage processes. Surface damage affects the inter-pixel capacitance and resistance, which can affect the sensor behavior in terms of cross-talk between pixels and an increase in noise, and thus has to be taken into account in the sensor design. The bulk damage is the main challenge for the detectors used in hadron collider experiments. The bulk defects in silicon detectors create additional energy levels in the band gap, resulting in three main effects: an increase in the leakage current, a change of the space charge in the depletion region, and charge trapping.

Leakage current

Energy levels created by defects that are close to the middle of the band gap act as generation-recombination centers, leading to a higher probability for electrons to be excited into the conduction band, resulting in an increase of the leakage current [36]:

$$\frac{\Delta I_{\mathrm{vol}}}{V} = \alpha\Phi. \tag{2.19}$$

Here V is the depleted volume and α is the current-related damage rate, which is independent of the initial resistivity of the silicon, the dopant concentrations, the production process of the silicon and the type of irradiation [41]. Eq. 2.10 expresses the temperature dependence of the leakage current. In the case of irradiated sensors, the leakage current can be in the range of mA even for temperatures below 0°C. Applying the high voltage will cause a significant power dissipation and self-heating of the device, potentially resulting in a *thermal runaway*. To avoid this effect, a highly efficient cooling system is of large importance for irradiated sensors.

Effective doping

Radiation-induced bulk defects behave as acceptors and change the initial effective doping concentration of the sensors as $N_{\mathrm{eff},0} = N_{\mathrm{D},0} - N_{\mathrm{A},0}$. Using the following parametrization, the resulting effective doping N_{eff} is expressed as a function of the received fluence Φ [42]:

$$N_{\mathrm{eff}}(\Phi) = N_{\mathrm{D},0}e^{-c_{\mathrm{D}}\Phi} - N_{\mathrm{A},0}e^{-c_{\mathrm{A}}\Phi} - b\Phi, \tag{2.20}$$

with the removal constants c_{D} and c_{A}, and b as the acceptor production rate. In this formula the generation of the donor states is neglected. Depending on the doping type, one of the initial doping concentrations, $N_{\mathrm{D},0}$ or $N_{\mathrm{A},0}$ is negligible. In the case of p-type silicon, N_{eff} is negative due to an excess of acceptors, while it is positive for the n-type silicon. The depletion voltage of the sensor of thickness d depends on the absolute effective doping concentration as [36]:

$$V_{\mathrm{fd}} = \frac{e|N_{\mathrm{eff}}|d^2}{2\epsilon_0\epsilon_{\mathrm{Si}}} \tag{2.21}$$

Therefore, for p-type silicon, the radiation causes an increase in the absolute effective space charge concentration, which increases the full depletion voltage. In the case of n-type silicon, initially $|N_{\mathrm{eff}}|$ and V_{fd} decrease until the $N_{\mathrm{eff}} = 0$. Further irradiation causes an increase in $|N_{\mathrm{eff}}|$ (dominated by acceptor-like defects) and the material behaves as p-type silicon. This effect is known as **type inversion** and for typical bulk doping concentrations occurs at a fluence of $\Phi \approx 2 \cdot 10^{12}\ \mathrm{n_{eq}/cm^2}$. The fluence dependency of the effective doping and full depletion voltage for a sensor with initial n-type bulk material is shown in the Figure 2.7.

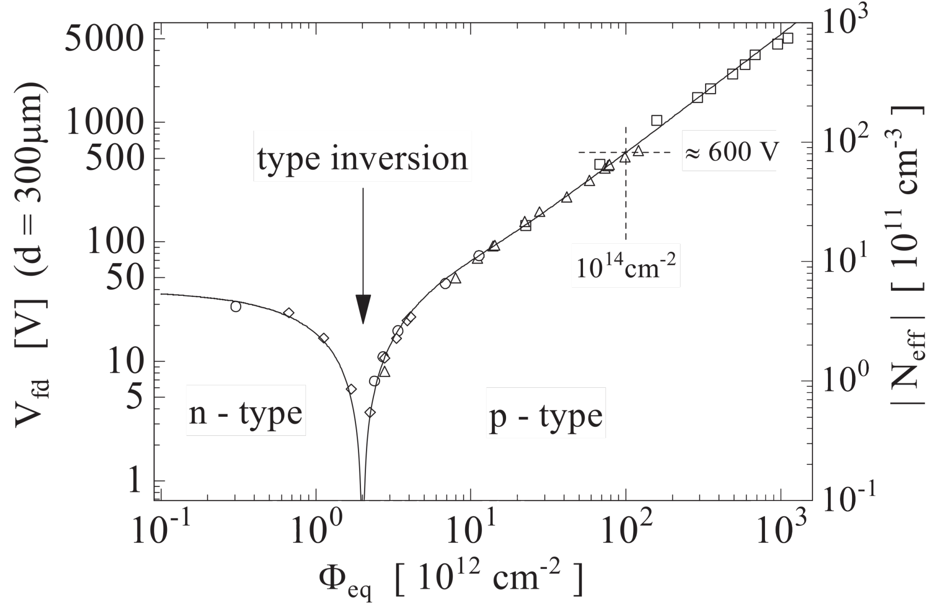


Figure 2.7: The full depletion voltage and effective doping concentration are shown as a function of the fluence for n-type 300 µm silicon sensor. This image is taken from Ref. [42].

Charge trapping

Radiation-induced defects also act as trapping centers and are occupied by charge carriers for times longer than the charge collection time, resulting in a reduced signal in the detector. A parameter that describes trapping is the trapping time τ_{t}, which is inversely proportional to the fluence Φ [42]:

$$\frac{1}{\tau_{\mathrm{t}}} = \frac{1}{\tau_{\mathrm{t},\Phi=0}} + \gamma\Phi, \tag{2.22}$$

where the parameter γ depends on the charge carrier and radiation type. Therefore, charge trapping leads to a reduction in the Charge Collection Efficiency (CCE), which is defined as the ratio of the collected charges after and before irradiation.

2.2.3 Annealing

The primary defects caused by irradiation can move through the crystal lattice and react with other defects or impurities, resulting in a recombination or the formation of new defect structures. This evolution in time of the radiation-induced defects is called *annealing* and is strongly temperature dependent. At room temperature, annealing effects are slow and progress over a timescale of years, while higher temperatures accelerate the process. The impact of the annealing process on the sensor properties is described below.

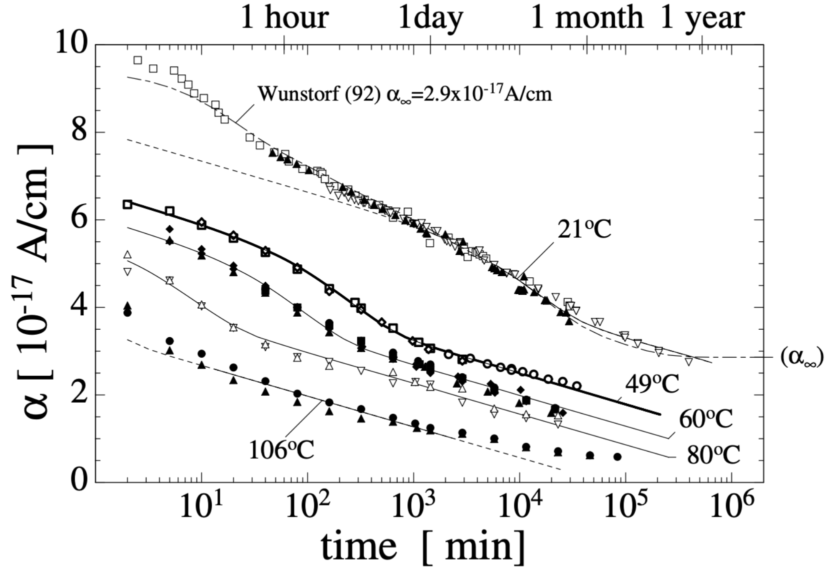


Figure 2.8: Current-related damage rate α as a function of annealing time. This image is taken from Ref. [41].

Leakage current

As shown in Figure 2.8, annealing is beneficial for the current-related damage rate, resulting in a decrease of the leakage current.

Effective doping

The change in the effective space charge concentration induced by the irradiation ΔN_{eff} as a function of annealing time is shown in Figure 2.9 and is described by the so-called Hamburg model as [41]:

$$\Delta N_{\text{eff}}(\Phi, t(T_{\text{a}})) = N_{\text{C}}(\Phi) + N_{\text{A}}(\Phi, t(T_{\text{a}})) + N_{\text{Y}}(\Phi, t(T_{\text{a}})), \tag{2.23}$$

where the time itself depends on the annealing temperature T_{a}. The first term, $N_{\text{C}}(\Phi)$, does not depend on the annealing time and denotes the *stable damage*. The second term, $N_{\text{A}}(\Phi, t(T_{\text{a}}))$, refers to the *short-term* or *beneficial annealing*, for times of the order of a few hours or less. The short-term annealing results in the decrease of the effective space charge concentration and thus the depletion voltage. The last contribution in Eq. 2.23, $N_{\text{Y}}(\Phi, t(T_{\text{a}}))$, is the *reverse annealing*. The long-term reverse annealing describes the increase of the full depletion voltage after some weeks at room temperature. For this reason, irradiated sensors are intentionally kept at room temperature for a short time, during which the depletion voltage decreases. To prevent the reverse annealing phase, they are then stored and operated at temperatures below 0°C.

Charge trapping

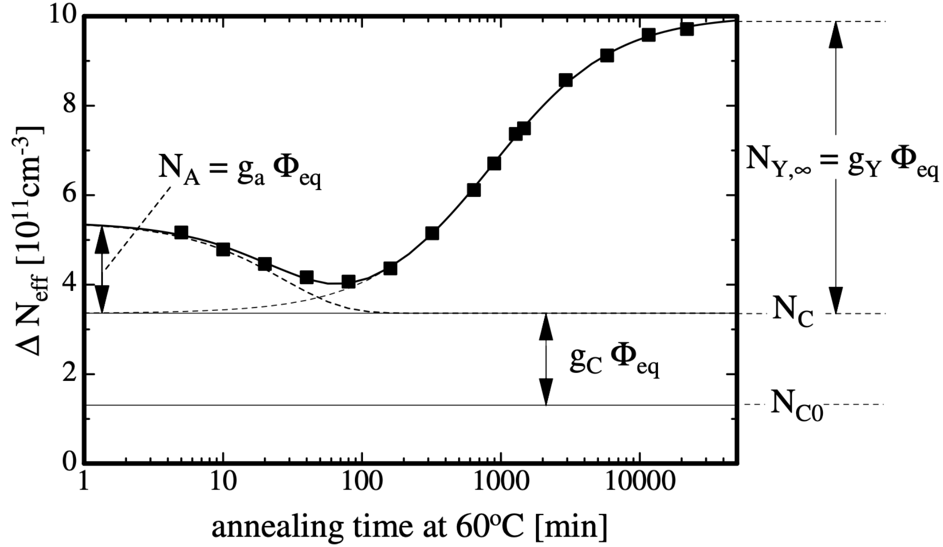


Figure 2.9: Typical annealing behavior of radiation-induced changes of the effective doping concentration. This image is taken from Ref. [41].

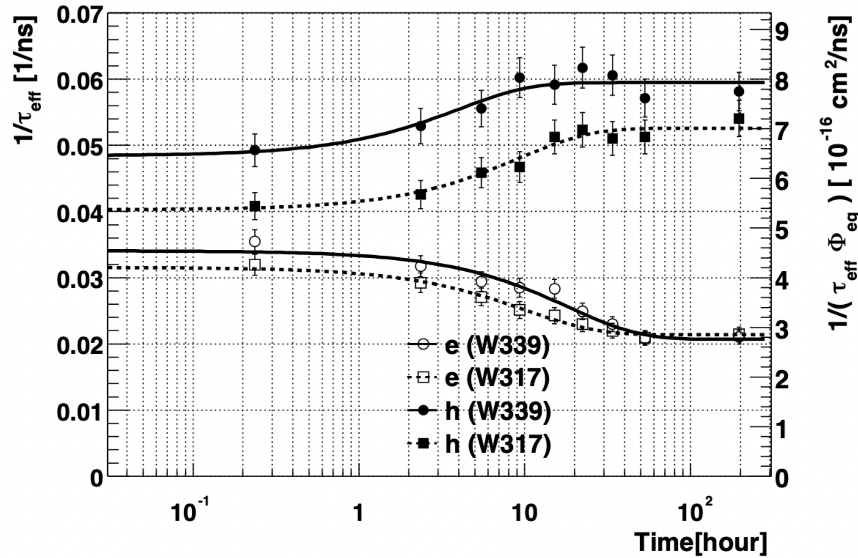


Figure 2.10: Annealing of effective trapping probability of electrons (e) and holes (h) at 60°C. Tested samples are diodes processed on a standard (W339) and oxigen enriched (W317) silicon wafer and irradiated with neutrons to a fluence of $7.5{\cdot}10^{13}$ n_{eq}/cm^2. This image is taken from Ref. [43].

The trapping time constants for electrons and holes as a function of annealing time, introduced in Eq. 2.22, are shown in Figure 2.10, for an annealing temperature of 60°C. The trapping probability increases for holes and decreases for electrons for annealing times of the order of ten hours [43].

3 Pixel modules

The development of segmented silicon detectors started in the 1970s with the need for fast and radiation-hard position detectors for fixed-target experiments in high energy physics. The milestone was reached in 1980 when it was demonstrated that the planar technology from the microelectronics industry can be adapted for detector fabrication [44]. The NA11 and NA32 experiments at CERN were the first to use a set of silicon detectors for precise particle tracking and vertex measurements [45, 46]. Since then, many large experiments have continued to develop and implement silicon detectors into their systems.

The position measurement with silicon detectors is achieved by implant segmentation, either strip-like, allowing a one-dimensional position measurement, or pixel-like, providing a two-dimensional position sensitivity. Each of the implants creates a pn-junction with the bulk of the sensor. The term pitch is used for the distance between implant centers. The implant thickness is usually a few microns, while the sensor thickness can range from 50 µm to a few hundred microns to allow for sufficient charge carrier generation.

Two different technologies are currently used for the production of pixel detectors: *monolithic* and *hybrid*. In monolithic pixel detectors, the readout electronics is implemented into the sensitive sensor volume, which offers the main advantages of reduced material budget and production costs. An example of devices produced in this technology are monolithic active pixel sensors (MAPS) like the Mimosa26 sensors, used for the EUDET-type Beam Telescopes (Section 4.3.2).

An illustration of a hybrid pixel detector is given in Figure 3.1.

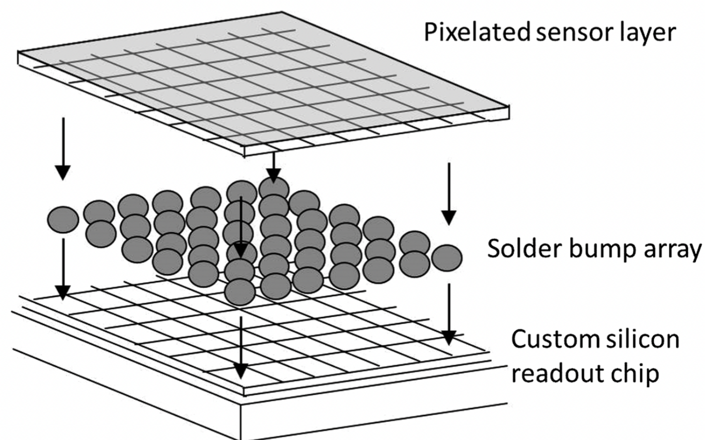


Figure 3.1: Sketch of a hybrid pixel detector. This image is taken from Ref. [47].

A hybrid pixel detector consists of a sensor and a readout chip, fabricated separately and interconnected in a process called *hybridization*. The benefit of the independent fabrication of the sensor and readout chip is the possibility to optimize each process, allowing the production of a large quantity of radiation-hard devices, suitable for operation in high energy physics experiments.

The hybrid technology is chosen for the ATLAS ITk pixel modules. Therefore, in this chapter, the details of the components of the hybrid detectors will be presented. The sensor manufacturing and layout will be discussed in Section 3.1. The front-end electronics and developed ITk pixel readout chips are presented in Section 3.2, while Section 3.3 is dedicated to the assembly procedure of the ITk pixel modules.

3.1 Sensor

The sensor is the sensitive part of a hybrid pixel detector, where the interaction between an incoming particle and the sensor material takes place. Here the pn-junction is usually asymmetric, composed of a lightly doped bulk material with highly doped implants.

The schematic view of one pixel cell, as a basic building block of the hybrid pixel detector, is given in Figure 3.2.

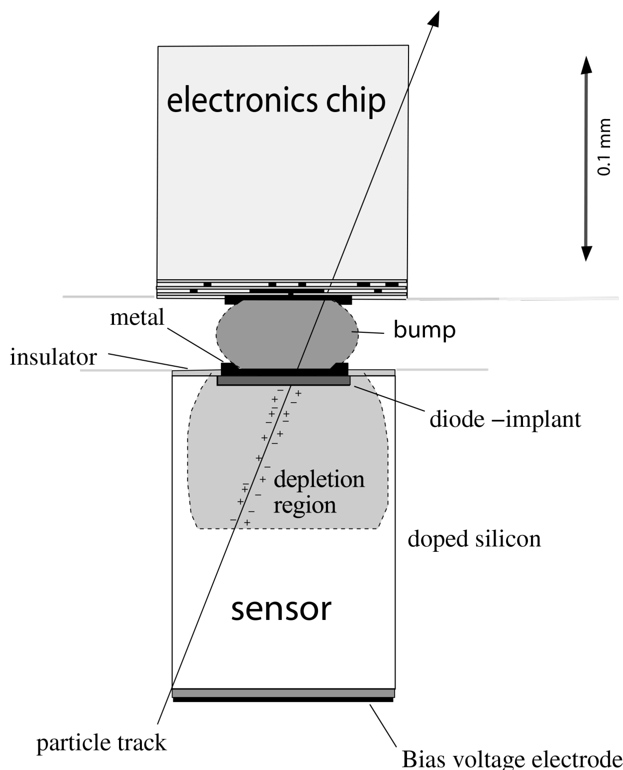


Figure 3.2: Schematic view of one pixel cell of a hybrid pixel detector. This image is taken from Ref. [36].

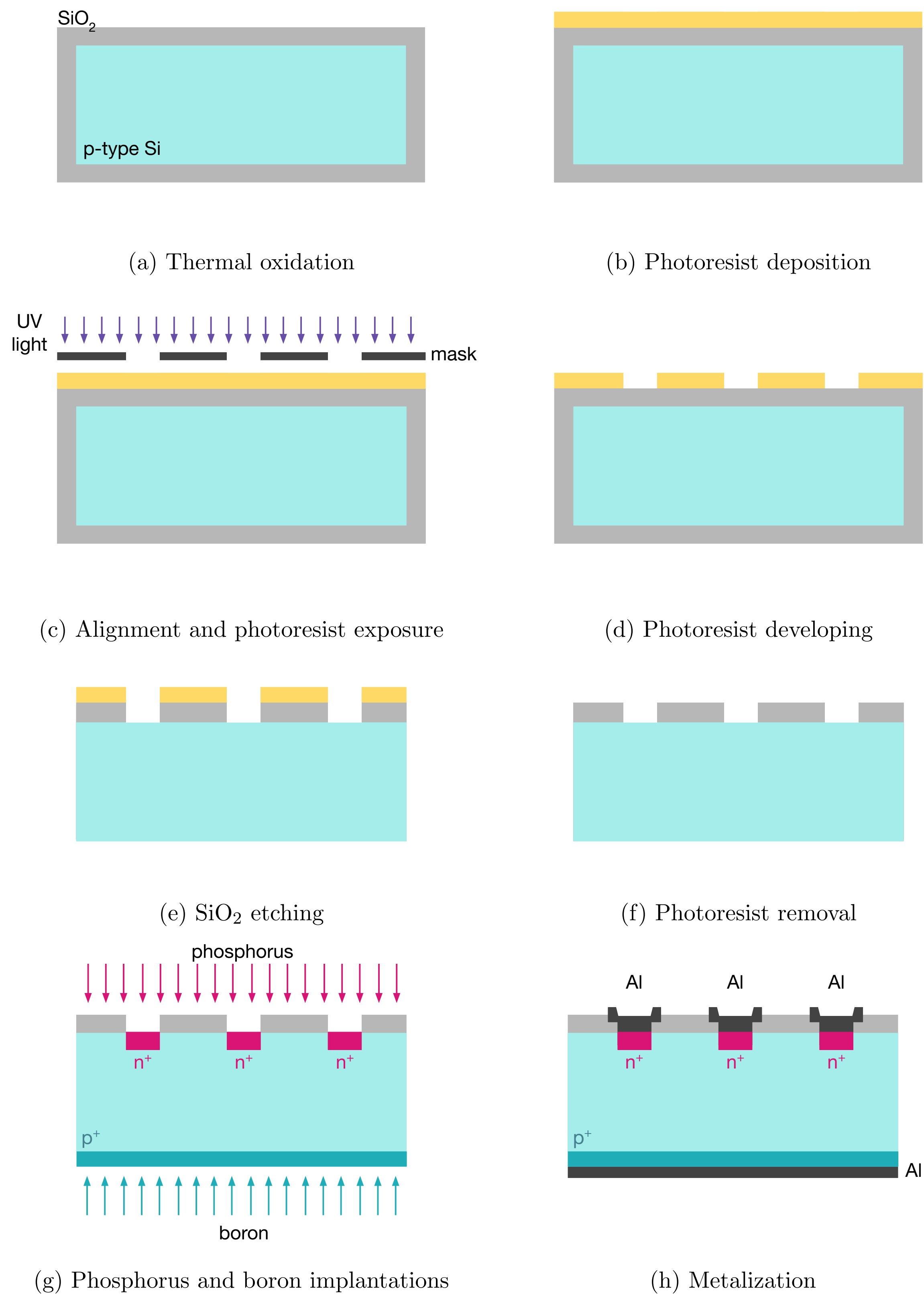
The dimensions of the pixel cell are chosen according to the required spatial resolution. A charged particle traversing the sensor generates electron-hole pairs along its path that, moving in a depletion region due to an electric field, produce a signal. The readout chip is needed to process induced signals and to obtain the hit information used for the reconstruction of the particle trajectory.

3.1.1 Manufacturing of planar sensors

The fabrication technology for silicon detectors is largely based on the planar process developed in the field of microelectronics, which enabled high reproducibility of finely segmented large devices without defects.

The main sensor production steps are illustrated in Figure 3.3 following the procedure introduced in 1980 [48]. The sensor manufacturing starts with detector grade high resistivity p-type silicon ingots, that can be produced by the float-zone (FZ) method, sliced into wafers. The wafer surface is polished to remove all natural oxides, followed by the process of *thermal oxidation* to grow the SiO_2 layer on its top. To achieve segmentation several steps are performed. First, a *photoresist* is deposited on the sensor surface. Then the patterning is performed using *photolithography* by exposing the photoresist to UV light through a mask (usually a chrome pattern on a glass). The mask transfer onto the wafer surface can be done by contact exposure, where the mask is pressed onto the wafer, or projective exposure where the pattern is transferred to the wafer by an optical system. During the development of the photoresist either illuminated areas (positive resist) or non-illuminated areas (negative resist) of the oxide are removed revealing the parts that should be *etched* away. This step is followed by the *implantation* of the pixel implants with the ions of the respective dopant (phosphorus for n-type implants), which are accelerated and shot directly into the silicon wafer at room temperature. Stopped doping atoms are usually not in regular places in the crystal lattice and are not electrically active. In addition, the implantation process damages the crystal lattice. Therefore, every implantation is followed by thermal treatment for electrical activation of the implanted ions and annealing. With this step, the segmentation of the sensor front side is completed. The backside is implanted with boron to form an ohmic contact. In the next step silicon nitride (Si_3N_4) and low temperature oxide (LTO) are deposited on both sides of the wafer and etched away over the n^+ implants to allow for their contact through these electrically insulating layers. The patterning is then performed again using the photoresist to form an aluminium layer over the pixel implants in the *metalization* step. The process is completed with the deposition of a passivation layer for protection against possible sparks that can occur after the interconnection of the sensor and readout chip. The passivation layer is left open in the areas where contacts to the readout chip must be made. For this purpose, the under bump metalization (UBM) layer is grown on the contact pads.

After the electrical tests at wafer level, wafers are diced and sensors are ready for the next step, which is the interconnection with the readout chips.



(a) Thermal oxidation

(b) Photoresist deposition

(c) Alignment and photoresist exposure

(d) Photoresist developing

(e) SiO_2 etching

(f) Photoresist removal

(g) Phosphorus and boron implantations

(h) Metalization

Figure 3.3: Main production steps for n^+-in-p planar pixel sensors, where "+" stands for highly-doped silicon.

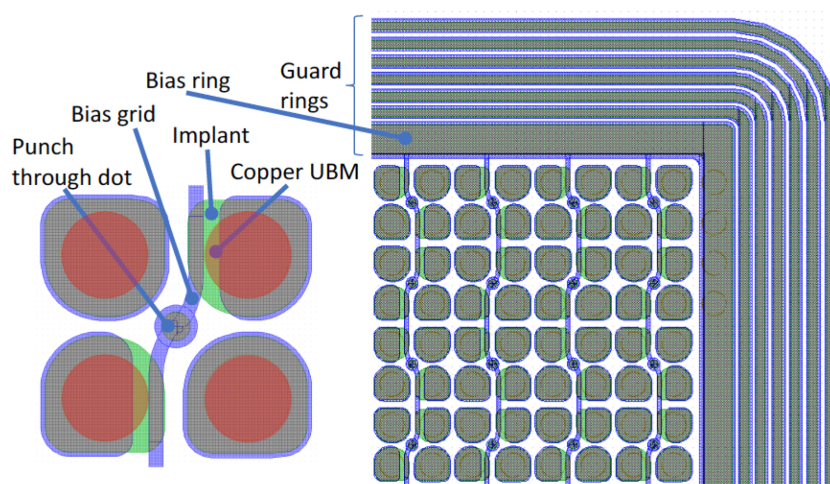


Figure 3.4: Four pixel cells are shown together with an overview of the sensor layout, and indicated guard rings and biasing structures. This image is taken from Ref. [49].

3.1.2 Sensor components

Besides the pixel cell, the sensor contains several additional structures indicated in Figure 3.4 that will be described below.

Guard rings

The cutting edge of the sensor is conductive due to the mechanical damage caused by the cutting procedure and thus is at the backside potential. Extending the depleted region to the cutting edge can cause a sudden increase of the leakage current due to the high electric field, resulting in a pn-junction breakdown. To establish a smooth voltage drop from the cutting edge to the pixel matrix, additional implantations are added in form of rings around the pixel matrix, referred to as *guard rings*. In n^+-in-p sensors, guard rings are implemented on the front side of the sensor. During operation, the backside is at a negative potential. The smoothness of the voltage drop improves with increased number of guard rings, which simultaneously increases the inactive area around the pixel matrix. The number of needed guard rings depends on the maximum bias voltage targeted. A multiple guard ring design allows reaching the kV range for the breakdown voltage. However, the maximum operational voltage is limited by the risk of sparks that will occur due to a too high voltage difference between the closely spaced readout chip almost at the ground potential and the sensor edge.

Biasing structure

The sensor production for a large experiment requires thousands of devices and thus needs to be optimized for a high yield. Therefore, it is crucial to test sensors at wafer level and before interconnection to the readout chip. Tests can be performed only if pixels are at a

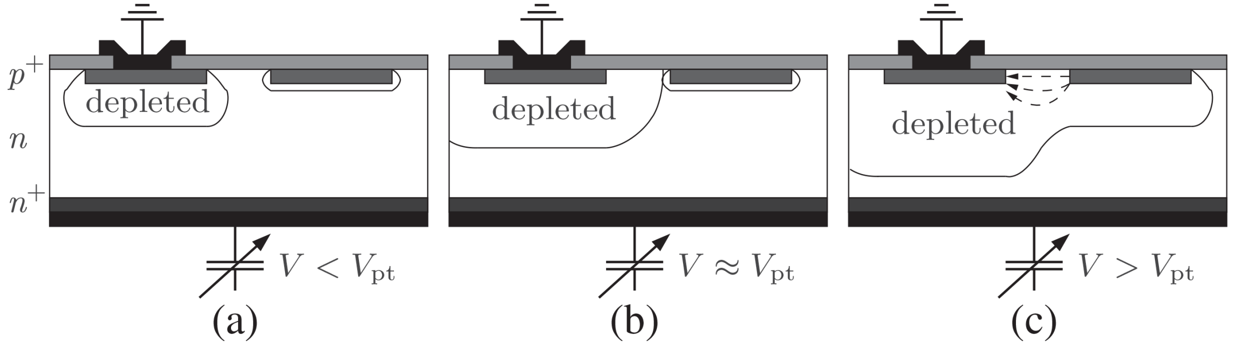


Figure 3.5: An illustration of the punch through effect for a p^+-in-n device. Only the left implant is grounded. The figures are for a) $V < V_{\mathrm{pt}}$, b) $V \approx V_{\mathrm{pt}}$ and c) $V > V_{\mathrm{pt}}$. See text for details. This image is taken from Ref. [36].

definite potential. This can be achieved by implementing a biasing structure in the sensor design.

One of the biasing methods is based on the *punch-through mechanism.* The pixels are grounded through a common implant around the pixel matrix, called *bias ring* and *bias grid* that run between every second column of pixels, as shown in Figure 3.4. The pixel implant itself derives its potential from the adjacent bias rail through a separate circular implant called *bias dot*, which is located either in an opening of the pixel implant itself or nearby. The potential distribution is done via the punch-through effect, which can be explained using Figure 3.5, considering a grounded and a floating implant at different backside potentials. For a backside voltage $V < V_{\mathrm{pt}}$, the floating implant, surrounded by its intrinsic depletion zone, will be at the potential of $V + V_{\mathrm{bi}}$, where V_{bi} is the built-in voltage of the undepleted bulk, while the depletion region of the grounded implant grows. With an increasing value of the backside voltage, the depleted zone of the grounded implant is extending further. The floating implant will be at the backside potential until the depletion region of the grounded implant reaches the floating pixel, which occurs for $V \approx V_{\mathrm{pt}}$. The potential of the floating implant is now determined by the potential of the grounded one. If the voltage is further increased ($V > V_{\mathrm{pt}}$), the potential of the floating implant stays almost constant and its depletion region grows. Charge carriers created in the depletion region are collected by the floating implant and they flow from there to the grounded one. The quantity V_{pt} is called punch-through voltage and depends on the distance between implants and the doping concentrations.

An alternative biasing structure consists of *bias resistors* on top of the pixel implants, connected with a wiggled metal line maximizing the overlap with the implants, as shown in Figure 3.6, or a *temporary metal* layer deposited on the sensor to shorten the pixels at wafer level. As the name indicates, this layer is removed before the interconnection to the readout chip.

Sensors with different biasing structures were studied with test-beams. They are compatible with the ITk requirements and therefore can be used in the final productions [49–51].

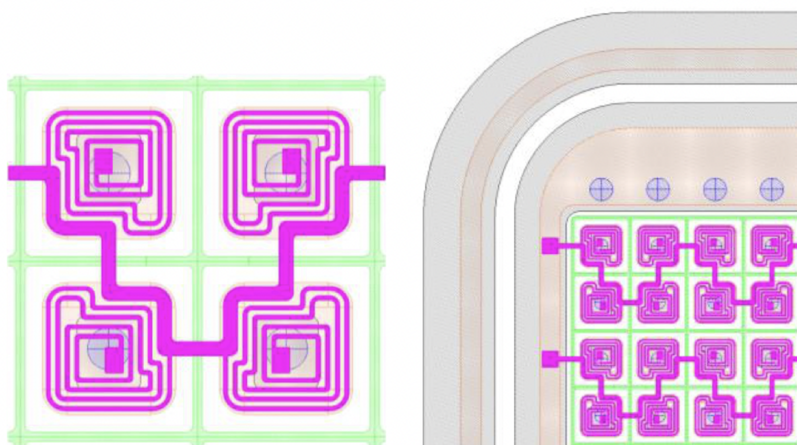
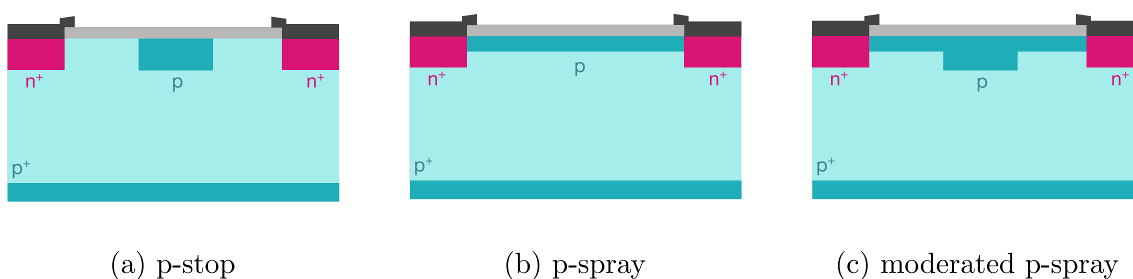


Figure 3.6: Sensor layout with a polysilicon resistor biasing structure. This image is taken from Ref. [50].

Inter-pixel isolation

In n^+-in-p sensors, an electron accumulation layer, induced by the positive charge of the oxide, forms around the implants and will shorten them. This can be prevented using one of the inter-pixel isolation solutions shown in Figure 3.7. The first one is the *p-stop* technique, which requires an additional photolithographic step for p^+ implantations between the n^+ pixels, which increases the fabrication costs. The second solution is the *p-spray* technique, where a thin homogeneous layer of low concentration p-dopant is deposited on the implant side of the silicon wafer, except for the implant region. The p-spray technique offers the advantage of narrow spacing between neighboring implants due to the absence of a photolithographic step and an increase in the breakdown voltage with radiation. To improve the high voltage stability of p-spray devices before irradiation, the *moderated* p-spray technique has been developed where a narrow region with a higher p-spray dose is created in the center between two pixel implants. This technique provides higher breakdown voltage before irradiation compared to the devices where the standard p-spray technique was implemented, while maintaining a good postirradiation performance [52].



(a) p-stop (b) p-spray (c) moderated p-spray

Figure 3.7: Simplified illustration of the three inter-pixel isolation techniques.

3.1.3 Spatial resolution and charge sharing

Spatial resolution is one of the key properties of position-sensitive detectors and is mainly determined by the pixel size. In the simplest case of a pixel sensor with a binary readout, where only information about the fact that a pixel was hit or not exists and no charge sharing information is available, the theoretical expectation for the spatial resolution can be computed if the following assumptions are valid:

- the threshold is adjusted such that only one pixel per track fires;
- the detector is hit by a uniform density of particles over a pixel pitch p, $D(x_{\mathrm{track}}) = 1/p$.

The average difference between the hit position x_{hit} and track position x_{track} for a pixel pitch p_{x} (with center at 0) in the x dimension is determined as [36]:

$$\sigma^2_{\mathrm{int,x}} = \int_{-p_{\mathrm{x}}/2}^{p_{\mathrm{x}}/2} (x_{\mathrm{track}} - x_{\mathrm{hit}})^2 D(x_{\mathrm{track}}) \mathrm{dx}_{\mathrm{track}} = \frac{p_{\mathrm{x}}^2}{12}. \tag{3.1}$$

Therefore, for $x_{\mathrm{hit}} = 0$, the so-called *binary resolution* or *intrinsic resolution* is given by:

$$\sigma_{\mathrm{int,x/y}} = \frac{p_{\mathrm{x/y}}}{\sqrt{12}}. \tag{3.2}$$

When a particle passes through a silicon detector, it produces a number of charge carriers that drift towards the electrodes due to the electric field present. As illustrated in Figure 3.8, these carriers can be collected by more than one electrode (implant) if: a particle passes close to the border of two pixels; an incident angle of the passing particle is such that it crosses the volume of two or more pixel cells or due to the diffusion of the carriers. This effect is called *charge sharing* and results in one or more pixels being fired by the same particle. Charge sharing improves the spatial resolution. A further improvement can be achieved using analog readout, where a signal is proportional to the collected charge. In the region where only one-pixel size clusters occur improved spatial resolution can be achieved by tilting the detector and using the Lorentz deflection.

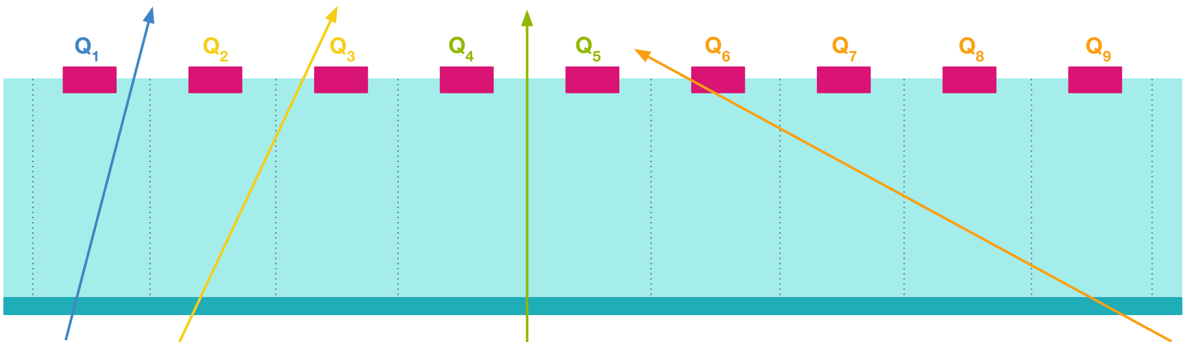


Figure 3.8: Formation of clusters of different sizes in silicon detectors.

3.2 Front-end electronics

The signals created in each pixel cell are extracted by readout chips, with several thousand electronic channels. This large number of channels can only be addressed with custom-designed electronic circuits. Although the existing pixel chips use different geometries, several building blocks are common to most designs. Chips can be divided into the *sensitive area*, which contains a matrix of rectangular or square pixels, and the *chip periphery*, where the sensitive area is controlled and global functions common to all pixels are located [36]. The *wire bonding* pads are located at the lower chip edge. The pixel unit cell in the active area and the corresponding sensor pixel usually have the same area. Typical circuit elements present in the pixel cell of the chip are shown in Figure 3.9.

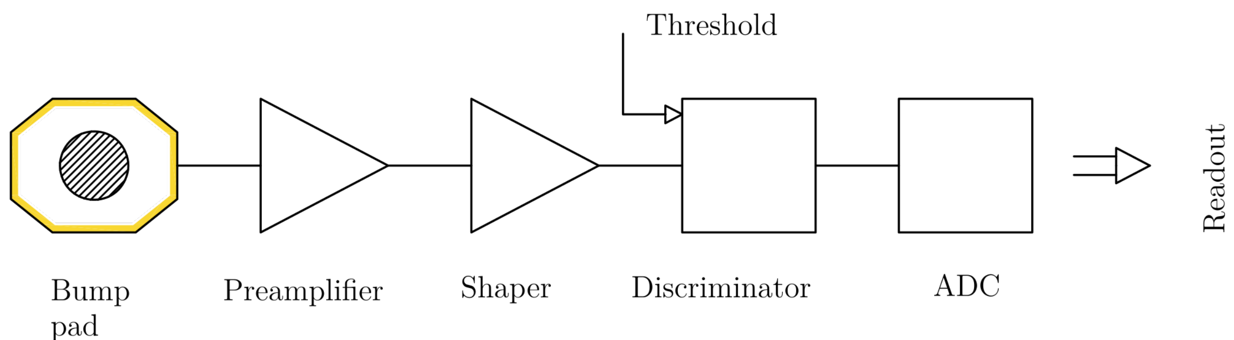


Figure 3.9: The elements of the pixel detector front-end electronics.

The *bump pad* is used for the electric connection to the sensor. To amplify a very small signal created by an incoming particle, a *charge sensitive amplifier* (CSA) is used, which integrates the current and generates a voltage with an amplitude proportional to the input charge. The signal charges have to be removed from the input node to read out successive signals close in time. For this purpose, a *feedback circuit* is used. To limit the bandwidth of the preamplifier output signal, a band-pass filter or *shaper* is often included, which is beneficial in the reduction of high- and low-frequency noise contributions due to the sensor leakage current. Signals with sufficiently large input charge are detected by the *discriminator* which compares the output of the shaper to a configurable threshold value. This value should be chosen in a way that the noise rate is kept at an acceptable level, while maximizing the detector efficiency. Threshold values vary between individual pixels, due to production fluctuations of doping concentrations, oxide thickness, voltage drop or preamplifier gain variations. The variations are compensated for by threshold tuning (Section 3.2.1). For applications where the arrival time of the signal needs to be detected with high precision, the rise time of the discriminator plays an important role. The "time walk" curve in Figure 3.10 shows that signals with high amplitudes cross the threshold earlier compared to low-amplitude signals. Various readout schemes are possible for pixel detectors, depending on the planned application. In the case of analog readout, signals that passed the charge threshold are sampled by an *analog-digital converter* (ADC) to quantify the collected charge. For fast-timing, the binary readout can be chosen, where

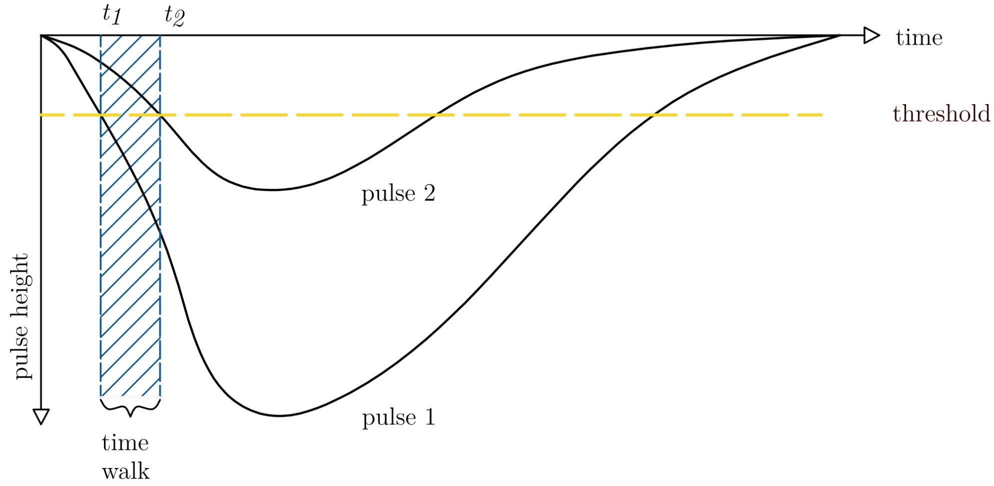


Figure 3.10: A diagram showing the time-walk between signals of different amplitudes.

only the information about the exceeded threshold is transmitted. The readout processing time is known as dead-time, during which signals above the threshold are not detected.

3.2.1 Chip tuning

The thresholds at chip level and pixel level need to be tuned to ensure an identical response of different pixels to identical signals.

A chip injection circuit is used to determine the threshold per pixel, by injecting a fixed charge multiple times and recording the percentage of detected signals. The procedure is repeated over the chosen charge interval. In the ideal case, this process would produce a step function, with 0% occupancy for all charges below the threshold and 100% occupancy for any charge above the threshold. However, due to the Gaussian-shaped electronic noise of each front-end channel, the step function is smeared into the so-called *S–curve*, as shown in Figure 3.11.

The threshold value is obtained by fitting the S–curve with a convolution of a step function and a Gaussian distribution which describes the probability of having a signal s for a certain injected charge Q as:

$$s(Q) = \frac{1}{2}\mathrm{erfc}\left(\frac{Q_{\mathrm{thr}} - Q}{\sqrt{2}\sigma_{\mathrm{noise}}}\right), \tag{3.3}$$

where the erfc is the complementary error function. The pixel threshold Q_{thr} is defined as the mean of the S–curve and σ_{noise} is equivalent to the electronic noise.

Before the chip tuning, a wide distribution of pixel thresholds is observed. The same threshold value for each pixel is achieved by global and local threshold tuning. Global threshold tuning will bring pixels with high and low thresholds close to the target value, by setting the best value of the global digital-to-analog converters (DACs) at chip level. With local threshold tuning, the TDAC settings of each pixel will be adjusted so that the threshold distribution per pixel is as narrow as possible around the target value.

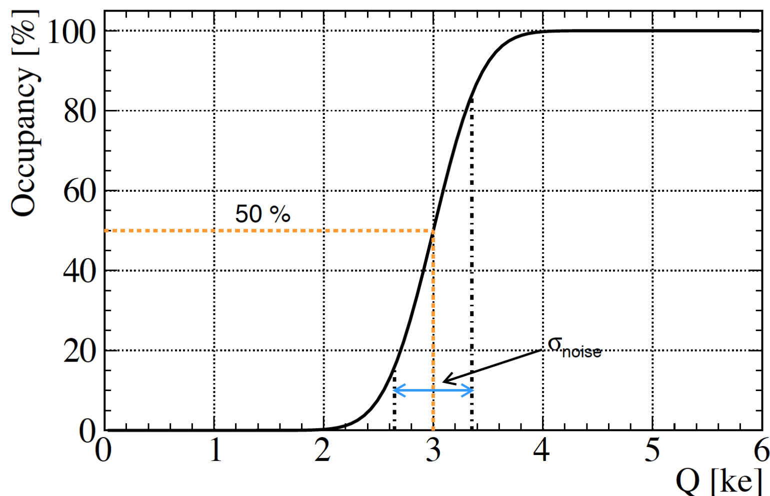


Figure 3.11: Example of a typical S-curve for one pixel. This image is taken from Ref. [53].

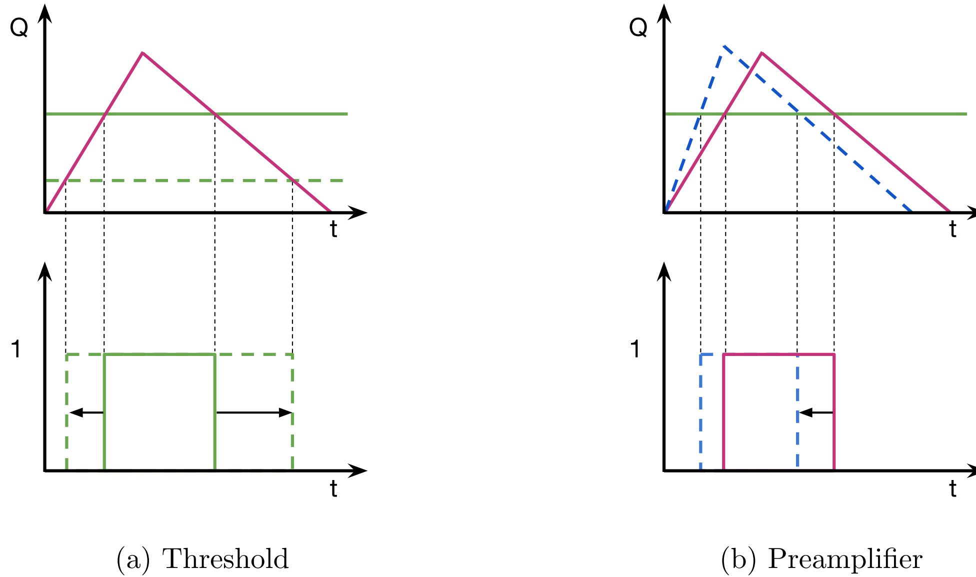
The Time-over-Threshold (ToT) response to a specific charge set by a user can be measured to test the preamplifier tuning of the readout chip. Similar to the threshold tuning, global and local preamplifier feedback current DAC settings are adjusted so that each pixel gives the predefined ToT response to the target charge. The charge to ToT conversion is affected by the discriminator threshold along with the preamplifier feedback current, as shown in Figure 3.12. Lowering the threshold increases the ToT for the same charge (Figure 3.12a), while increasing the feedback current lowers the ToT (Figure 3.12b). Therefore, ToT tuning is performed after the threshold tuning. For the ITk pixel detector, the ToT digitization is done with respect to the rising edges of the 40 MHz LHC clock and therefore one ToT unit corresponds to 25 ns and is known as bunch-crossing (bc) time.

3.2.2 RD53A prototype chip

The RD53A chip is the first experimental large scale readout chip developed within the RD53 Collaboration for HL-LHC upgrades of the ATLAS and CMS experiments. Its purpose is to demonstrate the suitability of the chosen 65 nm CMOS[1] technology for stable low-threshold, low-noise and low-power operation at high hit rates, and to verify the sufficient radiation tolerance [54]. As a prototype chip, it contains design variations for testing purposes and it is not intended to be used by the experiments in their final productions.

The sensitive area of the chip is arranged as a 192 × 400 pixel matrix, featuring a pixel cell of 50 × 50 µm^2. The chip size further extends outside of the pixel matrix, to include a 2 mm bottom-of-chip area that contains global and digital circuitry for biasing, configuring, monitoring, and the chip readout. A single row at the bottom chip edge holds rectangular passivation openings for wire bonding. An additional 200 µm space at the top of the chip

[1] Complementary Metal Oxide Semiconductor



(a) Threshold

(b) Preamplifier

Figure 3.12: The effect of the discriminator threshold and the preamplifier feedback current on the charge to ToT conversion.

contains a row of test pads in the same layout for dedicated measurements. The total chip size is $20.0 \times 11.8\ \mathrm{mm}^2$, which is about half of the size foreseen for the production chip version.

The RD53A pixel matrix contains three different front-end designs to allow detailed performance comparisons. They are identified as synchronous (128 columns), linear (136 columns) and differential (136 columns), as shown in Figure 3.13. The three front-end flavors feature a charge sensitive amplifier connected to a threshold discriminator whose output drives a ToT counter used for the analog-to-digital conversion of the signals [55]. The distinctive feature of the synchronous front-end is the use of so-called *auto-zero* functionality, where the internal capacitors are used to compensate for voltage offsets instead of a pixel-by-pixel threshold trimming. In front of the discriminator, the linear front-end uses a linear pulse amplification, while the differential front-end uses a differential gain stage. The differential and linear front-end designs are placed next to each other as they have the most similar functionality, allowing to have as large as possible area with nearly uniform response, which is useful for sensor characterization in measurements with particle beams. Common to all front-ends is the injection calibration circuit, used for pixel testing and calibration, which allows the generation of two consecutive signals of the same polarity and simultaneous injection of different amounts of charge into neighboring pixels.

The RD53A chip is designed to operate with serial powering and integrates so-called Shunt Low Drop-Out (SLDO) regulators [56], which are a combination of a linear LDO regulator and a shunt element. With this functionality it is possible to operate a chain of pixel modules in series by a constant current. The SLDO regulator provides regulated voltages for each front-end in a module and shunts any excess current. The design significantly evolved from the FE-I4 chip, over the RD53A chip towards the implementation in the

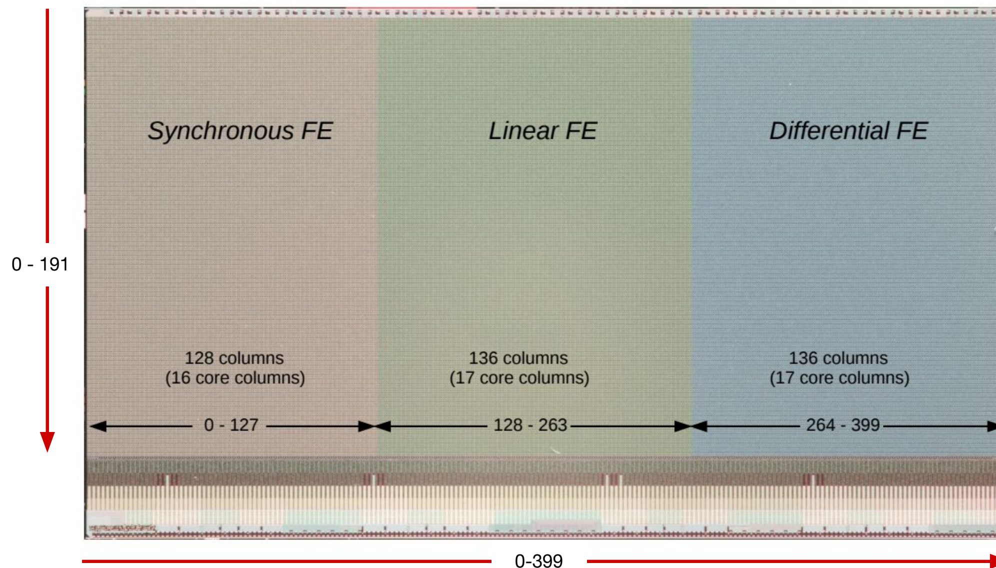


Figure 3.13: Arrangement of front-end flavors in the RD53A chip, with the pixel column number range of each flavor indicated. Pixel (0,0) is located in the top left corner. This image is taken from Ref. [54].

final production chip version, allowing to reduce the number of cables in the ITk pixel detector.

3.2.3 ITkPix full size chip

The ITkPixVn chip, which evolved from the RD53A prototype, is the full-size chip planned for the ITk pixel detector, where n refers to design iterations during which observed issues of the chip were fixed. The active area is organized as a 384×400 pixel matrix with a pixel cell of 50×50 µm^2. Each pixel can be considered as a combination of an analog front-end and a digital logic as illustrated in Figure 3.14a. Pixels are organized in analog islands, with four front-ends each, embedded in a flat digital synthesized "sea" as shown in Figure 3.14b. A single pixel core is shown in Figure 3.14c and contains 16 identical analog islands. Pixel cores are repeated in two dimensions to form the pixel matrix. The functional view of the ITkPix chip floorplan is shown in Figure 3.15. The chip bottom is considered a fixed element of the chip, as it contains global analog and digital circuitry needed to bias, configure, and readout the chip, and is determined by the width of the unique wire bonding pad frame which is 20 mm (50 column cores). The chip height is not constrained by the chip bottom, but it is limited by power and bias distribution as well as readout timing, and the chosen value is 48.

The analog front-end design is based on the differential flavor of the RD53A chip, with a further improved circuit. This is a pure analog circuit, without memory latches, flip-flops or counters. It consists of a pre-amplifier (first stage), a DC-coupled pre-comparator (second stage) and a comparator. The pre-amplifier has adjustable gain, continuous reset,

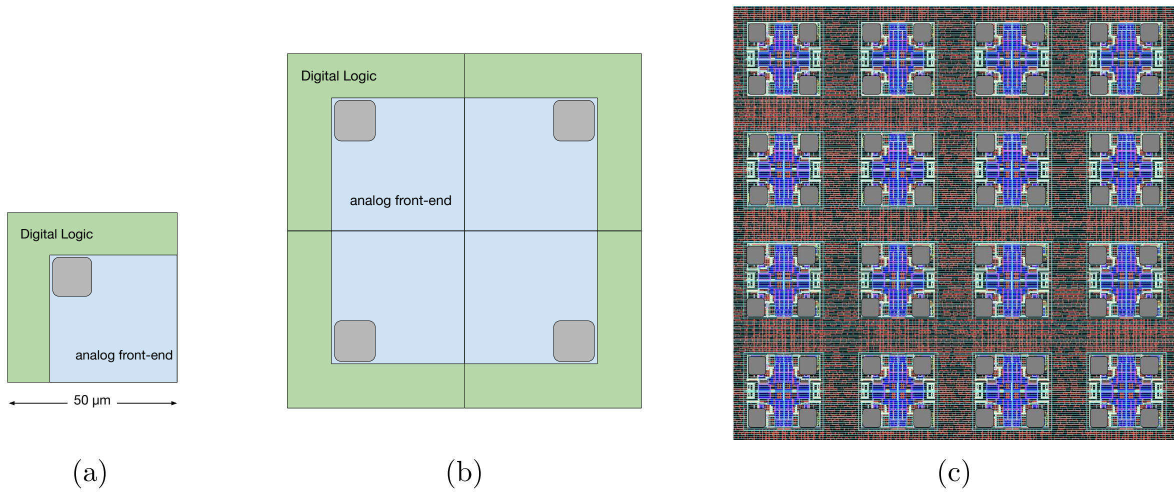


Figure 3.14: An illustration of: a) a single pixel of the readout chip; b) an analog island with four front-ends embedded in the digital logic; c) a pixel core with 16 identical islands. These images are taken from Ref. [57].

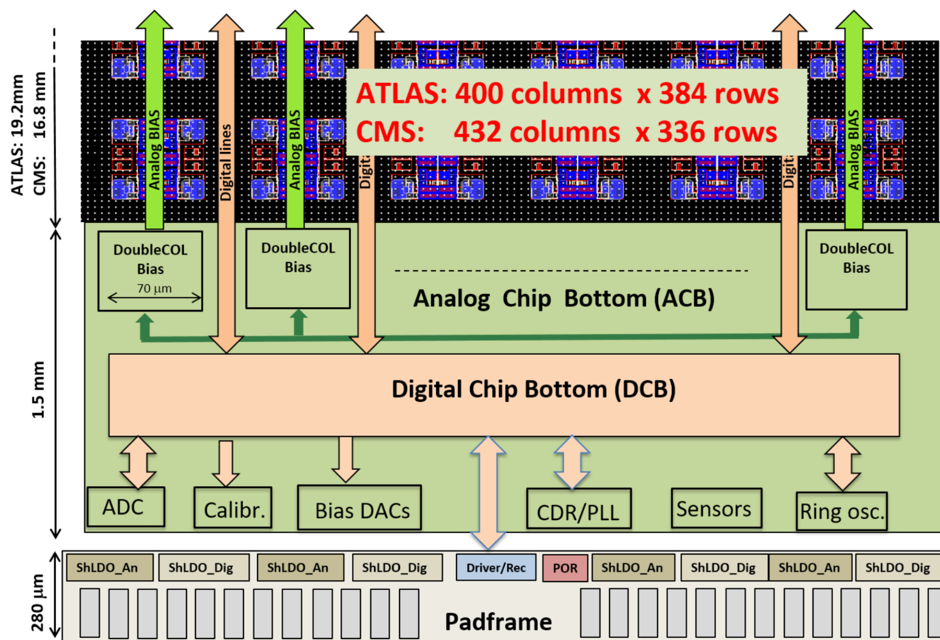


Figure 3.15: The functional view of the ITkPix chip floorplan. This image is taken from Ref. [58].

and a leakage current compensation circuit that can be enabled in case of high detector leakage currents (above 2 nA per pixel) to prevent saturation. The second stage acts as a differential threshold circuit, i.e. the global threshold is adjustable through two distributed threshold voltages instead of one. The comparator output is forwarded to the digital core where the ADC functionality is implemented by digitizing the ToT of the comparator pulse. To reduce congestion in the digital core, a 4-bit custom latch of the ToT memory was used for the first time in the ITkPixV1.0 chip. This first implementation contained a design bug that is patched in version ITkPixV1.1, where the ToT is reduced to a binary output. This chip version will be used for modules of the pre-production. The bug should be completely fixed in the production version of the chip called ITkPixV2.

The technical specifications of the ITkPix chip are summarized in Table 3.1.

Table 3.1: Technical specification of the ITkPix chip [59].

Quantity	Value
Chip size	21×20 mm^2
Pixel size	50×50 µm^2
Hit rate	3 GHz/cm^2
Trigger rate	1 MHz
Latency	512 bc
Data rate	5.12 Gbit/s
Minimum threshold	600 e
Radiation tolerance	500 Mrad
Power	$\leq$ 4 µA/pixel
Operating temperature	-40°C to +40°C

3.3 Module assembly

The ITk pixel detector will consist of single-chip modules with 3D sensors and four-chip modules (quad modules) with planar sensors. The size of the sensor is driven by the rate of defect that occur in the sensor production. As 3D sensors have low yield, they are used for single-chip modules, while planar sensors, with high yield, are chosen for multi-chip modules. Regardless of the sensor type, the module assembly procedure is performed in two steps:

- hybridization, where the interconnection of the readout chips to the sensor is performed by the hybridization vendor to obtain the so-called *bare module*;
- bare module to PCB assembly, performed by the ITk institutes.

Each of the steps will be discussed in more detail in the following.

3.3.1 Hybridization

In the hybridization process, the flip-chip technology is used to connect each pixel of the sensor to a pixel of the readout chip via solder bump balls of 20-30 µm diameter. For this process, the UBM is grown on the contact pads of the sensor and readout chip. On the chip side, electroplated solder bumps are deposited on the UBM layer by evaporation. The bump balls are shaped into spheres in a process called "reflow", where the wafer is heated to the phase transition temperature ($\approx$ 350°C) resulting in a collapse of the bump balls into truncated spheres due to the surface tension, allowing the electrical contact between the sensor and the chip [36].

3.3.2 Bare module to PCB assembly

For a bare module to be operational in a detector, the power and signal pads of the front-end chips have to be connected to remote power supplies and readout system hardware, respectively. Therefore, an additional layer of connectivity is required, usually implemented as a rigid or flexible printed circuit board (PCB). The bare module to PCB assembly step is divided into two stages: bare module to PCB gluing, followed by wire bonding.

Bare module to PCB gluing

During the prototyping phase, so-called single-chip cards (SCC) with RD53A chips were used. Each card consists of a custom-designed rigid PCB, with a dedicated area onto which a bare module is glued and subsequently wire-bonded for electric connections. The card is equipped with a LEMO connector for the bias voltage, a molex connector for the chip power, and a display-port connector for the data transmission, as shown in Figure 3.16.

The attachment of the quad bare module to the custom-designed flexible PCB is performed using the dedicated assembly tooling. In the following, the procedure based on the RD53A tooling is described. The main parts of the tooling are two aluminium jigs with vacuum inlets: one for holding the bare module (Figure 3.17a), the other for holding the flex PCB (Figure 3.17b). The bare module jig has three alignment pins for the correct relative positioning of the components. The flex jig has adjustment pin holes to align the flex frame and adjustment screws used to control the spacing between the components attached to the two jigs when they are connected. This spacing defines the desired glue height. Both jigs are used with a vacuum applied during the gluing procedure, which secures the position and flatness of the bare module and flex PCB. An additional part of the assembly tooling is the frame holding a stencil, which aligns the stencil to the flex jig and allows the glue deposition using a specific pattern that ensures glue coverage of at least 80%. After the glue application, the stencil frame is removed, followed by the placement of the flex jig onto the bare module jig. The pair of jigs is kept together for eight hours for glue curing.

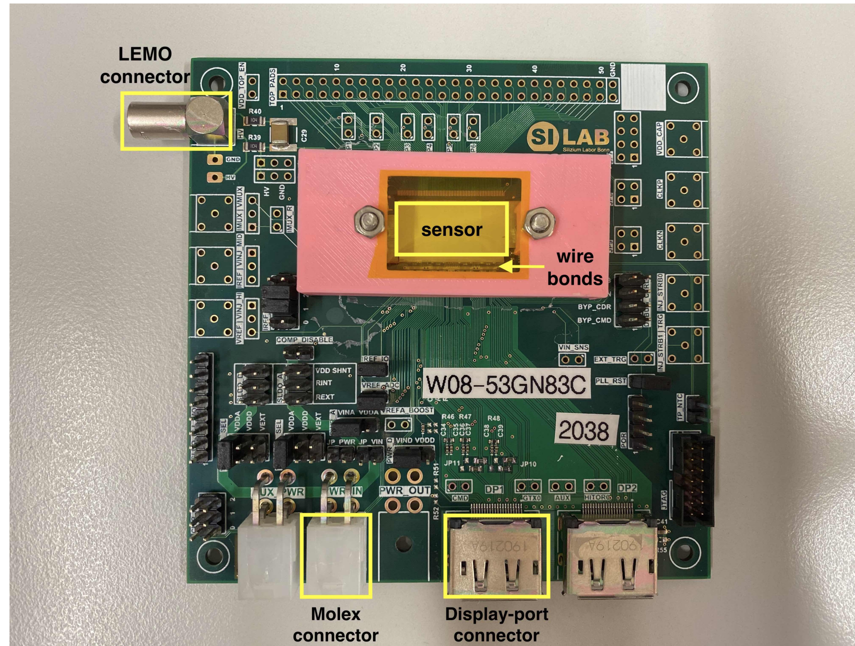
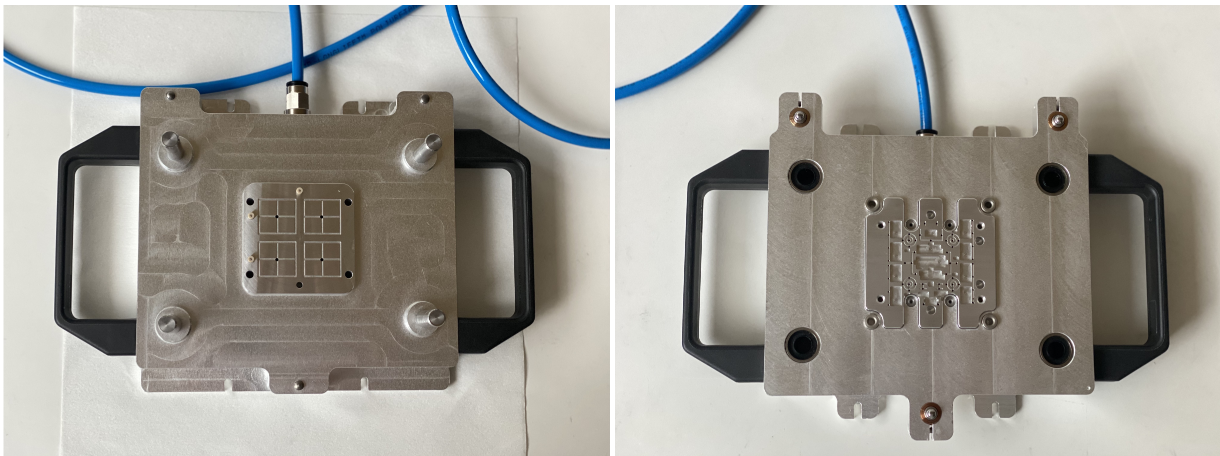


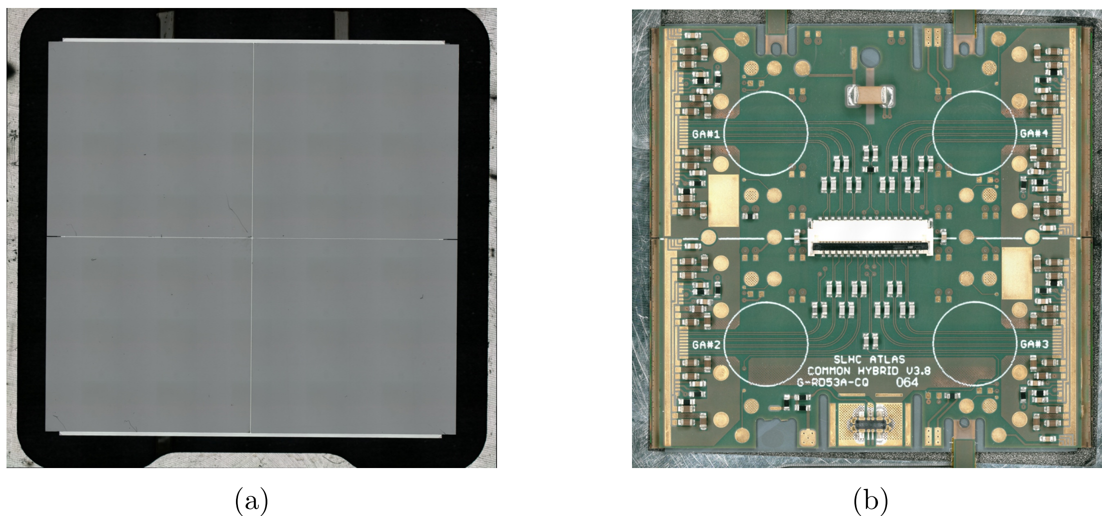
Figure 3.16: An example of an assembled single-chip card (SCC).



(a) Bare module jig

(b) Flex PCB jig

Figure 3.17: Module assembly jigs for attaching a flex to a bare module.



(a) (b)

Figure 3.18: Details of the RD53A quad module. Figure a) shows the bottom side of the bare module with four readout chips, while b) shows the assembled quad module.

Figure 3.18a shows the bare module, with the four chips on top of the sensor which is visible at two edges and in-between the chips. The assembled module is shown in Figure 3.18b featuring RD53A flex version 3.8. The rows of wire bonding pads are visible on the left and the right side.

Wire bonding

The gluing step is followed by the wire bonding between the front-end chip and the flex PCB, for powering, grounding, command and data communication. The procedure is performed using a wire bonding machine, which utilizes a bonding program to establish wire bonds following a specific diagram for detector operation defined by the chip design. The bonding parameters, such as touchdown force, ultrasonic power of the bond, head bond force, bond time and loop height are adjusted to ensure the desired quality of the bonds. The high quality of the wire bonds is crucial, as the assembled modules will be operated in the strong magnetic field environment of the ATLAS detector. This means that the wire bonds have to withstand the strong resonant oscillations that may occur if time-varying currents pass through them with frequencies close to their mechanical resonance frequency [60]. To measure the force required to break a wire, pull tests are performed on additional wires which are placed, but not needed for detector operation. Irradiated sensors require a high bias voltage of up to 600 V, which creates a large potential difference between the sensor and the readout chip. For the operation in the ATLAS detector, wire bonds must be protected (encapsulated) to reduce mechanical stress, movements caused by the Lorenz force, and corrosion. To avoid discharge near the module edge and to protect the wires, Parylene coating with a target thickness of 7 µm is applied after the wire bonding. Assembled modules are placed into module carriers for wire-bond protection during testing and shipping.

4 Instrumentation and experimental methods

In this chapter, the experimental setups and methods used to evaluate the performance of sensors and modules will be presented. These methods can be divided into laboratory and test-beam measurements.

All laboratory measurements are performed in a clean room environment. Sensor and bare module characterization are done using the probe station setup discussed in Section 4.1, while module electrical tests are done using the climate chamber setup, presented in Section 4.2. Section 4.3 is dedicated to the test-beam infrastructure. The data acquisition systems used for the measurements are summarized in Section 4.4.

4.1 Probe station setup

The sensor characterization is performed on a Cascade Microtech Summit 12000 probe-station. Measurements are performed by placing the sensor on the gold-plated aluminium chuck, and fixing it via vacuum. This probe station offers the possibility of testing 8-inch wafers or diced sensors. Sensor biasing is done with thin needles that can be precisely positioned, and the chuck itself. In addition, the chuck is connected to an Espec ETC-200L chiller, which enables the control of its temperature. The temperature and relative humidity in the probe station light-tight volume is monitored using a custom-designed environmental monitoring system [61]. The continuous flow of nitrogen during the measurement ensures low humidity. Before the irradiation, measurements are carried out at a chuck temperature of $T = (20 \pm 2)$°C. After the irradiation, measurements are performed at a chuck temperature of $T = (-25 \pm 2)$°C. A Keithley 6517B is used as a source meter and an Agilent E4980A precision LCR meter for capacitance measurements.

4.1.1 Current-voltage characteristics

One of the quality measures for the silicon sensor is the dependency of the leakage current on the applied bias voltage, known as the IV characteristics. A typical IV characteristics for a reverse-biased sensor is shown in Figure 4.1. The surface contribution arises when the depletion region reaches the backside. After reaching the full-depletion voltage V_{fd}, the IV curve shows a plateau where the increase in current is very small till the breakdown occurs at high voltages. The exact definition of the breakdown is application dependent.

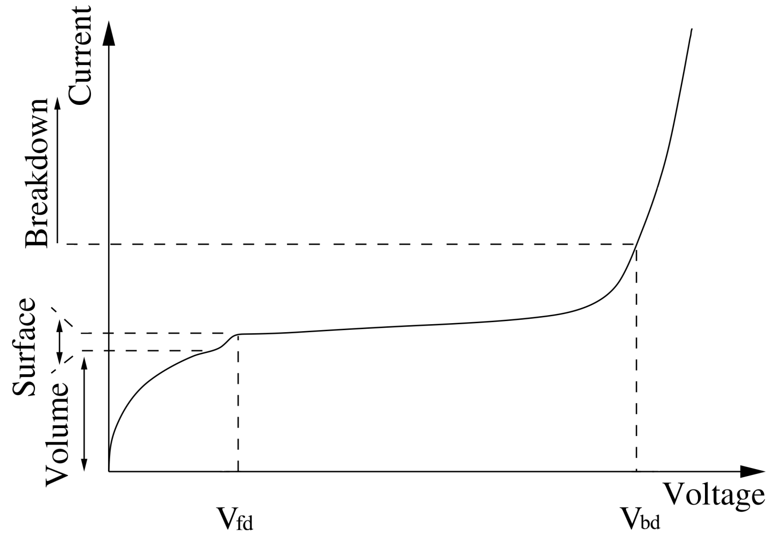


Figure 4.1: Typical shape of the IV-curve with indicated different current contributions. The image is modified from Ref. [36]

For the characterization of the sensors for the ITk, the breakdown voltage V_{bd} is defined as the minimum voltage value for which the leakage current increases by more than 20% over a voltage step of 5 V.

Characterization of all sensor structures is performed both before and after irradiation. Determined values for the breakdown voltage are compared with the ITk specifications for planar sensors. The voltage is applied to the backside of the sensor through the probe station chuck, while the bias ring is kept at ground potential by contacting it with a needle through dedicated openings in the passivation layer. For each applied voltage, ten subsequent measurements are performed after settling time of 2 s, and the resulting mean and standard deviation are calculated. After the flip-chipping, the measurement is performed by placing the bare module onto the chuck with the front-ends facing downwards. The bare module is biased by placing the needle on the backside of the sensor, while the ground is provided by contacting the dedicated wire bonding pad of the chip. Here, the chuck is not grounded. The IV probing for the two cases is illustrated in Figure 4.2.

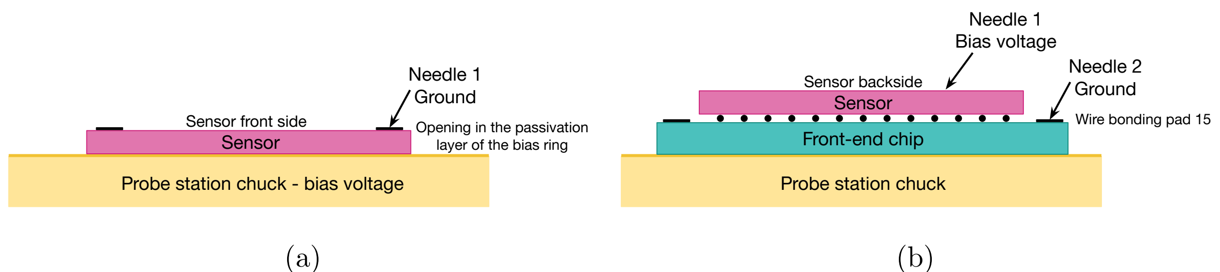


Figure 4.2: IV probing for a) the sensor and b) the bare module.

4.1.2 Long-term current stability

The pixel modules in the detector will be operated for long time intervals. Therefore, it is important to confirm the long-term stability of the leakage current at sensor level through the It measurement. The test is performed on a sensor biased with the typical operating voltage $V_{\text{op}} = V_{\text{fd}} + 50$ V for 48 hours, during which the leakage current is measured every ten minutes.

4.1.3 Capacitance-voltage characteristics

Although it is possible to determine the full-depletion voltage from the IV curve as the point at which a bulk current no longer increases, it is usually determined from the so-called capacitance-voltage characteristics. The capacitance of a pn-junction with substrate doping N can be calculated as two plates separated by the depletion region of distance W [36]:

$$C(V) = \epsilon_0 \epsilon_{\text{Si}} \frac{A}{W(V)} \approx A \begin{cases} \sqrt{\frac{\epsilon_0 \epsilon_{\text{Si}} e N}{2V}} & \text{for} \quad V < V_{\text{fd}} \\ \frac{\epsilon_0 \epsilon_{\text{Si}}}{d} & \text{for} \quad V > V_{\text{fd}}, \end{cases} \tag{4.1}$$

where d is the sensor thickness. Thus, according to:

$$\frac{1}{C^2} = \frac{1}{A^2} \begin{cases} \frac{2}{\epsilon_0 \epsilon_{\text{Si}} e N} \cdot V & \text{for} \quad V < V_{\text{fd}} \\ \left(\frac{d}{\epsilon_0 \epsilon_{\text{Si}}}\right)^2 = \text{const} & \text{for} \quad V > V_{\text{fd}}, \end{cases} \tag{4.2}$$

the quantity $1/C^2$ exhibits linear rise until V_{fd}, after which is constant, as shown in Figure 4.3. Therefore, full-depletion voltage is derived by displaying the $1/C^2$ as a function of the voltage and fitting the two branches with straight lines. This measurement is carried out using a probe station and an LCR meter coupled to an external voltage source, working at a frequency of 10 kHz.

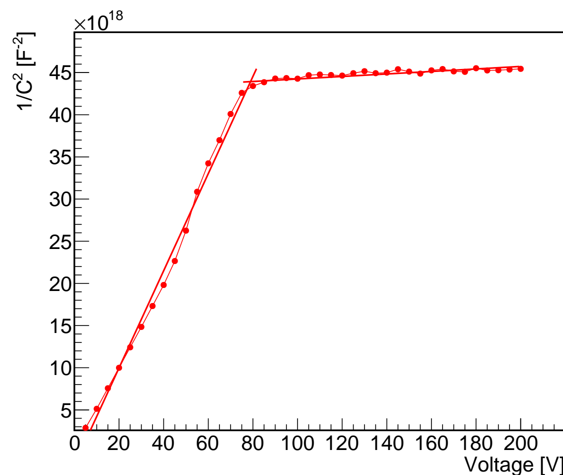


Figure 4.3: An example of the CV characteristics

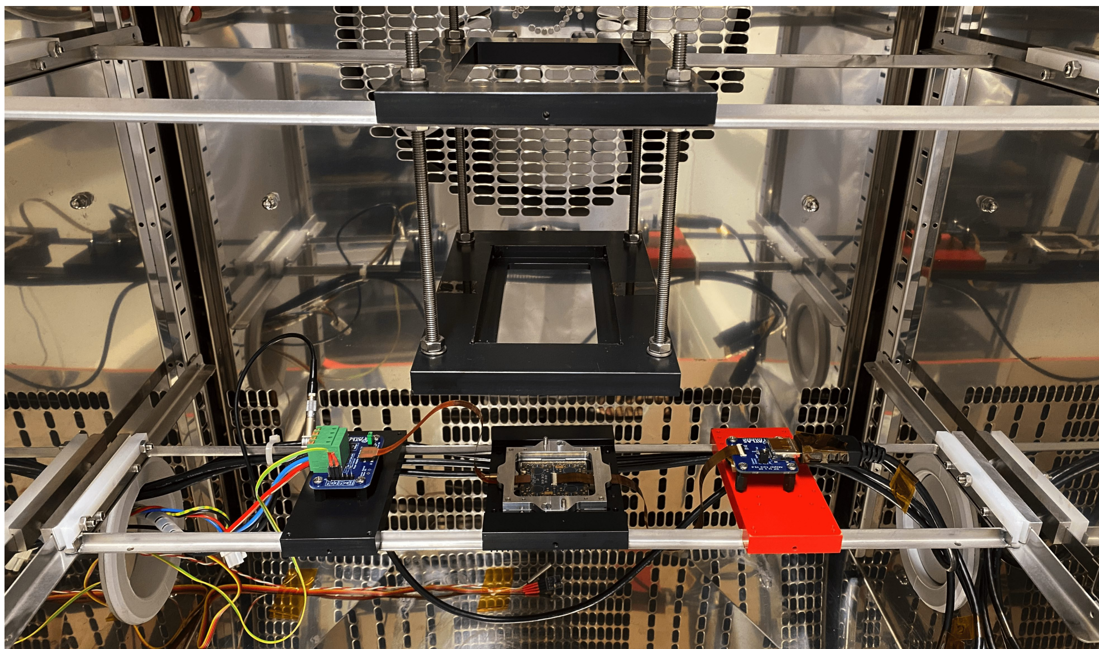


Figure 4.4: The module testing setup inside the climate chamber. From left to right are shown: the power adapter card, the quad module in a module carrier and the data adapter board. The lower part shows sensors used for the monitoring of the temperature and humidity, while the upper part shows the adjustable fixation for holding the radioactive sources.

4.2 Climate chamber setup

All laboratory measurements at module level are performed in a Vötsch VT7011 climate chamber, which provides a light-tight testing environment at a stable temperature and flushed with nitrogen. Figure 4.4 shows the part of this testing setup in the climate chamber, while the detailed schematic is given in Figure 4.5.

A Rohde & Schwarz HMP 4040 and a Keithley 2400 are used as low-voltage (LV) and high-voltage (HV) power supplies, respectively. Power supplies and climate chamber can be controlled remotely through the dedicated data acquisition computer, equipped with hardware components of the readout system required for testing.

The part of the setup inside the climate chamber consists of a custom-made jig with a heat sink, onto which a quad module in a carrier without the bottom cover can be mounted. Powering of the module is done through the power adapter card connected to the power supplies. The chip configuration and readout are performed through the data adapter board. This board is connected to the module with a thin flat cable, while the connection to the PC is realized with up to four independent display-port cables. Different power and readout cards are used depending on the chip version bump-bonded to a quad sensor. In addition, the setup is equipped with a movable tray for a radioactive source, to be placed above the module.

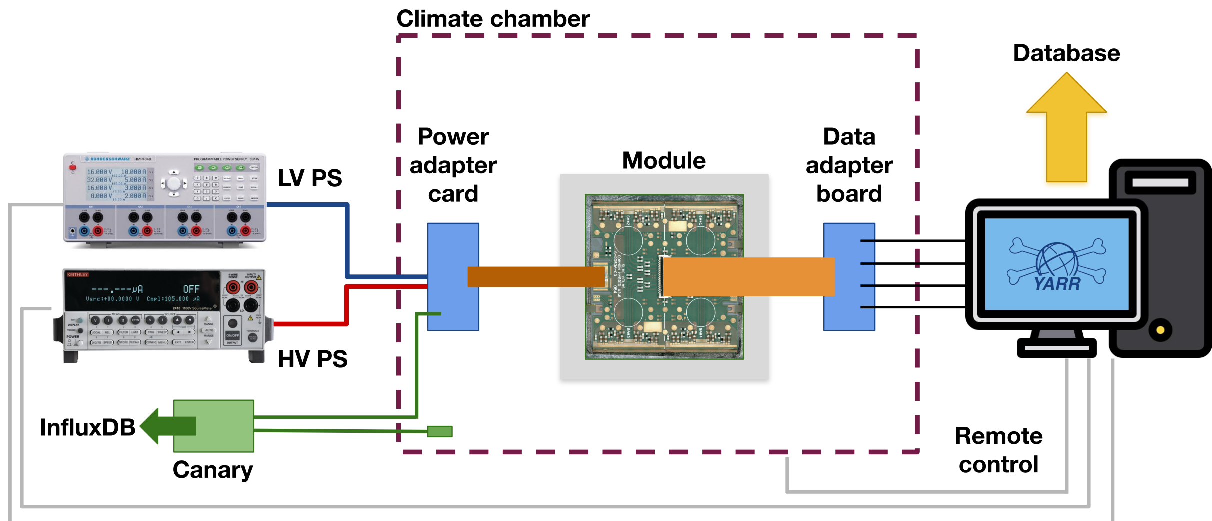


Figure 4.5: A detailed schematic of the climate chamber setup for the RD53A module characterization. The components are described in the text.

The temperature and humidity in the climate chamber are monitored using the Canary system, through PT1000 and SHT35 sensors. The same system is used to monitor the module temperature through the NTC on the flex PCB. To reduce humidity, the climate chamber is flushed with nitrogen during testing. Operational parameters, such as sensor leakage current and LV current, are monitored during the electrical characterization. Together with the environmental monitoring data, these are stored in the InfluxDB [62], a database used to store time-ordered data.

4.3 Test-beam infrastructure

Test-beam measurements are most powerful for the characterization of particle detectors in terms of hit efficiency and spatial resolution, in conditions close to those expected in collider experiments.

Particle beams are provided by dedicated accelerator facilities with well-defined characteristics, such as energy, intensity and type of particles. A series of tracking devices composed mostly of silicon pixel detectors with good spatial resolution, known as *beam telescopes*, are used for the track reconstruction, to evaluate the performance of the Device Under Test (DUT) that is usually placed at the center of the telescope. Test-beam measurements within this thesis were performed either at the DESY II or at the CERN North Area test-beam facilities, which will be briefly introduced below, followed by the description of the used beam telescope.

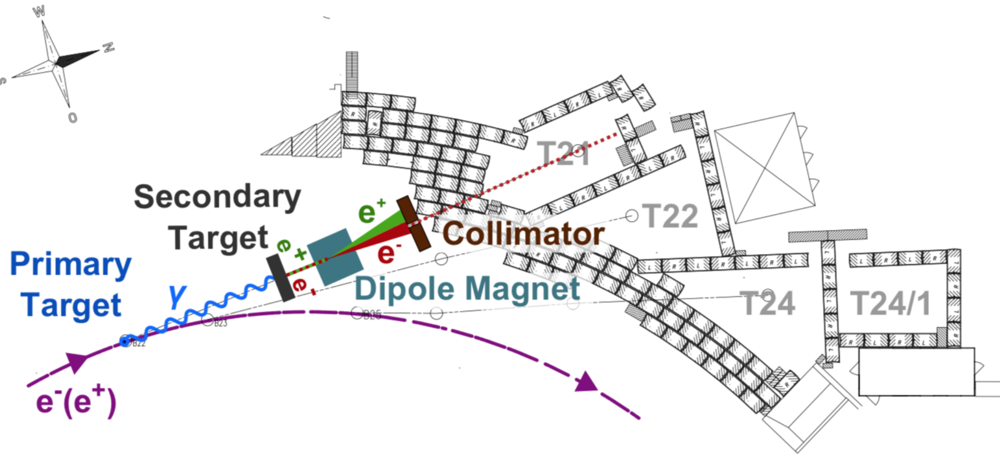


Figure 4.6: A schematic view of the beam generation at the DESY II Test Beam Facility for beam line TB21. This image is taken from Ref. [63].

4.3.1 Beam lines

DESY

The Deutsches Elektronen-Synchrotron (DESY) in Hamburg accelerates positrons and electrons and provides three independent beam lines with particle energies ranging from 1 GeV to 6 GeV. A schematic view of the beam generation is shown in Figure 4.6. The electron beam originating from DESY II is directed to a primary target (several microns thin carbon fiber) positioned in the DESY II beam orbit, generating Bremsstrahlung which is further directed to a secondary target (Cu or Al), resulting in a production of electron-positron pairs. Electrons and positrons are afterwards passing through a dipole magnet, which allows the selection of the preferred particle charge and momentum. The selected particles are then collimated by the controllable primary collimator and guided to the test-beam area located in Hall 2 [63]. An exchangeable fixed-size secondary collimator is located inside the beam area. Two beam lines are equipped with EUDET-type telescopes, used for the testing of the silicon sensors.

CERN-SPS

The beam facility in the CERN North Area offers several beam lines, illustrated in Figure 4.7. All test-beam measurements within this thesis are performed at the H6 beam line, equipped with an EUDET-type beam telescope. The proton beam extracted from the SPS is directed onto one of the three available targets (T2, T4 or T6), producing a high-resolution pion beam suitable for both experiments and tests. The T4 target receives the primary protons from SPS and produces the two beams H8 (high energy) and H6 (medium energy). The selection of the beam energy is possible via set of three magnets around the T4 target, referred to as *T4 wobbling* [64]. The Čerenkov Differential counter with

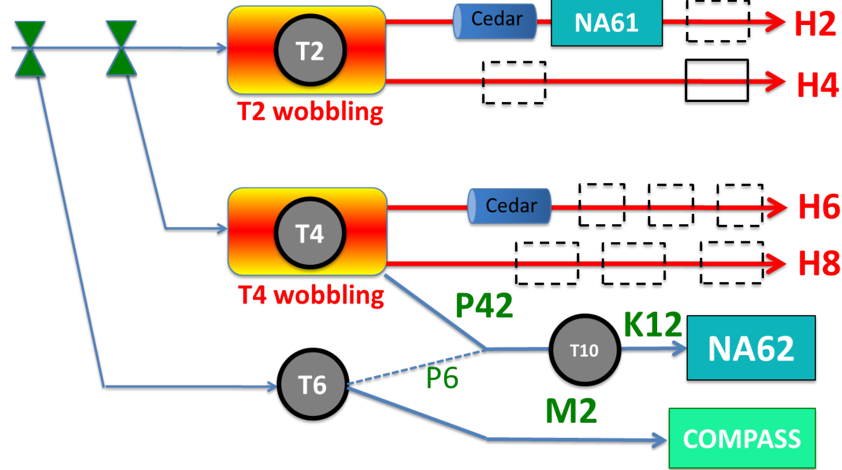


Figure 4.7: CERN-SPS North Area secondary beam lines. This image is taken from Ref. [66].

Achromatic Ring Focus (CEDAR) [65] is used for particle identification and separation of kaons and pions. This type of counter has an optical system to focus light in form of a ring. The particles with different masses are distinguished by the diameter of the ring. For measurements performed in this thesis, the beam of 120 GeV pion energy is used. Since many facilities need SPS extraction, the beam is delivered in spills lasting from 4.8 to 9.6 s, with a maximum flux of 10^7-10^8 particles per SPS extraction.

4.3.2 Beam telescopes

The EUDET-type beam telescopes are used in several test-beam facilities around the world. Figure 4.8 shows the DATURA beam telescope at the DESY II test-beam facility. The setup consists of six planes of Mimosas26 pixel sensors, four scintillators with photomultiplier tubes (PMTs) for triggering, a Trigger Logic Unit (TLU) providing trigger and time stamp information on particle passage, enabling synchronization of the telescope and the readout system used for the devices under test. For the data acquisition, the EUDAQ1 framework [67, 68] is used, which provides an easy way to merge the collected data into a single file during data taking. The framework details are presented in Section 4.4.3.

The six telescope planes are organized in an upstream and downstream telescope triplet. The Mimosa26 sensors of 50 µm thickness are built in a monolithic active pixel sensor (MAPS) technology. Each sensor is segmented into a 1152×576 pixel matrix of 18.4×18.4 µm^2 pixels, resulting in a total active area of 21.2×10.6 mm^2. The low sensor thickness ensures acceptable multiple scattering also for test-beam measurements with low energy particles. The binary resolution of 5.3 µm is improved by charge sharing, achieving a sensor resolution of 3.24 µm [69]. Each pixel sensor is mounted within an aluminium jig and installed on a movable aluminium frame that is continuously cooled down, keeping the sensor at 18°C. Two pairs of rectangular scintillators used for triggering are placed at the particle entrance and exit of the beam telescope. Each pair forms a cross that creates

Figure 4.8: The DATURA beam telescope with its sensor planes mounted on aluminium jigs. The boards on the top of each jig provide connections for power, clock, sensor configuration and data transmission. The transparent tubes connected to each jig are used for the water cooling of the sensors.

an overlapping area of approximately $20 \times 10\ \mathrm{mm}^2$, which covers almost the entire area of pixel sensors of the beam telescope. The Mimosa26 planes operate in a triggered rolling-shutter readout scheme, with a readout cycle and integration time of 115.2 µs. At each trigger, two cycles are read out, without any other hit timing information available.

For the beam telescope, a global coordinate system is defined as a right-handed Cartesian coordinate system, with the x and y axes defining the sensor plane and the positive z-axis along the beam direction.

Pointing resolution

The main feature of the beam telescope is its track resolution, which defines the precision with which a particle trajectory can be determined. This quantity is not constant along the trajectory and it depends on the intrinsic resolution $\sigma_{\mathrm{int,x/y}}$ of the sensors used to measure hits belonging to the track, the number of measurements and their z positions [69]. In addition, charged particles interact with the electric field of the nuclei of the traversed material, which leads to small deflections of the primary particle. When traversing any medium, the large number of these small deflections leads to the net effective deflection known as **multiple Coulomb scattering** illustrated in Figure 4.9.

This angular deflection of a charged particle has to be taken into account when discussing the pointing resolution of the beam telescope. This effect is more significant for low energy particles, as the standard deviation of the angular scattering distribution depends on the

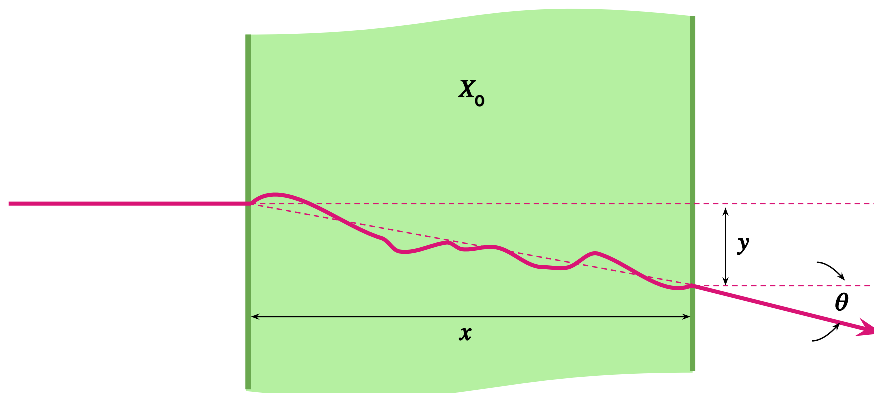


Figure 4.9: An illustration of the multiple Coulomb scattering, which leads to the effective deflection of the particle by an angle θ and a displacement y.

particle energy, particle type and the radiation length of the matter traversed [37]:

$$\theta_0 = \frac{13.6\ \text{MeV}}{\beta c p} \cdot z \cdot \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \ln\left(\frac{x z^2}{X_0 \beta^2}\right)\right], \tag{4.3}$$

with the velocity βc, the momentum p in MeV, the charge number z of the traversing particle and x/X_0 the thickness of the absorption medium in the units of the respective radiation length [37].

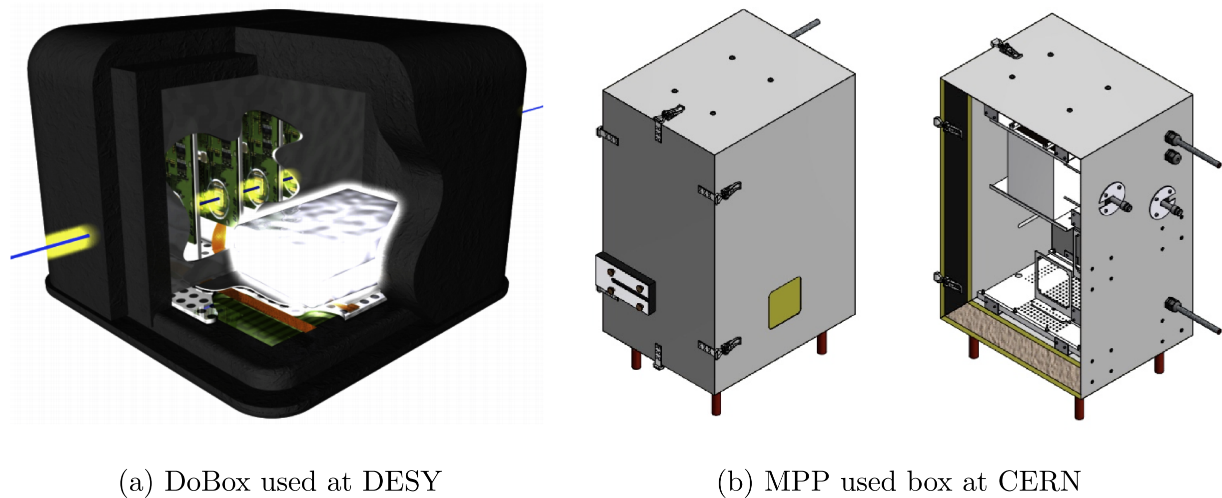
4.3.3 Cooling box

In all test-beam campaigns, the DUTs are placed in a cooling box, which is essential when testing irradiated modules. The design and material of the box are chosen so that sufficient tracking performance of the beam telescope is ensured.

At DESY, the used cooling box, designed by the Dortmund University group [70], is made of PPO[1] to minimize the contribution of multiple scattering. The layout of this DoBox is illustrated in Figure 4.10a. The box is divided into two volumes, the DUT volume and the dry ice volume, with a common bottom aluminium plate. The dry ice can be refilled or removed without opening the DUT volume. Using this setup, temperatures on DUTs between -50°C and -40°C can be achieved during the operation. To maintain low humidity and avoid any condensation, a constant nitrogen flow is supplied inside the DUT volume.

The cooling box used at CERN is developed and built at the MPP and is shown schematically in Figure 4.10b. The walls of the box consist of a 46 mm PUR[2] rigid foam insulation

[1]Poly Phenylene Oxide
[2]Polyurethane



(a) DoBox used at DESY (b) MPP used box at CERN

Figure 4.10: Cooling boxes used for test-beam measurements.

layer between two 1.5 mm thick aluminum plates. At the location of the beam line the aluminium plate is removed. The box is connected to a chiller and a nitrogen supply to allow for cooling and dry gas.

4.4 Data acquisition

4.4.1 YARR readout system

The Yet Another Rapid Readout (YARR) system [71] is a data acquisition (DAQ) system originally designed for the readout of FE-I4 chips, but due to its modular design was extended to support multiple front-end types, including the RD53A and ITkPix chips and multi-chip detector modules. The components of the YARR readout system are divided into hardware, firmware and software. The hardware supports multiple FPGA[3] platforms and is based on the Simple PCIe Carrier (SPEC) card. The used PCIe card has the Xilinx Series 7 FPGA. For the connection to the readout chip, the Ohio RD53A Multi Module Adapter is used. The FPGA has a simple firmware implementing only a basic buffer for commands and data. Unlike the traditional processing performed in the FPGA, the data processing is performed in the software on the host PC, allowing to utilize multi-core CPU architectures. The YARR software needs three components to perform the readout: a kernel driver to communicate with the firmware via PCIe, an engine driving the scans, and processors which analyze the received data.

The YARR readout system is used for configuration, tuning and operation of modules for both laboratory and particle-beam measurements. Using existing tuning scripts that change chip configuration parameters, the desired target threshold and ToT values can be achieved. Different scans are available to verify the digital and analog functionality of

[3] A field-programmable gate array

tested chips and to assess the quality of the performed tuning. The SPEC card has four mini display-port slots. This means that in the laboratory it is possible to test up to four quad modules simultaneously. At the test-beam, one of these slots is dedicated to the TLU to receive the trigger signal.

4.4.2 USBpix readout system

The USBpix system [72], designed at the University of Bonn, is used to tune and read out FE-I4 modules, that serve as a timing reference during the test-beam measurements. The hardware consists of a Multi-Input/Output (MIO) board, that holds the FPGA as well as the RJ45 connector for the EUDET telescope trigger interface and allows connection to chips of different flavors via adapter cards. For test-beam measurements, the USBPix system of the third generation with the so-called MMC3 board is used with integrated multi-chip support. The software used to configure and operate FE-I4 modules is called STControl and is fully integrated into the DAQ system.

4.4.3 EUDAQ framework

The EUDAQ software is a C++ implementation of a data acquisition framework, designed to run the EUDET-type beam telescope. The schematic of the EUDAQ architecture is shown in Figure 4.11. The main part of the EUDAQ framework is the *Run Control* which provides an interface for controlling the entire data acquisition system. All detector hardware is initialized, configured and read out by so-called *Producers*, through the commands received from the Run Control. The NI Producer is used as an interface between the EUDET-beam telescope DAQ (Anemome 1.3 LabView software) and the EUDAQ framework. In addition, a Producer needs to be implemented for any additional hardware (DUT-specific readout system) component. For ITk pixel modules the so-called YarrProducer is used. The STControl software used for configuration and readout of FE-I4 modules, is fully integrated into the EUDAQ framework, and therefore the STControl Producer is used for the data acquisition.

Event building denotes the process of merging event data from several detectors attributed to the same trigger. This process is performed online during the data acquisition by the *Data Collector*, which receives the data from all Producers, and combines them into a single file in native raw binary format, written to the disk (*Storage*). At the beginning and end of each run, a special event is attached. These are the beginning-of-run-event (BORE) and end-of-run-event (EORE), respectively. The BORE is used to store essential parameters needed for the correct interpretation of the data.

Two monitoring tools exist within the EUDAQ framework. The *Log Collector* receives log messages from all Producers and displays them to the user. The other important monitoring tool is the *Online Monitor*, which displays figures of the collected data using the internal converter plugins of the EUDAQ library for raw data decoding and thus allows data quality control. A converter plugin has to be implemented for each custom DAQ

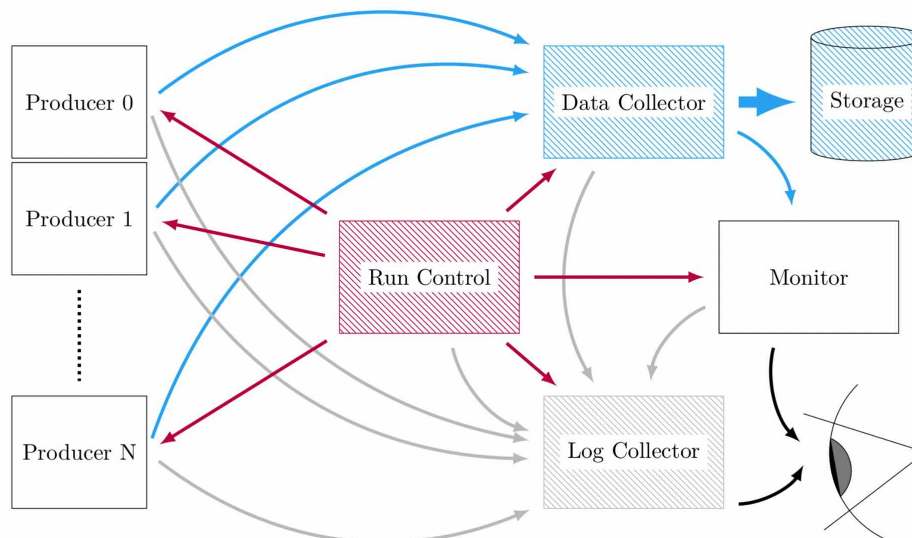


Figure 4.11: The schematic of the EUDAQ architecture. This image taken from Ref. [73].

system. For ITk pixel modules this is the YarrConverterPlugin. The important figures displayed by the Online Monitor are the hit maps, used to validate the alignment of any of the sensors with respect to the beam, and correlation histograms for each combination of coordinates for any pair of devices in the setup. The latter allows verifying that tested devices are synchronized in time.

5 RD53A module electrical characterization

As a part of the RD53A program of the ATLAS ITk Pixel group, eight quad modules have been assembled at the MPP. All modules have 150 µm thick sensors from three different manufacturers: Hamamatsu Photonics K.K. (HPK), Micron Semiconductor Ltd (Micron) and Semiconductor Laboratory of the Max-Planck Society (HLL). The chip thickness is either 150 or 400 µm. The details of the assembled modules are given in Table 5.1.

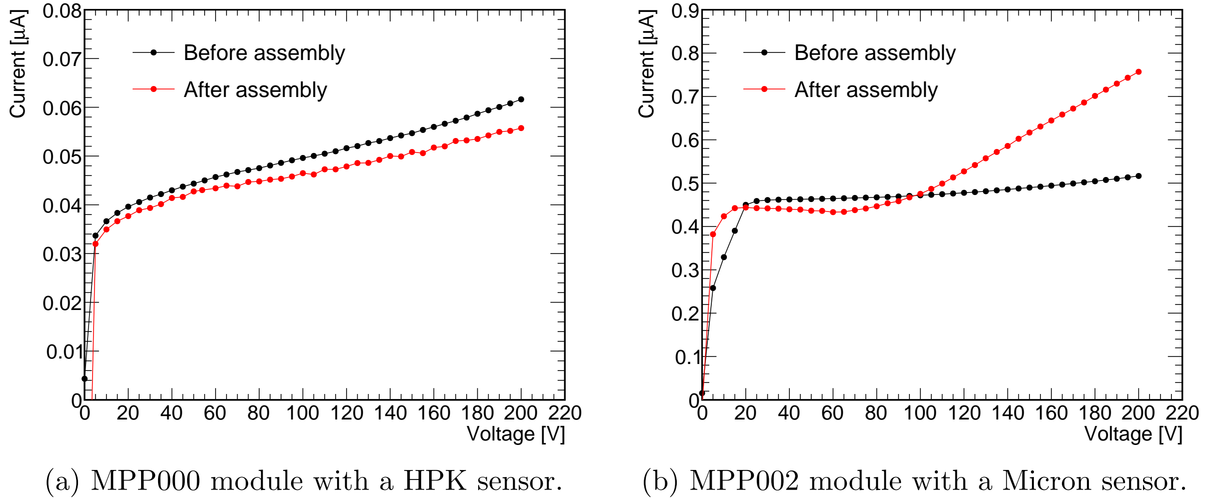
Table 5.1: Overview of the assembled RD53A quad modules. The quantity V_{fd} refers to the full depletion voltage of the sensor.

Local ID	Manufacturer	Chip thickness [µm]	V_{fd} [V]
MPP000	HPK	400	80
MPP001	HPK	400	80
MPP002	Micron	150	70
MPP003	Micron	150	65
MPP004	Micron	150	66
MPP005	Micron	150	70
MPP006	HLL	150	10
MPP007	HPK	400	80

In Section 5.1, the results of sensor IV measurements before and after the assembly are presented. The initial power-up tests and chip trimming are discussed in Section 5.2. At this step, the number of working chips per module can be determined, followed by chip trimming to bring the module into the ideal operational stage. Section 5.3 is dedicated to the SLDO cold start-up test, which allows to determine the lowest temperature at which chips can be configured. The detailed electrical characterization performed, including the chip tuning and bump-connectivity tests, is discussed in Section 5.4.

5.1 Sensor characterization

The sensor IV characterization is performed at the bare module reception stage (before the assembly) and after the assembly. Before the assembly, this measurement was performed at a probe station, as shown in Figure 4.2b. After the assembly, the measurement is performed in the climate chamber, where the sensor is biased through the power adapter card. Measurements are performed at 20°C. For the measurements before the assembly



(a) MPP000 module with a HPK sensor. (b) MPP002 module with a Micron sensor.

Figure 5.1: The IV measurements before and after the assembly for two tested modules. Statistical uncertainties are displayed and are smaller that the marker size.

this is the temperature of the chuck, while after the assembly this temperature is measured by the module NTC. The two typical cases observed for the IV characteristics before and after assembly are shown in Figure 5.1.

For all HPK sensors, the IV curve has the same shape for the two measurements (Figure 5.1a). The differences in the setup, especially the different ways to estimate the sensor temperature, could contribute to the small differences in the measured leakage current. For the shown example, the difference in leakage current measured at the two stages corresponds to a hypothetical ΔT of 0.5-1.3°C. No breakdown is observed within the voltage range tested.

The second case is the change in shape of the IV curve after the assembly (Figure 5.1b), with a slow rise of the leakage current. This is seen for all Micron sensors, except for the sensor of the module MPP005 for which the measurements at the two stages agree. In addition, the leakage current measured for Microns sensors is about ten times that of HPK sensors. However, the leakage current per area at the operational voltage is in the range 0.01-0.03 µA/cm^2. The non-irradiated ITk planar sensors should have leakage currents per area below 0.75 µA/cm^2 at the operational voltage and thus the measured values are within the specification.

Figure 5.2 shows the comparison of the leakage currents at the operational voltage for the eight pairs of measurements. The operational voltage is defined as $V_{\text{op}} = V_{\text{fd}} + 50$ V, where the full depletion voltage is obtained through the CV measurements on the test structures of the respective wafer and is listed in Table 5.1. Therefore, the operational voltages range from 60 V for HLL sensors, to 130 V for HPK sensors. The highest increase of the leakage current of ≈25% between the two stages is observed for the module MPP004.

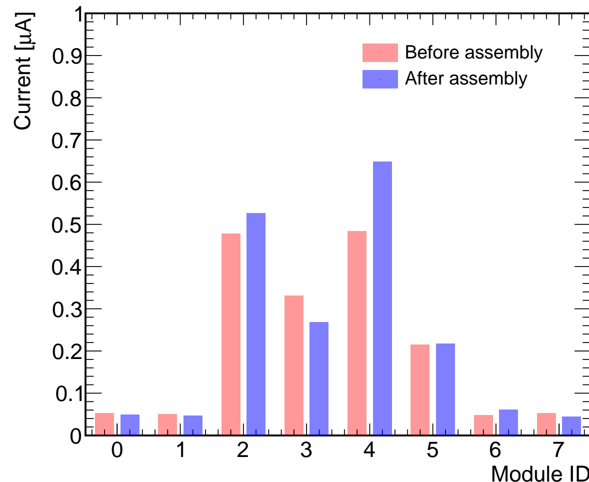


Figure 5.2: Comparison of the leakage current measured before and after the assembly at their operational voltages for all assembled modules.

5.2 Initial power-up and chip trimming

For each assembled module, the initial power-up test was performed at room temperature. Modules were powered in the SLDO mode with a constant current of 4.6 A, without biasing the sensor. The input voltage V_{in} of each chip is measured on dedicated probing pads. Measured values should be above 1.5 V, which was true for all assembled modules except for module MPP004, for which a value of 1.4 V was measured.

There are two internal regulator reference voltages for powering the chip core, analog (VDDA) and digital (VDDD). Before any chip configuration, the VDDA and VDDD of each chip are measured. If VDDA $\leq$ 1.14 V, pull-up resistors were soldered on the dedicated pads, using either 150 kΩ resistors (VDDA $\leq$ 1.09 V), or 300 kΩ (1.09 V $<$ VDDA $\leq$ 1.14 V). Values for VDDA measured on each chip before and after soldering of the pull-up resistor are shown in Figure 5.3, except for chip 4 of the MPP004 module, for which a value of 0.2 V was measured, indicating a dead chip. In total, five chips did not require any pull-up resistors. With soldered pull-up resistors, the VDDA value increases by 0.1 V ($R = 150$ kΩ) or 0.05 V ($R = 300$ kΩ). The measurements after adding pull-up resistors show VDDA values above 1.14 V for all chips, which allows to verify communication and default chip configuration. This testing step was not successful for the module MPP004 due to the low V_{in} value, where the chip configuration failed for all chips. This module was therefore excluded from further testing. In addition, chip 3 of the module MPP005 could not be configured and was disabled during further testing.

All working chips were trimmed according to the specification for optimal operation. This step includes adjusting corresponding chip parameters to ensure that the measured VDDA and VDDD values are as close as possible to 1.2 V. An additional chip trimming step is the ADC calibration, where the calibration output voltage (V_{cal}) corresponding to the median and high DAC settings of 500 and 3500 was measured at dedicated probing pads. The

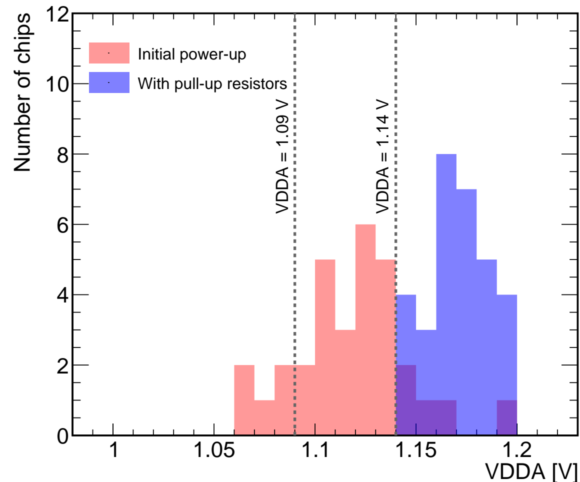


Figure 5.3: The measurement of the VDDA at the initial power-up stage and after soldering of the pull-up resistors.

measured V_{cal} values were compared to the ADC readings of the chip. The obtained values were fitted to a linear function as shown in Figure 5.4, where the fit parameters correspond to the ADC calibration parameters that were adjusted in the chip configuration file.

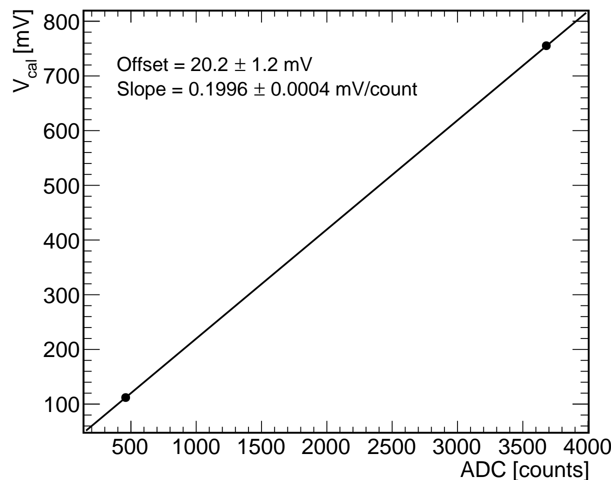


Figure 5.4: The ADC calibration for the module MPP006 - chip 4, with indicated values from a linear fit used as calibration parameters.

5.3 SLDO cold start-up test

In the ITk pixel detector modules will be operated in a serial powering scheme. Therefore, assembled modules were sent to the sites loading modules onto staves, where they are tested

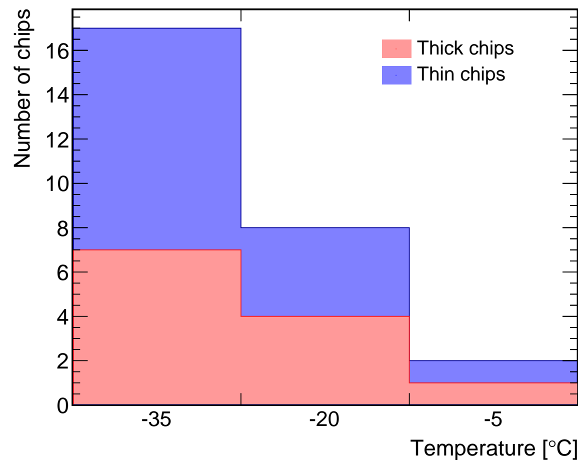


Figure 5.5: SLDO cold start-up temperatures for all tested chips.

in serial powering chains. As some of these tests were performed cold, the cold start-up test was needed for all assembled modules to investigate the behavior of RD53A chips at low temperatures. Each module was cooled down to the detector target temperature of −35°C and powered with a constant current of 4.6 A. If all chips started properly, the V_{in} should be close to the values measured at warm temperatures. To qualify the chip as working at cold temperatures, the default configuration and a digital scan were performed. If the cold start-up test at -35°C failed, the temperature was increased by 15°C and the test was repeated.

For all tested modules, results of the cold start-up test per chip are shown in Figure 5.5 separately for thick and thin chips. From all working chips at a warm temperature, 66.6% thin and 58.3% thick chips started at -35°C. By increasing the temperature to -20°C additional 26.7% thin and 33.4% thick chips were configured, while the remaining chips in both cases were finally configured at -5°C. A similar behavior is observed for the two chip thicknesses.

5.4 Full electrical test

Full electrical tests are performed with sensors biased to the operational voltage, as defined in Section 5.1. The YARR software was used to perform a series of scans, that do not alter the chip configuration, and tunings that start from the existing chip configuration and tune parameters to the chosen target values for threshold and ToT. The scans are divided into:

- pre-tuning scans;
- threshold and ToT tuning;

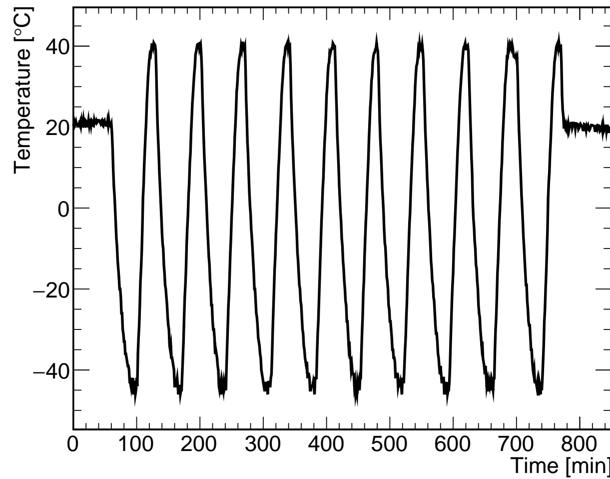


Figure 5.6: Temperature measured at the module during ten cycles between the target temperatures of −45°C and 40°C.

- post-tuning scans;
- bump-connectivity scans.

For thick chip modules, only the pre-tuning tests were performed which include digital, analog and threshold scans. In addition, the threshold and ToT tuning were done for two modules. Thin chip modules were tested following the entire quality control (QC) procedure, which also includes chip tuning and bump-connectivity tests. During the operation lifetime in the ATLAS detector, it is foreseen that modules will face around 100 thermal cycles down to −45°C, which can cause disconnected bumps due to thermal stress. Therefore, the presented testing sequence is followed by the thermal cycling procedure consisting of ten consecutive cycles between $T_{\mathrm{min}} = -45°\mathrm{C}$ and $T_{\mathrm{max}} = 40°\mathrm{C}$. The module temperature as a function of time during such a thermal cycling is shown in Figure 5.6. The soak time is defined as the time for which the module temperature T_{module} is within:

- $T_{\mathrm{min}} - 10°\mathrm{C} \leq T_{\mathrm{module}} \leq T_{\mathrm{min}} + 5°\mathrm{C}$;
- $T_{\mathrm{max}} - 5°\mathrm{C} \leq T_{\mathrm{module}} \leq T_{\mathrm{max}} + 10°\mathrm{C}$.

The thermal cycling procedure is optimized so that the soak time fulfills the requirement of ten minutes. To ensure that the dew point T_{DP} is $T_{\mathrm{DP}} \leq T_{\mathrm{module}} - 10°\mathrm{C}$, the climate chamber is flushed with nitrogen during the thermal cycling.

The post-tuning scans and bump-connectivity tests were repeated after this thermal cycling. Tests are performed separately for each front-end flavor, unless stated differently. All tests are performed at 30°C measured via the NTC on the powered module.

Where possible, the obtained results of four chips are combined and displayed for the entire quad module. The layout of the RD53A quad module with indicated orientation of the chips is shown in Figure 5.7. Note that columns of the readout chip are rows of the sensor, resulting in the pixel matrix of 800×768 pixels.

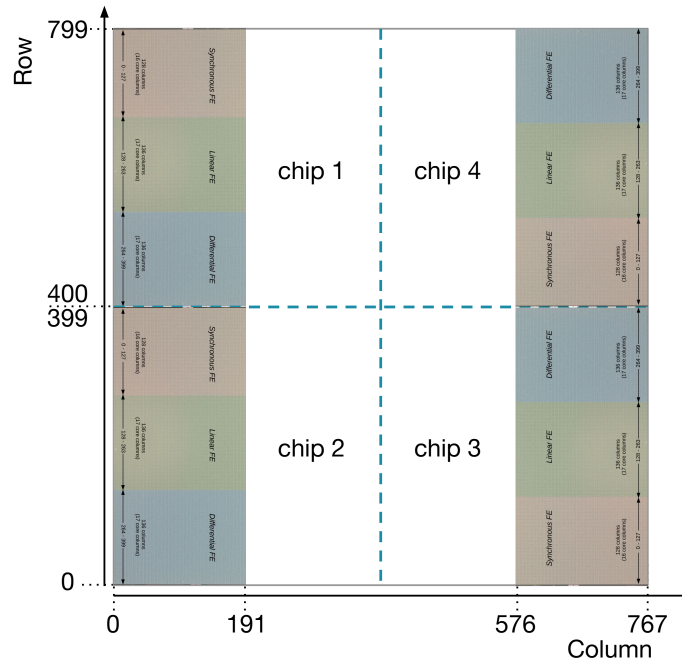


Figure 5.7: A quad module with indicated orientation of the RD53A chips. Pixel (0,0) is located in the bottom left corner.

5.4.1 Digital and analog scan results

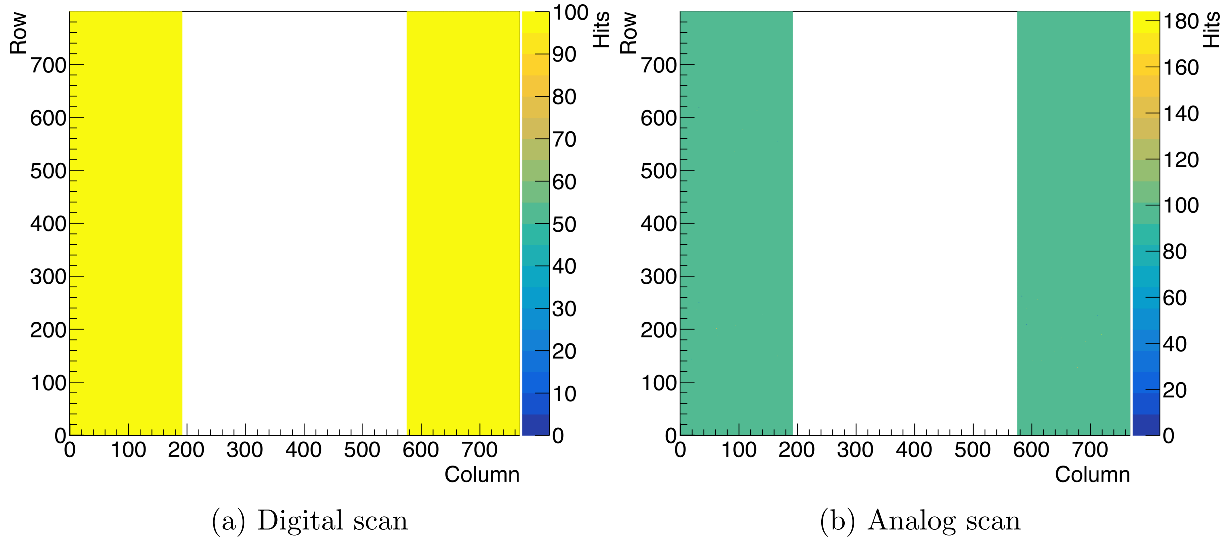
The digital and analog scans are part of the pre-tuning tests and allow to confirm the basic functionality of each chip before proceeding.

The digital scan allows testing of the digital functionality of the chip. The scan consists of injecting 100 digital pulses into the digital circuit of each pixel. The example occupancy map obtained with the digital scan for one of the tested modules is shown in Figure 5.8a, with all pixels showing 100% detection efficiency of injected pulses.

The analog scan allows the identification of pixels with failing analog circuit of each pixel. This scan is similar to the digital scan, where 100 analog pulses of high charge are injected into the configured analog circuit of the pixel. The example occupancy map obtained with the analog scan for one of the tested modules is shown in Figure 5.8b, where the majority of pixels show 100% detection efficiency of injected pulses with few noisy pixels.

Pixels failing the digital and analog scans are grouped into categories following the criteria given in Table 5.2.

None of the tested modules have chips with pixels failing the digital scan. The results of the analog scan were analyzed separately for each front-end flavor. The expressed results are calculated by dividing the number of identified pixels in each category by the total number of pixels of the investigated front-end flavor. Most relevant are the results for the differential front-end chosen for the final ITkPix chip. No pixels with failing analog functionality are observed for the synchronous front-end. The results for the remaining two



(a) Digital scan

(b) Analog scan

Figure 5.8: Example of occupancy map obtained with a) the digital scan and b) the analog scan for the MPP002 module. Few noisy pixels in the linear front-end are identified with the analog scan.

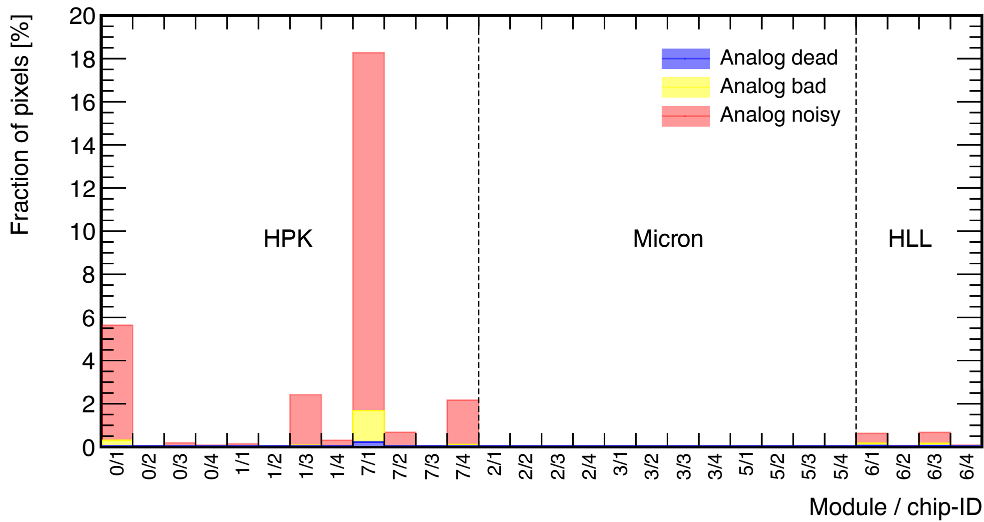
Table 5.2: The analysis criteria used for digital and analog scan results to identify failing pixels. These criteria were based on the IBL stave quality assurance criteria [74].

Failure category	Criteria
Dead pixel	Occupancy $< 1\%$
Bad pixel	$1\% <$ Occupancy $< 98\%$
Good pixel	$98\% \leq$ Occupancy $\leq 102\%$
Noisy pixel	Occupancy $> 102\%$

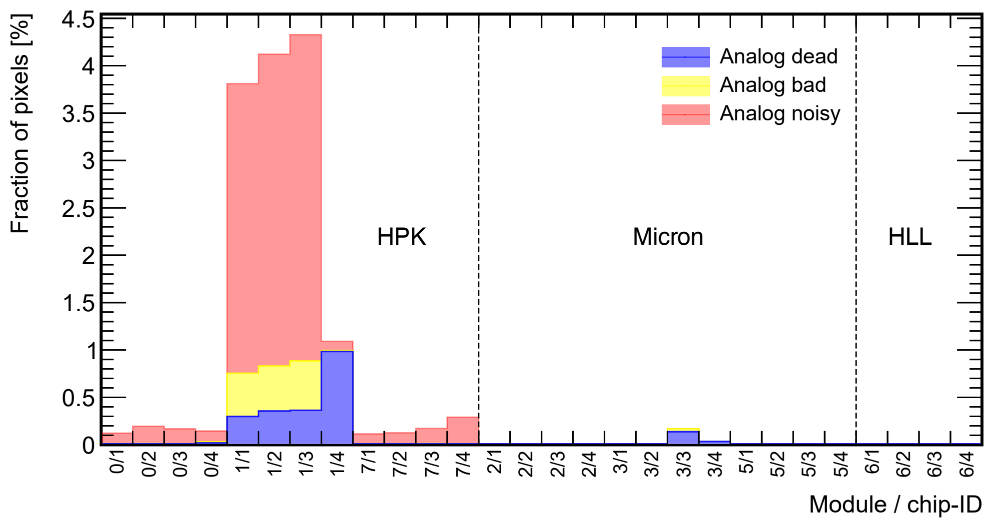
front-end flavors are shown in Figure 5.9, with stacked numbers of failing pixels in each category and as a function of the tested chip. Chips connected to the HPK sensors show higher numbers of noisy pixels for both front-end types than the chips bump-bonded to a sensor from the other two sensor manufacturers. This is the most visible for the module MPP001 where around 4% of pixels are failing the analog scan for the differential front-end of all but one chip, and one chip of the MPP007 module with 18% failing pixels this time for the linear front-end. From the remaining chips, the highest failure rates are observed for two chips connected to the HLL sensors, with 0.7% of linear font-end pixels failing the analog scan. The behavior of these pixels improves after the threshold tuning.

5.4.2 Threshold and ToT tuning

The threshold and ToT scans are part of the post-tuning tests. They allow to verify the quality of the tuning procedure. The synchronous front-end is tuned to 2500 e, while the



(a) Linear front-end



(b) Differential front-end

Figure 5.9: Histogram showing the per chip number of failing pixels in each category identified by the analog scan for a) the linear front-end and b) the differential front-end. The modules containing sensors from the same manufacturer are grouped together, see Table 5.1. The horizontal axis uses shortcuts for the chip identifier, e.g. MPP002/chip 1 reads 2/1.

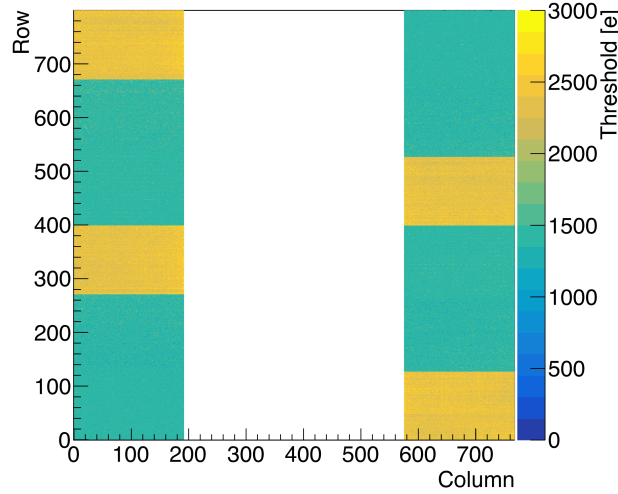


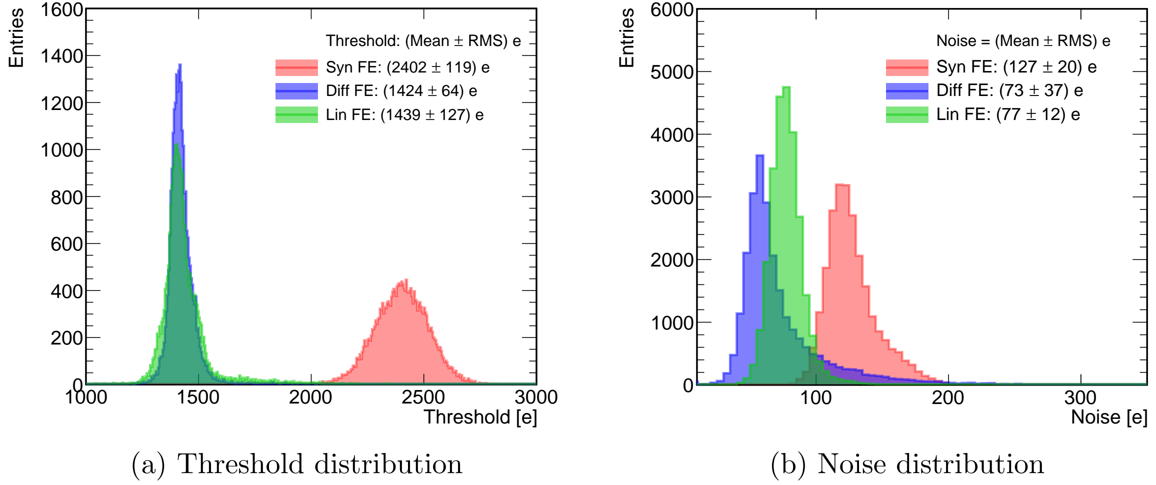
Figure 5.10: Example of the threshold map for module MPP002 after the front-end tuning to 2500 e (synchronous) and 1500 e (differential and linear) for the threshold.

linear and differential front-ends are both tuned to 1500 e. Figure 5.10 shows the achieved threshold for the different front-end flavors after the tuning.

The threshold and noise distributions for different flavors of one readout chip are shown in Figure 5.11, with indicated mean and RMS. Pixels for which the threshold tuning failed are excluded. The threshold distribution for the differential front-end is narrow around the mean threshold value. For the linear front-end, the distribution is slightly wider with a long tail towards higher thresholds. Although the threshold scan indicates a successful tuning, the distribution mean values are below the target threshold value. The corresponding mean noise varies between 73.0 ± 0.2 e for the differential up to 127.3 ± 0.1 e for the synchronous front-end. A long tail towards higher noise is observed for the differential front-end.

The mean threshold and corresponding noise values as a function of the tested chip are given in Figure 5.12 for the differential front-end. The overall mean values are also indicated in these figures. Values for mean and RMS are calculated using the entire distribution and in addition for the central 95% of the data, to better visualize the contribution of the outliers. Figure 5.12a shows consistent thresholds, however they are significantly below the target value for all tested chips. Tested chips bump-bonded to the HPK sensors have larger RMS values due to long tails present in these threshold distributions. This effect is mostly eliminated by considering 95% of the events and the resulting RMS are compatible with chips connected to the other two sensor types. Figure 5.12b indicates that the mean noise depends on the sensor type. A mean value of about 70 e is observed for modules with Micron or HLL sensors, while about twice that is observed for modules with HPK sensors for the same target threshold and front-end flavor.

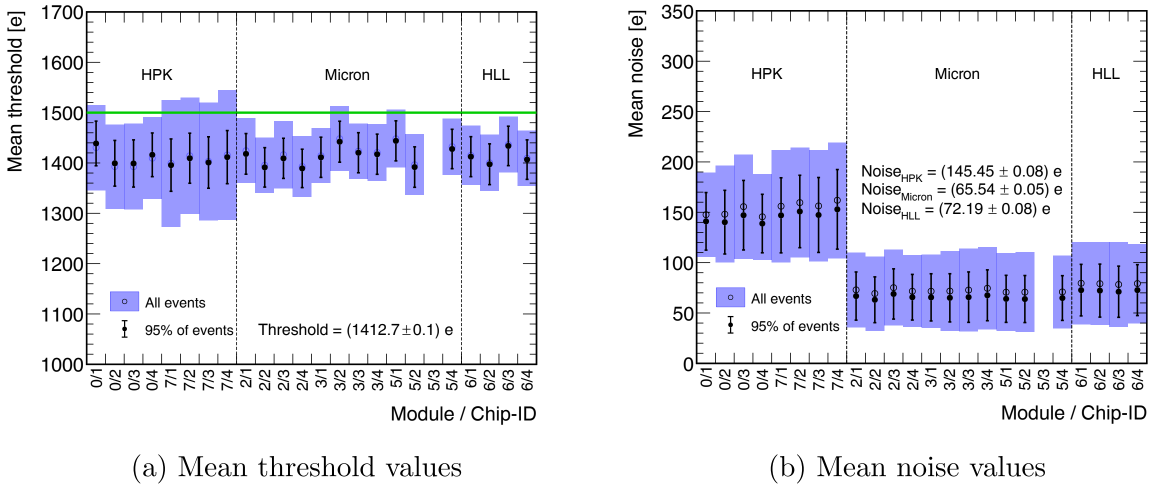
The target ToT value is 7 bc for 10000 e for all three front-end flavors. The mean ToT map for one tested module after the tuning, given in Figure 5.13, shows a uniform ToT response over the entire module area. The individual ToT distributions per front-end flavor are given



(a) Threshold distribution

(b) Noise distribution

Figure 5.11: a) Threshold and b) noise distribution of all three front-end flavors for one readout chip (MPP002/chip 1). The values listed are the mean and RMS.



(a) Mean threshold values

(b) Mean noise values

Figure 5.12: Mean a) threshold and b) noise as a function of the tested chip for tuned differential front-end. The uncertainties are indicating the RMS for the entire distribution and additionally for the central 95% of the data. For all tested chips the values listed in the figures are the mean and the statistical uncertainty in this mean.

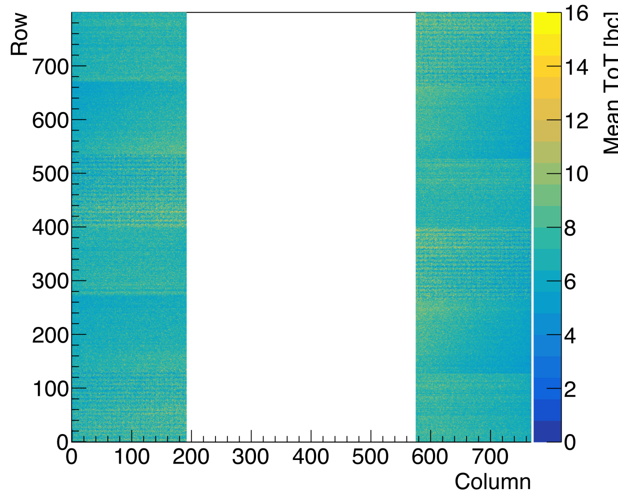
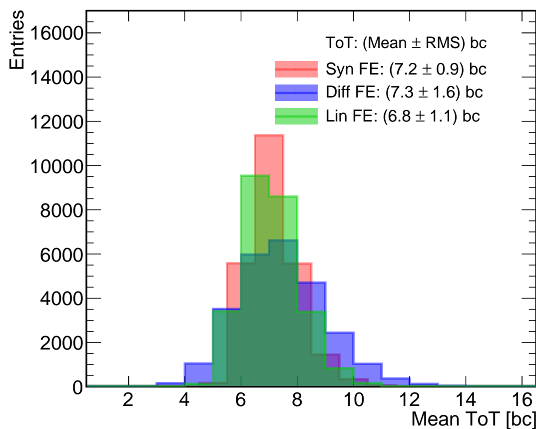
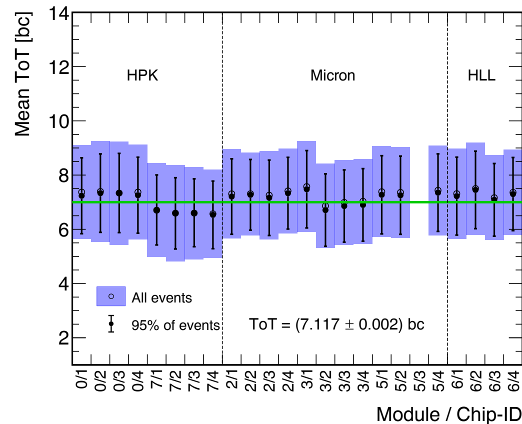


Figure 5.13: Example of the mean ToT map for module MPP002 after the ToT tuning to 7 bc for 10 ke.

in Figure 5.14a, with indicated mean and RMS. Although all three front-ends are tuned to the same target value, the distributions differ in their mean and widths. The average ToT as a function of tested chip for the differential front-end are given in Figure 5.14b, showing similar performances for all tested chips. The mean and RMS values are calculated for the entire distribution and in addition for the central 95% of the data.



(a) ToT distribution



(b) Mean ToT value for all tested chips

Figure 5.14: Figure a) shows the ToT distribution per front-end flavor for one tested chip. Listed values are the mean and RMS. Figure b) shows the average ToT value as a function of tested chip for the differential front-end. Here the uncertainties are indicating the RMS for the entire distribution and the central 95% of the data, while the listed value is the mean and the statistical uncertainty in this mean.

The mean and the uncertainty in this mean after the threshold and ToT tuning for all tested chips and different front-end flavors are summarized in Table 5.3. As for the differential front-end, the mean threshold is below the target value for the other two front-end flavors. For all front-end types the achieved ToT values after the tuning are close to the target value.

Table 5.3: The mean and the statistical uncertainty in this mean for the threshold and ToT per front-end for all tested chips.

Front-end flavor	Threshold [e]	ToT [bc]
Differential	1412.7 ± 0.1	7.117 ± 0.002
Linear	1403.9 ± 0.1	6.793 ± 0.001
Synchronous	2394.1 ± 0.1	7.043 ± 0.001

The mean noise and the uncertainty in the mean for chips connected to a sensor from the same manufacturer are summarized in Table 5.4. For all three front-end types, the mean noise observed for chips bump-bonded to the HPK sensors are about twice that of the chips connected to other two sensor types. The lowest noise is observed for chips bump-bonded to Micron sensors.

Table 5.4: The mean noise and the statistical uncertainty in this mean per front-end flavor calculated for chips connected to the same sensor type.

Front-end flavor	Noise [e]		
	HPK	Micron	HLL
Differential	145.45 ± 0.08	65.54 ± 0.05	72.19 ± 0.08
Linear	184.61 ± 0.03	76.54 ± 0.02	80.89 ± 0.03
Synchronous	270.31 ± 0.04	132.33 ± 0.04	139.47 ± 0.05

Besides verifying the tuning procedure, the threshold and ToT scans were used to identify the number of pixels per front-end with failed or bad tuning. The results following the criteria listed in Table 5.5 are shown in Figure 5.15.

The number of failing pixels depends on both the type of the sensor and the front-end flavor. The synchronous front-end has the least amount of pixels failing the threshold tuning, Figure 5.15a. Here the exception is module MPP007/chip 2 with a significantly higher number of failed pixels. For the remaining chips, differences are observed based on the sensor type. For chips connected to the HPK sensors, on average 0.70 ± 0.04 % of tested front-end pixels failed the tuning procedure, while this number is around 0.11 ± 0.01 % for the remaining chips. For the linear front-end, the distribution of badly tuned pixels is uniform over all tested chips with an average of 0.69 ± 0.02 %, Figure 5.15b. An additional contribution of pixels failing the threshold tuning is observed for chips bump-bonded to HPK sensors. Among the three front-end flavors, the highest number of failing pixels is observed for the differential front-end, Figure 5.15c. Here the S–curve fitting failed for around 3.6 ± 0.2 % of tested front-end pixels, regardless of the sensor type they are bump-bonded to. In addition, 1.6 ± 0.2 % of pixels failed the ToT tuning for chips connected

Table 5.5: The analysis criteria used to identify pixels failing threshold or ToT tuning [74]. The quantity T_{pix} refers to the single pixel threshold, T_{mean} and σ are mean and RMS of the threshold distribution.

Failure category	Criteria
Failed S–curve fit	Fit status is 0 or 4
Bad threshold tuning	$T_{\mathrm{pix}} > T_{\mathrm{mean}} + 5\sigma$
Bad ToT tuning	ToT = 0 bc or ToT = 15 bc

to HPK sensors, while this is not observed for the other two sensor or front-end types. Therefore, in the prototype implementation, the front-end flavor chosen for the production chip version performs the worst.

The distribution of pixels failing the threshold scan is not uniform over the pixels of the differential front-end. The information about successful or failed threshold tuning for each pixel is mapped onto a single core of 8×8 pixels. The obtained result is shown in Figure 5.16. Pixels for which the threshold tuning failed are mostly found in the first and last columns of the pixel core. This points to the discovered issue of a missing buffer element between the discriminator output of the differential front-end and the input of the digital pixel logic for some pixels in the core, which creates a significant capacitive load on the discriminator output.

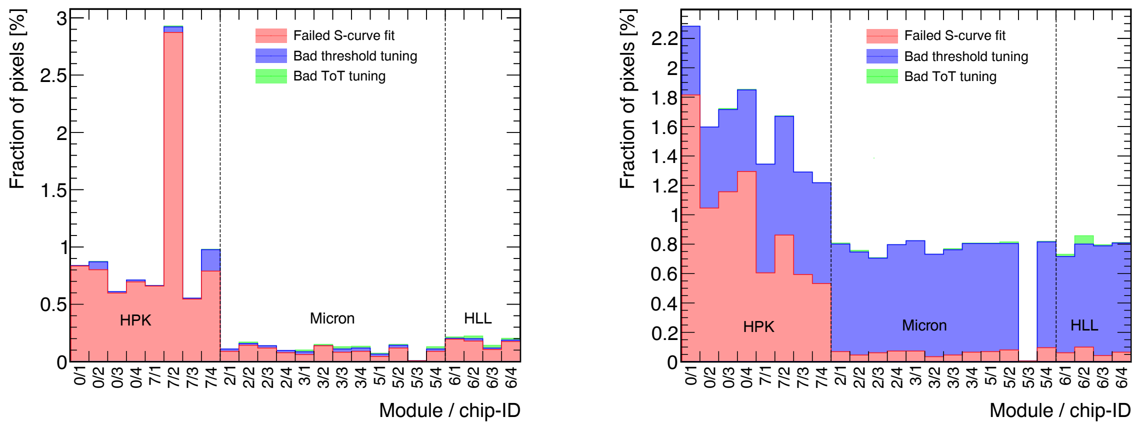
This parasitic capacitance leads to the degradation of the timing and ToT performances of affected pixels [75]. As a consequence not only the tuning is likely to fail for a subset of pixels, but their performance in terms of noise is also affected. For successfully tuned pixels, the mean noise as a function of the location of the pixel in the core is shown in Figure 5.17, separated into the sensor type, see Table 5.4. Hence, the results for chips connected to HPK sensors are shown in Figure 5.17a, while the results for Micron and HLL sensors are displayed together in Figure 5.17b. In both cases, the same group of pixels with excess noise is observed. Their location in the core agrees with that of the pixels with a missing buffer element. These pixels contribute to the long tails observed in the noise distributions of the differential front-end.

After fixing the observed issue, the performance of the differential front-end in the final chip version is expected to be much improved.

5.4.3 Bump-connectivity tests

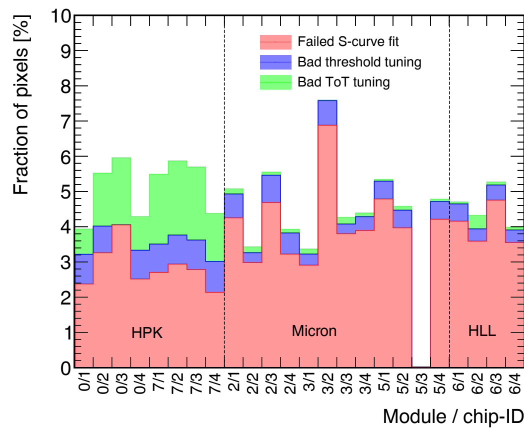
Two types of bump-connectivity tests were performed before and after the thermal cycling:

- crosstalk scan;
- source scan.



(a) Synchronous front-end

(b) Linear front-end



(c) Differential front-end

Figure 5.15: Histograms showing the number of pixels per category failing the threshold or ToT tunings as functions of the tested chip for all three front-end flavors.

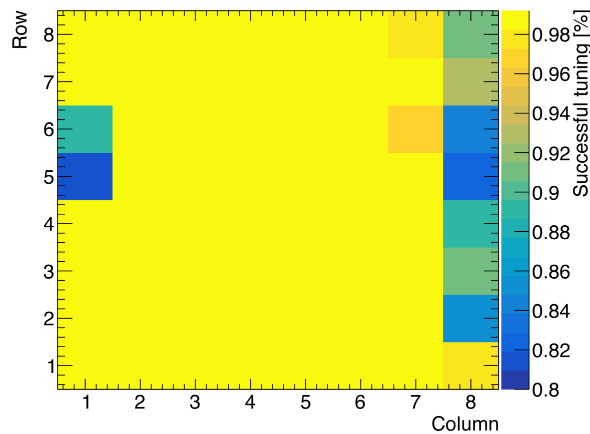
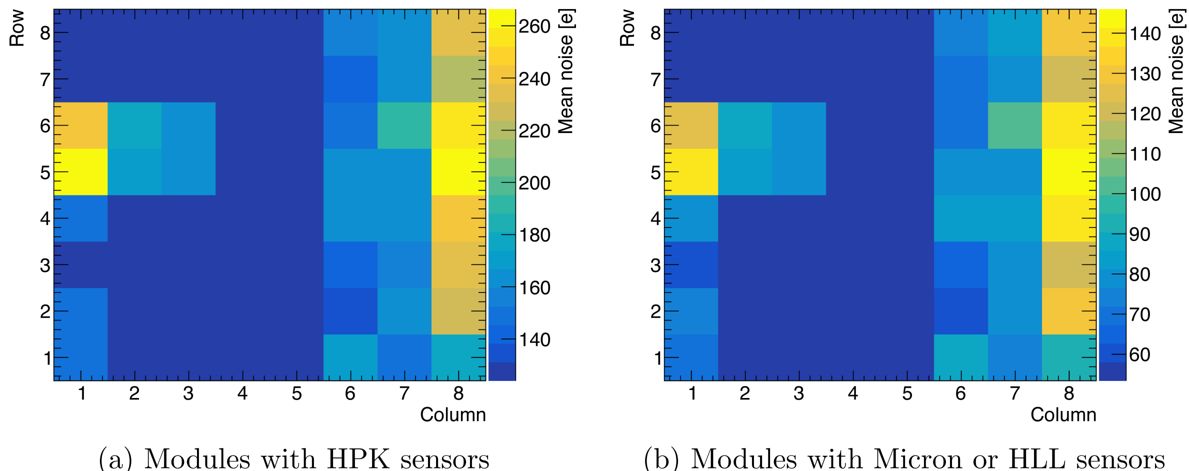


Figure 5.16: Successful threshold tuning as a function of the position of a pixel in a core.



(a) Modules with HPK sensors

(b) Modules with Micron or HLL sensors

Figure 5.17: Mean noise as a function of the position of a pixel in the core. Results are displayed for chips connected to a) HPK and b) Micron or HLL sensors.

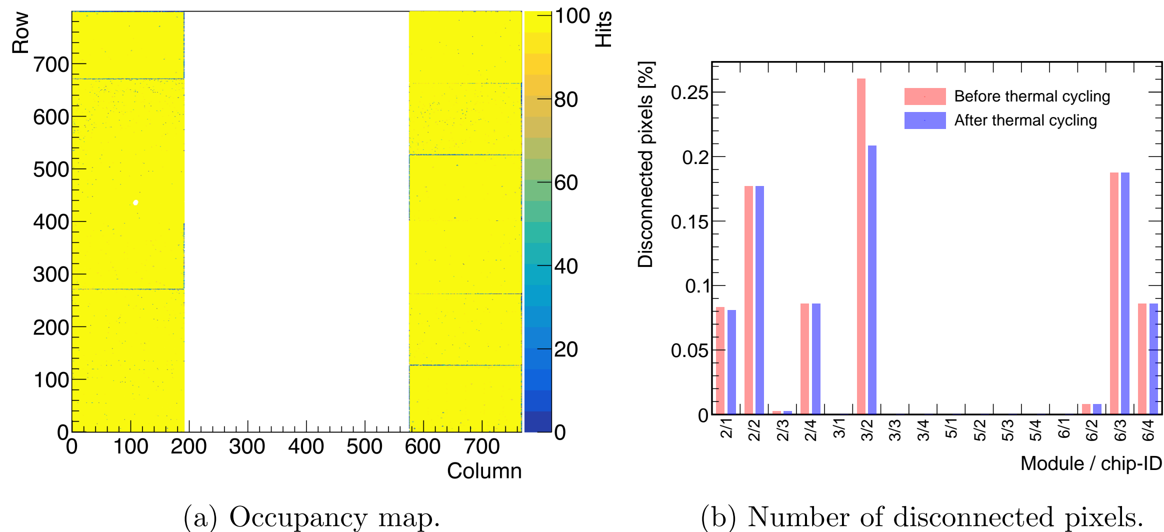
A charge injected into a single pixel can also induce signals in neighboring pixels due to the inter-pixel capacitance. This is referred to as crosstalk, which is unwanted in normal data taking, but can be utilized to identify pixels with disconnected bumps by injecting signals into their neighboring pixels and measuring the occupancy of the central pixel. The absence of crosstalk indicates that the pixel under investigation is disconnected. This scan can identify disconnected bumps only if neighboring pixels are connected and not masked.

The criteria used to identify disconnected bumps are given in Table 5.6. Pixels that were previously identified to fail the digital or analog scans, or the tuning procedures were excluded from this analysis.

Table 5.6: The analysis criteria for disconnected bumps used for the crosstalk scan [74].

Failure category	Criteria
Disconnected bump	Occupancy $< 1\%$
Maybe disconnected/merged bump	$1\% <$ Occupancy $< 98\%$
Connected pixel	$98\% \leq$ Occupancy $\leq 102\%$
Noisy pixel	Occupancy $> 102\%$

Figure 5.18a shows the occupancy map for the crosstalk scan, where many pixels without any or a low number of hits at the border of the tested front-end flavor are observed. As this is a feature of the independently performed scans and not of the readout chip, these pixels were not considered for the analysis. In Figure 5.18b the fractions of disconnected pixels per tested chip before and after the thermal cycling are shown. No increase in these numbers is observed. The largest difference between the two stages is observed for module MPP003/chip 2. The number of disconnected pixels per chip does not exceed 0.3%.



(a) Occupancy map.

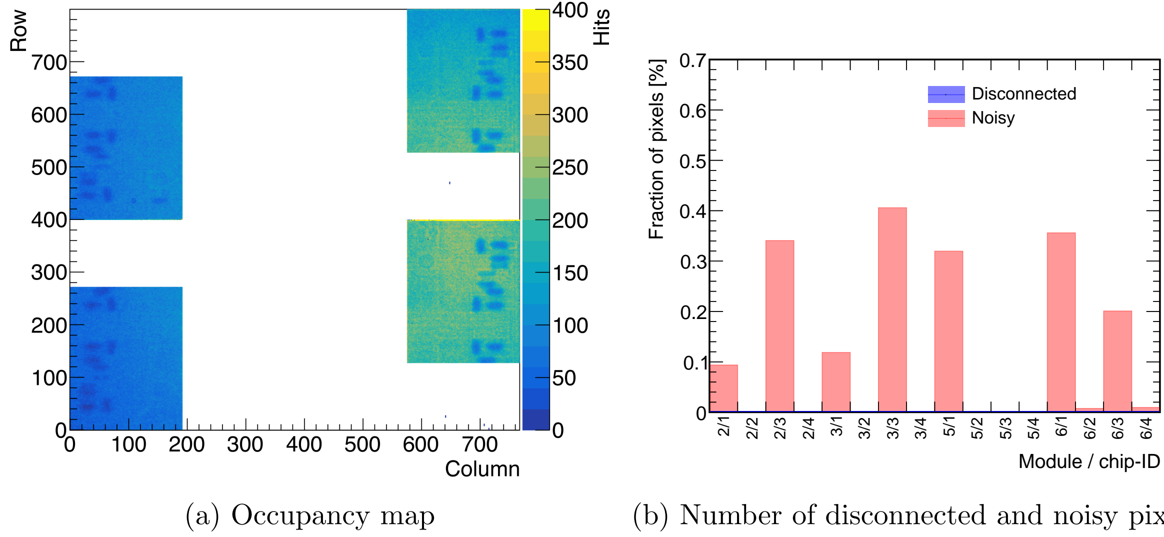
(b) Number of disconnected pixels.

Figure 5.18: Results on the bump-connectivity obtained with the crosstalk scan. Figure a) shows the occupancy map where boundaries between various front-ends are clearly visible, while b) shows the fraction of the disconnected pixels per chip before and after the thermal cycling.

Disconnected bumps can also be identified by placing a radioactive source above a quad module and recording the number of detected hits. For this test, the radioactive ^{90}Sr beta source with an activity of 14 MBq was used and the scan was performed with a random trigger frequency of 200 kHz for two hours. The distance between the source and the quad module was chosen such that all four chips were tested simultaneously, with an average of 50 recorded hits per pixel. The scan was performed for the linear and differential front-ends enabled at the same time. As both front-ends were tuned to the same threshold, the average number of recorded hits should not depend on the front-end flavor. Before using the radioactive source, a noise scan was run to identify and subsequently mask noisy pixels, which are excluded from the analysis. The example of an occupancy map for one of the tested modules is shown in Figure 5.19a. The mean number of hits per chip varies from 60 for chip 2 to more than 200 for chip 4. Most likely the source was placed closer to chips 3 and 4, resulting in higher numbers of hits recorded on these chips. The structures visible in the figure with lower numbers of recorded hits within a chip correspond to locations of the SMD[1] components along the wire bonds. This could be avoided if the scan duration was longer. The criteria used for the source scan are given in Table 5.7.

The criteria is given by the collaboration, but is applicable only if the mean of the hit distribution lies far from the minimum required number of hits per pixel (e.g., mean $\geq 50 + 3\sigma$). However, this was not satisfied for all tested chips. For example, for module MPP002/chip 2 the mean of the hit distribution is around 60 with an RMS of 20. Applying the criteria from Table 5.7 would result in a large number of pixels incorrectly identified as maybe disconnected. Therefore, the focus in this analysis is on the disconnected and noisy pixels.

[1]Surface Mount Devices



(a) Occupancy map

(b) Number of disconnected and noisy pixels.

Figure 5.19: Results on the bump-connectivity obtained with the source scan. Figure a) shows the occupancy map. The structures present correspond to the location of the SMD components on the flex. The synchronous front-end is not used. Figure b) shows the fraction of the disconnected and noisy pixels per chip for the linear and differential front-ends.

Table 5.7: The analysis criteria for disconnected bumps used for source scan. The quantity σ is the RMS of the hit distribution.

Failure category	Criteria
Disconnected bump	Hits $<$ 1
Maybe disconnected/merged bump	1 $<$ Hits $<$50
Connected pixel	$50 \leq$ Hits $\leq$ Mean + 5σ
Noisy pixel	Hits $>$ Mean + 5σ

The obtained results are shown in Figure 5.19b for the linear and differential front-end. No disconnected pixels are observed. The small fraction of noisy pixels observed for chips 1 and 3 of all modules are pixels of the inter-chip region, which are larger and therefore record more hits, a fact that is not accounted for in the specifications. This specification should be adjusted to $50 \cdot (A_\mathrm{p}/(50\ \mu\mathrm{m})^2)$, where A_p is the area of the investigated pixel.

Ideally, both types of bump-connectivity tests should identify disconnected bumps. However, the source scan did not identify any disconnected pixels, while some are indicated by the crosstalk scan.

5.5 Conclusions

The ITk pixel detector will consist of around 10 000 pixel modules. To make sure that the modules installed in the detector fulfill the requirements defined for the detector operation, each assembled module will be electrically characterized. Within this thesis, the experimental setup at the MPP was adapted and used to test eight RD53A quad modules assembled at MPP. These tests provide valuable experience in the procedures and a better understanding of the module behavior.

Due to the different chip versions foreseen for the pre-production, the chip calibration and trimming as well as the module characterization tests need to be modified. The analog scan for the RD53A modules was performed before the threshold tuning. In such case, there is a possibility that pixels identified as bad or noisy have threshold values far from the ideal one. For the tested chips, those connected to the HPK sensors show a larger number of noisy pixels. For chips bump-bonded to Micron and HLL sensors, the total number of failing pixels does not exceed 0.05% and 0.2% per chip, respectively. To more accurately determine the number of pixels failing digital and analog scans, during the pre-production these tests will be performed after the threshold tuning.

The results obtained by performing different scans provide insight into the dependency of the investigated quantities on the type of the sensor to which the readout chip is bump-bonded. This is true for determined noise values that are about twice as high for chips connected to the HPK sensors in comparison with those connected to either Micron or HLL sensors, regardless of the tested front-end flavor. The reason for this is the sensor design, with polysilicon resistors as biasing structure.

Other quantities, like the number of pixels failing the threshold tuning, depend on the front-end flavor. This number is highest for the differential front-end. Most of these pixels are those identified to be implemented with the missing buffer element in the analog/digital interface. The timing performance of these pixels is affected and in addition, they contribute to the long tails towards higher values in the noise distributions. The number of pixels failing the threshold and ToT tuning is around 2% for each of the tested chips.

Two types of scans were used to determine the number of disconnected and merged bumps. The crosstalk scan saves time and allows to avoid testing with a radioactive source. For tested modules, the number of disconnected pixels determined using this method does not exceed 0.3% per chip. After the thermal cycling, no increase in the number of disconnected pixels is observed. However, with this scan, it is not possible to investigate the pixels at the border of the tested front-end flavor, which in the presented results would be classified as maybe disconnected. The results of this scan should be reassessed for modules with ITkPix chips where only the differential front-end is implemented.

The source scan is the most reliable test to determine disconnected pixels. For none of the tested module disconnected bumps were found using this method. The test was optimized to test all chips simultaneously, while achieving a mean of 50 recorded hits per pixel. However, for a large number of pixels, mostly under the SMD components, the minimum required number of hits per pixel was not satisfied. The limit on the scan duration of two

hours was due to time constraints for sending the assembled and tested modules to the loading sites. Hence, the minimum number of recorded hits per pixel could be achieved if the scan duration was longer. For a reliable differentiation between merged bumps and connected pixels the duration should be extended.

6 New framework for test-beam analyses

Detectors for high energy physics experiments are characterized in test-beam measurements, by placing the device under test (DUT) in-between the two arms of a high-precision beam telescope, as discussed in Section 4.3.2. To analyze the performance of tested devices, tracks are reconstructed from recorded hits using a reconstruction framework. This procedure usually includes steps such as decoding and reading-in the raw test-beam data, clustering, software alignment, track reconstruction and final analysis of device properties.

So far, the ATLAS ITk pixel test-beam data have been analyzed using a pair of software packages: EUTelescope [76, 77] was used for the track reconstruction and TBmon2 [78] for the analysis of device properties. The development and support for the EUTelescope package have been discontinued, making this framework unsuitable for future use, as the number of pixel devices with novel features is always growing, requiring highly configurable software for data analysis. The EUTelescope package will be replaced by the Corryvreckan [79, 80] package, a new modular 4D software for the reconstruction and analysis of the test-beam data. The transition to the Corryvreckan framework required modifications and new code developments to analyze the data from ITk pixel modules. In Section 6.1 a brief description of the EUTelescope and TBmon2 packages is given as a basis for the comparison with the new framework, introduced in Section 6.2. As the analysis of test-beam data within this thesis is performed using the Corryvreckan framework, each of the reconstruction and analysis steps, including new developments, are presented in detail in Sections 6.3 and 6.4. The validation of the Corryvreckan framework for ITk pixel test-beam data is presented in Section 6.5.

6.1 EUTelescope and TBmon2

EUTelescope is a modular framework, comprised of a set of independent MARLIN[1] [81] processors written in the C++ programming language. Processors needed for each step of the reconstruction chain are listed in steering template files in the xml data format, while their input parameters are given in a single configuration file for the entire reconstruction chain. A set of external libraries is needed such as the Eigen3 [82] linear algebra library, the Millepede [83] package for the alignment and GBL[2] [84, 85] libraries for the track fitting,

[1]Modular Analysis and Reconstruction for the LINear Collider
[2]General Broken Line

as well as the ROOT [86] package. A typical workflow for data reconstruction consists of the following steps:

- The **data conversion** from the native format of the EUDAQ1 data acquisition system to the corresponding LCIO[3] format using the `EUTelNativeReader` processor. The LCIO event contains all data associated with the physical event, since the event building was performed during the data acquisition step. Within this step, pixels with an occupancy above the user-defined maximum value are identified using the `EUTelNoisyPixelFinder` processor and stored in the noisy pixels database.

- The **clustering** step groups hits close in space that likely belong to a single particle, into clusters. This step is performed using two processors: `EUTelSparseClustering` and `EUTelGeometricClustering`, providing the information of the cluster center index. Clusters that involve or are neighboring noisy pixels are removed from the cluster collection. The `EUTelHitmaker` processor is used to calculate the position of the hit from the cluster center index.

- The **software alignment** allows to achieve a precise alignment of the setup necessary for the track reconstruction. The procedure is divided into two stages: prealignment and alignment. The first stage is done using the `EUTelPreAligner` producer that corrects x and y misalignments of sensors. The final alignment is performed by the `EUTelGBL` processor in alignment mode, by simultaneously fitting the track and alignment parameters of all detector planes. For this step, the positions of the two outermost telescope planes are fixed.

- The **track reconstruction** consists of two steps: track finding and track fitting. Both are performed using the `EUTelGBL` processor, which expects the beam telescope to consist of six sensors, grouped into an upstream and a downstream triplet. The track finding algorithm starts by building a so-called *doublet*, a straight line track between a hit in the first and a hit in the last sensor of each triplet. To decrease the number of false combination, only doublets that have a slope within a user-defined limit are selected. To build a full track, the algorithm checks if a pair of doublets meets in the middle of the beam telescope within a specified spatial distance. This track finding method relies on multiple parameters that need to be set by the user. These are the maximum allowed:

  – distance of the hit and extrapolated track in the middle plane of each triplet;

  – slope of each doublet;

  – distance between doublets in the middle of the beam telescope;

  – distance of the hit on the DUT and the extrapolated track intercept.

  Track fitting is based on the GBL algorithm, which takes into account the effect of multiple scattering.

[3] Linear Collider Input/Output

The reconstructed data, including matched hits, cluster properties and hit and track position information are stored and later read into TBmon2 for analysis. In addition, two configuration files with general information about analyzed runs, tested devices, and settings for the analyses are required by the TBmon2 software. For each tested device, a geometry file with detailed information about the pixel arrangement is also provided. A typical analysis determines the hit efficiency of the tested device.

6.2 Corryvreckan framework

The Corryvreckan framework is written in the C++ language and employs a flexible, modular design. One of the main features of this framework is an offline event building which allows synchronization of data from detectors with different readout schemes, with or without a trigger, and if provided by a tested detector, use of the hit timing information in the clustering and tracking step. An additional advantage of the Corryvreckan framework is that it only depends on one external package, the well-maintained ROOT software.

6.2.1 Coordinate system

The global coordinate system for the entire setup is defined as a right-handed Cartesian coordinate system, with the positive z-axis along the beam direction, as described in Section 4.3.2. The local coordinate system is defined for each detector also as a right-handed Cartesian coordinate system, with the origin in the center of the pixel matrix, and the z-axis pointing to the readout side of the detector. This corresponds to the $\pm z$ coordinate of the global coordinate system.

6.2.2 Configuration

The reconstruction and analysis chain of the Corryvreckan framework and the detector geometry are configured with two text files: the *main* and *detector* configuration files, both based on the simplified version of the TOML [87] format.

Main configuration file

The main configuration file contains global parameters and the workflow of the reconstruction chain. An example of a Corryvreckan main configuration file is shown in Figure 6.1a The main configuration file starts with a `[Corryvreckan]` section that holds all global parameters, like the output directory, the path to the detector configuration file, and the name of the root file in which the results will be stored. Each following section represents a software module that performs a specific task in the reconstruction chain, followed by its configurable parameters. All global parameters as well as all configurable parameters

```
[Corryvreckan]
output_directory = "output"
detectors_file  =
"geometries/start.geo"
histogram_file = "output.root"

[EventLoaderEUDAQ]
file_name = "dataset.raw"
long_detector_id = false

[ClusteringSpatial]

[Correlations]

[Tracking4D]
momentum = 5.0GeV
track_model = "gbl"
spatial_cut_abs = 100um, 100um
exclude_dut = true
min_hits_on_track = 6
```

(a)

```
[planeID]
mask_file = "mask_planeID.txt"
material_budget = 0.00897
number_of_pixels = 400, 192
orientation = 0deg, 0deg, 0deg
orientation_mod = "xyz"
pixel_pitch = 50.0um, 50.0um
position = 0mm,0mm,422.00mm
spatial_resolution = 14.4um, 14.4um
time_resolution = 200ns
role = "dut"
type = "Rd53a"
```

(b)

Figure 6.1: Examples of Corryvreckan configuration files: a) main configuration file b) definition of an RD53A single-chip card in the detector configuration file.

available for each module are listed in the user manual [88]. For each recorded event, these modules are executed in the order specified in the main configuration file.

Detector configuration file

The detector configuration is divided into sections, each declared by the section header given in square brackets, containing parameters to describe detector properties such as the number and size of pixels as well as their position and rotation in the global coordinate system. The section header is used for the detector identification in the reconstruction chain. One section of the detector configuration file describing an RD53A single-chip card is shown in Figure 6.1b. Within the detector definition, a path to the file containing a list of masked pixels can be given. If `spatial_resolution` parameter is not specified, the intrinsic resolution of pitch/$\sqrt{12}$ will be assumed. The `material_budget` parameter allows to indicate the components of the DUT taken into account in the track reconstruction, and affects the tracking performance. The `time_resolution` parameter allows to include timing information, if provided by a tested detector or used data acquisition framework, in the clustering and track reconstruction step. The parameter `role` is of special importance as it specifies the behavior of the detector in the reconstruction chain. It can be configured as `role=`:

- `"dut"`: Device Under Test;
- `"reference"`: reference detector in respect to which software alignment is performed;

- `"passive"`: passive detector used as dead material in the track reconstruction;
- `"aux"`: auxiliary device that provides additional information for an event building but does not participate in the reconstruction, e.g. a Trigger Logic Unit.

6.2.3 Quad detector class

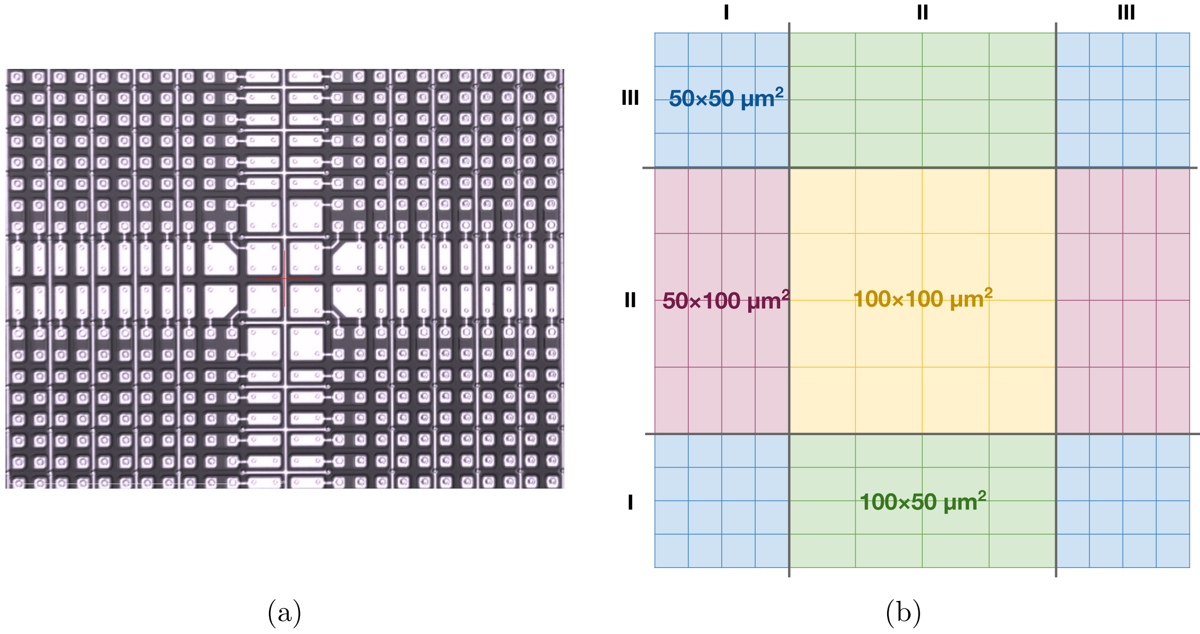
In the Corryvreckan framework any pixel detector by default has a uniform pixel matrix, with the pixel size specified in the detector configuration file. However, this is not the case for ITk pixel quad modules. In Figure 6.2a the so-called inter-chip region is shown, which refers to four middle columns and rows of the sensor. These are required to implement an active sensor region within the gap between chips bump-bonded to the quad sensor. To achieve this they contain pixels of different sizes, in comparison to the default 50×50 µm^2 pixel. These different pixel sizes are illustrated in a simplified way in Figure 6.2b.

A pixel detector with a uniform pixel matrix is defined by the `PixelDetector` geometry class of the Corryvreckan framework. This class defines the size of the detector, the in-pixel position of the track intercept and all functions that allow expressing the hit/track intercept position either in the local coordinate system, or by column and row indices. When using this class, the local hit position and in-pixel position on a quad module would be calculated incorrectly, with a shift of up to 100 µm. This would affect the software alignment and hit efficiency determination.

As a part of this thesis, a new detector class called `ITkPixQuad` has been developed in the Corryvvreckan framework, which can be used to describe the geometry of the quad sensor. In both dimensions, the sensor is divided into three regions as indicated in Figure 6.2b. If a pixel column index lies within region II, the pixel dimension in x will be 100 µm, otherwise it is 50 µm. The same holds for the y dimension. To take into account the non-uniform pixel matrix of quad sensors, several functionalities are modified. These are the calculation of:

- the local position from the column and row indices;
- the column and row indices from the local position;
- the sensor size;
- the in-pixel position from the local position, or column and row indices;
- the spatial resolution based on the pixel dimensions.

The quad module will be considered in the Corryvreckan framework instead of the pixel detector with a uniform pixel matrix by defining `coordinates = "cartesian_itkpixquad"`.



(a) (b)

Figure 6.2: Figure a) shows the enlarged view of the inter-chip region of the planar quad sensor. The square pads in the center have dimensions 100×100 µm². Figure b) shows this inter-chip region with the various pixel sizes, indicated by the colors.

6.3 Data reconstruction

In this section, each step of the typical reconstruction chain for the ITk pixel test-beam data will be described. The example of the reconstruction and analysis flow, after the masking of the noisy pixels (Section 6.3.2) and the software alignment (Section 6.3.5), is illustrated in Figure 6.3. It includes the following software modules:

- the event loader to convert the input data into the pixel objects (Section 6.3.1);
- the clustering module to combine neighboring pixels into clusters (Section 6.3.3);
- the correlation module for data quality control and software alignment verification (Section 6.3.4);
- the tracking module for the track reconstruction using clusters from telescope planes (Section 6.3.6);
- the DUT track association module (Section 6.3.7);
- the analysis modules, to determine the performance of the DUT (Section 6.4).

A given software module in the Corryvreckan framework is equivalent to the corresponding processor of the EUTelescope framework. Many perform the same task. For the transition to the new framework, the first step was to identify software modules that can perform required reconstruction steps and optimize parameter values to achieve satisfying results. Afterwards, a set of main configuration files was created, following the workflow presented

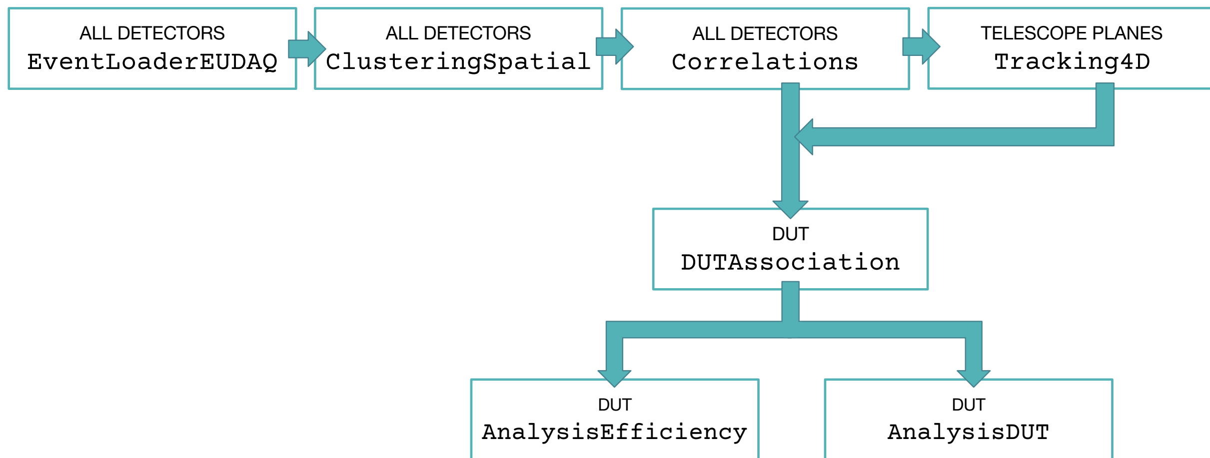


Figure 6.3: The example of test-beam data reconstruction and analysis flow after the masking of noisy pixels and the software alignment. Some software modules are executed for all detectors in the setup, while others only consider telescope planes or DUTs, as indicated in the boxes.

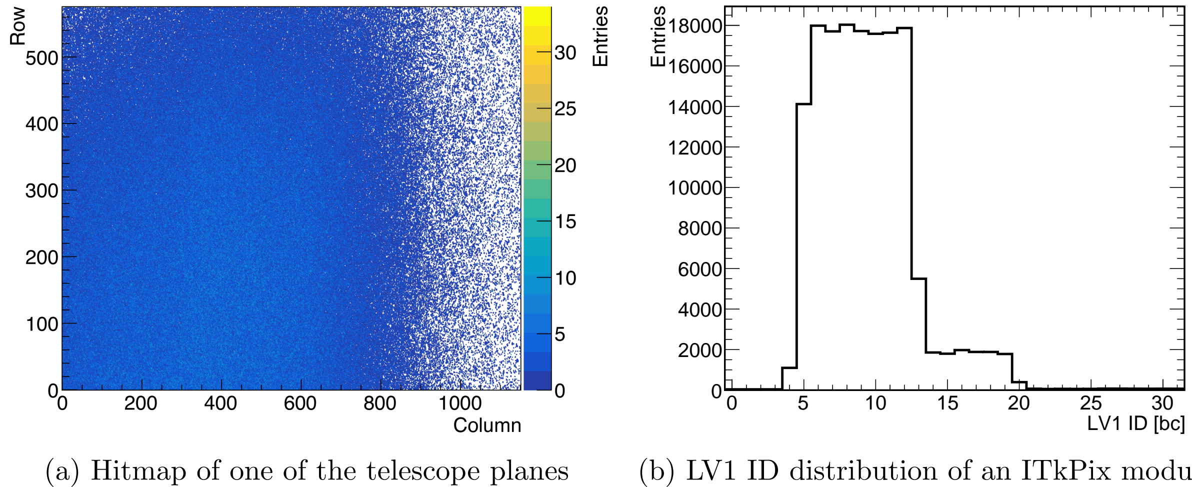
in Section 6.1, to be used for future analyses with minimal modifications, such as the path to the dataset to be analyzed, the beam energy or detector identifications.

6.3.1 Data input

Data can be loaded into the Corryvreckan framework either as raw data or as data objects. To read-in raw data files, several event loader modules are available in the Corryvreckan framework. They depend on the DAQ system used during the test-beam data taking or the tested detectors. As an output of the raw data file processing, the information about the pixel hit parameters are stored as data objects (e.g. pixels, clusters, tracks) for each event on the clipboard, the temporary information storage during the event processing. It is also possible to store the data objects in a root file at any point in the reconstruction chain and read them back into the framework for further analysis using the `[FileWriter]` and `[FileReader]` software modules.

As previously discussed, the data acquisition framework used during the test-beam campaigns is EUDAQ1 (Section 4.4.3). Therefore, the event loader module used for the ATLAS ITk Pixel test-beam data is `[EventLoaderEUDAQ]`. This converts the data from EUDAQ-native raw format to the format readable by Corryvreckan, using the DAQ-specific EUDAQ converter, called the YarrConverterPlugin. The DUT readout system records the data per chip. To read-in the data from quad modules, the YarrConverterPlugin was modified to map the data from four readout chips onto a single detector plane, while taking into account the chip orientation.

Additional modifications were done in the `[EventLoaderEUDAQ]` module. The hit maps were added to allow for data quality control already at the first step of the reconstruction.



(a) Hitmap of one of the telescope planes (b) LV1 ID distribution of an ITkPix module

Figure 6.4: Example of histograms added to [EventLoaderEUDAQ]: a) a hit map b) an LV1 ID distribution of an ITkPix module, where each bin represents a time frame of 25 ns length. In the case of Mimosa26 detectors, one time frame corresponds to 115.2 µs, i.e. to about 4600 bc.

In the case of ITk pixel modules, for each trigger, there is the LV1 ID time window for data taking, which consists of 32 time frames (bunch-crossings) in unit of 25 ns. This information is available in the raw data, but originally was not passed to the Corryvreckan framework. Therefore, an additional parameter was added to the [EventLoaderEUDAQ] module, called `use_eudaq_frames` that, if set true, will allow the assignment of the corresponding LV1 ID to each recorded hit. In addition, LV1 ID distribution histograms are created for each detector.

Example figures added to the [EventLoaderEUDAQ] software module are shown in Figure 6.4. Figure 6.4a shows the hit map of one of the telescope planes. The area with a non-uniform hit distribution is due to the beam profile, as the beam spot was not at the center of this Mimosa26 sensor. Figure 6.4a shows of the LV1 ID distribution of an ITkPix module, with around 90% of hits collected within 9 time frames (5-13) and a long tail to larger LV1 IDs.

6.3.2 Noisy pixel treatment

The raw data loaded into the Corryvreckan framework contain hits created by particles and noise hits that cannot be distinguished per se. For the data reconstruction, it is important to eliminate noise hits. Therefore, a pre-processing step is performed to mask pixels, either because they are classified as noisy, or because they were already disabled during the chip tuning.

Noisy pixels are masked using the so-called `frequency` method of the [MaskCreator] software module. Using this algorithm, for each detector in the setup, pixels that record

more hits than the freely chosen parameter multiplied by the average number of hits per pixel are identified and added to the respective mask file. The same step is performed in the EUTelescope framework. Here, this method is only used for the treatment of noisy pixels on the telescope planes. The DUTs are treated differently, as follows.

Before the data taking, all noisy pixels of the DUTs are usually excluded during the chip tuning, a procedure explained in Section 3.2.1. At the test-beam, modules were retuned multiple times and the chip configuration files used during the data taking were not always available. Therefore, as a part of this thesis, an additional method is added to the `[MaskCreator]` module, called `mask_dead_pixels`. This is used to identify pixels already masked during the chip tuning as those without any recorded hit over the entire dataset, consisting of either a single run or multiple runs. Those are added to the previously created mask file. The same masking method is used in the analysis with the TBmon2 software.

6.3.3 Cluster formation

A particle traversing through a silicon detector will release free charge carriers that move towards the electrodes due to the applied bias voltage. As a result of charge sharing, a signal may be created in more than one pixel by the same particle. Therefore, in the next step of the reconstruction chain, the module `[ClusteringSpatial]` is used to group all hit pixels close in space into clusters. For the x dimension, the index of the cluster center position $\overline{n}$ is calculated using the charge-weighted center-of-gravity method as:

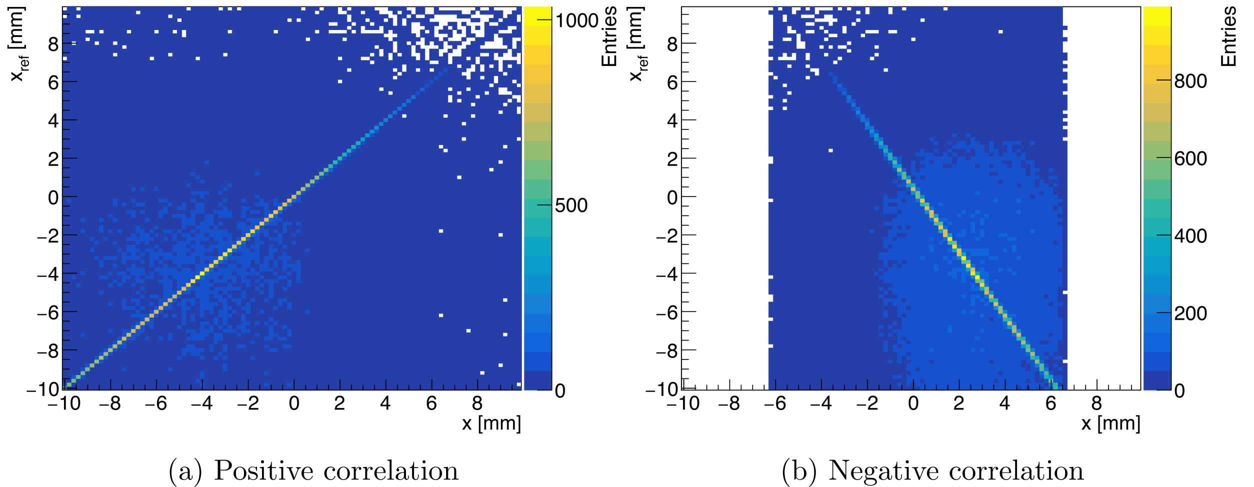
$$\overline{n} = \frac{1}{Q} \sum_{i=1}^{N} n_{\mathrm{i}} \cdot q_{\mathrm{i}}, \tag{6.1}$$

where n_{i} and q_{i} refer to the column index (starting from zero) and recorded charge of the i-th pixel in the cluster, Q is total charge and N is the cluster size. If the information about the recorded charge is not available, the cluster center position is calculated using the arithmetic mean. The index of the center position of the cluster is converted to the hit position in local coordinates x_{hit} (with the origin in the center of the sensor) as:

$$x_{\mathrm{hit}} = x_{\mathrm{pitch}} \cdot (\overline{n} - (N_{\mathrm{x}} - 1) \cdot 0.5), \tag{6.2}$$

where x_{pitch} and N_{x} are the pixel size and number of pixels in x dimension, assuming a uniform pixel matrix. In the case of the quad module, Eq. 6.2 is modified in the following way:

$$x_{\mathrm{hit}} = \begin{cases} x_{\mathrm{pitch,IC}} \cdot N_{\mathrm{x,IC}} \cdot (-0.5) + x_{\mathrm{pitch}} \cdot (\overline{n} - (N_{\mathrm{x}} - N_{\mathrm{x,IC}} - 1) \cdot 0.5) & \text{for} \quad \text{hit} \in \text{I} \\ x_{\mathrm{pitch,IC}} \cdot (\overline{n} - (N_{\mathrm{x}} - 1) \cdot 0.5) & \text{for} \quad \text{hit} \in \text{II} \\ x_{\mathrm{pitch,IC}} \cdot N_{\mathrm{x,IC}} \cdot 0.5 + x_{\mathrm{pitch}} \cdot (\overline{n} - (N_{\mathrm{x}} + N_{\mathrm{x,IC}} - 1) \cdot 0.5) & \text{for} \quad \text{hit} \in \text{III}, \end{cases} \tag{6.3}$$



(a) Positive correlation

(b) Negative correlation

Figure 6.5: Example of correlation figures for the x coordinate.

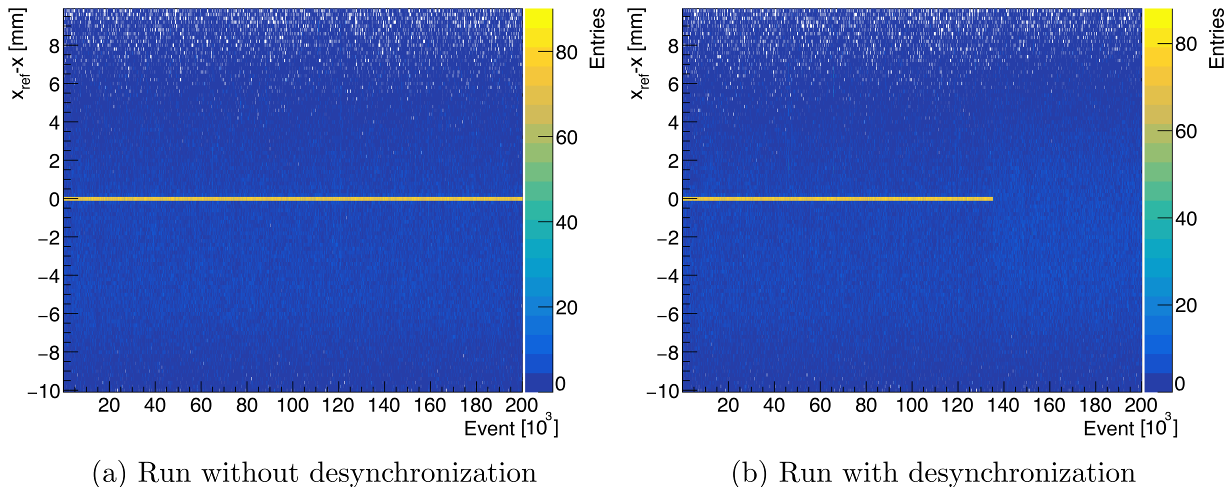
where $N_{\text{x,IC}}$ is the number of pixels of the inter-chip region per row, $x_{\text{pitch,IC}}$ is the largest dimension of the pixel in the inter-chip region, and I, II and III refer to regions indicated in Figure 6.2b. The intrinsic spatial resolution of detectors defines the uncertainty in the calculated hit position and influences the tracks χ^2. For quad modules the hit position uncertainty will vary based on the pixel size.

6.3.4 Correlations

The correlation histograms provide important information for both orientations of the detectors and the overall data quality control. The correlations can be calculated at any stage, by calling the `[Correlations]` software module in the main configuration file. For the same coordinate of two devices synchronized in time, diagonal structures as those shown in Figure 6.5 are visible. In the Corryvreckan framework these figures are created with respect to the reference plane. The positive correlation indicates that devices have the same orientation (Figure 6.5a), while an anti-correlation means that the device is mirrored in that coordinate with respect to the reference plane, which should be corrected for in the detector configuration file (Figure 6.5b). If no diagonal structure is visible for the same coordinate of two devices, one should investigate the x versus y correlation figures, where an existing correlation would indicate a 90° rotation around the z-axis. Uniform hit distributions in all figures indicate that devices are not synchronized in time.

The desynchronization can happen during the data taking. To be able to identify if and at which point this occurred, additional figures are added to the `[Correlations]` module, in which the differences between the cluster positions at each detector and the reference plane are calculated in both directions:

$$\begin{aligned} \Delta x &= x_{\text{ref}} - x \\ \Delta y &= y_{\text{ref}} - y \end{aligned} \tag{6.4}$$



(a) Run without desynchronization

(b) Run with desynchronization

Figure 6.6: Difference of the cluster position in x and its reference as a function of the event number, for a) a good run and b) a run in which a desynchronization is observed.

and displayed as a function of the event number. Example figures for two different runs taken with the same configuration, are given in Figure 6.6.

Figure 6.6a shows a structure around zero throughout the entire run, indicating synchronous data taking. Figure 6.6b shows the same structure up to the event number $135{\cdot}10^3$. From this event onwards, the hit distribution is uniform. This indicates the point at which the desynchronization happened, and subsequent events should not be considered for the analysis.

6.3.5 Software alignment

For all detectors, the raw data contain only basic pixel hit information, such as the column, row, charge (in units of the ToT) and timestamp. The information about the position and orientation of the detector planes is provided to the reconstruction framework with a precision of about 1 mm, which is not sufficient for precise tracking. Therefore, a software alignment is performed to ensure a high-precision calculation of the track intercepts with all detector planes. As for the EUTelescope framework, the software alignment is performed in two stages: prealignment and alignment.

Prealignment

For the first stage of the software alignment the module `[Prealignment]` in the Corryvreckan package is used, in which the difference between the cluster position at each detector and the reference plane is calculated using Eq. 6.4 as in the `[Correlations]` module. By applying the shift which corresponds to the largest calculated difference, the

positions of the detectors transverse to the beam are adjusted with a precision of a few hundred µm. The final output of the prealignment stage is an updated detector configuration file.

Alignment

The output detector configuration file of the prealignment stage and large spatial matching criteria (multiples of the pixel size) allow to perform a first track reconstruction. This is used as an input to the second stage of the alignment, where the prealignment is refined including the three rotations. The track reconstruction is performed using only telescope planes. The track model is a configurable parameter and affects the result of the alignment (for details see Section 6.3.6).

Telescope planes are aligned simultaneously using the `[AlignmentTrackChi2]` software module, which implements an algorithm that iteratively refits individual tracks and minimizes the track χ^2 values using Minuit2 [89]. The track χ^2 is defined as a quadratic sum of biased residuals (see below) divided by their uncertainties. The procedure of fitting tracks and optimizing the detector positions and orientations, while reducing the spatial matching criteria, is repeated until a sub-micron precision in the change of alignment constants is achieved. Once all telescope planes are aligned, the DUT alignment is performed by using the reconstructed telescope tracks and minimizing the distance between the position of a DUT cluster assigned to the track and the track intercepts with that plane, implemented in the `[AlignmentDUTResidual]` module. The z positions of all detectors cannot be aligned and are fixed to their measured values in the beam area.

Good alignment is indicated by a narrow residual distribution that is centered around 0. The residual distribution is obtained from the distance between the intercept of the track with the detector x_{track} and the position of the associated cluster center x_{hit}, as illustrated in Figure 6.7, hence the residual in x is given by:

$$x_{\text{r}} = x_{\text{track}} - x_{\text{hit}}. \tag{6.5}$$

The standard deviation of the residual distribution is known as the residual width. As an output of the software alignment there are two possible residual distributions: biased or unbiased. The term biased residual describes the situation in which the hit information of the detector under investigation is included in the track reconstruction. The biased residual width can be expressed as:

$$\sigma_{\text{b}}^2 = \sigma_{\text{int}}^2 - \sigma_{\text{tel}}^2, \tag{6.6}$$

where σ_{tel} is the telescope pointing resolution at the detector under investigation. In contrast, the term unbiased means that the hit information of the detector under investigation is not included in the track reconstruction. The unbiased residual width can be expressed as:

$$\sigma_{\text{u}}^2 = \sigma_{\text{int}}^2 + \sigma_{\text{tel}}^2, \tag{6.7}$$

and can be used to estimate the spatial resolution of a tested detector.

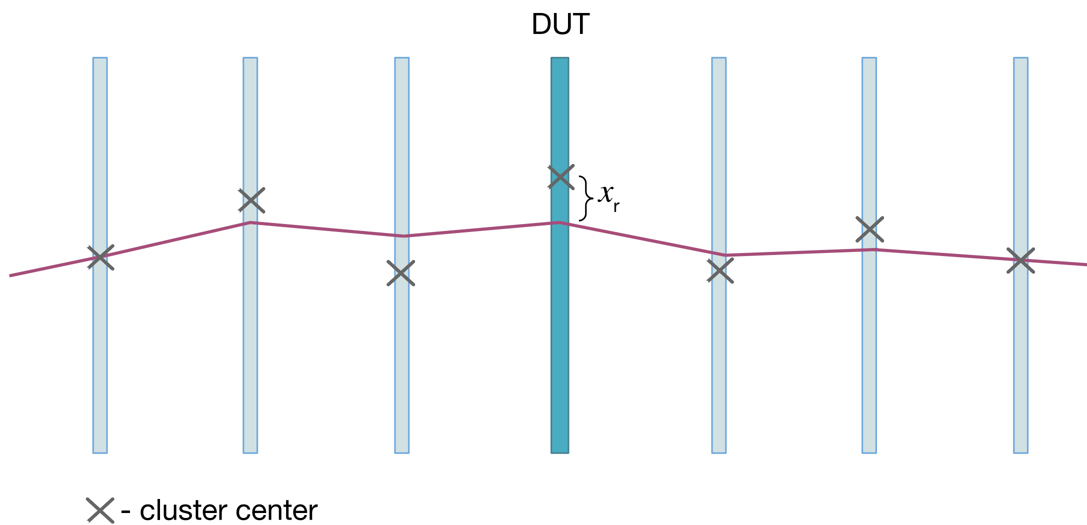


Figure 6.7: Simplified illustration of the track reconstruction performed by the GBL algorithm for a setup with the beam telescope and a single DUT. The cluster center for each detector plane as well as the residual on the DUT are indicated.

6.3.6 Track reconstruction

The track reconstruction is performed in two steps: track finding and track fitting. The biggest difference between the EUTelescope and Corryvreckan test-beam data analysis is in the track finding algorithm. The Corryvreckan tracking module used for the analysis done as a part of this thesis is called `[Tracking4D]`. This track finding algorithm first builds a straight line track candidate by combining clusters on the first and last detector planes that recorded a hit. Clusters on planes in-between are added if they fulfill spatial requirements. Contrary to the many required parameters in the EUTelescope software, to perform track reconstruction in the Corryvreckan framework with the tracking module chosen, the main required parameter is the maximum allowed residual for any plane participating in the reconstruction. This spatial limit can be specified in two ways:

- a single fixed value for all detectors in the setup;
- an intrinsic spatial resolution multiplied by an user-configurable value for each detector in the setup. This is particularly useful if detectors participating in the track reconstruction have different pixel sizes.

In both frameworks the GBL algorithm is used for track fitting, which simultaneously includes uncertainties from the position measurement and from multiple scattering, resulting in a reconstructed trajectory given by a set of lines with kinks at the detector planes as illustrated in Figure 6.7.

The precise track reconstruction requires a correct material budget estimation. The expression:

$$(\frac{x}{X_0})_{\text{total}} = \sum_{i=1}^{N} \frac{x_{\text{i}}}{X_{0,\text{i}}} \tag{6.8}$$

defines the material budget of a given scattering medium as the sum of the physical thicknesses of the materials x_{i} normalized to their radiation lengths $X_{0,\text{i}}$, where N is the number of layers.

6.3.7 DUT track association

To study the performance of the device tested, clusters on the DUT are assigned to the tracks using the `[DUTAssociation]` software module. The spatial limits (x_{limit}, y_{limit}) in both dimensions can be configured. These are compared to the distance between the position of the nearest pixel in a cluster and the track intercept with the DUT plane for both dimensions (x_{dist}, y_{dist}). To associate a cluster to the track, the following condition has to be fulfilled:

$$\frac{x_{\text{dist}}^2}{x_{\text{limit}}^2} + \frac{y_{\text{dist}}^2}{y_{\text{limit}}^2} \leq 1. \tag{6.9}$$

The choice of the spatial limit for the DUT to cluster association has an impact on the hit efficiency calculation. The pixel of the cluster that is nearest to the track intercept is compared to the track position to prevent an efficiency loss from δ-electrons, where the cluster center is further away from the track incidence point due to the secondary charge deposition.

6.4 Analysis

The Corryvreckan package allows track reconstruction and performance evaluation of the tested devices within the same framework. Depending on the quantities of interest, one or multiple analysis modules are included in the reconstruction and analysis workflow.

6.4.1 Hit efficiency

The hit efficiency is one of the main detector properties investigated with particle beams. It is defined as the ratio of the number of reconstructed tracks with an associated cluster on the DUT ($N_{\text{associated}}$) and the total number of tracks intersecting this DUT (N_{total}):

$$\epsilon = \frac{N_{\text{associated}}}{N_{\text{total}}}. \tag{6.10}$$

As recommended by the Particle Data Group, the uncertainty in the hit efficiency is calculated using the default ROOT `TEfficiency` method which applies a Clopper-Pearson confidence interval of one standard deviation [90].

Since the readout time per frame of the Mimosa26 modules is 4607 times that of the ATLAS pixel modules, most tracks contain only telescope hits. For this reason, a timing reference or so-called reference DUT is used, which is usually a non-irradiated, previously tested and well-performing LHC type pixel module. Only telescope tracks with a matching hit on the reference DUT are considered for the analysis. This unbiased track selection was previously performed within the TBmon2 framework. To replicate the same analysis method, an additional parameter `require_associated_cluster_on` was added to the existing `[AnalysisEfficiency]` module, which allows specifying the reference DUT.

Assuming that pixels with the same geometry behave the same, the hits and tracks from all pixels are mapped onto the coordinates of a single pixel to derive the so-called in-pixel efficiency map, which allows a detailed analysis of the hit efficiency as a function of the position within the pixel.

6.4.2 New analysis module

The results of the analysis are: the in-pixel hit efficiency and the efficiency as a function of row/column as well as the residual distributions for clusters of various sizes. As the in-pixel hit efficiency, cluster size and residual distributions all depend on the pixel geometry, a new analysis module, `[AnalysisITkPixQuad]`, implementing non-uniform pixel matrix, is added to the Corryvreckan framework to determine:

- the cluster size distribution in the x and y dimensions;
- the residual distribution in the x and y dimensions for clusters composed of one or two pixels;
- the hit efficiency.

With this, all quantities can be determined for a chosen pixel size.

6.5 Validation of the new analysis framework

Before choosing the Corryvreckan framework as the standard tool for the analysis of ATLAS ITk pixel test-beam data, a validation was performed. For this purpose, several datasets were analyzed using the new framework and the results obtained were compared with those previously achieved using a combination of the EUTelescope and TBmon2 packages. Whenever possible, the configurable parameters of the Corryvreckan modules were set to those values used in the EUTelescope or TBmon2 packages.

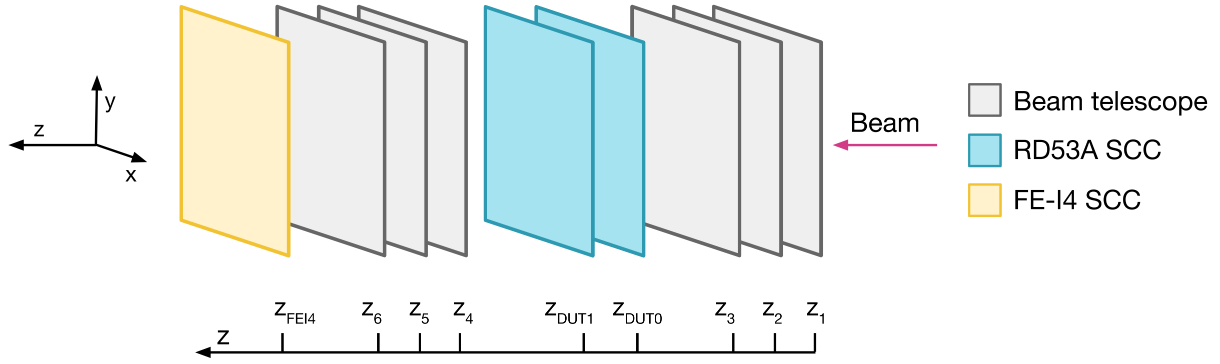


Figure 6.8: A schematic representation of the June 2020 test-beam setup. The distances between telescope planes are around 11 cm, while the spacing between the upstream and downstream telescope triplet is around 35 cm. Between the two telescope arms modules are mounted in the cold box.

6.5.1 Overview of tested modules

The datasets analyzed are recorded at the DESY II test-beam facility during the June 2020 test-beam campaign, with an electron energy of 5.0 GeV. This test-beam campaigns was used to qualify sensor manufacturers for the ITk pixel module production. The experimental setup consists of:

- the EUDET-type beam telescope (Section 4.3.2);
- one **ATLAS FEI4** single-chip module, with 250×50 µm^2 size pixels arranged as a 80×336 pixel matrix, that could be used as a reference DUT;
- two **ATLAS RD53A** single-chip modules, with sensors of either 100 µm or 150 µm thickness and two possible pixel layouts: 100×25 µm^2 or 50×50 µm^2.

A simplified illustration of the setup is shown in Figure 6.8. The measured z positions of the modules for the given test-beam campaign are given in Table 6.1. The details of the analyzed RD53A single-chip modules are given in Table 6.2. In total, datasets from three batches are considered, where batch refers to a series of runs taken with the same detector configuration. The datasets are chosen such that the Corryvreckan framework can be used for analysis of the data from modules of different sensor thicknesses, pixel layouts and fluences. As the main goal of this study is to compare the performance of the two reconstruction frameworks, the two RD53A modules tested per batch are only identified by the ID numbers assigned to tested devices by the converter plugin. No reference to the actual type of module is given.

Table 6.1: Measured detector z positions in the test-beam area.

	z_1	z_2	z_3	z_{DUT0}	z_{DUT1}	z_4	z_5	z_6	z_{FEI4}
[mm]	0	111	222	355	425	571	681	793	835

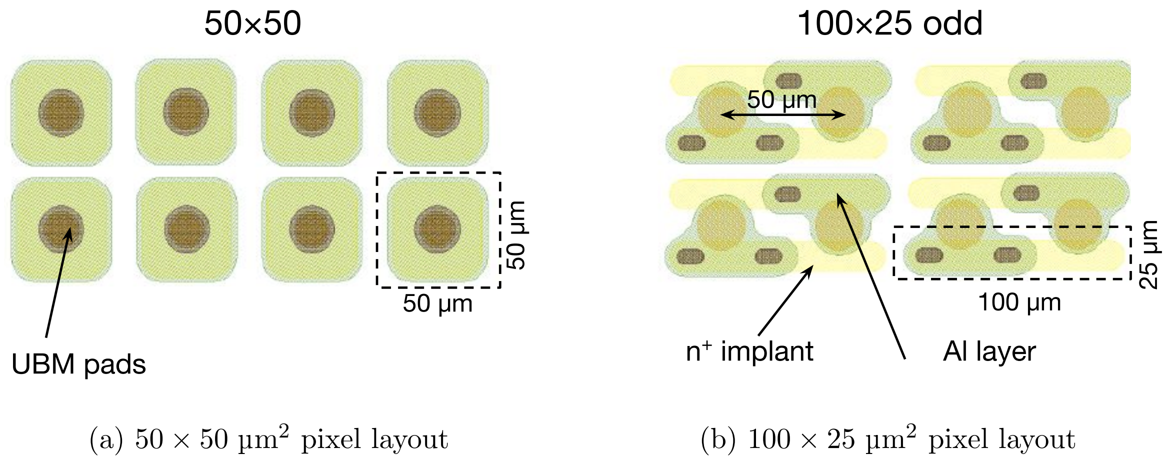
Table 6.2: An overview of the tested RD53A single-chip modules. The DUT ID corresponds to the location of the DUT in the setup.

Batch	DUT ID	Pixel area [µm × µm]	Thickness [µm]	Punch-through bias	Fluence [10^{15} n_{eq}/cm^2]
1	0	100 × 25	150	yes	0
	1	50 × 50	100	no	0
9	0	50 × 50	100	no	0
	1	50 × 50	100	no	0
11	0	50 × 50	100	yes	5
	1	50 × 50	150	no	5

6.5.2 Data input

To analyze data from RD53A single-chip cards, additional modifications of the YarrConverterPlugin were performed. These modifications were necessary since the column/row information of the hit pixel recorded by the YARR readout system is given in the coordinate system of the RD53A readout chip, which has 50 × 50 µm^2 pixel cell, while the tested sensors have various pixel layouts (50 × 50 µm^2, 100 × 25 µm^2 or 25 × 100 µm^2) and bump-bonding schemes for pixels with different dimensions in x and y. Two possible pixel layouts are shown in Figure 6.9. Figure 6.9a shows the regular 50 × 50 µm^2 pixel, while Figure 6.9b shows the 100 × 25 µm^2 pixel layout with the so-called odd bump-bonding scheme, which means the first row of channels on the readout chip is connected to the odd rows on the sensor.

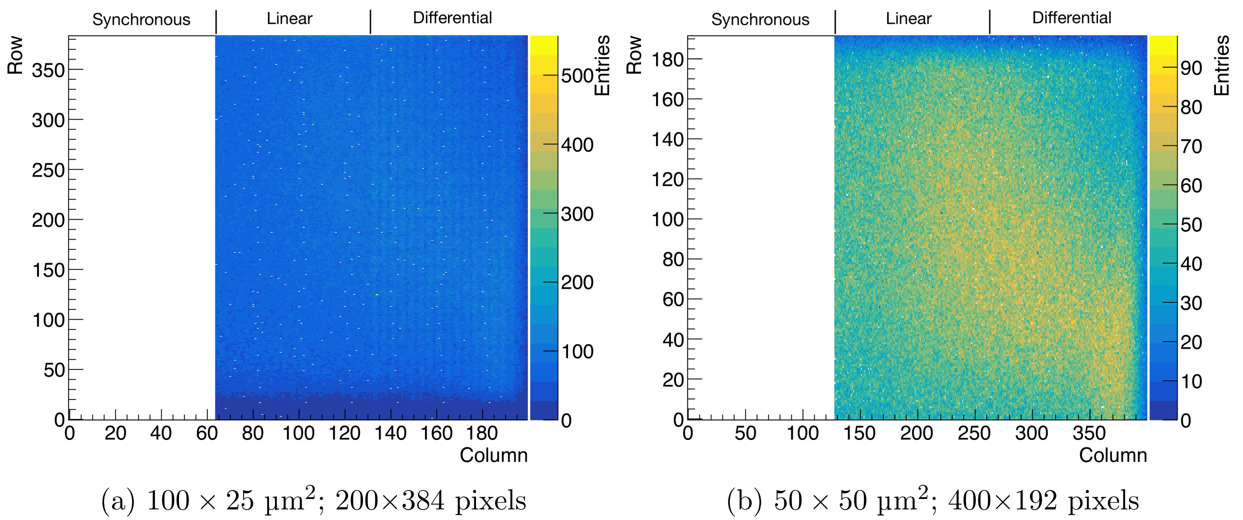
A mapping of the readout chip geometry to the sensor geometry was performed within the EUTelescope framework by providing additional geometry files. In the case of the Corryvreckan framework, the detector description is given in a single detector configuration file. Information about the layout of the tested devices is passed to the YarrConverterPlugin via an external text file and the mapping from the chip to the actual sensor geometry is performed before the data are processed by the Corryvreckan framework. A visual representation of recorded hits, hit maps, are shown in Figure 6.10, indicating that the Corryvreckan package can correctly handle data from devices with different pixel layouts. This is important for testing of ITk pixel modules with 3D sensors, for which both pixel layouts are accepted for production. The area without recorded hits belongs to the disabled synchronous front-end.



(a) 50×50 µm^2 pixel layout

(b) 100×25 µm^2 pixel layout

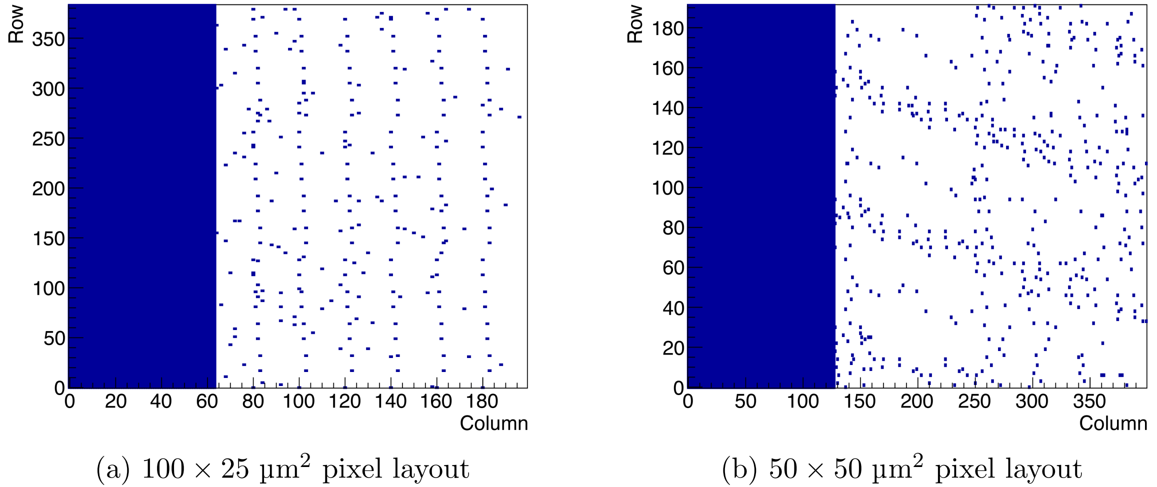
Figure 6.9: Two possible pixel layouts of the RD53A pixel sensors. Figure a) shows 50×50 µm^2 pixels, while b) shows the 100×25 µm^2 pixels with the odd bump-bonding scheme. These figures are modified from Ref. [91].



(a) 100×25 µm^2; 200×384 pixels

(b) 50×50 µm^2; 400×192 pixels

Figure 6.10: Hit maps created by the Corryvreckan framework for devices of different pixel layouts. Figure a) is for a pixel size of 100×25 µm^2, while b) is for 50×50 µm^2 pixels. The different front-end flavors are indicated.



(a) 100×25 µm^2 pixel layout

(b) 50×50 µm^2 pixel layout

Figure 6.11: Maps of masked pixels created by the Corryvreckan framework for devices of different pixel layouts. Figure a) is for a pixel size of 100×25 µm^2, while b) is for 50×50 µm^2 pixels.

6.5.3 Pixel mask creation

Masked pixels play an important role in the reconstruction and analysis of the test-beam data, with direct impact on the hit efficiency determination. To mask noisy pixels, a limit of 50 is used, meaning that all pixels with recorded numbers of hits of more than 50 times the average number of hits per pixel are masked.

Pixels masked during the chip tuning are identified as those that did not record any hit in all runs of the same batch. The number of events used to identify those pixels is at least 2 million for the analyzed datasets. The masked pixels for two tested devices implementing different pixel layouts are shown in Figure 6.11.

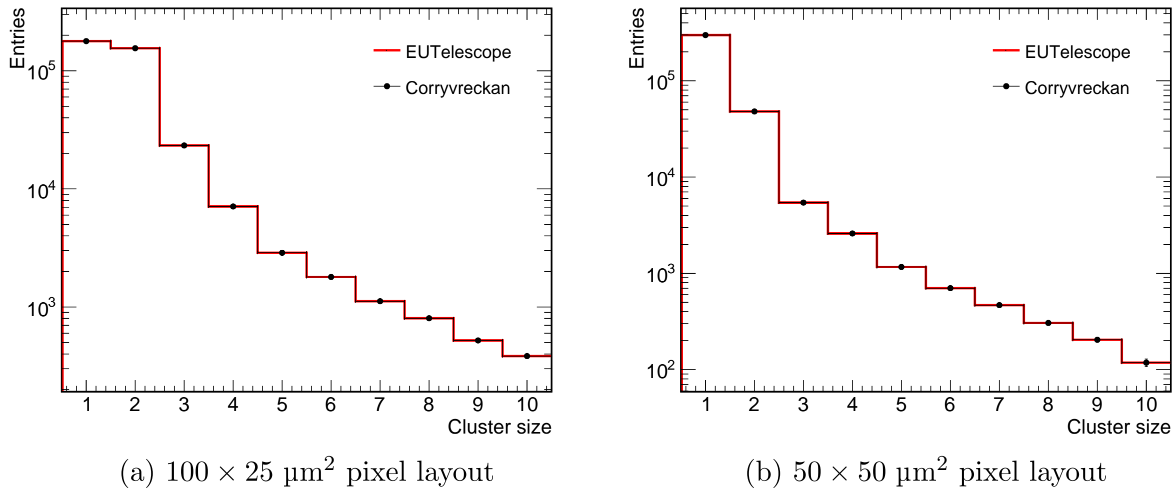
The used RD53A chip contains three different readout concepts, but in the analyzed datasets at most two of those are simultaneously used during the data taking. Depending on the pixel layout, masked pixels up to column 63 or 127 belong to the disabled synchronous front-end. The comparison of the numbers of masked pixels using this method in the Corryvreckan and TBmon2 packages with those masked during the chip tuning is given in Table 6.3. Ideally, the chip configuration file, which contains a list of all disabled pixels, should be used for the data analysis. However, due to chip retuning and subsequent remasking, it is possible that the latest saved chip configuration file is not the one that is actually used for the test-beam data taking. This is most likely the case for batch 1, where the numbers of pixels masked by the TBmon2 and Corryvreckan packages are comparable, but differ with respect to the number of masked pixels listed in the chip configuration file. For batches 9 and 11, the numbers of masked pixels for the three cases are compatible.

Table 6.3: A comparison of the numbers of masked pixels using different methods.

Batch	DUT ID	Chip tuning	The difference in the number of masked pixels with respect to the chip tuning	
			TBmon2	Corryvreckan
1	0	24576	270	267
	1	25475	-453	-453
9	0	24721	-2	-4
	1	24580	14	3
11	0	51462	3	1
	1	50850	1	0

6.5.4 Cluster formation

The EUTelescope and the Corryvreckan frameworks use the same clustering algorithm based on the spatial information of the recorded hits. In Figure 6.12 the cluster size distributions obtained with both frameworks are compared for the devices of different pixel layouts, indicating identical result for this step of the data reconstruction.



(a) $100 \times 25\ \mu m^2$ pixel layout

(b) $50 \times 50\ \mu m^2$ pixel layout

Figure 6.12: Comparison of the cluster size distributions obtained with the EUTelescope and Corryvreckan frameworks for devices of different pixel layouts. Figure a) is for a pixel size of $100 \times 25\ \mu m^2$, while b) is for $50 \times 50\ \mu m^2$ pixels. Uncertainties are statistical only and smaller than the symbol size.

6.5.5 Software alignment

The software alignment is the first step in which the track reconstruction is performed. As discussed in Section 6.3.6, the set of required parameters as well as the track finding

Table 6.4: The intrinsic spatial resolution per detector type used in the detector configuration file, calculated as pitch/$\sqrt{12}$. Although the expected value for the telescope planes is 5.3 µm, the value of 5.2 µm was used as in the reconstruction performed using the EUTelescope software.

Detector type	Pixel size [µm^2]	Intrinsic spatial resolution [µm]	
		x	y
Mimosa26	18.4 × 18.4	5.2	5.2
RD53A	100 × 25	28.9	7.2
RD53A	50 × 50	14.4	14.4
FEI4	250 × 50	72.2	14.4

Table 6.5: Summary of materials and their radiation lengths contributing to the material budget [92].

Material	Radiation length [cm]
Silicon	9.37
Kapton	28.57
Air	$3.039 \cdot 10^4$
Aluminium	8.897

procedures for this step differ between the two frameworks. The width of the residual distribution is affected by the intrinsic spatial resolution assumed in the detector configuration file. For a fair comparison of the two frameworks, the spatial resolution for each detector in the Corryvreckan framework is set to the value used in the EUTelescope package, listed in Table 6.4. Irrespectively of the cluster size, the software assigns the intrinsic spatial resolution as its position uncertainty. For the material budget of the telescope planes, the value of $0.0075 \cdot X_0$ is used taking into account the sensor and contributions from Kapton foils [69]. To be compatible with the EUTelescope framework, in this comparison the material budget of the DUT planes is calculated only from the sensor thickness. The radiation lengths of all materials contributing to the material budget are given in table Table 6.5.

Telescope alignment

For the software alignment, telescope plane 4 is chosen as the reference plane. Figure 6.13a shows the differences in x calculated using Eq. 6.4 for telescope plane 3 before and after the prealignment, indicating an initial misalignment of -0.69 mm and subsequent successful prealignment performed by the Corryvreckan framework. The quality of the prealignment, as well as the synchronization with respect to the reference plane is verified by the 2D correlation map shown in Figure 6.13b. The same conclusions hold for the not-shown y dimension.

The initial track reconstruction for the telescope alignment is performed starting with a large spatial distance of 300 µm and reduced with each iteration to approximately the pixel pitch. To confirm the good quality of the telescope alignment, the tracking module is

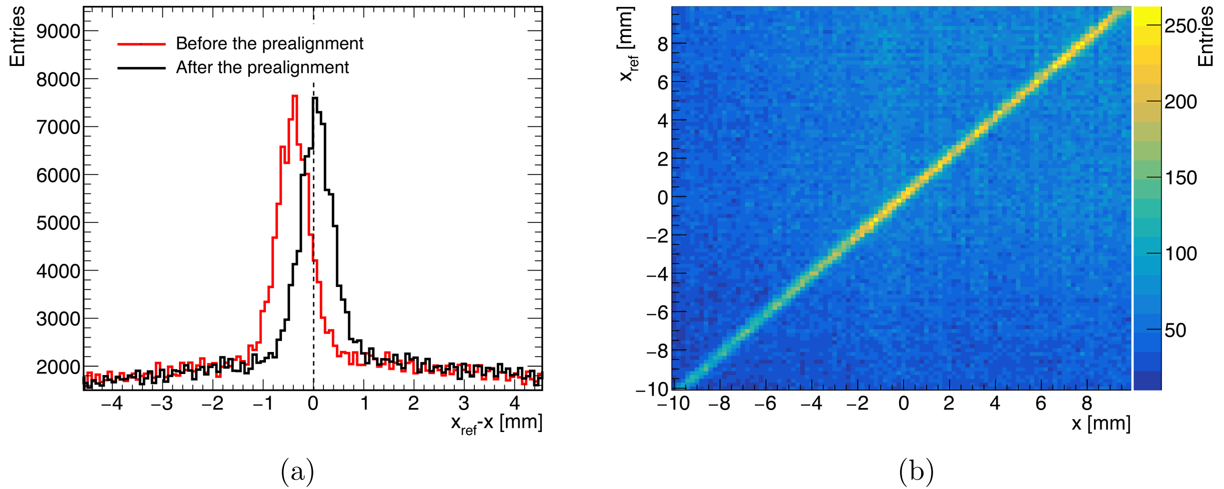


Figure 6.13: Figure a) shows the differences in x between the cluster positions on the telescope plane 3 and the reference plane before and after the prealignment. Figure b) shows the correlation of these two values after the prealignment.

configured to require at least six hits to form a track. The spatial matching criteria for the track acceptance is set to 100 µm in both dimensions, which is about five times the pixel pitch of the telescope planes. The example of the biased residual distribution in x and y dimensions for the telescope plane 3 is shown in Figure 6.14. The residual distribution of each telescope plane is fitted to a Gaussian. In this analysis, the residual width is identified with the standard deviation. For the shown residual distributions, the measured residual width coincides with the expected intrinsic spatial resolution.

The comparison of the biased residuals obtained with the Corryvreckan and EUTelescope frameworks is given in Figure 6.15. A similar behavior of the residuals from the two inner planes is observed. The same holds for the four outer planes. In both cases, the largest residual width is observed for telescopes plane 3 and 4, which are closest to the cooling box, hosting two tested DUTs. The track resolution worsens towards the outer planes, which decreases the difference with respect to σ_{int} and hence the residual width of the outer planes. These observations are compatible with the performance of the EUDET-type beam telescope [69].

The telescope residual widths obtained with both frameworks agree. However, the values for plane 4 of $\sigma_4 = (5.76 \pm 0.01)$ µm exceed the intrinsic spatial resolution given in Eq. 6.6, where the uncertainty is statistical. This can be attributed to an underestimated material budget, i.e. only the sensor is taken into consideration. The material budget plays a crucial role in the GBL algorithm. For a low material budget, the algorithm assigns a smaller uncertainty to the scattering. The correct estimation of the material budget should include both sensor and front-end, and any additional support structure. The bare single-chip modules are glued to an aluminium support of 500 µm thickness. Therefore, the telescope performance is investigated when the material budget estimation is calculated taking into account all contributing components using Eq. 6.8. The results

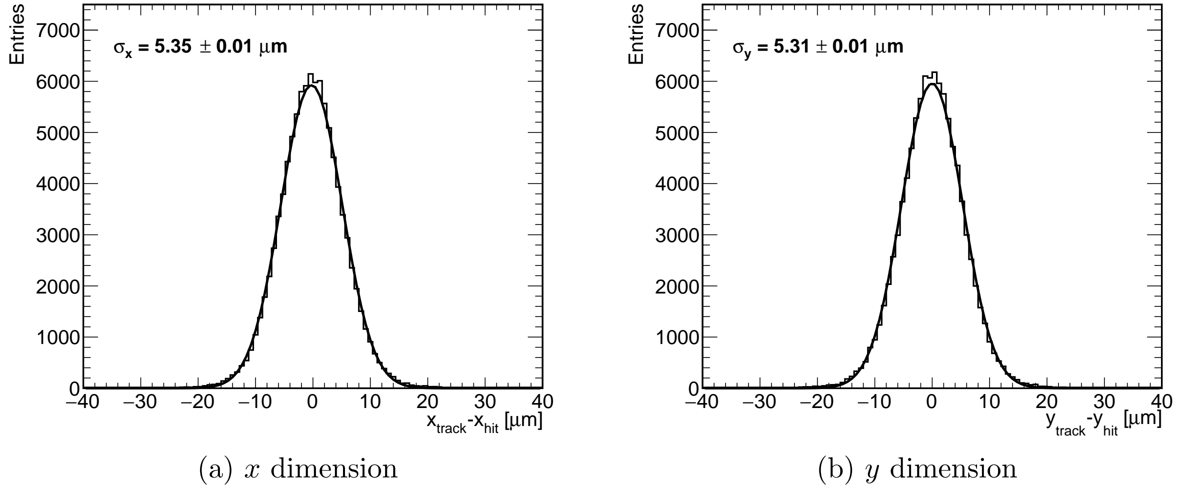


Figure 6.14: The distribution of biased residuals for the telescope plane 3 after the telescope alignment in a) the x and b) in y dimension. The values quoted are the standard deviation and its statistical uncertainty, as obtained from a fit to a Gaussian.

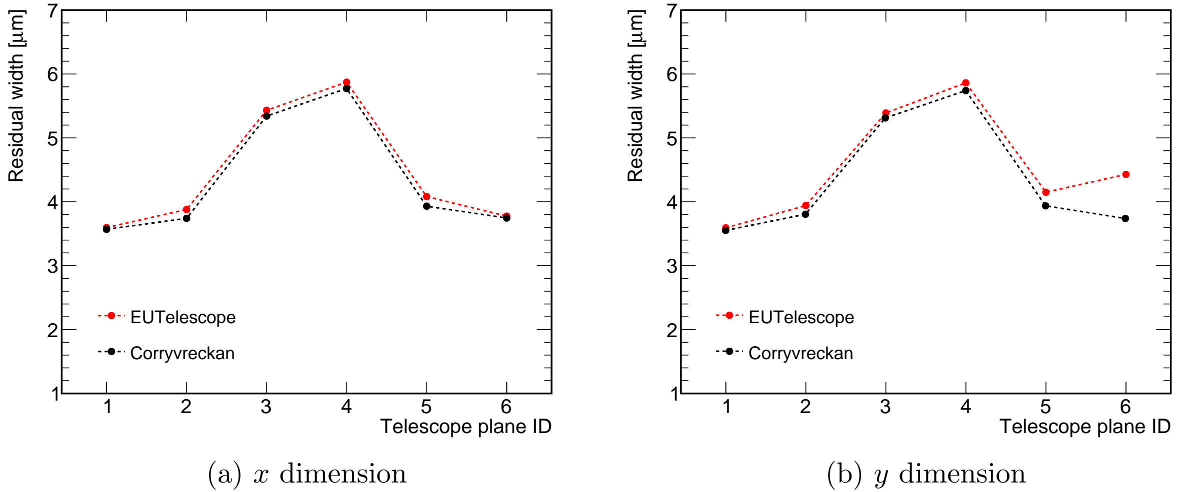
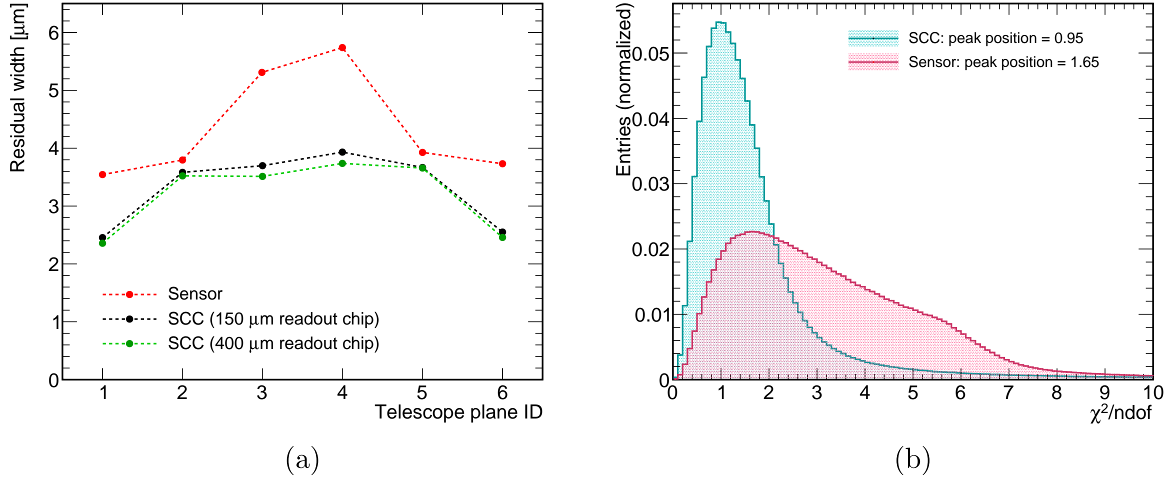


Figure 6.15: The comparison of biased residual widths in both dimensions for all telescope planes, as determined with the Corryvreckan and EUTelescope frameworks.

obtained are shown in Figure 6.16a. The investigated cases of calculating the material budget are indicated as:

- Sensor: only the silicon sensor is used;
- SCC: all main components of the single-chip card (sensor, front-end chip and aluminium support) are used.

Two front-end thicknesses were considered: 150 µm and 400 µm. With the more accurate



(a) (b)

Figure 6.16: Figure a) shows the residual width for each telescope plane as function of the material budget used in the analysis, while b) displays the χ^2/ndof of reconstructed tracks using a GBL track model for two assumptions on the material budget.

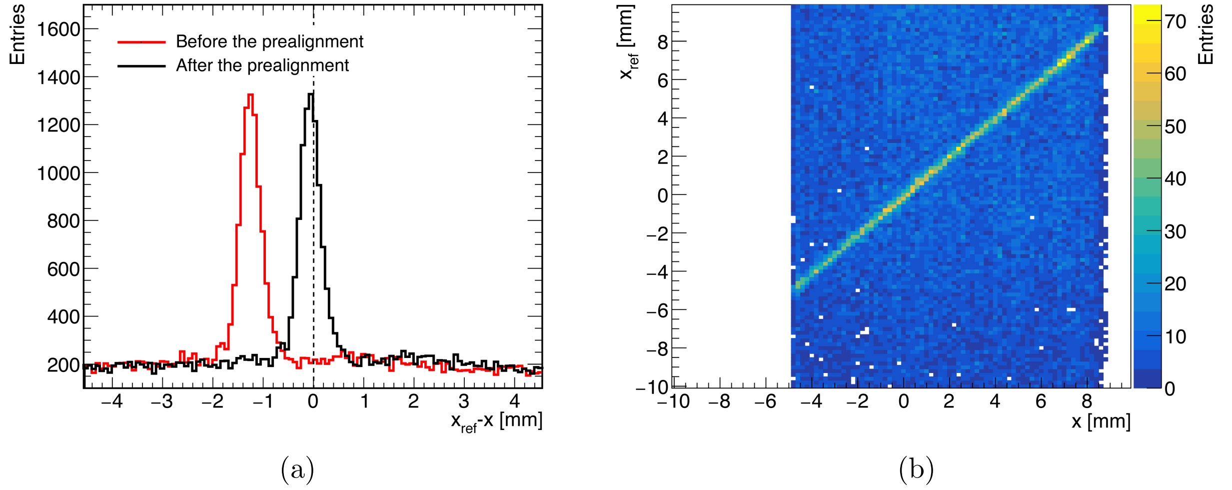
material budget, the overall performance of the telescope is improved, leading to a biased residual width below 4 µm for all planes. In addition, a more uniform performance of the inner telescope planes is observed.

The quality of track fitting is verified with the χ^2 per number of degrees of freedom (ndof) distribution. The impact of the estimated material budget given to the Corryvreckan framework on the quality of the track fit is shown in Figure 6.16b, for two investigated cases of calculating the material budget, i.e. the sensor and all main components of the single-chip card. For the chip, a thickness 150 µm is assumed. The peak positions of both distributions are indicated. The track fitting quality considerably improves, when considering all components in the material budget. The corresponding distribution peaks at 0.95 and exhibits a steep decrease to higher χ^2/ndof values.

DUT alignment

The successful alignment of the beam telescope is followed by the DUT alignment. Figure 6.17a shows the difference in x between the cluster positions for one of the tested devices and the reference plane before and after the prealignment. Based on the peak position, the estimated initial x coordinate for this plane was shifted by -1.19 mm with respect to the reference plane, which corresponds to an offset of more than 20 pixels. Figure 6.17b indicates successful prealignment performed by the Corryvreckan framework. The same is observed for the not-shown y dimension.

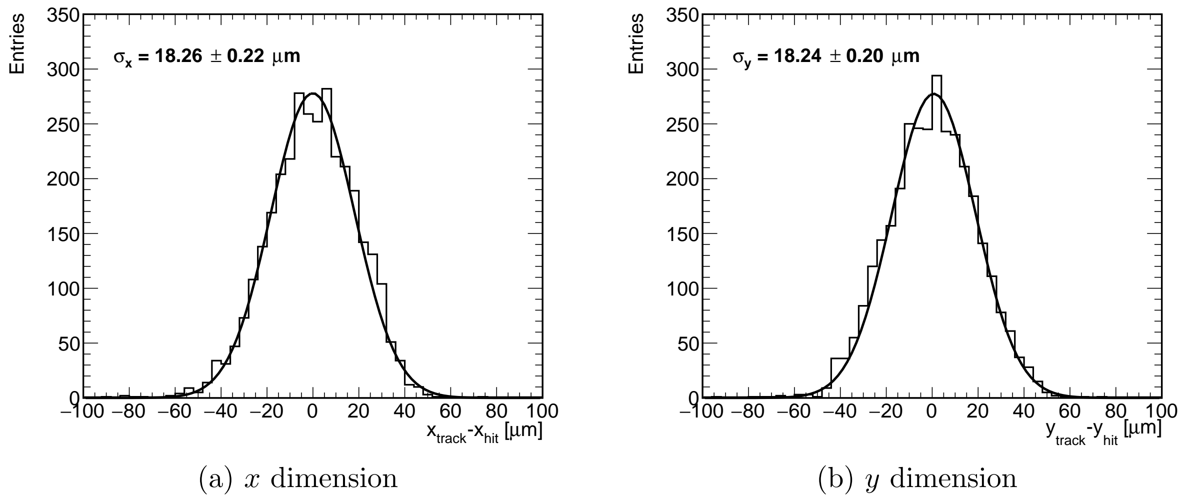
For the DUT alignment, 100 000 telescope tracks are used. Clusters on DUT planes are assigned to the reconstructed tracks if they are within the user-defined spatial limit, starting with a large value, that is incremently decreased to the pixel pitch. Figure 6.18



(a)

(b)

Figure 6.17: Figure a) shows the differences in x between the cluster positions on the DUT plane 0 and the reference plane before and after the prealignment. Figure b) shows the correlation of these two values after the prealignment.



(a) x dimension

(b) y dimension

Figure 6.18: The distribution of unbiased residuals for one tested device after the alignment in a) the x and b) in the y dimension. The values quoted are the standard deviation and its statistical uncertainty, as obtained from a fit to a Gaussian.

shows examples of unbiased residual distributions in x and y for one of the tested RD53A modules. The residual width in both dimensions agree with the expectation for a sensor with $50 \times 50\ \mu m^2$ pixel size and a telescope resolution of about 11 µm, see Eq. 6.7.

In Table 6.6 the comparison of the unbiased residual widths obtained with the Corryvreckan and EUTelescope frameworks is given for all tested devices. Results achieved with the Corryvreckan framework are compatible with the expectation for respective pixel sizes, taking into account a telescope resolution in the range of 10-12 µm, and are close to

Table 6.6: Comparison of the unbiased residual widths for analyzed sensors obtained with the Corryvreckan and EUTelescope softwares.

Batch	DUT ID	Pitch [µm]	Quantity	Corryvreckan	EUTelescope
1	0	100	x residuals [µm]	29.3 ± 0.2	29.3 ± 0.2
		25	y residuals [µm]	12.8 ± 0.1	8.4 ± 0.1
			Associated tracks	7166	7434
	1	50	x residuals [µm]	18.3 ± 0.2	18.1 ± 0.2
		50	y residuals [µm]	18.1 ± 0.2	17.8 ± 0.2
			Associated tracks	6936	6970
9	0	50	x residuals [µm]	18.1 ± 0.2	17.8 ± 0.2
		50	y residuals [µm]	18.1 ± 0.2	17.6 ± 0.2
			Associated tracks	6567	6670
	1	100	x residuals [µm]	31.3 ± 0.2	-
		25	y residuals [µm]	11.9 ± 0.1	-
			Associated tracks	6730	-
11	0	50	x residuals [µm]	18.3 ± 0.2	17.9 ± 0.2
		50	y residuals [µm]	18.2 ± 0.2	17.9 ± 0.2
			Associated tracks	3230	3300
	1	50	x residuals [µm]	17.8 ± 0.2	17.1 ± 0.2
		50	y residuals [µm]	17.8 ± 0.2	17.5 ± 0.2
			Associated tracks	3280	3357

those obtained using the EUTelescope package. However, systematically lower values are obtained with the EUTelescope software. The largest difference in achieved residual width is observed for the short dimension of the sensor with 100 × 25 µm^2 pixels. The larger value obtained with the Corryvreckan framework is compatible with the expected unbiased residual width, taking into account a telescope resolution of around 10.6 µm. The numbers of tracks with an associated cluster on the DUT per 100 000 telescope tracks is also compared, showing similar results between the two frameworks.

6.5.6 Hit efficiency

The data analysis of the validation study is dedicated to the determination of the hit efficiency, as this was the main detector property investigated during this test-beam campaign. For the hit efficiency measurement in the Corryvreckan framework, DUT clusters are assigned to the reconstructed telescope tracks with the maximum matching distance in both directions set to two times the pixel size, equal to the value chosen in the analysis with the TBmon2 software. The hit efficiency is calculated according to Eq. 6.10. The following tracks are not included in N_{total}:

- tracks intersecting the DUT in areas neighboring masked pixels, with one pixel tolerance;
- tracks with $\chi^2/\text{ndof} > 6$, following the limit set in the TBmon2 framework.

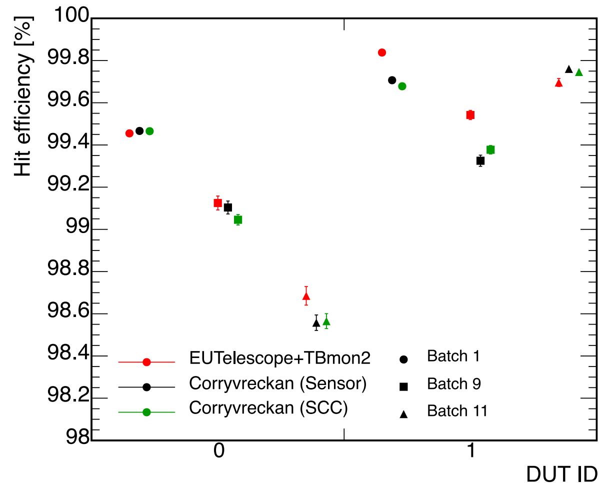


Figure 6.19: Comparison of the determined hit efficiencies using either the combination of the EUTelescope and TBmon2 packages or the Corryvreckan framework.

The hit efficiency is determined for one DUT at a time, while the second DUT is used as the reference DUT. Figure 6.19 shows the comparison of the hit efficiencies per batch, obtained with a combination of the EUTelescope and TBmon2 packages to results achieved using the Corryvreckan software, considering two different assumptions on the material budget.

Obtained values are given in Table 6.7. Even without taking into account systematic uncertainties, very similar results are observed with both frameworks. The different material budget has only a small impact on the hit efficiency, as the spatial acceptance range to associate clusters on the DUT to reconstructed tracks is large enough. The differences in the determined hit efficiency may be caused by the different track finding algorithms and additional limits applied to the reconstructed tracks in the TBmon2 software, where, to suppress noise contributions, only hits with an LV1 ID within user specified limits are considered.

6.5.7 Conclusions

Measurements with particle beams play a crucial role in understanding the properties and behavior of newly developed devices, like the ITk pixel modules. Therefore, it is essential to have a reliable and highly configurable software to analyze these data. The Corryvreckan framework was recognized as a promising software for upcoming ITk pixel test-beam measurements. The study presented here was used to set-up the reconstruction and analysis flow in the Corryvreckan framework, to identify areas where additional functionalities were needed and implement them, and lastly, to compare the results achieved with those obtained with the previously used combination of the EUTelescope and TBmon2 packages. Initial steps of the reconstruction, such as loading-in the raw data, regardless of the pixel layout, identifying pixels that require masking and clustering, can all be done, while

Table 6.7: Obtained values for the hit efficiency using the combination of the EUTelescope and TBmon2 packages and the Corryvreckan framework. For the results marked with Sensor, only the sensor is taken into account in the dead material, while SCC indicates the more complete dead material estimation of the entire device and its support. The uncertainties are statistical only.

Batch	DUT ID	$\epsilon_{\text{EUTelescope+TBMon2}}$ [%]	$\epsilon_{\text{Corryvreckan}}$ (Sensor) [%]	$\epsilon_{\text{Corryvreckan}}$ (SCC) [%]
1	0	99.46 ± 0.01	99.47 ± 0.01	99.47 ± 0.01
	1	99.84 ± 0.01	99.71 ± 0.01	99.68 ± 0.01
9	0	99.13 ± 0.03	99.17 ± 0.03	99.16 ± 0.03
	1	99.54 ± 0.02	99.68 ± 0.03	99.69 ± 0.03
11	0	98.69 ± 0.04	98.56 ± 0.04	98.57 ± 0.04
	1	99.69 ± 0.02	99.76 ± 0.02	99.75 ± 0.02

achieving compatible results as in the previously used framework. It was demonstrated that successful alignments of the telescope and DUTs planes are achieved, with results compatible to those obtained with the EUTelescope framework. In addition, it was shown that a careful estimation of the material budget improves the measurements with low energy particle beams and thus impacts the overall telescope performance and track fitting. The hit efficiencies determined with the two analysis frameworks mostly agree within their statistical uncertainties. With the additional functionalities needed to properly account for the non-uniform pixel matrix of the quad sensors being included, the Corryvreckan framework is now ready to be used for future test-beam measurements.

7 Quad module performance with particle beams

The prototype RD53A quad modules were for the first time operated and tested with particle beams during a series of test-beam campaigns performed in 2021. The evaluation of their properties was enabled by the further development of the data reconstruction and analysis framework presented in Sections 6.2.3 and 6.4.2. The results of these tests are discussed in Section 7.1. In 2022, two quad modules with the full-size chip ITkPixV1.1 were available for test-beam measurements. The obtained results are presented in Section 7.2. The performance of both types of quad modules is evaluated in SPS test-beam campaigns, with beams of pions with an energy of $E = 120$ GeV.

7.1 RD53A quad modules

The test-beam setup is illustrated in Figure 7.1. At most two modules are mounted at the same time in the cooling box between the two telescope arms. Each module is secured in a module carrier and mounted onto a custom-made aluminium frame with a required adapter cards for powering and readout. The spacing between telescope planes is around 15 cm. To accommodate the cooling box, the distance between the upstream and downstream telescope arms is around 45 cm. The measured z positions of the modules are given in Table 7.1. The RD53A SCC was mounted between the second and third telescope planes and was used as a timing reference (reference DUT) for the analysis. Quad modules are operated with all working chips enabled. Due to their relatively large size compared to the beam spot, and the location of the chips bump-bonded to the sensor, it is not possible to simultaneously illuminate the entire sensor area read out with four chips. Therefore, the performance of only the part of the sensor read out by a single chip, is evaluated at a time. To achieve this, the module is moved perpendicular to the beam and data taking is performed at each position. All tested modules have 150 µm thick planar sensors. Their properties are listed in Table 7.2.

The temperature at which the measurements are performed is controlled using the chiller. The non-irradiated RD53A SCC is operated at room temperature, as it is mounted outside the cold box. Testing of the non-irradiated quad modules is performed with the chiller temperature set to 0°C. When testing the irradiated quad module cooled only by the chiller, the lowest achieved temperature measured via the NTC of the module was −5°C. At this condition, due to the high leakage current, the data taking was performed for a bias voltage of $V_{\text{bias}} = -200$ V. To reach a lower temperature and test the module at the

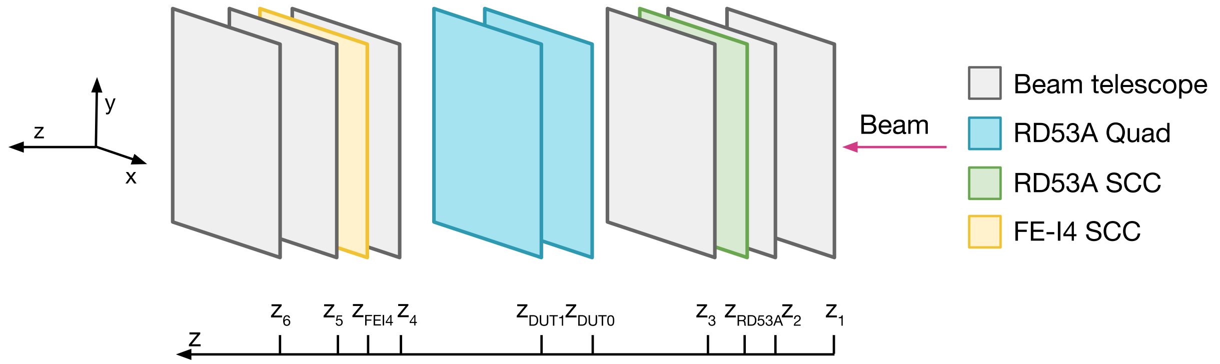


Figure 7.1: A schematic representation of the October 2021 test-beam setup. Between the two telescope arms modules are mounted in the cold box.

Table 7.1: Measured detector z positions in the test-beam area for RD53A quad module testing.

	z_1	z_2	z_{RD53A}	z_3	z_{DUT0}	z_{DUT1}	z_4	z_{FEI4}	z_5	z_6
[mm]	0	152	182	304	469	569	763	790	915	1067

Table 7.2: Overview of the tested RD53A quad modules. The information about the sensor manufacturer, chip thickness, biasing structure and fluence are given.

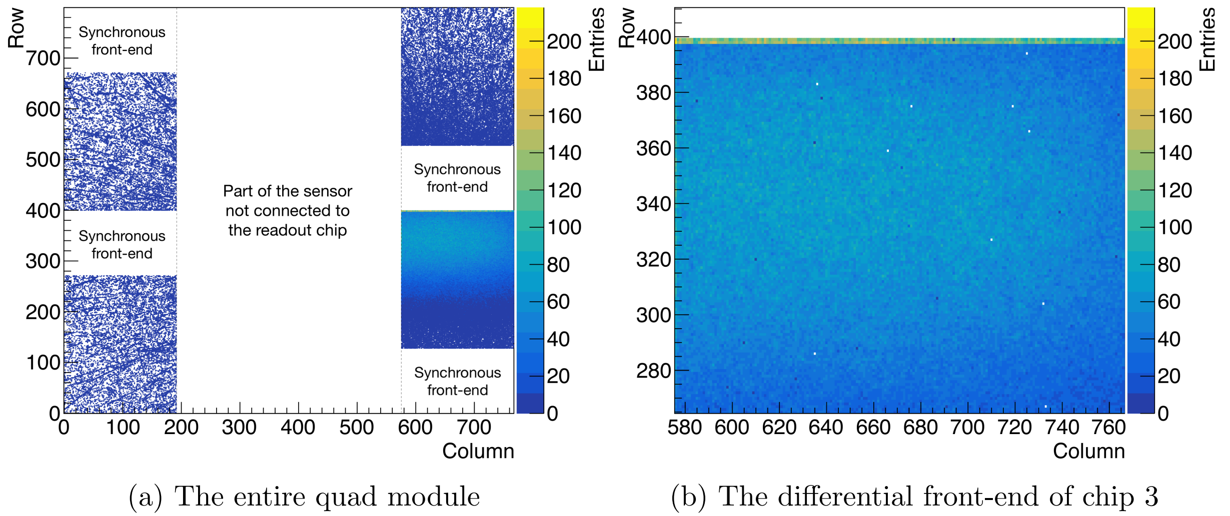
Internal ID	Manufacturer	Chip thickness [µm]	Biasing structure	Fluence [10^{15} n_{eq}/cm^2]
Q8	HPK	400	polysilicon resistors	0
Q2	Micron	150	punch-through	0
Q4	HPK	400	polysilicon resistors	5

target voltage of $V_{\text{bias}} = -600$ V, the chiller cooling was combined with dry-ice cooling. The measured temperature on modules during the testing, including other operational parameters are listed in Table 7.3.

In Figure 7.2a hits recorded with the Q2 module are shown, indicating a successful combination of data from two front-ends of the four individual readout chips onto a single detector plane. In this example, the beam is positioned mostly on the differential front-end of chip 3, see Figure 5.7. The areas in the hit map without recorded hits correspond to either the disabled synchronous front-end, or to the part of the sensor that is not connected to the readout chip, as these are the RD53A modules. To confirm the functionality of the inter-chip region, one of the investigated quantities is its hit efficiency. Given by the layout in Figure 5.7, this can only be performed for the differential front-end of chip 1 or 3, provided the beam is properly positioned. The hit map of the differential front-end of chip 3 in Figure 7.2b shows the uniform hit distribution for all pixels, except those in

Table 7.3: The parameters at which modules were operated during the data taking. The quantity I_{LV} refers to the current used to power the module, V_{bias} is the voltage at which the sensor was operated and I_{leak} is the corresponding leakage current. In addition, the chips disabled during the data taking are indicated. The discriminator threshold of all modules was tuned to 1500 e.

Module	Disabled chip ID	I_{LV} [A]	V_{bias} [V]	T [°C]	I_{leak} [µA]
Q8	2	3.4	−130	20	-0.2
Q2	-	4.4	−100	25	-4.8
Q4	3	4.4	−200	-5	-1900.0
	2 and 3	6.5	−600	-30	-100.0



(a) The entire quad module

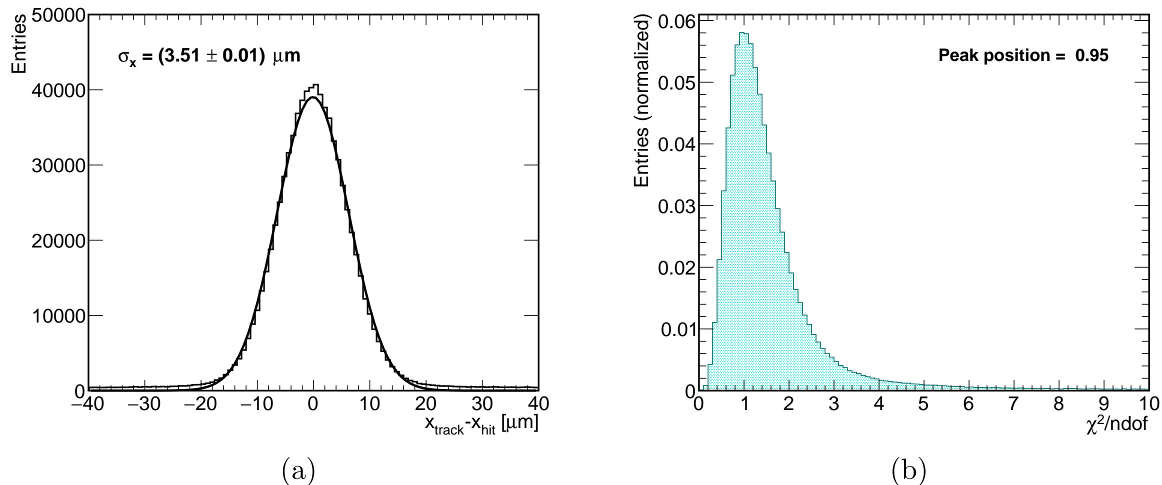
(b) The differential front-end of chip 3

Figure 7.2: Hits recorded by the quad module Q2 with the beam spot positioned on chip 3. Figure a) shows the entire quad module, while b) shows only the differential front-end of chip 3, with its two rows of the inter-chip region at the top of the figure.

the last two rows that recorded about twice the number of hits. This is expected as these pixels belong to the inter-chip region and are 50×100 µm^2 in size, i.e. have twice the area of the other pixels.

To create a pixel mask, all datasets obtained with the same conditions are combined. Pixels that did not receive any hit over the total number of events exceeding one million, are masked.

To achieve good telescope alignment and track fitting, a good estimate for the intrinsic resolution of telescope planes is needed, since this value is used as the uncertainty in the cluster center positions for the GBL algorithm. For the SPS test-beam data, this value is set to 3.25 µm as a mean intrinsic resolution over the six sensors according to Ref. [69],



(a) (b)

Figure 7.3: Figure a) shows the distribution of biased residuals in x for the telescope plane 3 after the telescope alignment, while b) shows the χ^2/ndof distribution of the corresponding reconstructed tracks.

instead of 5.2 µm used in Section 6.5. The example of a residual distribution for one of the telescope planes is shown in Figure 7.3a. The χ^2/ndof distribution is shown in Figure 7.3b as a measure of the quality of the track fitting. The distribution peaks at 0.95 with a steep decrease to the higher values.

The data were taken in so-called batches, where each batch refers to a collection of runs taken with the beam positioned on one of the chips. Initially, the software alignment was performed using only a single run from a batch. The telescope alignment of this step was used for all runs in a batch, while the DUT alignment is refined for each run before proceeding to the next reconstruction step. This was of special importance for the irradiated module, due to the box movement caused by the melting of the dry-ice. Tracks are reconstructed with a requirement to have a hit on the reference DUT and a spatial requirement of 100 µm in both dimensions.

7.1.1 Analysis

For the analysis of the RD53A quad module data, an additional requirement is applied on reconstructed tracks based on the LV1 ID of the hit on the reference DUT. The comparison of the LV1 ID distributions of the RD53A SCC and the quad module Q2 during the same run is shown in Figure 7.4. Both distributions show a similar behavior where the majority of the hits are recorded over multiple bunch-crossings, with long tails. However, an offset between the two distributions exists, meaning that there is a possibility that the hits on the two devices belonging to the same particle are not recorded during the time window corresponding to the same trigger.

To perform the analysis, clusters on the DUTs have to be assigned to the reconstructed

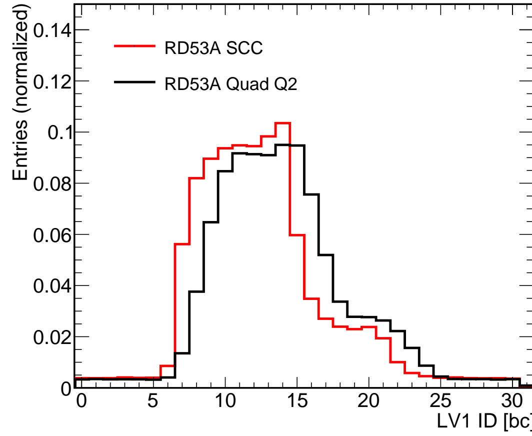


Figure 7.4: Comparison of the LV1 ID distributions for the RD53A SCC and the quad module Q2.

tracks. The criteria for the LV1 ID, as well as the spatial limits for the DUT-cluster to track association are investigated for two non-irradiated quad modules as shown in Figure 7.5. The comparison is done for default-size (50×50 µm^2) pixels as well as for the pixels of the inter-chip region. The hit efficiency of two quad modules, for different LV1 ID limits for the hits on the reference DUT, is shown in Figure 7.5a. For the two investigated pixel regions, the lowest hit efficiency is determined when the entire range (LV1 ID $\in$ [0, 31]) is used, i.e. no timing limit is applied. The hit efficiency is improved when the LV1 ID is constrained to the central part of the distribution, where the majority of hits are collected (LV1 ID $\in$ [7, 25], LV1 ID $\in$ [7, 15]). For the last two cases, obtained hit efficiencies agree within their statistical uncertainties. To minimize the fraction of rejected tracks, hits with LV1 ID between 7 and 25 are used for the analysis.

The data analysis of RD53A single-chip modules was performed with the spatial limit for the association of DUT–clusters to track of twice the pixel pitch. Therefore, for a quad sensor, this requirement is 100 µm. The present limitation of the software is to have a single value for an entire sensor. To confirm that this value is sufficient also for the inter-chip region where pixels are larger, the hit efficiency is determined as a function of this spatial criteria. The obtained results are shown in Figure 7.5b. For an acceptance range above 100 µm, the hit efficiencies of both pixel regions reach a stable high value and thus this acceptance range is used for the analysis of the data from quad modules. The differences in the hit efficiencies for 50×50 µm^2 pixels for two tested quads are due to the different biasing structure implemented into the sensor design, see Table 7.2.

Besides timing and spatial criteria, the track selection is influenced by additional requirements. Reconstructed tracks that are intersecting the DUT in areas neighboring masked pixels and have χ^2/ndof > 3 are not considered for the analysis. Figure 7.6 shows the fraction of discarded tracks based on different criteria with respect to the total number of reconstructed tracks for different chips of the quad module Q2. The fraction of tracks discarded due to high χ^2/ndof value is around 20% for all chips on this module. The number

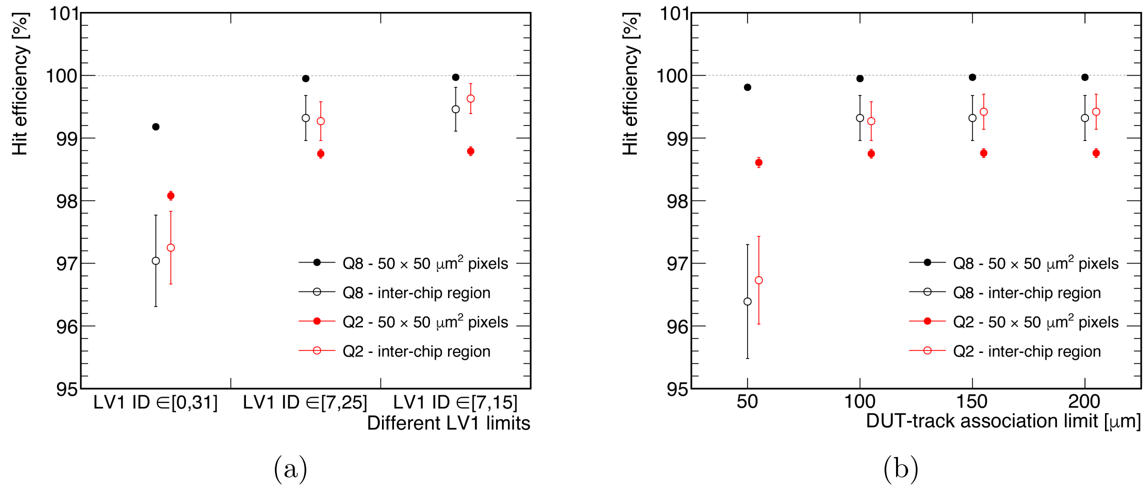


Figure 7.5: Hit efficiency as a function of a) different LV1 ID limits and b) DUT-cluster association spatial criteria. Both figures show hit efficiencies separately for default-size pixels and for those of inter-chip region of two non-irradiated quad modules.

of discarded tracks due to a masked neighbor fluctuates over the four tested chips, as it is influenced by the position of the beam on the module. Besides the disabled synchronous front-end, the RD53A quad modules feature a large number of pixels that are not connected to the channels of the readout chip and are treated as masked in the reconstruction software. For measurements where the beam is illuminating the border between two chips (e.g., chip 1), the number of discarded pixels is around 28%. Around 5% of tracks on all chips are discarded due to the requirement on the LV1 ID. Accepted tracks are used to investigate the distributions of cluster sizes, as well as hit efficiency and spatial resolution. The obtained results for each of these will be presented in turn.

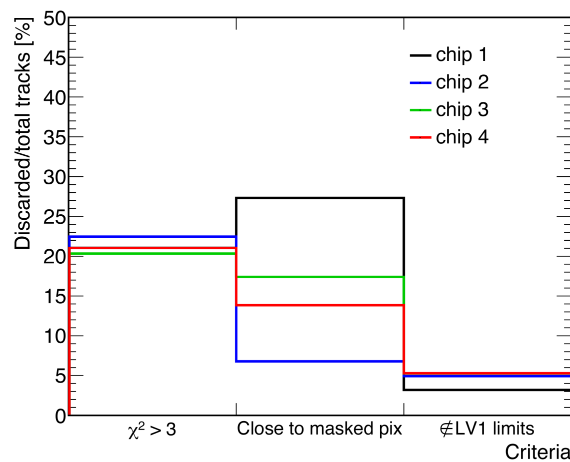


Figure 7.6: Discarded tracks based on different criteria.

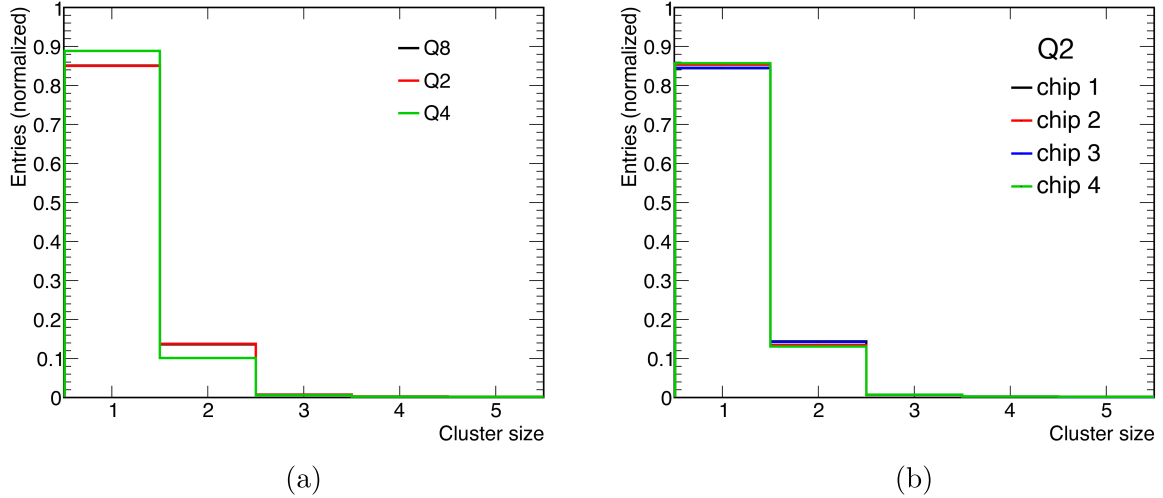
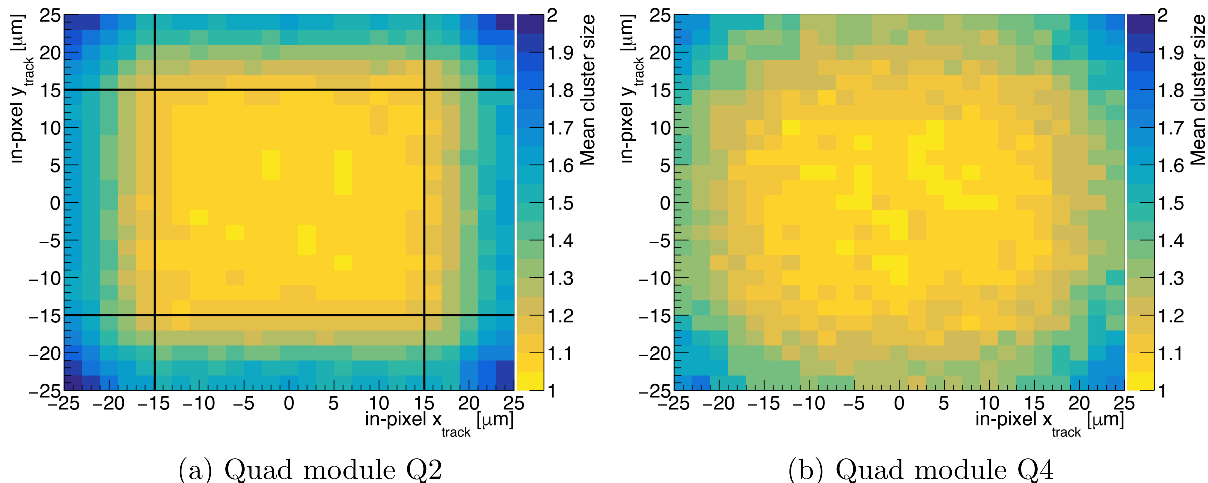


Figure 7.7: Comparison of cluster size distributions for pixels in the x dimension for a) all tested quad modules and b) different chips of the module Q2.

7.1.2 Cluster size distribution

The comparison of the cluster size distributions in x summing over all active chips of the tested quad modules is shown in Figure 7.7a. In all cases, the majority of passing particles create one-pixel size clusters. The fraction of such events is around 85 ± 0.1 % for non-irradiated modules (quads Q8 and Q2) and 88.8 ± 0.1 % for the irradiate module (quad Q4), where the uncertainties are statistical. Around 13.8 ± 0.1 % of total events induce two-pixel size clusters for non-irradiated modules, while higher cluster size contributions, induced by δ-electrons, are negligible. For the irradiated module, the cluster size two contribution is lower, i.e. only around 10.1 ± 0.1 % of events, due to the reduced charge sharing after the irradiation. As the pixel layout is symmetric, the cluster size distributions for columns and rows look alike. The distribution of cluster sizes does not depend on the tested chip of a quad, and is therefore uniform over the sensor area, as shown in Figure 7.7b.

The cluster size as a function of the track intercept within a pixel cell is shown in Figure 7.8. All quantities are discussed only for clusters assigned to the reconstructed tracks that intersect the sensor area with 50×50 µm^2 size pixels. Figure 7.8a shows the in-pixel mean cluster size map for one of the non-irradiated quad modules. The average cluster size of around one occurs for tracks intercepting pixels anywhere within the central 30×30 µm^2 pixel area. This number gradually increases towards the pixel border with two-pixel size clusters occurring if a track passes in a very small area near the four pixel corners. In Figure 7.8b the in-pixel mean cluster size map for the irradiated module is shown. Here, due to the decrease in charge sharing after irradiation, the probability for two-pixel size clusters is reduced even in the pixel corners.



(a) Quad module Q2

(b) Quad module Q4

Figure 7.8: In-pixel mean cluster size map of 50×50 μm^2 pixels for a) a non-irradiated and b) a quad module irradiated to a fluence of $5{\cdot}10^{15}$ n_{eq}/cm^2.

7.1.3 Hit efficiency

As the central area of the sensor is not read out, it was not possible to characterize the center of the quad module. To determine the hit efficiency, the module with all working chips enabled is tested with the beam spot positioned on different chips. Obtained values are compared with the ITk requirements for planar pixel sensors of 150 μm thickness:

- $\epsilon > 98.5\%$ for non-irradiated sensors;
- $\epsilon > 97\%$ at $V_{bias} = -600$ V for sensors irradiated to a fluence of $5{\cdot}10^{15}$ n_{eq}/cm^2.

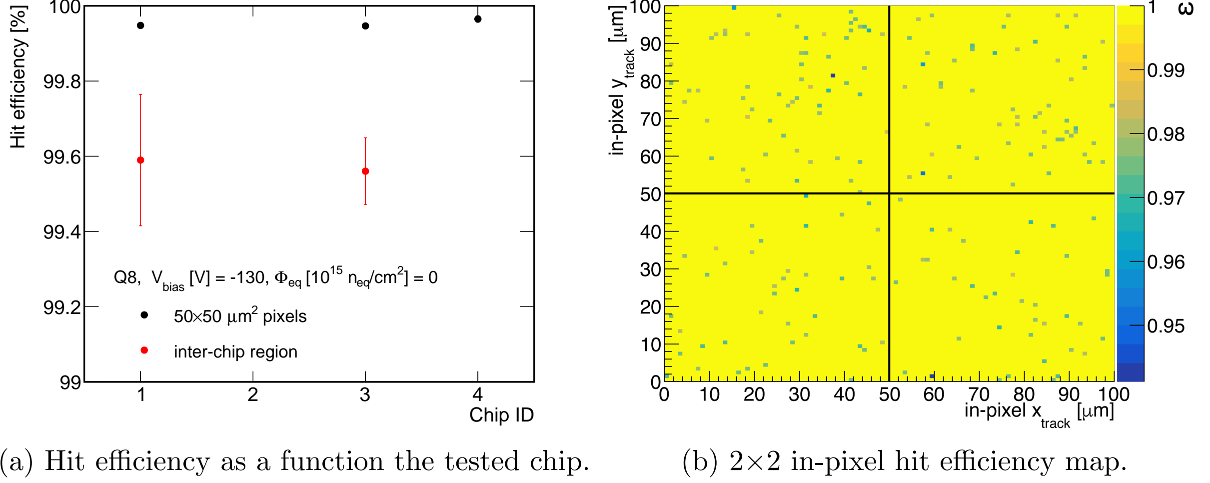
The results are discussed separately for default-size pixels and the inter-chip region for each of the tested quad modules.

Quad module Q8

The hit efficiency as a function of the tested chip for the two investigated pixel regions is shown in Figure 7.9a. As expected, the hit efficiency does not depend on the chip. The value of $\epsilon = (99.953 \pm 0.004)$ % is obtained for 50×50 μm^2 pixels. The uncertainties in quoted efficiencies are statistical only.

Figure 7.9b shows the hit efficiency as a function of the track intercept. Here, hits and tracks from all pixels are mapped onto the area of $2{\times}2$ neighboring pixels, each 50×50 μm^2 in size. A uniform hit efficiency map is observed for this quad module with the HPK sensors.

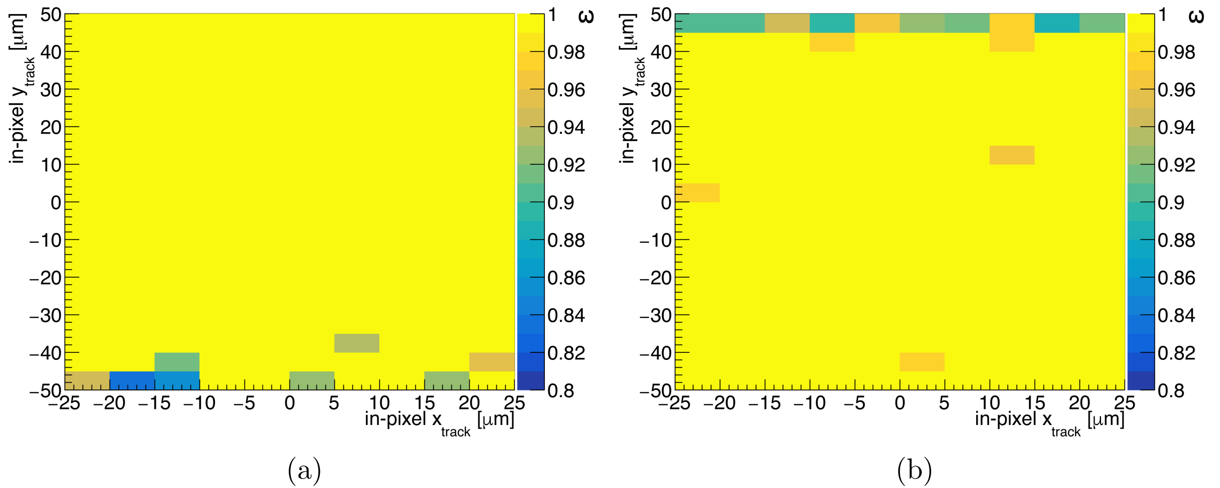
The determined hit efficiency of the inter-chip region is $\epsilon = (99.58 \pm 0.10)$ %, which is below the value obtained for default-size pixels, but within the ITk requirements for non-irradiated sensors. Figure 7.10 shows the in-pixel hit efficiency map for 50×100 μm^2 size



(a) Hit efficiency as a function the tested chip.

(b) 2×2 in-pixel hit efficiency map.

Figure 7.9: Quad module Q8 with the polysilicon resistors as biasing structure, operated at $V_{\text{bias}} = -130$ V and for a threshold tuning to 1500 e. Figure a) shows the hit efficiency as a function of tested chip, while b) shows the 2×2 in-pixel hit efficiency map for 50×50 µm^2 pixels.

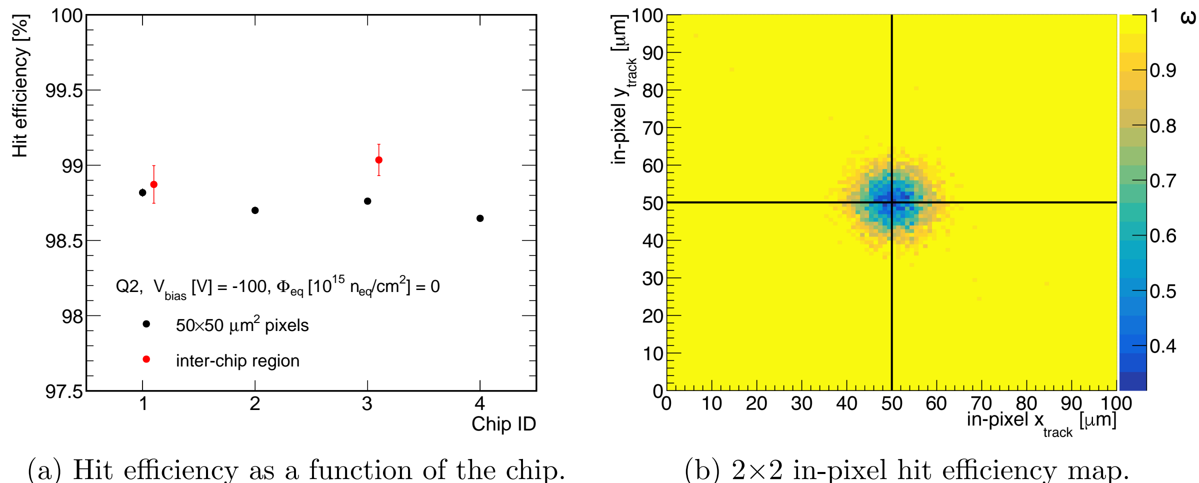


(a)

(b)

Figure 7.10: In-pixel hit efficiency maps for 50×100 µm^2 size pixels of the inter-chip region between front-ends of a) chips 1 and 2; b) chips 3 and 4 of the quad module Q8.

pixels. The in-pixel maps are shown for pixels at the border between the differential front-end of chip 1 (3) and the synchronous front-end of chip 2 (4) in Figure 7.10a (Figure 7.10b). Due to lower numbers of tracks, maps are shown with a larger bin size than that used for the default-size pixels. Discussed pixels have masked neighbors of the synchronous front-end on the bottom (top) for the inter-chip region between front-ends 1 and 2 (3 and 4), which results in the decrease of the hit efficiency along the border between the two chips.



(a) Hit efficiency as a function of the chip.

(b) 2×2 in-pixel hit efficiency map.

Figure 7.11: Quad module Q2 with the punch-through biasing, operated at $V_{\text{bias}} = -100$ V and for a threshold tuning to 1500 e. Figure a) shows the hit efficiency as a function of tested chip, while b) shows the 2×2 in-pixel hit efficiency map for 50×50 µm^2 pixels.

Quad module Q2

For the non-irradiated quad module Q2, the hit efficiency as a function of the tested chip is shown in Figure 7.11a. The hit efficiency for default-size pixels is determined to be $\epsilon = (98.73 \pm 0.01)$ %, while the value of $\epsilon = (98.95 \pm 0.08)$ % is determined for the pixels of the inter-chip region. Both values are within the ITk requirements for non-irradiated sensors.

The 2×2 in-pixel hit efficiency map for 50×50 µm^2 size pixels is shown in Figure 7.11b, where a region with significantly lower efficiency is observed in the center, which corresponds to the position of the bias dot (not present in Q8). The area of four neighboring pixels, excluding the bias dot, has a uniform hit efficiency above 99%.

Figure 7.12 shows the in-pixel hit efficiency map for 50×100 µm^2 size pixels. As for module Q8, the region with the lower efficiency is observed along the edge of the pixel that borders masked pixels. In addition, a structure with lower efficiency is visible in the pixel corner due to the bias dot, which has a smaller impact on the larger pixels, resulting in a higher efficiency than that observed for the default size pixels.

Quad module Q4

Due to increased noise in the differential front-end, the data taking for the irradiated quad module was performed with only the linear front-end enabled. Therefore, it was not possible to determine the hit efficiency of the inter-chip region. The hit efficiency as a function of the tested chip for two different bias voltages is shown in Figure 7.13a.

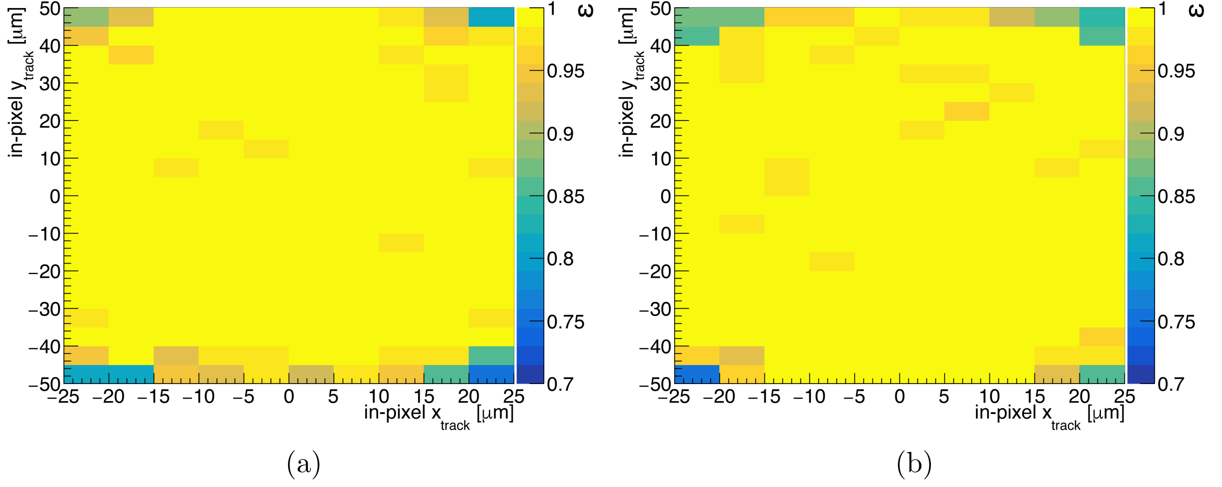
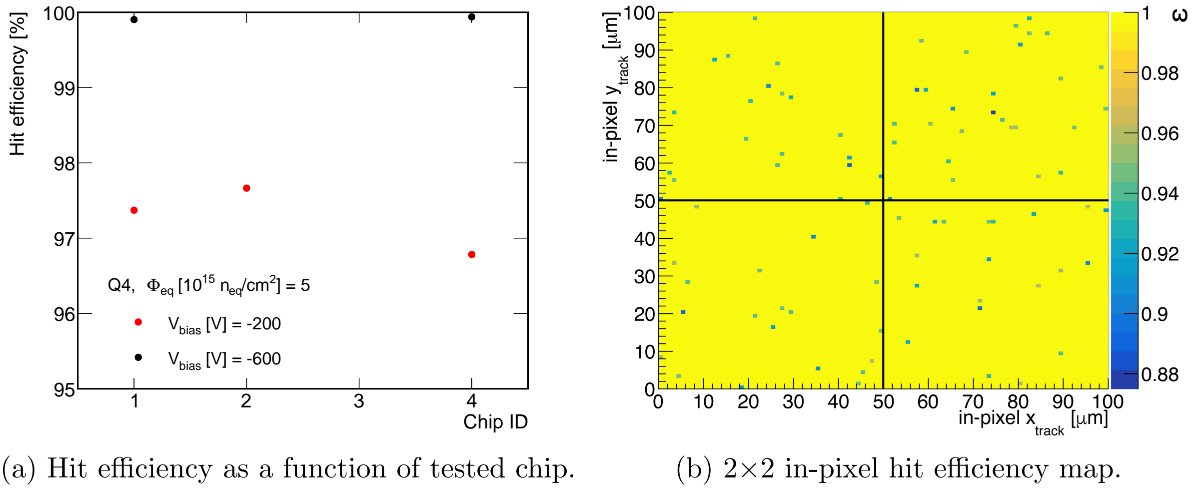


Figure 7.12: In-pixel hit efficiency maps for 50×100 µm^2 size pixels of the inter-chip region between front-ends of a) chips 1 and 2; b) chips 3 and 4 of the quad module Q2.

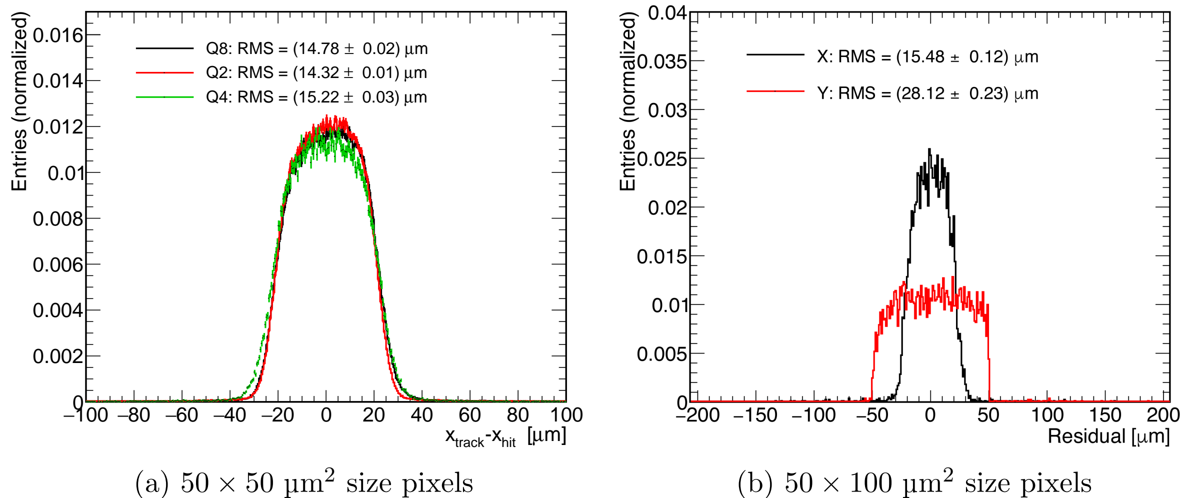


(a) Hit efficiency as a function of tested chip.

(b) 2×2 in-pixel hit efficiency map.

Figure 7.13: Quad module Q4 with the polysilicon resistors as biasing structure, irradiated to a fluence of $5{\cdot}10^{15}$ n_{eq}/cm^2. The discriminator threshold was tuned to 1500 e. Figure a) shows the hit efficiency as a function of tested chip at two bias voltages, while b) shows the 2×2 in-pixel hit efficiency map for 50×50 µm^2 pixels at $V_{\text{bias}} = -600$ V.

At $V_{\text{bias}} = -200$ V, the measured efficiency is $\epsilon = (97.27 \pm 0.02)$ %. At $V_{\text{bias}} = -600$ V, it is $\epsilon = (99.921 \pm 0.005)$ %, which is within the ITk requirements for irradiated modules. In Figure 7.13b the in-pixel hit efficiency map for 50×50 µm^2 size pixels at $V_{\text{bias}} = -600$ V is shown. A uniform hit efficiency is observed over the 2×2 in-pixel map, as it was the case for the non-irradiated module with the same sensor design.



(a) 50×50 µm^2 size pixels

(b) 50×100 µm^2 size pixels

Figure 7.14: Comparison of residual distributions for a) 50×50 µm^2 size pixels of all tested quad modules in x and b) for the two dimensions of the inter-chip region.

7.1.4 Spatial resolution

The residual distributions for two investigated pixel regions are shown in Figure 7.14. The residual distribution in x for tracks intercepting the sensor with 50×50 µm^2 pixels are compared for three quad modules and shown in Figure 7.14a. The indicated RMS values are compatible with the expectation for the given pixel size. The residual distribution of the irradiated quad module Q4 is wider than those of the non-irradiated modules. This is due to the reduced charge sharing after irradiation and an additional contribution of multiple scattering, as this module was surrounded by 10 cm of dry ice during the measurement. Due to the higher beam energy, the residual widths are smaller than those obtained at the DESY II test-beam facility for sensors with the same pixel layout, discussed in Section 6.5.5.

The residual distribution for tracks intercepting the sensor within the inter-chip region is shown in Figure 7.14b. The indicated RMS values for the x and y dimensions are consistent with the expectation for 50×100 µm^2 pixels. Due to the larger datasets available for the ITkPix quad modules, more detailed studies on the spatial resolution of the inter-chip region are performed with those.

7.2 ITkPix quad modules

The testing setup resembles the one used for the RD53A quad modules testing, with only few modifications. The module was mounted on a frame, to which a heat sink is attached for an improved regulation of the module temperature. Besides the beam telescope and tested quad module, the setup included the FE-I4 SCC mounted between the first two telescope planes and used as a timing reference. The spacing between the individual telescope planes is kept the same.

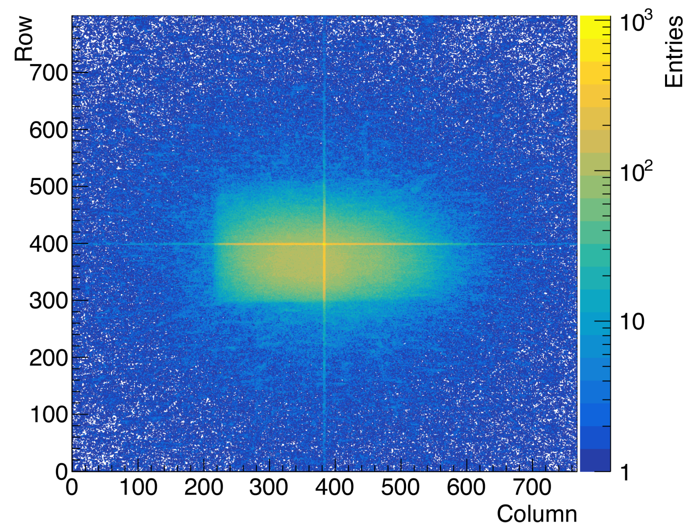
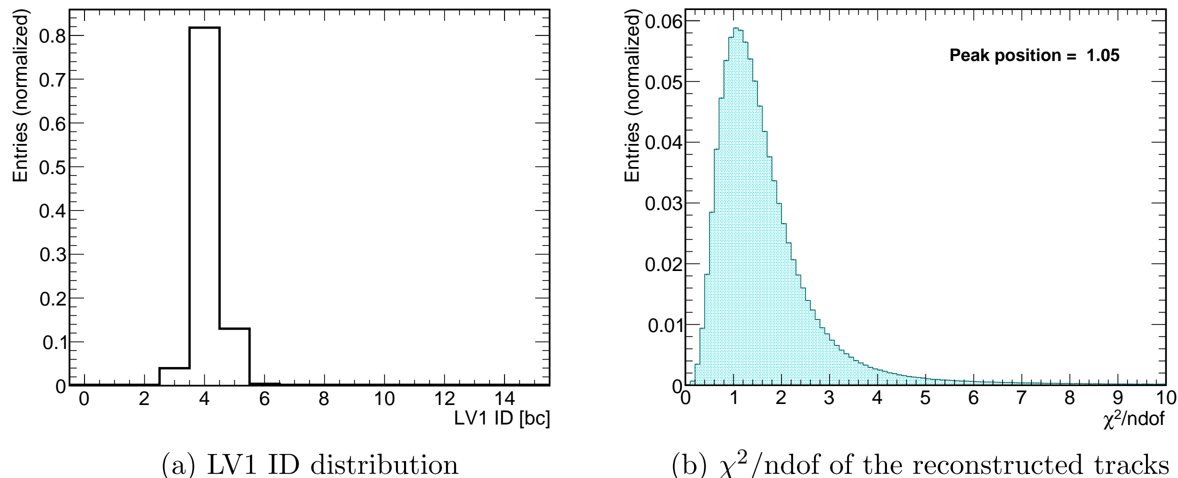


Figure 7.15: The hitmap recorded with the Q9 module for $V_{\text{bias}} = -100$ V and discriminator threshold tuned to 1500 e.

Two non-irradiated ITkPixV1.1 quad modules, with their internal IDs Q6 and Q9, have been available for testing during the time of this thesis. They both feature a 150 µm thick sensor from the HPK manufacturer. The module Q6 has the prototype sensor, also used for the assembly of RD53A modules, where 50% of the inter-chip region pixels are not functioning due to a known problem in the design of the routing of the pixels in the two central columns and rows. The module Q9 features the sensor from the pre-production. Figure 7.15 displays hits recorded with the Q9 module, with a visible structure in the center of the sensor, due to the larger pixels of the inter-chip region that recorded more hits. The module was positioned so that the beam is illuminating its central part to allow the investigation of various pixel sizes, so far inaccessible when testing RD53A quad modules. The majority of hits is recorded in the area defined by the overlap of the scintillators used for triggering, which is smaller than the size of the quad module, see Section 4.3.2.

The list of pixels to be masked in the analysis was created relying on the chip configuration files after the tuning that were stored in the BORE of raw data files. This feature was added to the YarrProducer during the ITkPixV1.1 module testing. Using this method, around 0.1% of pixels on the module Q6 were masked, while this number is only around 0.03% for module Q9. In addition, two central rows and columns of the Q6 module were masked due to the above mentioned problem in the sensor design and thus the total number of masked pixels for this module is around 0.7%.

Track reconstruction was performed using the same set of parameters as for the RD53A quad module analysis. The hit on the reference DUT, which in this case was an FE-I4 SCC, was required without any LV1 ID limits applied. Figure 7.16a shows the LV1 ID distribution for the FE-I4 SCC. Here, the distribution spreads over fewer bins, compared to one of the RD53A SCC used during the RD53A module testing, with more than 80% of the hits recorded within a single bin that is away from the time window boundaries. The



(a) LV1 ID distribution

(b) χ^2/ndof of the reconstructed tracks

Figure 7.16: Figure a) shows the LV1 ID distribution for the FE-I4 module. Figure b) shows the χ^2/ndof distribution of the reconstructed tracks.

Table 7.4: Mean threshold and noise achieved after the tuning with sensor biased to $V_{\text{bias}} = -100$ V.

Module ID	Target threshold [e]	Mean threshold ± RMS [e]	Mean noise ± RMS [e]
Q6	2000	1967 ± 19	106 ± 5
Q9	1500	1492 ± 17	111 ± 5
	2000	1982 ± 21	112 ± 5

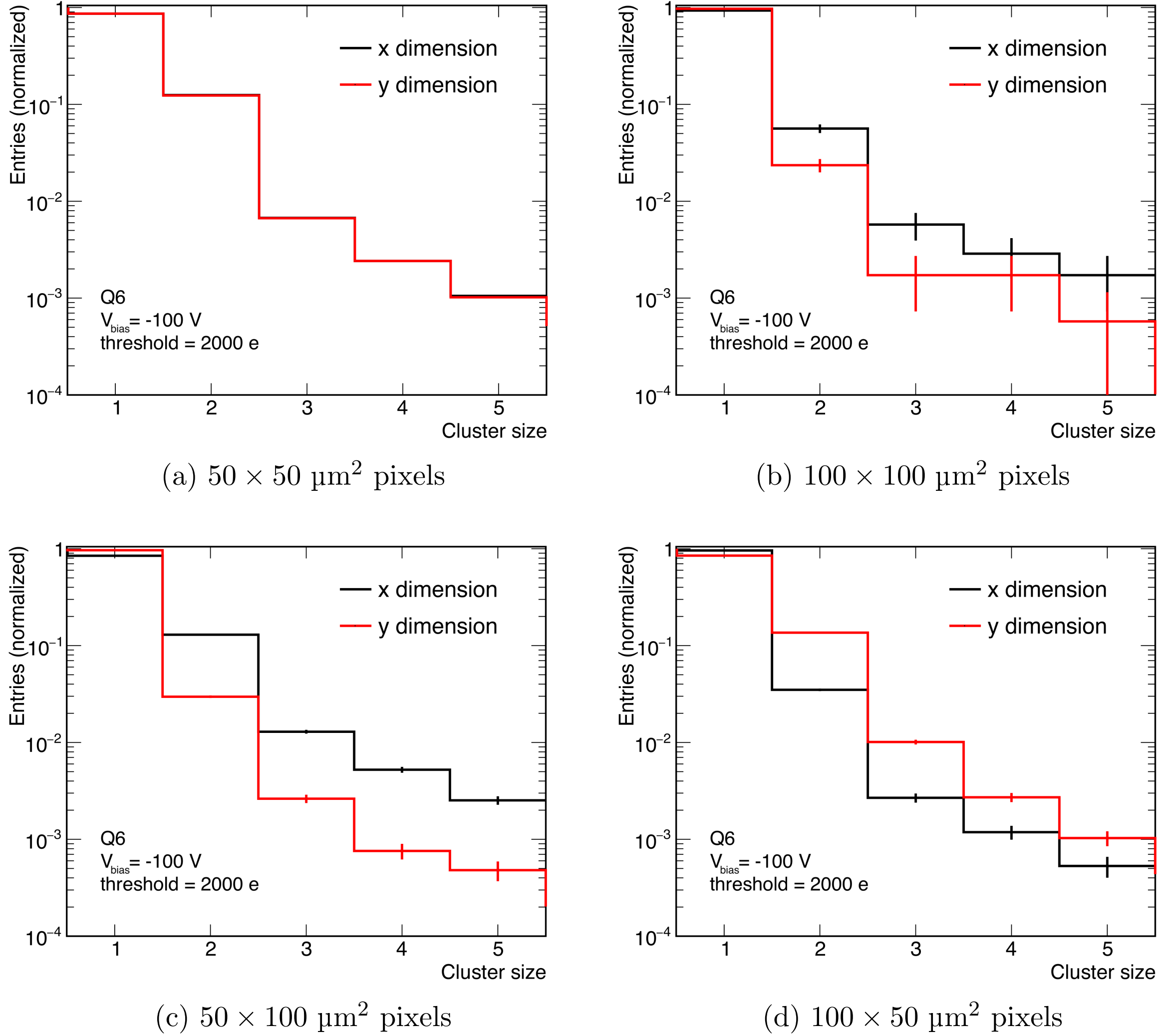
quality of track fitting is again verified with the χ^2/ndof distribution shown in Figure 7.16b, which peaks at 1.05 and decreases towards high values. Around 20% of the reconstructed tracks are discarded due to the unfulfilled χ^2/ndof requirement. Around 9% of tracks on the module Q6 are discarded as they intercept the module in areas with masked neighbors, while this fraction is only around 0.3% for the module Q9.

More than five million events were collected with the Q6 module. This large dataset allows the investigation of different properties for various size pixels. With the module Q9 data were taken at reverse bias voltages between 20 V and 120 V and thresholds of 1500 and 2000 electrons. As these are the first tested ITkPixV1.1 quad modules, details about the achieved mean threshold and corresponding noise for the sum of all four chips are given in Table 7.4.

The cluster size, hit efficiency and spatial resolution are discussed separately.

7.2.1 Cluster size distribution

The cluster size distributions in both dimensions were investigated for various pixel sizes of the quad module. The results are shown in Figure 7.17.



(a) 50×50 µm^2 pixels

(b) 100×100 µm^2 pixels

(c) 50×100 µm^2 pixels

(d) 100×50 µm^2 pixels

Figure 7.17: Cluster size distribution for various pixel sizes of the quad module Q6, for sensor biased to $V_{\text{bias}} = -100$ V and discriminator threshold tuned to 2000 e. The uncertainties are statistical only.

Only clusters on the quad modules assigned to the reconstructed tracks are considered. For 50×50 µm^2 pixels (Figure 7.17a), around 86% of tracks cause one-pixel size clusters, 12% of tracks cause two-pixel size clusters, while larger cluster sizes occur in less than 2% of events. For 100×100 µm^2 pixels (Figure 7.17b), more than 95% of the tracks are inducing one-pixel size clusters. Here, only four pixels, each belonging to a different chip are included in the analysis. For 50×100 µm^2 and 100×50 µm^2 pixels, the distributions depend on the pixel dimension. Along the direction in which a pixel has the size of 50 µm, similarly to Figure 7.17a, one-pixel size clusters occur in around 85% of events, while this number is 10% larger in the dimension where the pixel is larger.

The mean cluster size as a function of track intercept within the pixel matrix is shown in Figure 7.18. As observed for RD53A quad modules, two-pixel size clusters occur only if tracks are passing through a small area at four pixel corners.

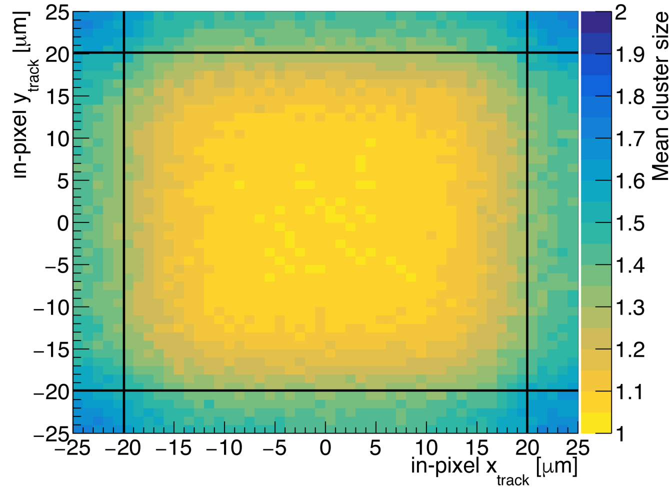


Figure 7.18: In-pixel mean cluster size map of 50 × 50 μm^2 pixels for the Q6 module, operated at $V_{\text{bias}} = -100$ V and discriminator threshold tuned to 2000 e.

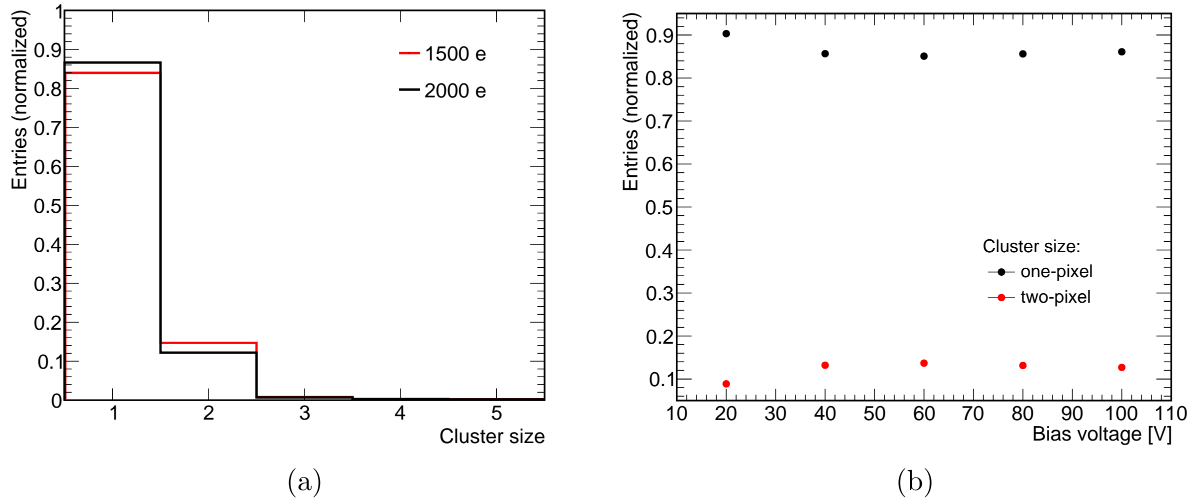


Figure 7.19: Figure a) shows the cluster size distribution for two different threshold settings at $V_{\text{bias}} = -100$ V. Figure b) shows the fraction of one and two-pixel size clusters as a function of the bias voltage at a threshold tuning of 2000 e.

Figure 7.19 shows the cluster size distribution in x as a function of threshold or bias voltage. The number of events inducing two-pixel size clusters decreases with increasing threshold, as seen in Figure 7.19a. The fraction of two-pixel size cluster events is 12.69 ± 0.04 % at 2000 e, compared to 15.15 ± 0.05 % at 1500 e. As shown in Figure 7.19b, for a partially depleted sensor, one-pixel size clusters occur in 90% of the events. With increased bias voltage also the fraction of two-pixel size clusters increases.

7.2.2 Hit efficiency

The measured hit efficiencies are discussed separately for the two tested modules.

Quad module Q6

The hit efficiency as a function of track intercept within the pixel area is shown in Figure 7.20 for the different pixel sizes, introduced in Figure 6.2b. The bin size is larger for pixels of the inter-chip region. In addition, a different treatment of masked pixels is applied. For 50×50 µm^2 pixels, the standard procedure of rejecting tracks that intercept pixels with a masked neighbor is used. However, this could not be used for the pixels of the inter-chip region as it would lead to the exclusion of all tracks that pass this area due to the two central rows and columns been masked.

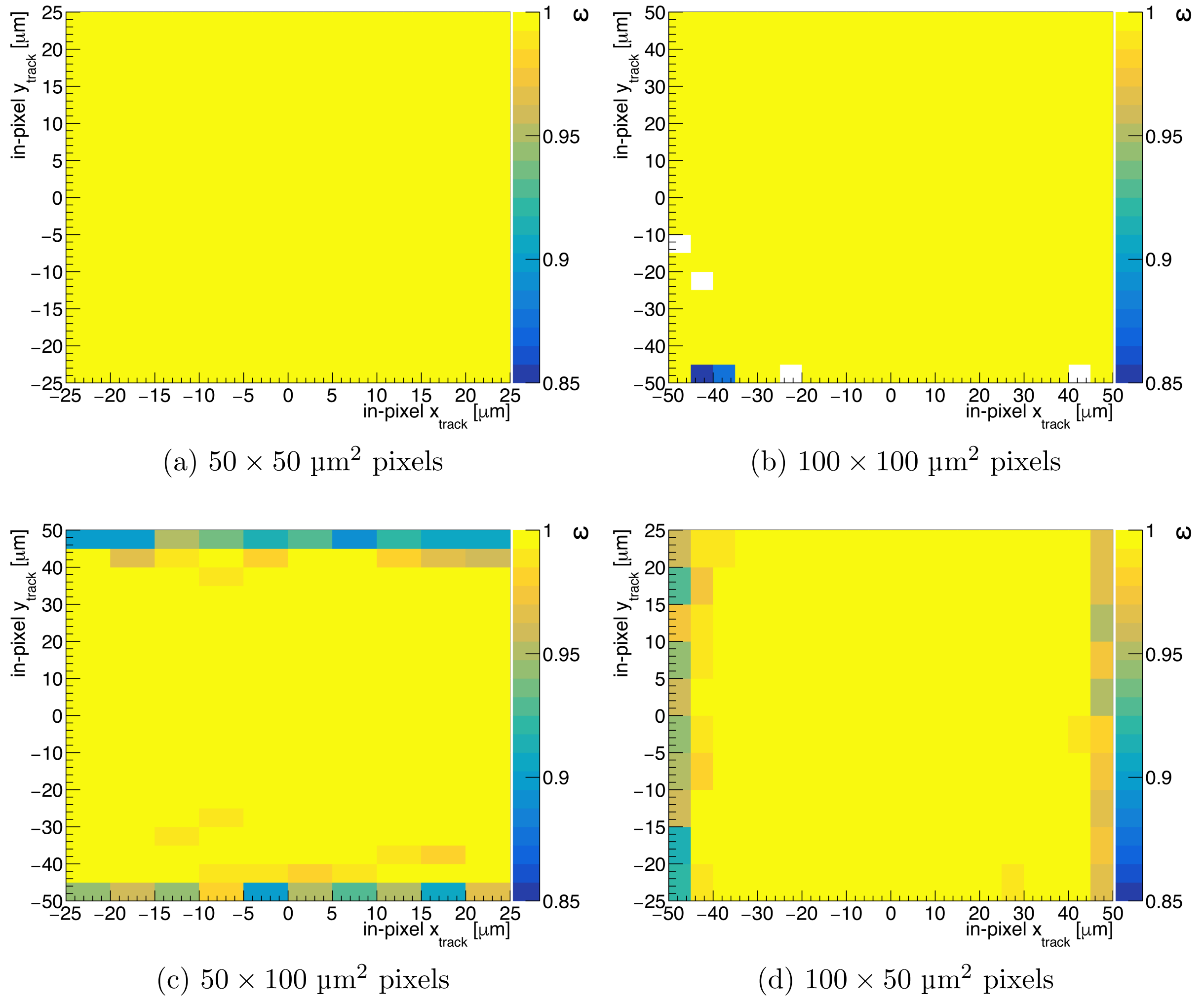
The determined hit efficiency values are summarized in Table 7.5. More than 77% of all tracks accepted for analysis are intercepting the module in the areas covered by pixels of 50×50 µm^2 size. For this pixel type, the hit efficiency of $\epsilon = (99.954 \pm 0.001)$ % was obtained. Around 0.06% of all reconstructed tracks are passing through the center of the quad module where 100×100 µm^2 pixels are. For this case the determined hit efficiency is $\epsilon = (99.7 \pm 0.1)$ %. The in-pixel hit efficiency maps for these two pixel sizes, shown in Figures 7.20a and 7.20b, are uniform.

Hit efficiencies of $\epsilon = (99.23 \pm 0.03)$ % and $\epsilon = (99.39 \pm 0.03)$ % are determined for pixel sizes 50×100 µm^2 and 100×50 µm^2, respectively. Again, in-pixel hit efficiency maps for the two cases show the regions of lower efficiency along the 100 µm (50 µm) dimension for 50×100 µm^2 (100×50 µm^2) pixels, due to the masked two central rows (columns) of the inter-chip region.

Table 7.5: The hit efficiency for the various pixels sizes of the Q6 module at $V_{\text{bias}} = -100$ V and for a threshold tuning to 2000 e.

Pixel size [µm^2]	Hit efficiency [%]
50×50	99.954 ± 0.001
50×100	99.23 ± 0.03
100×50	99.39 ± 0.03
100×100	99.7 ± 0.1

The hit efficiency as a function of column or row is shown in Figure 7.21. Both figures are shown for the ranges of pixels with sufficient illumination by the beam. Hit efficiencies of above 99.9% are determined for most of the columns and rows, except for pixels of the inter-chip region.



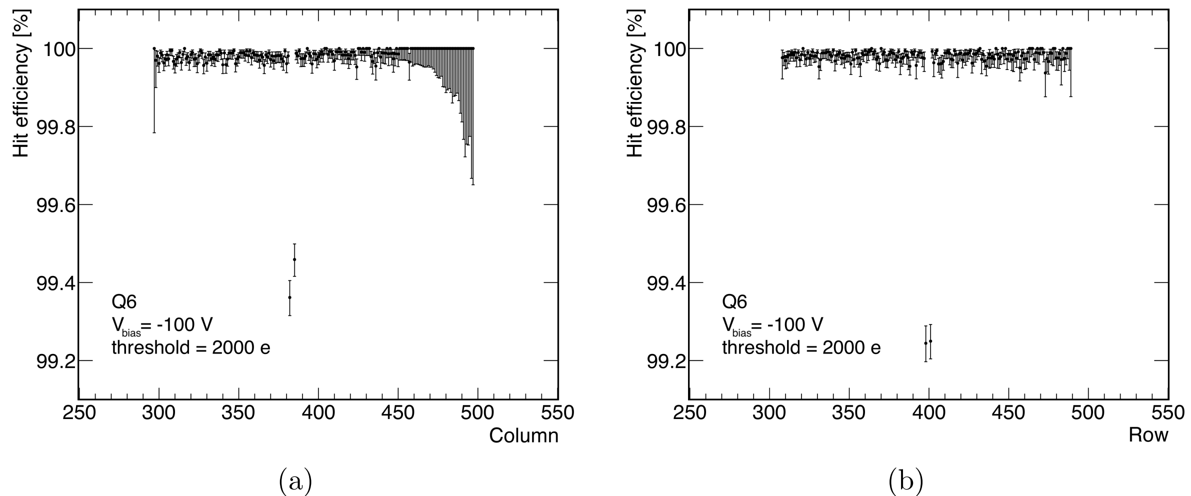
(a) 50 × 50 μm² pixels

(b) 100 × 100 μm² pixels

(c) 50 × 100 μm² pixels

(d) 100 × 50 μm² pixels

Figure 7.20: In-pixel hit efficiency maps for various pixel sizes of the quad module Q6 operated at $V_{\text{bias}} = -100$ V and for a threshold tuning to 2000 e.



(a)

(b)

Figure 7.21: Hit efficiency as a function of a) column and b) row, summing over all pixels in the respective other dimension, for quad Q6 operated at $V_{\text{bias}} = -100$ V and for a threshold tuning to 2000 e.

Quad module Q9

The quad module Q9 was tested at different operational conditions. At $V_{\text{bias}} = -100$ V, the data were taken at two target thresholds: 1500 e and 2000 e. The determined hit efficiencies for different pixel flavors are summarized in Table 7.6. For all pixel sizes, a decrease in the hit efficiency is observed at the higher threshold tuning. The hit efficiencies for 50×100 µm^2 and 100×50 µm^2 pixels are around 99.8% for a discriminator threshold of 2000 e. This is higher in comparison with the Q6 module, as here the effect of the efficiency loss due to the neighboring masked pixel is not present. The lowest efficiency of around 98.6% is observed at 2000 e for the largest pixel size. This is due to one of the 16 pixels, with a hit efficiency of around 77%. However, this is not observed at the lower threshold, hinting to a tuning problem.

The hit efficiency as a function of the track intercept over the area of around 2×1 cm^2 determined by the size of the overlapping scintillators is shown in Figure 7.22. The beam spot is at the center of the quad module. No dependence of the hit efficiency on the readout chip is observed.

The hit efficiency as a function of applied bias voltages was investigated at the threshold of 2000 e. The obtained results are shown in Figure 7.23 for all pixel types. The previously identified problematic pixel in the central part of the sensor is excluded from this analysis. A hit efficiency above 99% is observed for all pixel sizes even at $V_{\text{bias}} = -20$ V, while the depletion voltage of this sensor is $V_{\text{fd}} = -60$ V. Assuming that 80 electrons are created per micron of depleted silicon, MIPs would create 12000 electrons in a 150 µm thick sensor. At $V_{\text{bias}} = -20$ V, the width of the depletion region would be around 80 µm, which is already enough to create a signal well above the discriminator threshold.

Table 7.6: The hit efficiency for the various pixels sizes of the Q9 quad module at bias voltage of $V_{\text{bias}} = -100$ V and for two threshold settings.

Pixel size [μm^2]	1500 e	2000 e
50 × 50	99.792 ± 0.006	99.545 ± 0.008
50 × 100	99.93 ± 0.02	99.84 ± 0.02
100 × 50	99.94 ± 0.02	99.80 ± 0.03
100 × 100	99.9 ± 0.1	98.6 ± 0.4

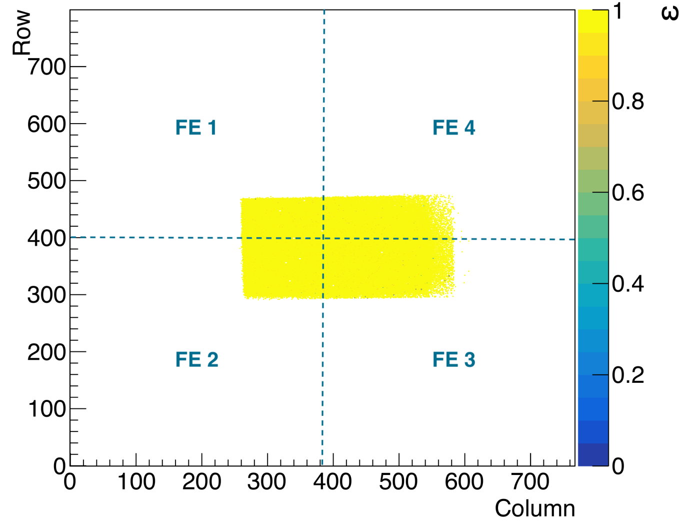


Figure 7.22: Hit efficiency for Q9 over the sensor surface accepted by the trigger scintillators at $V_{\text{bias}} = -100$ V and disciriminator threshold tuned to 1500 e.

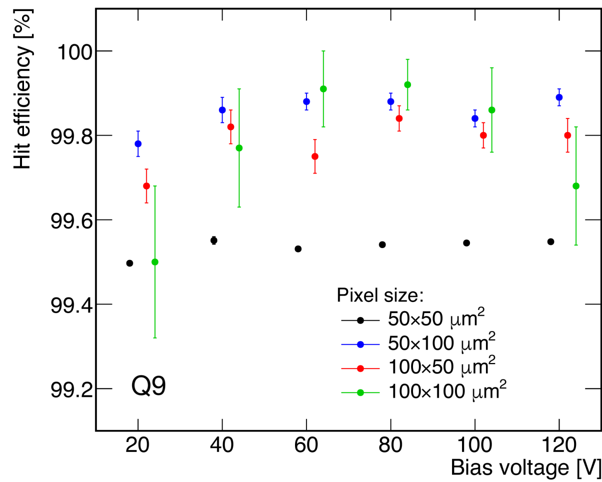


Figure 7.23: Hit efficiencies for the different pixel types as functions of the bias voltage at a tuned threshold to 2000 e. For better visibility, the data taken at the same bias voltage are horizontally displaced.

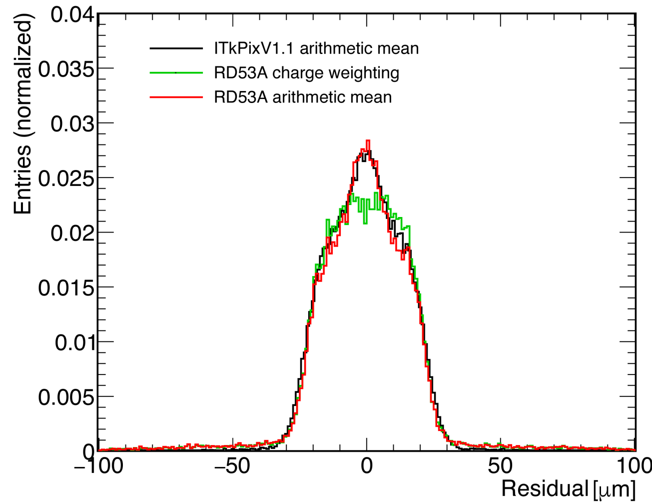
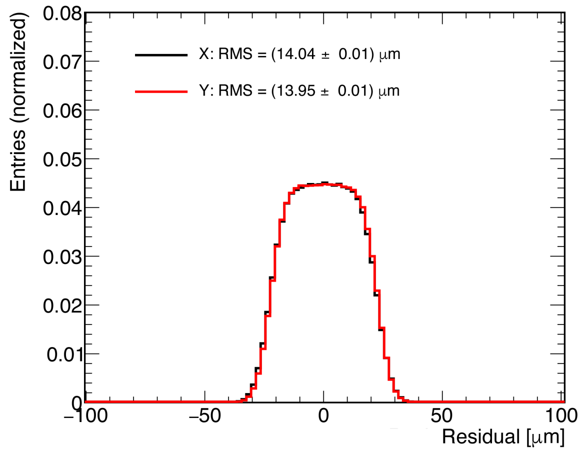


Figure 7.24: Distribution of unbiased residuals for the ITkPixV1.1 module Q6 compared to the one from an RD53A module calculated with two clustering algorithms.

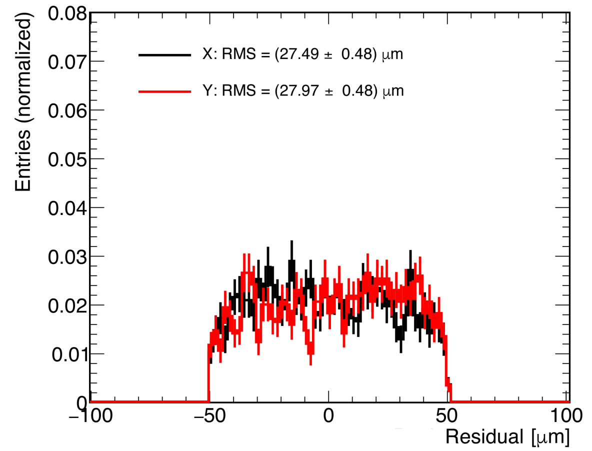
7.2.3 Spatial resolution

Due to the known problem of the ToT memory latch in the ITkPixV1.1 chip, all pixels have a ToT value of 7. Therefore, the cluster center is obtained using the arithmetic mean, instead of the charge weighting center-of-gravity method. As a consequence, the distribution of unbiased residuals has a specific shape, with a wide peak around zero, instead of a flat region. To confirm that the clustering algorithm is the reason for the shape distribution of the unbiased residuals for the ITkPixV1.1 quad modules, it is compared with the RD53A quad module distributions for both clustering methods, as shown in Figure 7.24. Indeed, this special shape of the distribution is visible for both types of modules when using the arithmetic mean to calculate the cluster center position.

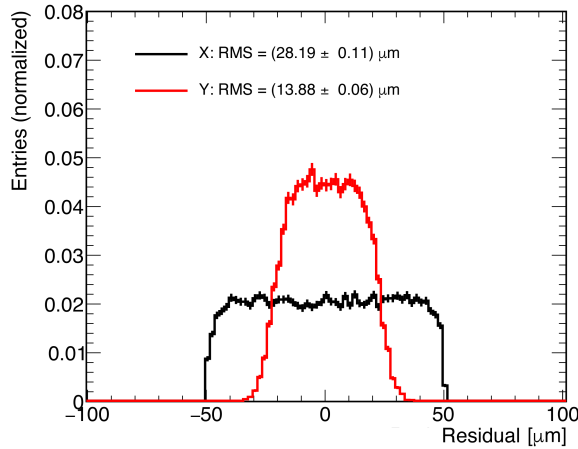
As the determination of the cluster center is not affected for one-pixel size clusters, which do represent more than 85% of all events, only this case will be discussed. The residual distributions in x and y for various pixel sizes are shown in Figure 7.25. The indicated histogram RMS values are compatible to the expectation for their respective pixel sizes, i.e. σ_{int} (50 µm) = 14.4 µm, σ_{int} (100 µm) = 28.9 µm. However, they are slightly below the expectation, as only tracks that induce one-pixel size clusters are included in the analysis. Tracks intercepting pixels near the edge will lead mostly to two-pixel size clusters and therefore the pixel area where one-pixel size clusters occur is smaller than the actual pixel size, see e.g. Figure 7.18.



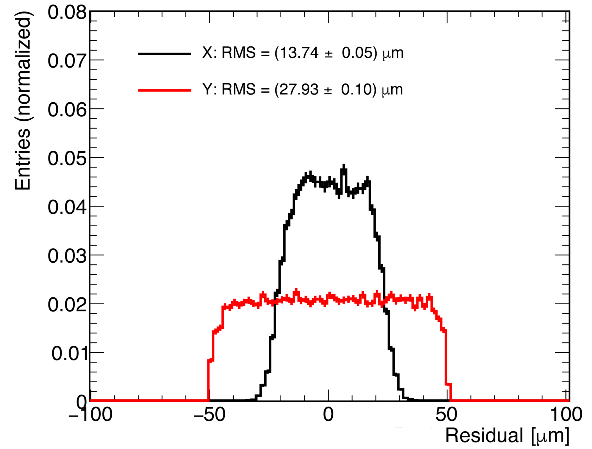
(a) 50 × 50 µm^2 pixels



(b) 100 × 100 µm^2 pixels



(c) 100 × 50 µm^2 pixels



(d) 50 × 100 µm^2 pixels.

Figure 7.25: Residual distributions for various pixel sizes of the quad module Q6 operated at $V_{\text{bias}} = -100$ V and for a threshold tuning to 2000 e.

7.3 Conclusions

During the test-beam campaigns in 2021, three RD53A quad modules with prototype sensors from two manufacturers were successfully tested. One of the tested modules was irradiated to a fluence of $5 \cdot 10^{15}$ n_{eq}/cm^2. These tests allowed not just to verify the operation of the quad modules in the test-beam setup, but to test the software development performed to accommodate the non-uniform layout of the quad sensor. It is observed that the charge sharing decreases with irradiation, leading to fewer two-pixel size clusters created by passing tracks. For both non-irradiated and irradiated modules, the obtained hit efficiencies are within the ITk requirements for planar sensors. A value of around 98.7% is obtained for the module featuring the Micron sensor with punch-through, while around 99.9% is achieved for modules with HPK sensors and polysilicon resistors as a biasing structure. The first validation of the inter-chip region was achieved by illuminating the area of interest with the beam. In this case the hit efficiency obtained is around 98.9% and 99.5% for modules with Micron and HPK sensors, respectively.

A more detailed study of the inter-chip region was possible in 2022 with two ITkPixV1.1 modules, featuring the full-size chip and sensors from the same manufacturer. However, one of these modules has the HPK sensor from the prototype production, that contained a design bug in the inter-chip region leading to pixels not properly connected to the chip. An improvement in the analysis was achieved by using the chip configuration file after the tuning to determine which pixels should be masked for the data reconstruction. Using this method, around 0.7% of pixels are masked for the module with the prototype sensor and only 0.03% for the one with the sensor from pre-production. It is observed that the charge sharing increases with increased reversed bias voltage and decreased threshold. The obtained results for the hit efficiency are consistent with those achieved with the previously tested RD53A module featuring the same sensor type. No efficiency loss is observed for the pixels of the inter-chip region. In addition, a hit efficiency above 99% is observed even at a bias voltage of $V_{bias} = -20$ V for a sensor with $V_{fd} = -60$ V. The width of the residual distributions agree with the expectation for various pixel sizes.

8 Quality assurance of the pre-production sensors

Quality Assurance (QA) measurements are planned to be performed mainly during the pre-production phase to prevent mistakes and defects in the manufacturing process and gain confidence that the manufactured sensors fulfill all ITk requirements. The pre-production refers to the initial production of 10% of the total number of sensors. The measurements involve sensor characterization using the probe station setup described in Section 4.1.

The MPP is involved in the sensor QA activities for the Micron 100 µm thick sensors, which will be used for the assembly of Layer 1 modules. The requirements for sensors of this thickness are summarized in Table 8.1.

Table 8.1: The requirements on the leakage current, depletion voltage and breakdown voltage for the 100 µm thick planar sensors. The measurements are performed at 20°C for non-irradiated and at −25°C for irradiated sensors.

Measurement	Requirement
CV	$V_{fd} < 60$ V
IV	I_{leak} (V_{fd} + 50 V) < 0.75 µA/cm^2 (before irradiation)
	I_{leak} (300 V) < 20 µA/cm^2 ($\Phi_{eq} = 2 \cdot 10^{15}$ n_{eq}/cm^2)
	I_{leak} (400 V) < 35 µA/cm^2 ($\Phi_{eq} = 5 \cdot 10^{15}$ n_{eq}/cm^2)
	$V_{bd} > V_{fd}$ + 70 V (before irradiation)
It	Variations of I_{leak} are within ± 25% over 48 h

For this thesis, several structures from one diced wafer were available for these measurements. The wafer map is given in Figure 8.1. On each wafer, five quad sensors, identified with letters A-E, are placed, together with additional test structures (TS). The punch-through biasing is implemented in the sensor design. In this chapter only measurements performed on the quad and single-chip (TS type F, in further text referred to as TSF) sensors will be discussed. All measurements are performed with reverse bias. Out of those available, two single-chip sensors were irradiated to a fluence of $2{\cdot}10^{15}$ n_{eq}/cm^2, while one single-chip and two quad sensors were irradiated to a fluence of $5 \cdot 10^{15}$ n_{eq}/cm^2. The temperature of the probe station chuck was set to 20°C for non-irradiated sensors and to −25°C for irradiated sensors. During all measurements, the relative humidity measured in the probe station volume was below 20%.

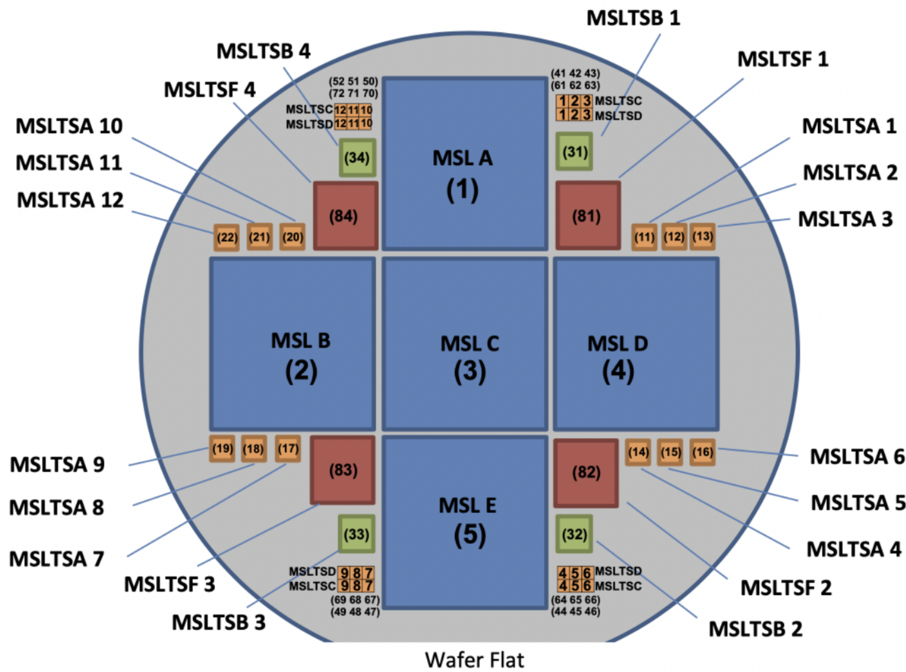


Figure 8.1: Wafer map for the sensor production by Micron Semiconductor Ltd (MSL), containing five quad sensors MSL A-E and test structures MSLTSX n, where X refers to the type of the structure and n is the number that depends on its location on the wafer.

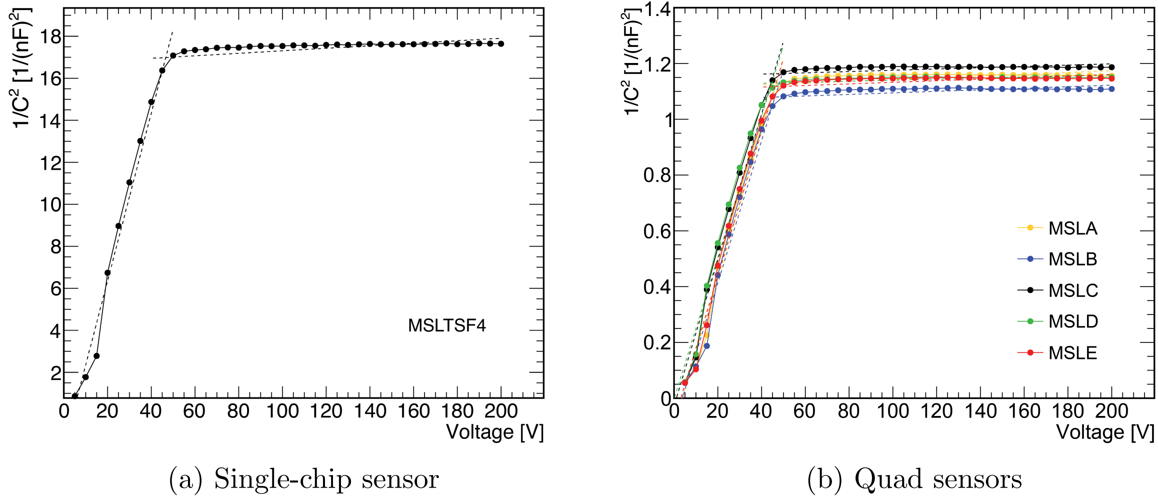
8.1 Capacitance-voltage characteristics

The results of the CV measurement are given in Figure 8.2, separately for one single-chip (TSF4) and five quad sensors. Obtained values for the full-depletion voltage are in the range of 40-45 V, which is within the ITk requirements, see Table 8.1. The capacitance determined for the fully depleted single-chip sensor is around 240 pF, and around 930-950 pF for quad sensors, which is expected as they are four times as large.

8.2 Current-voltage characteristics

The IV measurements on the non-irradiated sensors were performed in a voltage range of 0-200 V. This range was extended to 600 V for irradiated sensors. The current compliance was set to 20 µA for two sensors that were planned to be sent for the irradiations, while 100 µA was used for the other three quad sensors. For measurements of the irradiated sensors, the current compliance was increased to 500 µA.

Figure 8.3 shows the leakage current per area as a function of the bias voltage for tested sensors. In addition, measurements for non-irradiated quad sensors performed by the manufacturer before and after dicing are normalized to $T = 20°\mathrm{C}$ and displayed. No breakdown is



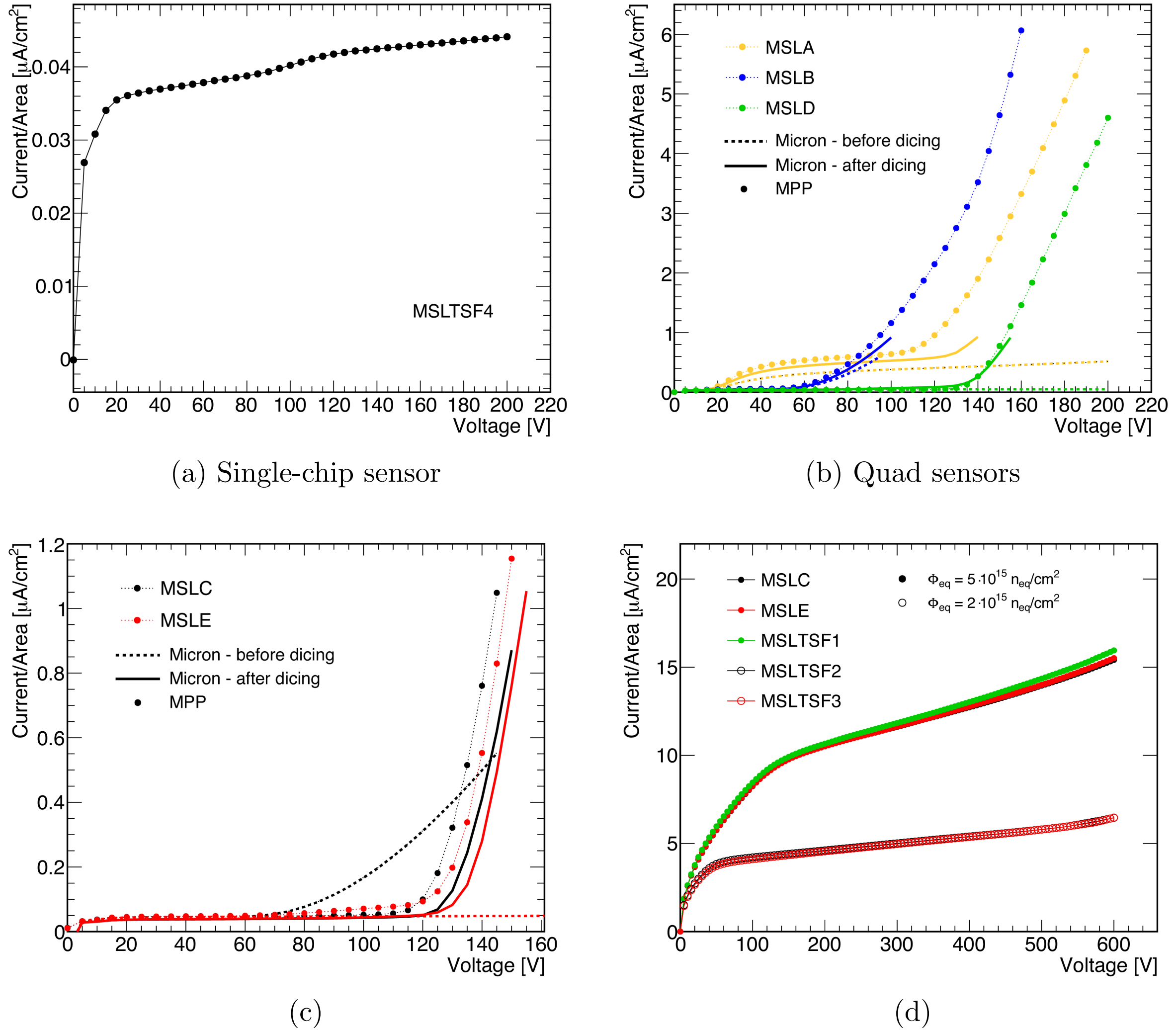
(a) Single-chip sensor (b) Quad sensors

Figure 8.2: The inverse capacitance squared as a function of the bias voltage measured for a) one single-chip and b) all non-irradiated quad sensors.

observed for the non-irradiated single-chip sensor in the tested voltage range (Figure 8.3a). The results for the quad sensors are displayed separately for sensors A, B and D in Figure 8.3b, and in Figure 8.3c for sensors C and D that were later sent to irradiation. For all sensors, a decrease of the breakdown voltage is observed after dicing. The exception is the measurement for the sensor C, which shows an early breakdown before dicing. Although the shape of the IV curve obtained at MPP agrees with that of the manufacturer after dicing, the obtained breakdown voltage is lower. Nevertheless, the ITk requirement on the breakdown voltage is satisfied for sensors C, D and E. The measured leakage current per area at 95 V for these sensors is around 0.05 µA/cm^2 at 20°C. One of the quad sensors (B) has a breakdown voltage of around 60 V. For quad sensor A, the leakage current increases for voltages between 20 V and 40 V, after which the curve has the typical shape and a breakdown around 110 V. Both observations are consistent with measurements performed by the manufacturer. In Figure 8.3d the leakage current per area as a function of bias voltage for the irradiated quad sensors C and E, and three irradiated single-chip sensors is shown. No breakdown is observed for the measured bias voltages. Measurements for the quad sensors and the single-chip sensor TSF1, irradiated to a fluence of $5{\cdot}10^{15}$ n_{eq}/cm^2, agree. The same holds for the single-chip sensors TSF2 and TSF3, that are irradiated to a fluence of $2{\cdot}10^{15}$ n_{eq}/cm^2. The leakage current per area at 300 V is around 5 µA/cm^2 for sensors irradiated to a fluence of $2{\cdot}10^{15}$ n_{eq}/cm^2, and around 13 µA/cm^2 at 400 V for those irradiated to a fluence of $5{\cdot}10^{15}$ n_{eq}/cm^2. Both values are within the ITk requirements.

8.3 Long-term current stability

For the non-irradiated quad sensor D, the current stability test was performed at different bias voltages. The results are shown in Figure 8.4a. For this sensor V_{fd} is around 40 V



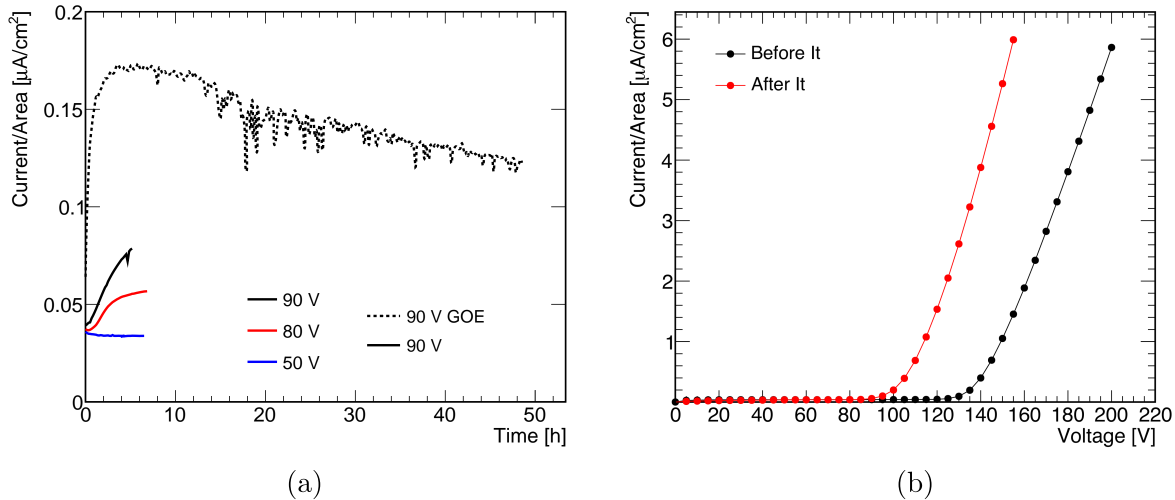
(a) Single-chip sensor

(b) Quad sensors

(c)

(d)

Figure 8.3: Leakage current per area as a function of bias voltage for different sensors. Figure a) shows the result obtained for the non-irradiated single-chip sensor (TSF4). In figure b) obtained results for quad sensors A, B and D are displayed. Results for quad sensors C and E are shown in figure c) before and in d) after irradiation. In addition, in d) are shown the results from irradiated single-chip sensors. In b) and c) also the measurements from the producer obtained before and after dicing are shown. Statistical uncertainties are displayed, but are smaller than the marker size.



(a)

(b)

Figure 8.4: Figure a) shows the leakage current variation with time for three different bias voltages, while b) shows the IV measurements performed before and after the leakage current stability test (It).

(Figure 8.2b), leading to an operation voltage of 90 V. The breakdown voltage is around $V_{\text{bd}} = 140$ V (Figure 8.3b). The measurement was performed for only five hours, instead of the required 48 hours, due to the observed continuous increase of the leakage current for bias voltages 80, 90 V, i.e. close to the operational voltage. The leakage current is stable for the bias voltage around the full-depletion voltage. In addition, the It measurement of 48 hours was performed by the University of Göttingen, confirming the increase of the leakage current in the first five hours of the measurement, after which a decrease is observed. However, the measured leakage current at the same bias voltage is higher than that measured at the MPP. Figure 8.4b shows the IV measurement performed before and after the leakage current stability test, where a decrease of the breakdown voltage is observed after the sensor was biased for a long time. More data is needed to understand if this is a feature of this sensor or of all non-irradiated Micron sensors. All measurements were performed at a relative humidity below 10%.

Figure 8.5 shows the same measurement performed at 400 V on two irradiated quad sensors. For both, a steep decrease of the leakage current is observed within the first five hours of the measurement, after which the current is stable. Overall fluctuations of the leakage current are within the ITk requirements.

8.4 Conclusions

Sensor characterization was performed for selected structures from one 100 µm thick Micron wafer from the pre-production. The full-depletion voltage for all quad sensors is around 45 V, and thus within the ITk requirements. Three out of five tested quad sensors are considered good in terms of the observed breakdown voltage and leakage current per area

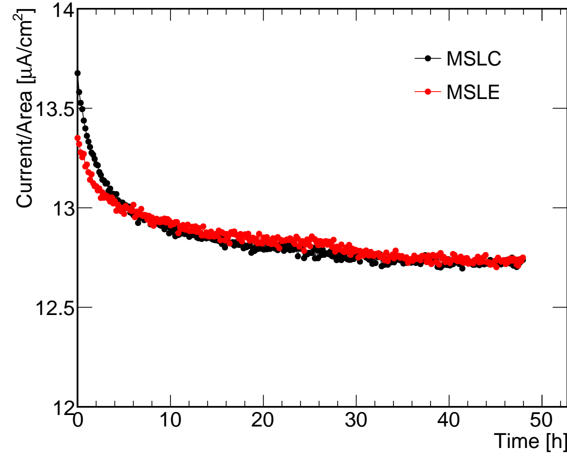


Figure 8.5: Leakage current stability test at 400 V for quad sensors C and E irradiated to a fluence of $5{\cdot}10^{15}$ n_{eq}/cm^2.

at the operational voltage. For quad sensors irradiated to the fluence of $5\cdot10^{15}$ n_{eq}/cm^2 no breakdown is observed up to 600 V. The IV measurements for quad and single-chip sensors irradiated to the same fluence agree. The leakage current stability test performed for five hours on one non-irradiated sensor revealed a continuous increase of the leakage current with time when the bias voltage is close to the expected operational voltage. For the same measurement time, the increase of the leakage current is observed by the University of Göttingen as well, after which the leakage current decreases. In addition, a decrease of the breakdown voltage is observed when a sensor is biased for a long time. The same measurement on two irradiated sensors for 48h shows a leakage current variations within the specifications.

9 Conclusions and outlook

In collider experiments tracking detectors are crucial to precisely determine the trajectories of charged particles. The ITk collaboration is constructing a new ATLAS all-silicon tracking system with improved tracking performance despite the challenging environment of the high luminosity LHC. The extensive R&D campaign to choose the most suitable sensor technology was successfully completed. The thin n^+-in-p sensor technology developed by the MPP was chosen, which implements thinner sensors and smaller pixel sizes with respect to the original pixel detector of the ATLAS experiment. The next step for the ITk pixel project is the production, assembly and testing of pixel modules.

One aspect of this thesis was the evaluation of the performance of the first assembled modules with RD53A prototype chips in a series of laboratory measurements, as a preparation for the routine testing of the modules assembled at MPP. For this, the testing setup was produced and optimized. The chip parameters, discriminator threshold and ToT of the readout chips were tuned. Three RD53A front-end flavors were tested separately. A series of scans was performed to confirm the tuning quality and determine the numbers of pixels that fail different testing stages. Obtained results gave an insight into details of the module behavior with respect to the sensor type they are featuring. The noise values determined for the modules with HPK sensors are around twice that of the modules with Micron or HLL sensors. The achievable mean discriminator threshold for all chips is significantly below the target threshold regardless of the sensor type to which the chip is bump-bonded or the front-end flavor. It was observed that for around 4% of pixels of the chosen differential front-end flavor, the tuning of the discriminator threshold failed. Most of these pixels are those identified to be implemented with the missing buffer element between the discriminator output and the input into the digital logic. The performance of the differential front-end is expected to be improved in the production version of the chip. To assess the quality of the bump-bonding process, two types of scans were performed which determine the fraction of disconnected pixels. The first type is the crosstalk scan, which is fast and can be used to early discover a potential problem with bump-bonds. As indicated by the name, this scan can only be used to identify disconnected pixels if their neighbors are connected. Using this method, around 0.3% of disconnected pixels per chip were found. No increase in this number was observed after the thermal cycling ten times between $-45°$C and 40°C, indicating sufficient rigidity against thermal stress. The more reliable method for identifying disconnected bumps is to use a radioactive β source and identify pixels that do not record any hit. No disconnected pixels were identified using this method. The performed module characterization also allows identifying parts of the testing procedure that require further optimization before entering the phase of module assembly with pre-production sensors. For the ^{90}Sr source at MPP, to ensure that the

minimum required number of hits per pixel is satisfied for all pixels, including those under the SMD components, the scan duration should be at least three hours. Thermal cycling is a lengthy procedure of more than ten hours. In the context of the setup optimization for the pre-production, this step should be performed for multiple modules simultaneously. The same is true for the long-term stability test, where modules are read out continuously for 48 hours. The corresponding adaptations of the setup are ongoing.

Besides the laboratory measurements, quad modules were tested with particle beams. These tests are crucial, since the modules are operated in realistic conditions, with external trigger signals and in synchronization with other detectors. The ITk project is entering the phase of pre-production, where modules featuring sensors from different manufacturers will be tested before and after the irradiation. To enable smooth and quick evaluation of the device performance from collected test-beam data, it is essential to have a reliable and highly configurable software. The Corryvreckan package was recognized as a software that fulfills these requirements. The transition to the new framework for the ITk pixel test-beam group was performed within this thesis. This included setting up the reconstruction and analysis flow and further software development necessary for the quad module testing with sensors employing a non-uniform pixel matrix. The last step was a performance validation, used to confirm that results achieved at each reconstruction step using the Corryvreckan framework are consistent with those obtained with the previously used combination of the EUTelescope and TBmon2 packages.

During 2021 and 2022, five quad modules were tested with particle beams. These include three RD53A quad modules with 150 µm thick prototype sensors from two manufacturers, HPK and Micron, out of which one was irradiated to a fluence of $5 \cdot 10^{15}$ n_{eq}/cm^2. These first tests were used to verify the operation of the quad modules in the test-beam setup and to validate the software development performed to enable the study of the properties of various pixel sizes on the quad module. For both non-irradiated and irradiated modules, the hit efficiency obtained is within the ITk requirements for planar sensors. For modules with HPK sensors, the efficiency above 99.9% was determined before and after irradiation. The measurement after irradiation was performed at $V_{\text{bias}} = -600$ V. A lower efficiency of around 98.7% was determined for the module with Micron sensors, with implemented punch-through biasing structures. Among the tested quad modules, two featured the full-size chip ITkPixV1.1 and 150 µm thick sensors from HPK. One of the tested modules has the HPK sensor from the prototype production. Obtained results for the hit efficiency are consistent with those obtained for the previously tested RD53A module featuring the same sensor type. The hit efficiency above 99.8% was obtained for various pixel sizes of the inter-chip region. In addition, a hit efficiency above 99% is observed even at a bias voltage of $V_{\text{bias}} = -20$ V for a sensor with a full-depletion voltage of -60 V. Besides analyzing the data from the ITkPix quad module, the presented analysis was successfully used for the evaluation of the performance of ITkPix modules with 3D sensors. The width of the residual distribution agrees with the expectation for the respective pixel size across all tested quad modules. All modules are tested at perpendicular beam incidence. In such conditions, the majority of passing tracks, around 85%, are inducing one-pixel size clusters. In the ITk detector this situation is rare as it corresponds to $\eta = 0$. Most of the modules will be traversed at a smaller inclination angle. Therefore, one of the planned tests

for the upcoming test-beam campaigns is to perform measurements at various inclination angles and investigate the charge sharing effect. In addition, more detailed hit efficiency determinations as functions of the discriminator threshold and bias voltage after irradiation are planned to be performed.

During the pre-production, a series of quality assurance tests will be performed at sensor level to confirm the desired quality of the manufactured sensors. As a part of these measurements, the characterization of sensors from one 100 µm thick Micron wafer was performed within this thesis. All five tested sensors have the full-depletion voltage within the ITk requirements. Three of those fulfilled the requirements for breakdown voltage and leakage current at the operational voltage. Two sensors were irradiated to a fluence of $5 \cdot 10^{15}$ n_{eq}/cm^2. The IV measurements after the irradiation show no breakdown up to 600 V. For one of the non-irradiated quad modules it was observed that the breakdown voltage decreases after the sensor was biased for a long time. In addition, the leakage current stability test, performed over five hours on the same sensor, showed an increase of the leakage current with time. This test was performed over 48 hours at the University of Göttingen, that confirmed the increase of the leakage current during the first five hours of measurement, after which a decrease was observed. In addition, the two irradiated sensors fulfill the requirement for long-term current stability. This observation is reported to the sensor manufacturer and will be followed up by additional measurements performed on sensors and test structures from different wafers, when available.

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Šejla Hadžić, Munich 2023

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