Properties of High-Capacitance Gate Dielectrics and their Application in Low-Voltage Organic Thin-Film Transistors

Michael Geiger

München 2022

Properties of High-Capacitance Gate Dielectrics and their Application in Low-Voltage Organic Thin-Film Transistors

Michael Geiger

Dissertation
der Fakultät für Physik
der Ludwig-Maximilians-Universität
München

vorgelegt von
Michael Geiger
aus Wernau am Neckar

München, den 16.03.2022

Erstgutachter: Prof. Dr. Thomas Weitz
Zweitgutachter: PD. Dr. Bert Nickel
Tag der mündlichen Prüfung: 26.04.2022

Kurzfassung

Organische Dünnschichttransistoren (TFTs) stellen vielversprechende Bauelemente für die Erschließung zukünftiger elektronischer Anwendungsgebiete dar. Die geringen Prozesstemperaturen bei der Abscheidung von organischen Halbleitern ermöglichen den Einsatz von unkonventionellen Substratmaterialien, einschließlich hochflexibler Kunststoffe. Damit lassen sich neuartige elektronische Bauelemente wie beispielsweise flexible Aktiv-Matrix-Displays oder biokompatible Sensoren realisieren. Eine Schlüsselkomponente organischer TFTs ist das Gate-Dielektrikum.
In der vorliegenden Arbeit werden verschiedene Aspekte eines hybriden Gate-Dielektrikums, bestehend aus einer dünnen Metalloxid-Schicht und einer molekularen selbstorganisierten Monolage (SAM), untersucht. Dabei steht die Rolle der Metalloxid-Schicht im Mittelpunkt. Der erste Teil der Arbeit hat zum Ziel, eine theoretische Methode zur Quantifizierung von Fallenzuständen für TFTs mit dünnem Gate-Dielektrikum anwendbar zu machen und damit den Einfluss der Oberflächenrauheit des Dielektrikums auf die Eigenschaften der TFTs besser zu verstehen. Die zentralen Aspekte im zweiten Teil der Arbeit sind die Optimierung bestehender Herstellungsprozesse des Gate-Dielektrikums und die Erforschung eines neuartigen hybriden Dielektrikums, um eine verbesserte Leistungsfähigkeit von organischen TFTs und Schaltungen zu erzielen.
Zunächst wird eine bestehende Methode zur quantitativen Bestimmung der Zustandsdichte von Fallenzuständen in TFTs weiterentwickelt, um erstmals TFTs mit niedrigen Betriebsspannungen analysieren zu können. Die Oberflächenrauheit des Gate-Dielektrikums wird isoliert variiert und dessen Einfluss auf die Eigenschaften des TFTs bestimmt. Die Ergebnisse zeigen, dass Korngrenzen in der Halbleiterschicht, die durch die Oberflächenrauheit des Gate-Dielektrikums verursacht werden, den Ladungstransport stark behindern, und betonen die Wichtigkeit einer glatten Oberfläche für die Herstellung organischer TFTs. Im nächsten Teil wird der Herstellungsprozess einer Aluminiumoxid-Schicht (AlO_x) mittels Plasmaoxidation untersucht. Die Plasmaleistung und die Dauer des Plasmaprozesses zeigen einen großen Einfluss auf die elektrischen und oberflächenbezogenen Eigenschaften von bloßen AlO_x-Schichten und hybriden AlO_x/SAM Dielektrika. Die Charakteristika von organischen TFTs, welche auf diesen Dielektrika basieren, werden analysiert und eine optimale Kombination von Plasmaleistung und -dauer identifiziert. Im letzten Teil dieser Arbeit wird ein neuartiges hybrides Gate-Dielektrikum entwickelt, in dem die Metalloxid-Komponente aus plasmagewachsenem Titanoxid (TiO_x) besteht. TFTs, in denen ein hybrides TiO_x/SAM Dielektrikum verwendet wird, zeigen hervorragende elektrische Eigenschaften und einige der Kenngrößen stellen Bestwerte für organische TFTs dar.

Abstract

Organic thin-film transistors (TFTs) are promising devices for future electronic applications. The possibility to deposit organic semiconductors at relatively low process temperatures makes it possible to fabricate organic TFTs on unconventional substrate materials, including highly flexible polymeric substrates. The use of these substrate materials enables the realization of novel electronic systems such as flexible active-matrix displays or biocompatible sensors. A key component of organic TFTs is the gate dielectric.
In this work, different aspects of a hybrid gate dielectric, consisting of a thin metal-oxide layer and a molecular self-assembled monolayer (SAM), for the use in organic TFTs are investigated. The focus here is on the role of the metal oxide layer. The objective of the first part of this work is to develop a theoretical method for quantifying trap states applicable to TFTs with a thin gate dielectric and thus to improve the understanding of the influence of the surface roughness of the gate dielectric on the performance of bottom-gate TFTs. The key aspects of the second part of the work are the optimization of existing fabrication processes of the gate dielectric and the exploration of a novel hybrid dielectric to achieve an improved performance of organic TFTs and circuits.
Initially, an established method for the quantitative analysis of the density of trap states in TFTs is extended in order to accurately apply the method to TFTs with low operating voltages for the first time. The degree of the surface roughness of the gate dielectric is varied in an isolated manner and its influence on the properties of organic bottom-gate TFTs is investigated. The results show that grain boundaries in the semiconductor layer, induced by the surface roughness of the gate dielectric, severely hinder charge transport and emphasize the importance of a smooth surface for the fabrication of organic TFTs. In the next part, the fabrication process of aluminum oxide (AlO_x) films by means of plasma oxidation is studied. The plasma power and the duration of the plasma exposure show a significant influence on the electrical and surface properties of bare-AlO_x and hybrid AlO_x/SAM dielectrics. The characteristics of TFTs based on these dielectrics are analyzed and an optimal combination of plasma power and plasma duration is identified. In the last part of this work, a novel hybrid gate dielectric is developed in which the metal-oxide component consists of a plasma-grown titanium oxide (TiO_x) film. Organic TFTs with a hybrid TiO_x/SAM dielectric show excellent electrical properties and some of the characteristics set performance records for organic TFTs.

Contents

Chapter 1

Introduction

Transistors are the most important active components of modern electronics. They are fundamental to virtually all electronic systems and omnipresent in our (increasingly digital) daily live. Since the first prototypes in the late 1940s an estimated volume of over 10 sextillion (10^{22}) transistors have been manufactured to date.[1–3] Persistent research and great technological and financial efforts brought transistors to a state, where nowadays, integration densities of over 100 million transistors per square millimeter are achieved.[4] This means that several billions of transistors are implemented in a conventional mobile phone. The vast majority of all transistors are metal-oxide-semiconductor field-effect transistors (MOSFETs) fabricated on the surface of single-crystalline silicon wafers, in which case the silicon serves as substrate and active semiconductor material. In terms of dynamic performance in combination with integration density, transistors based on single-crystalline silicon are unchallenged and superior for the implementation in microprocessors or solid-state memories.

When dynamic performance and integration density are not vital but large-area applications are desired, a different type of transistor is required, as the substrate size of single-crystalline silicon wafers is limited (currently the largest single-crystalline silicon wafers have a diameter of 300 mm). The thin-film transistor (TFT) is a field-effect transistor in which individual layers are sequentially deposited as thin films. Thus, the substrate material is not necessarily the same material as the semiconductor. The most common TFT is based on hydrogenated amorphous silicon (a-Si:H) which is deposited by plasma-enhanced chemical-vapor deposition (PECVD) onto glass substrates. These TFTs are largely employed in the active-matrix of liquid-crystal displays (AMLCD) or organic light-emitting diode displays (AMOLED). Typically the process temperatures for silicon-based TFTs exceed 200 °C and therefore the choice of substrate materials is very limited (usually glass). Future electronic devices such as rollable and bendable displays or conformable sensors require the utilization of flexible substrates. However, flexible plastic substrates do not withstand high process temperatures. One approach to circumvent this issue is the reduction of the process temperatures of silicon-based transistors. Another approach is the development of novel plastic substrates with an increased glass-transition temperature. As third approach the use of novel semiconductor materials, which can be processed at lower

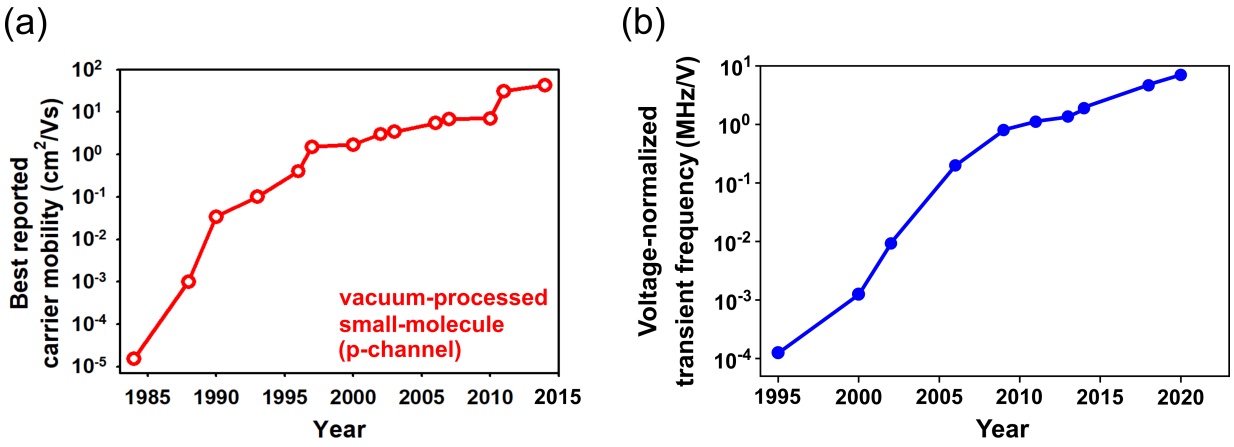


Figure 1.1: (a) Evolution of the charge-carrier mobility of organic small-molecule semiconductors deduced from field-effect transistor (FET) measurements. Adapted from references 5 and 6. (b) Literature overview of the highest voltage-normalized transit frequencies of organic TFTs over time. This value characterizes the dynamic performance of TFTs and is essential for most electronic applications. Adapted from reference 7.

temperatures, is possible. For the latter strategy organic semiconductors come into play. Organic semiconductors have been known since the late 1940s,[8] and can generally be divided into two classes: small molecules and polymers. Although both share many basic characteristics, there are some differences in terms of deposition methods, morphology, molecular structure and the associated charge transport properties. In this thesis, exclusively organic small molecules are employed and thus polymers will not be covered explicitly in the following.

The first significant benefit of organic semiconductors is the possibility to deposit them at temperatures close to room temperature. This makes it possible to use novel, in particular flexible, substrate materials. Flexible polymeric substrates but also exotic substrate materials such as paper or fabric are suited for organic electronics.[9–12] Typical deposition methods for organic semiconductors are deposition by thermal sublimation in vacuum and deposition from solution.

The second benefit of organic semiconductors is that organic chemistry makes it possible to synthesize a huge variety of organic semiconductors, for which the material properties can be purposefully manipulated. Thus, it is possible to develop semiconductors according to specific needs including organic molecules suited for either n- or p-type TFTs, molecules with increased solubility, enhanced intermolecular ordering or a tailored energy gap.[13–16]

Transistors based on organic semiconductors were first demonstrated in the 1980s and since then their performance steadily improved.[17,18] The evolution of two important performance metrics, i.e. the charge-carrier mobility of organic semiconductors and the transit frequency of organic TFTs, is shown in Figure 1.1. However, at the current state of the

art, organic TFTs have not reached a state which enables a commercialization of the technology and organic TFTs are still mainly subject to academic research. Much effort is put into the development of new organic molecules with improved properties. In particular, the enhancement of the charge-carrier mobility and the long-term stability have been (and are) subject to intense research.[19,20] State-of-the-art organic small-molecule semiconductors such as dinaphtho-[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) and its derivatives have charge-carrier mobilities well above $1\,\mathrm{cm}^2/\mathrm{Vs}$ and an excellent air stability.[21–24] However, besides the choice of the organic semiconductor material, a key factor for a well-functioning organic TFT is the gate dielectric of the transistor. The gate dielectric is vital for many essential characteristics of the TFTs including the power consumption, the threshold voltage, the subthreshold swing and the bias-stress stability.[25–27] In addition, for the inverted (bottom-gate) device architecture of TFTs, the surface properties of the gate dielectric have pronounced influence on the growth and quality of the semiconductor film. In the presented thesis, the approach of an ultrathin hybrid gate dielectric consisting of a metal oxide combined with a molecular self-assembled monolayer (SAM) is a recurrent and central topic. The implications of such a hybrid gate dielectric on the quantitative analysis of trap states in organic TFTs are analyzed and the impact of the properties of the hybrid gate dielectric on the performance of organic TFTs is investigated. In addition, established hybrid $\mathrm{AlO_x}$/SAM dielectrics are optimized and novel hybrid $\mathrm{TiO_x}$/SAM dielectrics are developed and demonstrated in order to further improve the performance of organic TFTs.

The presented thesis is a cumulative dissertation with the following structure: Chapter 2 covers the required fundamentals. The results of this thesis led to four publications which are presented in Chapter 3 to 6. Each publication is preceded by a brief summary of the state of the art, the objective and the central conclusions. The thesis concludes with a summary and an outlook in Chapter 7.

Chapter 2

Fundamentals

This chapter starts with some classical semiconductor physics. The presented concepts and terminology (e.g. electronic bands, density of states function, molecular-orbital overlap etc.) are required for further discussions in the Chapter 3 to 6. The broad introduction of general concepts in semiconductor physics is progressively reduced to concepts for organic semiconductors and organic transistors (i.e. field-effect transistors operating in the accumulation regime, based on intrinsic semiconductors). The last part of this chapter deals with organic small-molecule semiconductors. Their chemical and structural properties are introduced and consequences for the charge transport in organic semiconductors are covered. Comprehensive explanations and derivations can be found in the text books by S.M. Sze and K.K. Ng,[28] S. Hunklinger[29] and P. Stallinga,[30] as well as in the lecture courses by H. Klauk,[31] and J. Weis.[32]

2.1 Electronic States in Crystalline Semiconductors

2.1.1 Bloch Theory and the Formation of Electronic Bands

Ideal crystalline semiconductors consist of a periodic lattice of atoms. This crystal lattice causes a periodic electrostatic potential for electrons:

$$V(\vec{r}) = V(\vec{r} + \vec{R}), \tag{2.1}$$

with $\vec{r}$ the position vector and $\vec{R}$ the crystal lattice periodicity. Quantum mechanically, this situation for an electron can be approached by the Bloch theory, i.e. by solving the time-independent Schrödinger equation for a single electron in a periodic potential:[33]

$$\left[-\frac{\hbar^2}{2m}\vec{\nabla}_{\vec{r}}^2 + V(\vec{r})\right] \Psi_{\vec{k},N}(\vec{r}) = E_{\vec{k},N}\Psi_{\vec{k},N}(\vec{r}), \tag{2.2}$$

with $\hbar$ the Planck constant h divided by 2π, m the mass of the electron and ∇ the Nabla operator. The explicit mathematical formalism for solving this equation depends on the used ansatz (e.g. tight-binding method, Fourier series method, $\mathrm{k} \cdot \mathrm{p}$ perturbation method,

etc.). The resulting electron wave functions $\Psi_{\vec{k},N}$ and electron energies $E_{\vec{k},N}$ are characterized by the quantum numbers $\vec{k}$ and N, denoted as wave vector and band index. For each point in $\vec{k}$-space, an infinite number of electron waves $\Psi_{\vec{k},N}$ and corresponding energies $E_{\vec{k},N}$ with $N = 1, 2, 3...$ exist, see Figure 2.1. The spatial probability density of such a Bloch electron is delocalized: It can vary within the elementary cell of the crystal, but has a translation symmetry of

$$\Psi_{\vec{k},N}(\vec{r}) = \Psi_{\vec{k},N}(\vec{r} + \vec{R}) \tag{2.3}$$

and is therefore spread over the entire crystal. For the electrical properties of the material, a crucial quantity is the relation between the electron energy $E_{\vec{k},N}$ and the wave vector $\vec{k}$. For a fixed band (i.e., a fixed number for N), the function $E_N(\vec{k})$ defines the dispersion relation for electrons in that band. The graphical trace of this relation yields the band structure of the material, shown in Figure 2.1(a). The exact shape of the band structure can be complex and for a complete representation of the band structure a four-dimensional space is required ($E_N(k_\mathrm{x}, k_\mathrm{y}, k_\mathrm{z})$). Thus, the projection of the band structure on the energy-axis is often used, which is called band model and requires only two dimensions (see Figure 2.1(b)). An energetic range not covered by any bands is called band gap ΔE. Many properties of a semiconducting material are determined by electronic states near the minimum and the maximum of bands next to the band gap. These band extrema can be approximated locally by a parabolic energy dispersion:[34]

$$E(\vec{k}) = \frac{\hbar^2 \vec{k}^2}{2m^*}. \tag{2.4}$$

In that case, electrons near the band minimum or maximum are treated as free electrons with an effective mass m^*. For the electrical properties of the material, not only the available energies of the electronic states are important, but also their density. This is captured by the density-of-states function, which represents the number of electronic states per unit volume and unit energy. For a quasi-free electron gas, with a parabolic energy dispersion, the density-of-states function $D(E)$ is proportional to the square-root of the electron energy:

$$D(E) \propto {m^*}^{\frac{3}{2}} \sqrt{E}. \tag{2.5}$$

2.1.2 Intrinsic Semiconductors

In an ideal crystalline semiconductor, there are no electronic states in the band gap as discussed in the section above. Consequently, for each electron which is excited into the conduction band (CB), a hole is created in the valence band (VB). Therefore, the concentration of electrons n and the one of holes p are equal for all temperatures T:

$$n(T) = p(T). \tag{2.6}$$

The condition given in Equation 2.6 characterizes an intrinsic semiconductor. The chemical potential μ^{ch} is located exactly in the middle of the band gap for $T = 0\,\mathrm{K}$ and slightly shifts

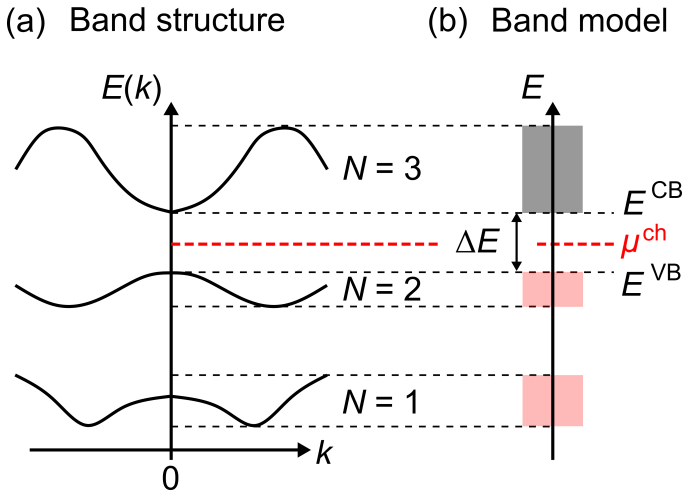


Figure 2.1: (a) Schematic of a band structure of a semiconductor. For each band index N, the electron energy $E_N(k)$ is traced in k-space. Next to minima and maxima of the band structure, the dispersion relation can typically be approximated by parabolas. (b) The projection of the band structure on the energy-axis yields the band model. A band gap ΔE is an energetic range without any electronic states available. The band just below the band gap is called valence band (VB), the band above the band gap is called conduction band (CB).

if the effective masses of the charge carriers in the conduction band m_n^* and the valence band m_p^* differ:[35]

$$\mu^\mathrm{ch}(T) = \frac{E^\mathrm{CB} + E^\mathrm{VB}}{2} + \frac{3}{4} k_\mathrm{B} T \ln\left(\frac{m_\mathrm{p}^*}{m_\mathrm{n}^*}\right), \tag{2.7}$$

with k_B the Boltzmann constant. The probability of an electronic state being occupied is given by the Fermi-Dirac distribution function:

$$f_\mathrm{FD}(E, \mu^\mathrm{ch}, T) = \frac{1}{\exp\left[\frac{E-\mu^\mathrm{ch}(T)}{k_\mathrm{B}T}\right] + 1}. \tag{2.8}$$

To determine the electron density n (hole density p) of an intrinsic semiconductor the product of the density of available states at a certain energy $D_\mathrm{n}(E)$ ($D_\mathrm{p}(E)$) and of the occupation probability of the states at this energy $f_\mathrm{FD}(E)$ ($[1 - f_\mathrm{FD}(E)]$) is integrated over all energies:

$$n = \int_{-\infty}^{\infty} D_\mathrm{n}(E') f_\mathrm{FD}(E') \mathrm{d}E', \tag{2.9}$$

$$p = \int_{-\infty}^{\infty} D_\mathrm{p}(E') [1 - f_\mathrm{FD}(E')] \mathrm{d}E'. \tag{2.10}$$

In Figure 2.2 this calculation is illustrated graphically.

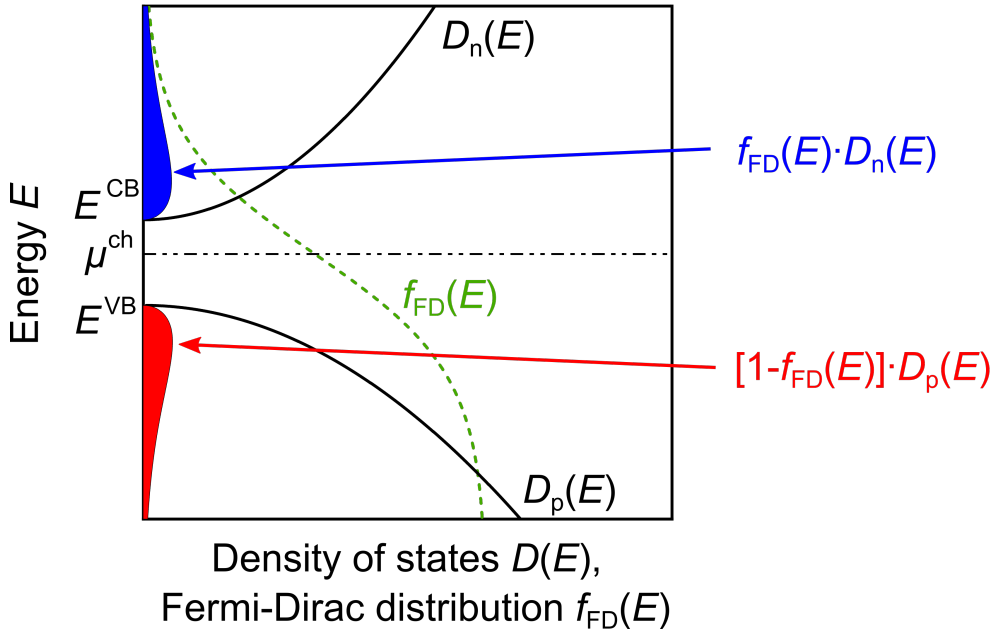


Figure 2.2: Density-of-states functions for electrons D_n and holes D_p and the Fermi-Dirac distribution function f_{FD} for $T > 0\,K$. The density of electrons which are excited into the conduction band is represented as blue area, the density of holes in the valence band is represented as red area. Due to charge neutrality both areas have to be equal and the chemical potential μ^{ch} adjusts accordingly. Adapted from reference 29.

2.1.3 Extrinsic Semiconductors

The small concentration of free charge carriers in intrinsic semiconductors at room temperature can be increased by doping, i.e., by intentionally substituting a small amount of atoms of the host lattice by atoms with a different number of valence electrons. If the energy levels of these foreign doping atoms are close enough to the conduction band or valence band of the host semiconductor, they can be ionized at room temperature and provide additional free charge carriers. The foreign atoms are classified as either donors if they deliver an electron to the conduction band, or acceptor if they accept an electron from the valence band and thus create a hole as free charge carrier (see Figure 2.3).
In general, the free charge-carrier concentration in such an extrinsic semiconductor is

$$n(T) \neq p(T), \tag{2.11}$$

since one type of doping agent usually prevails. A semiconductor which is doped with donors is called n-type semiconductor, a semiconductor which is doped with acceptors is called p-type semiconductor. Already a small doping concentration, e.g., one dopant within 10^9 host atoms, leads to free charge carriers that largely exceed the number of intrinsic free charge carriers. Doping is essential for a wide range of electrical behavior

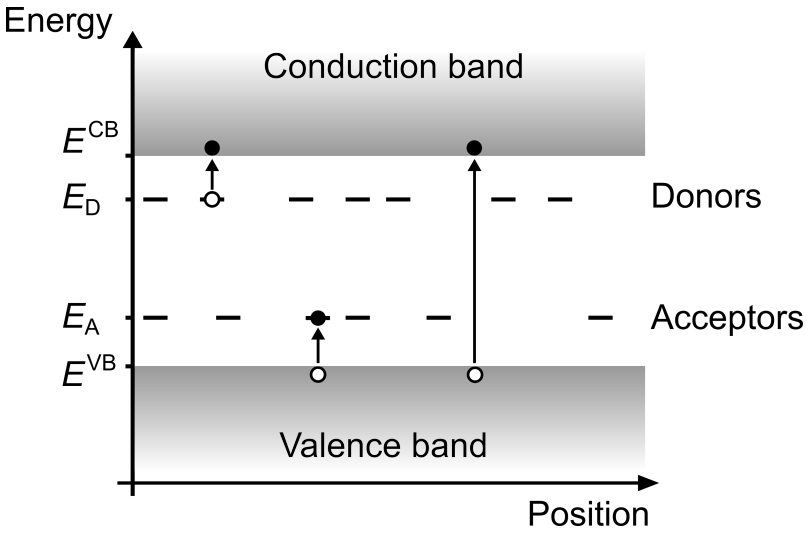


Figure 2.3: Band diagram of an extrinsic semiconductor. Discrete energy levels of donors, just below the conduction band, and acceptors, just above the valence band, can be ionized at room temperature and provide additional free charges.

that semiconductors can exhibit and is key for the technology of many semiconductor devices. Even though extrinsic semiconductors have a broad temperature dependence, only intermediate temperatures will be considered in the following. For these intermediate temperatures all dopants are completely ionized. In an electrically isolated semiconductor, the charge balance is conserved. Therefore, the electron concentration in the conduction band $n(T)$ plus the concentration of acceptors n_A, all having captured an electron, is equal to the hole concentration in the valence band $p(T)$ plus the concentration of donors n_D, all having lost an electron:

$$n(T) + n_\mathrm{A} = p(T) + n_\mathrm{D}. \tag{2.12}$$

Since for intermediate temperatures, the chemical potential is far away from the conduction band and valence band, the Fermi-Dirac distribution function (Equation 2.8) can be approximated by an exponential function (Boltzmann distribution function) and the charge-carrier concentration given in Equation 2.9 and 2.10 transforms each to:

$$n = \widetilde{n}_0 \exp\left[-\frac{E^\mathrm{CB} - \mu^\mathrm{ch}}{k_\mathrm{B}T}\right], \tag{2.13}$$

$$p = \widetilde{p}_0 \exp\left[-\frac{\mu^\mathrm{ch} - E^\mathrm{VB}}{k_\mathrm{B}T}\right], \tag{2.14}$$

and depends exponentially on the separation of the chemical potential and the conduction band (valence band).
In field-effect transistors, this separation and thus the concentration of charge carriers can be modified by applying an external electrostatic potential, and this will be covered in the next section.

2.2 Surface-Charge Concentration

For the derivation of the modulation of the surface-charge concentration in a semiconductor by the presence of an electric field, the consideration of a sandwich structure consisting of a metal, an insulator and a semiconductor is sufficient. In the following, the accumulation and depletion of charge carriers at the surface of a semiconductor (i.e., the surface of the semiconductor at the insulator/semiconductor interface) will be derived. Since only a surface is considered, all problems can be reduced to one spatial dimension.
In equilibrium, the electrochemical potential μ^{elch}, consisting of the internal non-electrical chemical potential μ^{ch} and of the internal electrostatic potential ϕ, is constant:

$$\mu^{\mathrm{elch}} = \mu^{\mathrm{ch}} - e\phi = \mathrm{const.} \tag{2.15}$$

Applying a bias to the metal electrode causes a shift of the electrochemical potential in the semiconductor with respect to the electrochemical potential in the metal electrode. This leads to a change in the electrostatic potential $\phi(x)$ which drops linearly over the insulator and reaches into the semiconductor, thus leading to bending of the bands relative to the electrochemical potential. Far away from the insulator/semiconductor interface the electrostatic potential vanishes, $\phi(x \to \infty) = 0$, which means that Equation 2.13 and Equation 2.14 for the free charge-carrier concentrations are still valid and no additional charge carriers are induced there by the electrostatic potential. In the vicinity of the insulator/semiconductor interface, the hole concentration and electron concentration are given by the separation of the band edges and the electrochemical potential and therefore by the electrostatic potential:

$$n(x) \approx \widetilde{n}_0 \cdot \exp\left[-\frac{E^{\mathrm{CB}}(x) - \mu^{\mathrm{elch}}}{k_{\mathrm{B}}T}\right] \tag{2.16}$$

$$= n_0 \cdot \exp\left[+e\frac{\phi(x)}{k_{\mathrm{B}}T}\right], \tag{2.17}$$

$$p(x) \approx \widetilde{p}_0 \cdot \exp\left[-\frac{\mu^{\mathrm{elch}} - E^{\mathrm{VB}}(x)}{k_{\mathrm{B}}T}\right] \tag{2.18}$$

$$= p_0 \cdot \exp\left[-e\frac{\phi(x)}{k_{\mathrm{B}}T}\right]. \tag{2.19}$$

The local electrostatic potential $\phi(x)$ is connected to the local net charge concentration $\rho(x)$ by the Possion equation:

$$\frac{\partial^2\phi(x)}{\partial x^2} = -\frac{\rho(x)}{\varepsilon\varepsilon_0}, \tag{2.20}$$

with ε the permittivity of the semiconductor and ε_0 the permittivity of vacuum. The net charge concentration is:

$$\rho(x) = e\left[p(x) + n_{\mathrm{D}}(x) - n(x) - n_{\mathrm{A}}(x)\right]. \tag{2.21}$$

With $n_{\mathrm{D}}(x) \approx n_0$ and $n_{\mathrm{A}}(x) \approx p_0$ and inserting Equation 2.17 and Equation 2.19 the Poission equation reads as:

$$\frac{\partial^2\phi(x)}{\partial x^2} = -\frac{e}{\varepsilon\varepsilon_0}\left(p_0 \cdot \left(\exp\left[\frac{-e\phi(x)}{k_{\mathrm{B}}T}\right] - 1\right) - n_0 \cdot \left(\exp\left[\frac{e\phi(x)}{k_{\mathrm{B}}T}\right] - 1\right)\right). \tag{2.22}$$

Integrating the left side of the equation over the potential from the bulk of the semiconductor (where $\phi(x \to \infty) = 0$) to its surface (where $\phi(x = 0) = \phi_{\mathrm{S}}$) leads to:

$$\int_0^{\phi_{\mathrm{S}}} \frac{\partial^2\phi(x)}{\partial x^2}\,\mathrm{d}\phi = \int_0^{S} \frac{\partial|\vec{E}(x)|}{\partial x}|\vec{E}(x)|\,\mathrm{d}x = \int_0^{E_{\mathrm{S}}} |\vec{E}|\,\mathrm{d}|\vec{E}| = \frac{1}{2}E_{\mathrm{S}}^2. \tag{2.23}$$

Integrating the right side yields:

$$-\frac{e}{\varepsilon\varepsilon_0}\int_0^{\phi_{\mathrm{S}}}\left(p_0 \cdot \left(\exp\left[\frac{-e\phi(x)}{k_{\mathrm{B}}T}\right] - 1\right) - n_0 \cdot \left(\exp\left[\frac{e\phi(x)}{k_{\mathrm{B}}T}\right] - 1\right)\right)\mathrm{d}\phi \tag{2.24}$$

$$= -\frac{e}{\varepsilon\varepsilon_0}\frac{k_{\mathrm{B}}T}{-e}\left(p_0 \cdot \left(\exp\left[\frac{-e\phi_{\mathrm{S}}}{k_{\mathrm{B}}T}\right] + \frac{e\phi_{\mathrm{S}}}{k_{\mathrm{B}}T} - 1\right) - n_0 \cdot \left(\exp\left[\frac{e\phi_{\mathrm{S}}}{k_{\mathrm{B}}T}\right] + \frac{e\phi_{\mathrm{S}}}{k_{\mathrm{B}}T} - 1\right)\right). \tag{2.25}$$

Using Gauss's law the electric field at the surface E_{S} can be connected to the surface-charge concentration Q_{S}:

$$Q_{\mathrm{S}} = \varepsilon\varepsilon_0 E_{\mathrm{S}}, \tag{2.26}$$

and finally an expression for the surface-charge concentration in dependence of the surface potential is obtained:

$$Q_{\mathrm{S}} = \sqrt{2k_{\mathrm{B}}T\varepsilon\varepsilon_0}\sqrt{p_0 \cdot \left(\exp\left[\frac{-e\phi_{\mathrm{S}}}{k_{\mathrm{B}}T}\right] + \frac{e\phi_{\mathrm{S}}}{k_{\mathrm{B}}T} - 1\right) - n_0 \cdot \left(\exp\left[\frac{e\phi_{\mathrm{S}}}{k_{\mathrm{B}}T}\right] + \frac{e\phi_{\mathrm{S}}}{k_{\mathrm{B}}T} - 1\right)}. \tag{2.27}$$

A graphical illustration of this relation is shown in Figure 2.4 with the characteristic regimes of operation for a p-type FET. By varying the surface potential the charge-carrier concentration at the surface of the semiconductor can be increased by several orders of magnitude. Since transistors based on intrinsic organic semiconductors (which are employed in this work) are operated in the accumulation regime, only this regime will be discussed in more detail. In this regime, majority charge carriers are accumulated and exceed by far the number of minority charge carriers (if any). For intrinsic semiconductors the distinction between majority and minority charge carriers is obsolete and only one type of charge carrier is present. In either case, Equation 2.27 can be simplified by neglecting one type of charge carriers and the dominant contribution of ϕ_{S} to Q_{S} is the exponential term. Therefore, in the accumulation regime, the dependency of the surface-charge concentration on the surface potential is given by:

$$Q_{\mathrm{S}} \propto \exp\left[\frac{|e\phi_{\mathrm{S}}|}{2k_{\mathrm{B}}T}\right]. \tag{2.28}$$

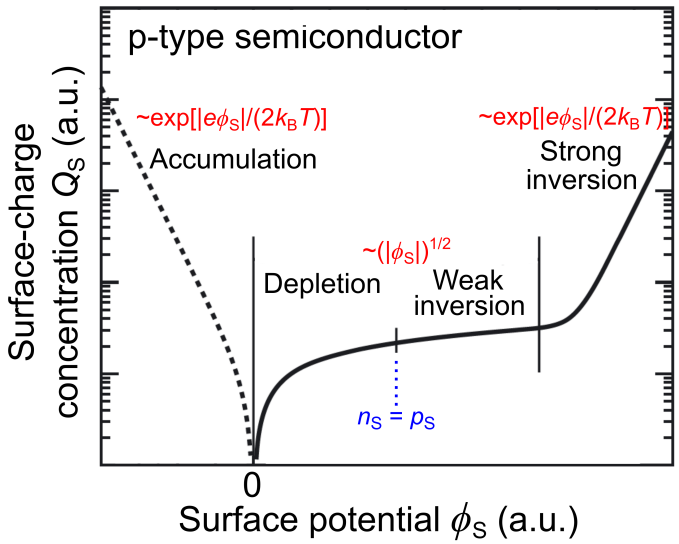


Figure 2.4: Surface-charge concentration of a p-type semiconductor plotted as a function of the surface potential. For the different regimes of operation, the dominant term contributing to the surface charge is given. For the accumulation regime, the surface charge has an exponential dependence on the surface potential and can be varied by orders of magnitude. Adapted from reference 36.

It is evident that applying a bias to the metal electrode will modify the surface potential ϕ_S. However, the exact relation between the applied voltage and the surface potential is not trivial and depends on several geometric and materials specific parameters. Furthermore, the $\phi_S(V_{bias})$-relation is in general non-linear which has severe effects on the current-voltage characteristics of FETs (as will be discussed in Section 2.3). A detailed analysis of the surface potential ϕ_S and the calculation of ϕ_S as a function of the applied bias will be presented in Chapter 3.

2.3 Basic FET Equations

So far, a capacitor structure was discussed in which case charge carriers are accumulated at the interface between the insulator and the semiconductor. In a field-effect transistor (FET), there are two additional electrodes in parallel to the insulator/semiconductor interface. Applying a voltage between these two electrodes creates an electric field in which the accumulated charge carriers can move and a current can flow from one electrode to the other one. Figure 2.5 shows a schematic cross-section of an FET. The surface-charge concentration in a metal-insulator-semiconductor device (Equation 2.27) can be used for an FET device in a slightly modified form. The applied drain-source voltage V_{DS} creates a potential $\phi_{DS}(y)$ in parallel to the insulator/semiconductor interface which counteracts the potential of the gate electrode $\phi(x)$. Thus, an effective electrostatic potential $\psi(x, y) = \phi(x) - \phi_{DS}(y)$

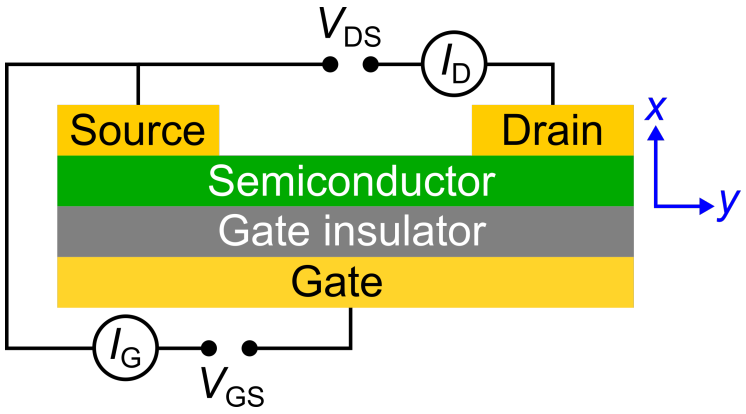


Figure 2.5: Schematic cross-section of a field-effect transistor. Please note the convention used in this chapter: The x-direction is perpendicular and the y-direction is parallel to the insulator/semiconductor interface.

is introduced. This affects the hole and electron concentrations in the vicinity of the insulator/semiconductor interface and $\phi(x)$ has to be substituted by $\psi(x, y)$ in Equation 2.17 and 2.19. Thus, the surface-charge concentration is no longer constant along the channel of the FET, but varies with the position along the y-coordinate:

$$Q_S(y) \propto \exp\left[\frac{e(\phi_S - \phi_{DS}(y))}{2k_B T}\right] - \exp\left[\frac{e\phi_{DS}(y)}{k_B T}\right] \text{(for accumulation)}. \tag{2.29}$$

In general, there are two mechanisms that cause movement and thus a current of the accumulated charge carriers. One type of current is the diffusion current which is a movement of the charge carriers caused by a gradient in the charge concentration $\frac{dQ_S}{dx}$ and can be described by Fick's law:[37]

$$I \propto D\frac{dQ_S}{dx}, \tag{2.30}$$

with D the diffusion coefficient.
The other type of current is the drift current which is a movement of the charge carriers caused by the presence of an electric field E and can be described by Ohm's law:

$$I \propto Q_S \mu E, \tag{2.31}$$

with μ the charge-carrier mobility.
For small values of V_{GS} (called the subthreshold regime) the induced charge concentration is small and drift currents are insignificant as they depend linearly on the absolute value of the charge concentration (see Equation 2.31). According to Equation 2.29 the accumulated charge concentration depends exponentially on ϕ_S. Since ϕ_S is partly compensated by ϕ_{DS} at the drain electrode, but not at the source electrode, there is a significant gradient of the charge-carrier concentration along the channel. Therefore, the drain current in the subthreshold regime is dominated by diffusion currents. An important quantity to

characterize a field-effect transistor in the subthreshold regime is the subthreshold swing S, which is defined as:[28]

$$S := \frac{\partial V_{\mathrm{GS}}}{\partial \log_{10}(I_{\mathrm{D}})}, \tag{2.32}$$

and states the change in the gate-source voltage required to change the drain current I_{D} by one decade.
For large values of V_{GS} a significant charge concentration is accumulated and the drain current is dominated by drift currents. According to Ohm's law the drain current can be calculated by inserting the appropriate term for Q_{S}:

$$I_{\mathrm{D}} = \frac{W}{L}\mu \int_0^{V_{\mathrm{DS}}} Q_{\mathrm{S}}\, \mathrm{d}\phi_{\mathrm{DS}}. \tag{2.33}$$

This equation can in general not be solved analytically. In addition, this equation only yields the drain current as a function of the surface potential $I_{\mathrm{D}}(\phi_{\mathrm{S}})$. To obtain the relation between the drain current and the gate-source voltage, the relation $V_{\mathrm{GS}}(\phi_{\mathrm{S}})$ has to be known which is also in general not easily deducible.

2.3.1 Charge-Sheet Model

Typically for the analysis of charge transport in FETs a much more simplified model is used in order to obtain an analytical expression for the drain current. For large values of the gate-source voltage V_{GS} it is assumed that all accumulated charges reside within a layer with a thickness of zero at the interface of the gate insulator and the semiconductor. Thus, the system is treated as a plate capacitor with one electrode being the gate electrode and the other electrode being the accumulated charge sheet.[38] The accumulated charge concentration is calculated with the simple equation for a plate capacitor:

$$Q(y) = C_{\mathrm{diel}}(V_{\mathrm{GS}} - V_{\mathrm{th}} - \phi_{\mathrm{DS}}(y)), \tag{2.34}$$

with C_{diel} the unit-area capacitance of the dielectric, V_{th} the threshold voltage, which accounts for a work function difference of the semiconductor and the gate and any charged states that do not contribute to the current, and with ϕ_{DS} the potential along the channel caused by the potential difference between the source and drain electrode. Applying a voltage between the drain and source electrode creates an electric field giving rise to a drift current which can be calculated using Equation 2.33:

$$I_{\mathrm{D}} = \frac{W}{L}\mu\, C_{\mathrm{diel}} \int_0^{V_{\mathrm{DS}}} (V_{\mathrm{GS}} - V_{\mathrm{th}} - \phi_{\mathrm{DS}})\, \mathrm{d}\phi_{\mathrm{DS}} \tag{2.35}$$

$$= \frac{W}{L}\mu\, C_{\mathrm{diel}} \left[(V_{\mathrm{GS}} - V_{\mathrm{th}})V_{\mathrm{DS}} - \frac{V_{\mathrm{DS}}^2}{2} \right]. \tag{2.36}$$

For small values of V_{DS} ($|V_{\mathrm{DS}}| \ll |V_{\mathrm{GS}} - V_{\mathrm{th}}|$) the last term in Equation 2.36 can be neglected. Thus, the channel acts as an ohmic resistor and the drain current depends linearly on the applied drain-source voltage. When the drain-source voltage increases, the potential of the

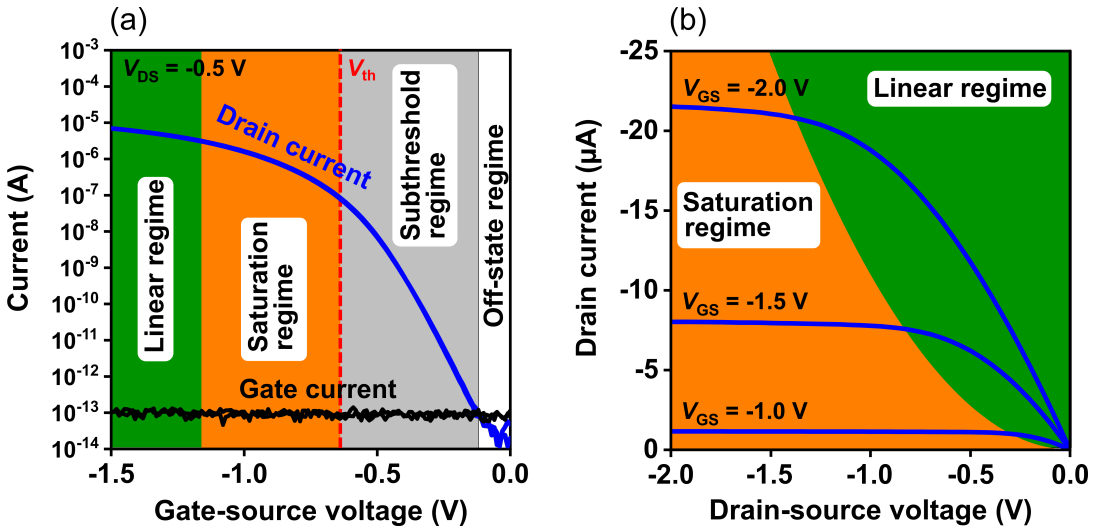


Figure 2.6: (a) Transfer characteristic and (b) output characteristic of a p-channel organic TFT. The different regimes of operation are highlighted.

gate electrode ϕ_S is increasingly compensated by the potential of the drain electrode ϕ_D. For $V_{DS} = (V_{GS} - V_{th})$ no potential is present in the channel region at the drain electrode and there is almost no accumulated charge $Q \approx 0$, which is called pinch-off point. An increase of V_{DS} shifts the pinch-off point closer to the source electrode but does not lead to an increase in the drain current. Thus, this regime of operation is called saturation regime. By substituting $V_{DS} = (V_{GS} - V_{th})$ in Equation 2.36, an equation for the drain current for large values of V_{DS} ($|V_{DS}| \gg |V_{GS} - V_{th}|$) is obtained:

$$I_D = \frac{W}{2L} \mu C_{diel} (V_{GS} - V_{th})^2. \tag{2.37}$$

Based on the equations of the drain current, a definition of the field-effect mobility and the transconductance ($g_m := \partial I_D / \partial V_{GS}$) via the derivative of the transfer curves is possible.

For $|V_{DS}| \ll |V_{GS} - V_{th}|$ (linear regime):

$$I_{D,lin} = \frac{W}{L} \mu C_{diel} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right), \tag{2.38}$$

$$\mu_{lin} = \frac{L}{W C_{diel} V_{DS}} \frac{\partial I_D}{\partial V_{GS}}, \tag{2.39}$$

$$g_{m,lin} = \frac{W}{L} \mu C_{diel} V_{DS}. \tag{2.40}$$

For $|V_{DS}| \gg |V_{GS} - V_{th}|$ (saturation regime):

$$I_{D,sat} = \frac{W}{2L} \mu C_{diel} (V_{GS} - V_{th})^2, \tag{2.41}$$

$$\mu_{sat} = \frac{2L}{W C_{diel}} \left(\frac{\partial \sqrt{I_D}}{\partial V_{GS}} \right)^2, \tag{2.42}$$

$$g_{m,sat} = \frac{W}{L} \mu C_{diel} (V_{GS} - V_{th}). \tag{2.43}$$

Transfer and output characteristics of a field-effect transistor with the different regimes of operation are exemplary shown in Figure 2.6.

2.4 Organic Semiconductors

2.4.1 Electron Configuration and Conjugation

The main ingredient of organic materials is the carbon atom. The main ingredients of organic semiconductor materials are conjugation and the opening of an energy gap.[30] The electronic properties of an organic material are determined by the structural arrangement of the molecules in the solid and the arrangement of the atoms within the molecules. A single, free carbon atom in its ground state has the electron configuration of $1s^2 2s^2 2p^2$. When forming a molecule its electronic structure (i.e., the spatial and energetic properties of the electrons) can be described by the formation of molecular orbitals from the combination of atomic orbitals. This concept is called orbital hybridization. In the case of carbon, two of its six electrons occupy the inner $1s$ orbital and do not participate in the hybridization. Solely the four electrons in the outer $2s$ and $2p$ orbitals play a role for the hybridization. For carbon there are three different types of orbital hybridization (sp hybridization, sp^2 hybridization and sp^3 hybridization) depending on which of the atomic orbitals ($2s$, $2p_x$, $2p_y$, $2p_z$) participate in the hybridization.
For organic semiconductors the sp^2 configuration is the most relevant one. In this case, the $2s$ orbital hybridizes with the $2p_x$ and $2p_y$ orbitals and forms three degenerated hybrid orbitals (sp^2 orbitals) as shown in Figure 2.7(a). These three sp^2 orbitals are arranged spatially within one plane. The not hybridized p_z orbital aligns perpendicularly to this plane. A prominent example in which the carbon exhibits the sp^2 hybridization is the benzene molecule (see Figure 2.7(b)). Overlapping sp^2 orbitals of adjacent carbon atoms as well as overlapping sp^2 orbitals of carbon atoms and $1s$ orbitals of hydrogen atoms form molecular σ orbitals which are localized within the molecular plane. The p_z orbitals of the individual carbon atoms, sticking out of the molecular plane, also hybridize and form a molecular π orbital which is delocalized over the entire molecule, i.e., the spatial distribution of the electrons in the π orbitals is not assigned to one atom but to the whole molecule. Molecules possessing such π orbitals are called conjugated systems. The number of orbitals is conserved when forming molecular orbitals from atomic orbitals. Half of the molecular orbitals have a higher energy than the atomic orbitals (anti-binding orbitals),

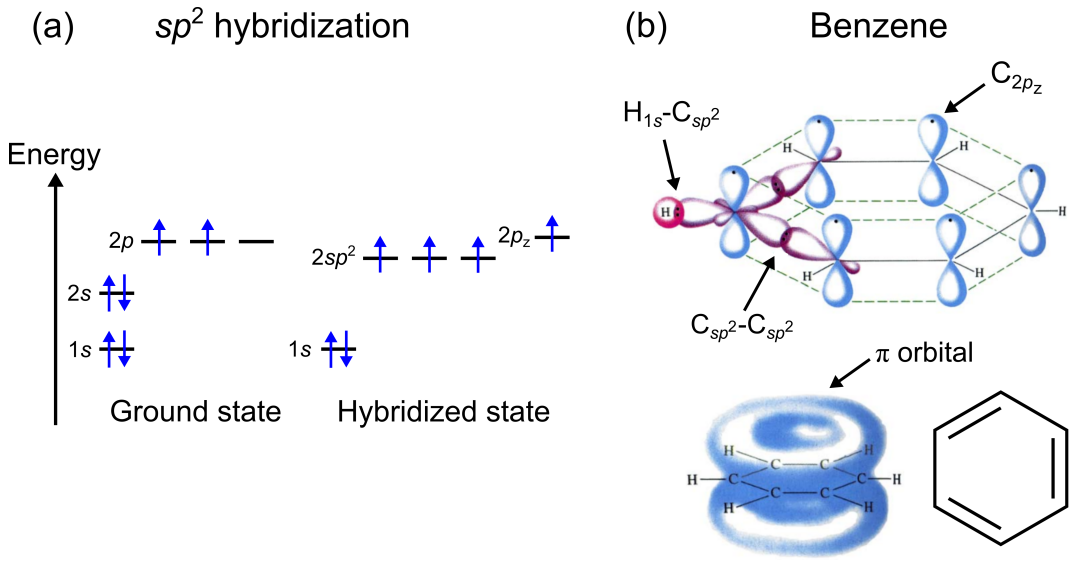


Figure 2.7: (a) Energetic structure of a carbon atom in its ground state and in the sp^2 hybridization. The $2s$ orbital and two $2p$ orbitals hybridize and form three degenerated $2sp^2$ orbitals. (b) Atomic orbitals of the individual atoms in a benzene molecule. The $2p_z$ atom orbitals of the six carbon atoms hybridize and form a delocalized π orbital. Adapted from reference 39.

the other half has a lower energy than the atomic orbitals (binding orbitals). For the optical and electrical properties of the material the spatial distribution and the energy of the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) are the most relevant. The energy of the LUMO corresponds to the electron affinity, the energy of the HOMO corresponds to the ionization energy and the energetic distance between LUMO and HOMO can be seen as equivalent to the band gap in inorganic semiconductors. For benzene this energy gap has a value of approximately 6.8 eV which qualifies it as an insulator. With an increasing number of carbon atoms contributing to the π orbital, the energy gap is reduced. For example, a pentacene molecule consists of five linearly fused benzene rings (see Figure 2.8(a)) and has an energy gap of around 2.1 eV which makes the material a semiconductor. Benzene rings are a major building block of organic semiconductors.

2.4.2 Organic Small-Molecule Semiconductors

Due to the almost infinite possibilities of organic chemistry to modify molecules by attaching side groups or substituting certain atoms in a molecule, it is possible to tune the electronic and material properties of organic semiconductors. In general, organic semiconductors can be divided into two groups: Small-molecule materials and polymers. Basic

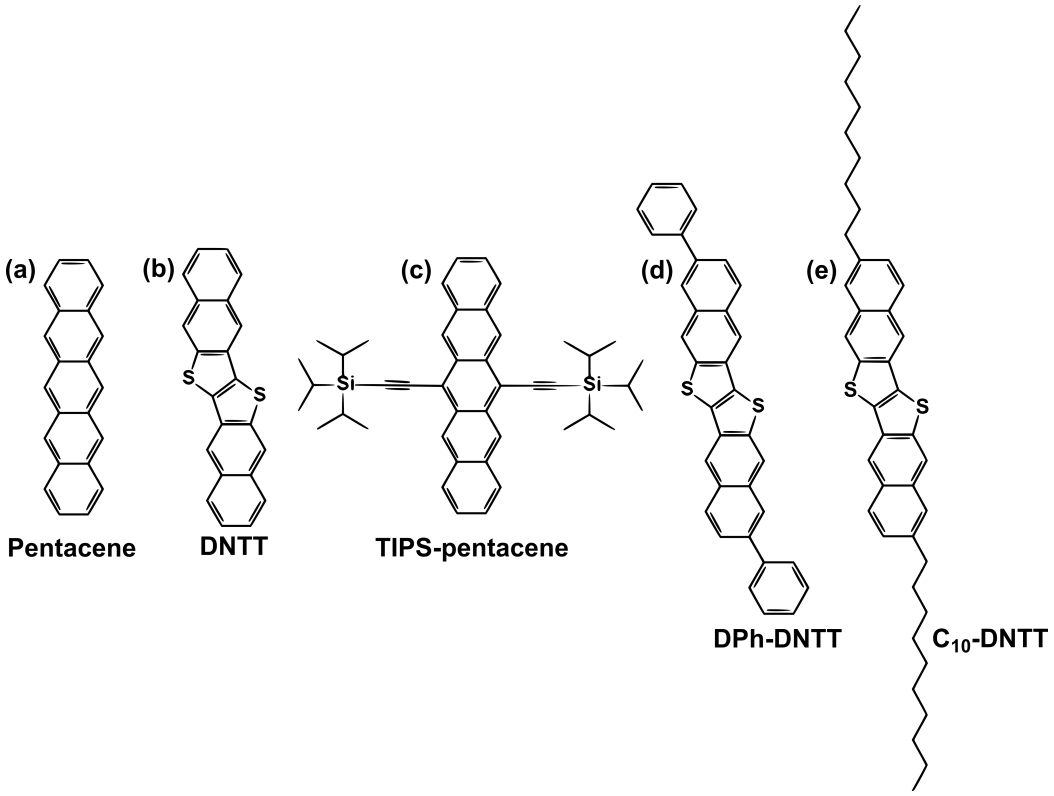


Figure 2.8: Exemplary small-molecule semiconductors in which specific modifications of the original pentacene molecule lead to beneficial material properties: (a) Pentacene, (b) dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene with increased air stability, (c) tri-isopropylsilyl-ethynyl-pentacene which is soluble, (d) diphenyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene with enhanced charge-carrier mobility and (e) didecyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene with enhanced charge-carrier mobility.

concepts described here apply to both. However, in this work exclusively small-molecule materials are employed and therefore special features of polymers will not be discussed. In the following, a few prominent examples of organic small-molecule semiconductors will be given in which the molecules were specifically modified in order to exhibit advantageous properties compared to the unmodified molecule. The molecule dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT; Figure 2.8(b)) is a pentacene analogue in which the inner of the five benzene rings is replaced by two fused thiophene rings.[21] The conjugated character of the molecule is preserved, but the HOMO energy is lowered. Therefore, the molecule is less prone to oxidation and the air stability is significantly enhanced compared to pentacene. Attaching tri-isopropylsilyl-ethynyl (TIPS) groups to the conjugated core of pentacene enhances the solubility of the molecule, thus making processing from solution possible (Figure 2.8(c)).[40] Side groups can also influence the degree of orbital overlap

of adjacent molecules within the solid and therefore affect the efficiency of charge transport from one molecule to another. One example is the functionalization of a DNTT core molecule with phenyl side groups (diphenyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene; DPh-DNTT; Figure 2.8(d)) or alkyl side groups (didecyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene; C_{10}-DNTT; Figure 2.8(e)) to enhance the charge-carrier mobility.[24,41]

2.4.3 Charge-Transport Mechanism

The development of universal charge-transport models for organic semiconductors is challenging and there is no consistent model which fully covers all experimental observations in organic semiconductor materials.[42] In molecular crystals of organic semiconductors, the intra-molecular charge transport is based on the delocalized π orbitals of the HOMO and LUMO which can be suitably described within the concept of hybridization (see Section 2.1). However, the inter-molecular charge transport is complex and can be influenced by many intrinsic and extrinsic factors. A root cause lies in the weak van-der-Waals bonding forces between the individual organic molecules. Therefore, the coupling between the electronic orbitals of neighboring molecules is weak and the orbital overlap is small. These weak interactions are susceptible to factors including the molecular ordering (which in turn can be significantly influenced by the fabrication technique), interactions with adjacent materials in the FET and temperature.[43–47] Moreover, organic materials are typically characterized by a much higher defect density compared to inorganic single crystals. These defects can significantly influence the charge transport. A variety of models have been developed to describe charge transport in organic materials, mostly with the focus on a particular aspect of the transport phenomena. The fundamental difference in the description of most models lies in the treatment of the localization of charge carriers and to which degree it is incorporated into the model. The nature of trap states and two widely used charge-transport models with opposing approaches are briefly discussed in the following.

Trap States

In general, a trap state is an electronic defect in which the wave function of a captured charge carrier condensates on a spatially very limited region – the charge carrier is localized. The energy levels of trap states which are most relevant for semiconductors lie within the energy gap. A subtle difference to dopants (see Chapter 2.1.3) is the charged state when occupied: Whereas a dopant is electrically neutral when occupied, a trap state is electronically charged when occupied. For organic semiconductors, there are some important differences compared to inorganic semiconductors in the context of trap states. The usually larger energy gap of organic semiconductors (typically $3-4\,\mathrm{eV}$) compared to the band gap of inorganic semiconductors ($1-2\,\mathrm{eV}$) makes the formation of trap states with much deeper energy levels possible. Furthermore, the dielectric constant of organic semiconductors ($\varepsilon \approx 3$) is substantially smaller than that of inorganic semiconductors ($\varepsilon > 12$).[48,49] Thus, charged states, like occupied traps, in organic semiconductors are less effectively screened and have a severe impact on the surrounding energy landscape.

The origin of trap states can be disorder, chemical impurities or extrinsic factors like interfacial or environmental effects. The disorder can be categorized into static disorder and dynamic (thermal) disorder. Static disorder typically arises from structural defects, which can extend from the molecular scale (e.g. point defects and dislocations of molecules) to the device scale (e.g. extended line defects and grain boundaries in the semiconductor).[50,51] Every inhomogeneity in the structural order of the organic semiconductor affects the intermolecular orbital overlap and locally changes the electronic structure which can lead to the formation of trap states. Also dynamic disorder, arising from the thermal motion of the molecules, results in fluctuations of the intermolecular electronic coupling. On short timescales, the molecular orbital overlap can become so small that charge carriers are localized, however on long time scales the carriers can eventually move in the semiconductor. This transient localization is proposed to act as a main source of disorder in highly ordered organic semiconductors (single) crystals.[52–54] Apart from disorder, chemical impurities in the semiconductor can act as trap states, if the energy levels of the guest molecules are different from those of the host material. Typical chemical impurities are synthesis byproducts of the organic semiconductor, chemically degraded organic semiconductor molecules or chemicals introduced in the course of the fabrication process.
For the charge transport in organic transistors the gate dielectric/semiconductor interface plays an outstanding role as the charge-carrier channel is formed in close vicinity to this interface. Hence, trap states at this interface and close to it are particularly important. For silicon oxide, dangling bonds are known to be a notorious source of traps states and for metal oxides a non stochiometric ratio of metal and oxygen can lead to electrically active states in the dielectric. Also extrinsic impurities on the gate dielectric/semiconductor interface are a severe source of trap states among which absorbed water molecules are reported to represent a major reason for the formation of deep trap states.[55,56] Furthermore the polarizability of the gate dielectric material induces the formation of polarons in the organic semiconductor which in the extreme case of strong coupling can lead to self-trapping of the charge carriers.[46,57,58]
The exact identification of trap states and their origin in organic semiconductors are complex and often an interplay between different factors is observed, such as the presence of structural defects in the vicinity of chemical defects and vice versa,[59] or the translation of poor quality of the gate dielectric/semiconductor interface to poor and trap-ridden semiconductor ordering (as will be discussed in Chapter 3).[60,61]

Band-Like Transport

To model charge transport in organic semiconductors, one approach (of which the multiple trapping and release model is the most prominent representative)[62,63] starts from the prerequisite that the overlap of the molecular orbitals of neighboring molecules is sufficient to lead to the formation of narrow electronic bands. In these bands, coherent band transport is possible (in accordance to crystalline inorganic semiconductors as discussed in Chapter 2.1) and represents the inherent transport mechanism. Defects and disorder are treated as a perturbation of the system and are incorporated as localized states in the

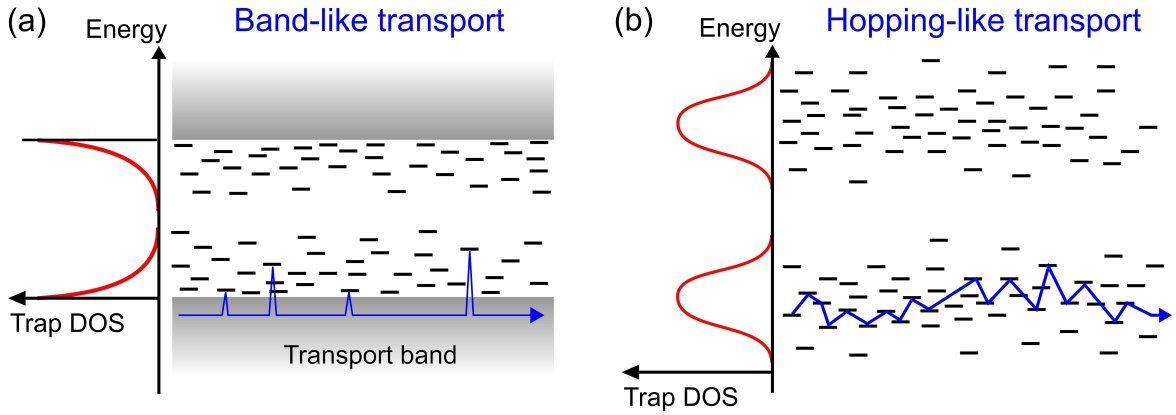


Figure 2.9: (a) Illustration of the transport mechanism for a band-like transport. Charge carriers frequently get trapped in localized states and are thermally released again. In an extended transport band, charge transport is possible. (b) Illustration of hopping-like transport. There are no electronic bands, but charge carriers can hop from one localized state to another by phonon-assisted tunneling.

band gap of the material. Transport is modeled by activation of charge carriers from the localized states into the extended bands by the application of an electric field or thermal activation (see Figure 2.9(a)). Typically, the localized states are not described as discrete energy levels but as a distribution of localized states modeled as a Gaussian or Exponential.[64,65] The energetic distribution of these states (i.e. the density-of-states function) in the band gap is essential for the transport properties of the semiconductor. The band-like approach for describing charge transport typically fits best for highly ordered organic semiconductor (poly-)crystals with large charge-carrier mobilities of about $1\,\mathrm{cm}^2/\mathrm{Vs}$ and sets the basics for the analysis in Chapter 3.

Hopping-Like Transport

The other approach for modeling charge transport in organic semiconductors starts from the premise that there are no electronic bands, but transport is completely dominated by the presence of localized states. The motion of the charge carriers is described by a hopping transport from one localized state i to another localized state j (see Figure 2.9(b)). This hopping process can be thermally activated and/or assisted by tunneling. In its simplest form, it is described by the Miller-Abrahams equation.[66] The hopping rate w_{ij} consists of a tunneling probability (which is dependent on the spatial distance between the localized

states R_{ij}) and a probability to absorb a phonon for an hop to a state with a higher energy (which is dependent on the energetic difference of the states $E_j - E_i$):

$$w_{ij} = \nu_0 \cdot \begin{cases} \exp\left[\frac{-2R_{ij}}{\xi}\right] \cdot \exp\left[-\frac{E_j - E_i}{k_B T}\right] & \text{for } E_j - E_i > 0 \\ \exp\left[\frac{-2R_{ij}}{\xi}\right] & \text{for } E_j - E_i \leq 0 \end{cases} \tag{2.44}$$

where ν_0 is the attempt-to-escape frequency, ξ is the localization radius of the charge carrier, k_B is the Boltzmann constant and T the temperature. Among hopping models several extensions and modifications exist to emphasize the certain aspects of the transport like the energetic distribution of the electronic states, polaronic contributions, dependence of the electric field or carrier concentration.[67–69] Typically these hopping models are an appropriate description of charge transport for materials at the low-mobility end of the spectrum of organic semiconductors (with a high degree of disorder) as it is the case for amorphous films.

Chapter 3

Quantitative Analysis of the Density of Trap States in Semiconductors by Electrical Transport Measurements on Low-Voltage Field-Effect Transistors

3.1 Discussion

3.1.1 State-of-the-Art

The energy gap of polycrystalline or amorphous semiconductors is typically characterized by localized states which act as charge-carrier traps and significantly influence the electrical and optical properties of the semiconductor. The density and energetic distribution of these trap states are described by the density of trap states (trap DOS), in units of traps per unit volume and unit energy ($cm^{-3}eV^{-1}$). A variety of experimental methods to access the trap DOS in semiconductors have been developed, including photoemission spectroscopy,[70,71] Kelvin-probe force microscopy,[72–74] photoconductivity measurements,[75,76] electron spin resonance spectroscopy,[77] capacitance-voltage measurements,[78–80] and electrical transport measurements.[81] Fundamental differences between these methods include the requirements for the sample geometry, the accessible energy range and the spatial region in which the trap DOS is examined. Typically, optical methods like photoemission spectroscopy or photoconductivity measurements probe the trap DOS mainly in the bulk of the semiconductor, whereas Kelvin-probe force microscopy is sensitive to the semiconductor/air interface and capacitance-voltage measurements and electrical transport measurements are mainly probing the dielectric/semiconductor interface.
Electrical transport measurements were successfully employed in the past to determine the trap DOS for field-effect transistor devices based on amorphous silicon or organic semiconductors.[62,82–86] In principle, the underlying trap DOS is extracted from measured

transfer characteristics of the transistors. However, there are several techniques among the electrical transport measurements which differ regarding the basic assumptions of the theoretical model and the exact experimental details. The methods can be divided into two classes: One class requiring transfer characteristics which are measured at different temperatures to extract a trap DOS (also referred as temperature methods), and the other class for which a transfer characteristic at a single temperature is sufficient to determine the trap DOS.[81] Methods that do not require different temperatures bring several advantages: (1) The resulting trap DOS is not disturbed by additional temperature-dependent effects (e.g. temperature dependence of the carrier mobility or of the contact resistance). (2) The trap DOS can be determined for several temperatures individually and thus the temperature dependency of the trap DOS itself can be traced.[87] (3) The experimental effort is significantly reduced. In a comprehensive comparison between different methods that utilize electrical transport measurements to extract the trap DOS in organic semiconductors, Kalb et al. found the method after Grünewald et al. to be very reliable and unambiguous.[81,88] The Grünewald method is one of the few non-temperature-dependent methods and was successfully employed for transistors based on many different (organic) semiconductors in the past.[84,86,87,89–99]

3.1.2 Objective

A fundamental drawback of the original Grünewald method is its limitation to transistors with a thick gate dielectric, i.e., a low unit-area capacitance of the gate dielectric and thus operating voltages of several tens of volts. Low-voltage organic transistors (operating at a few volts) are particularly interesting for the application in future electronic devices, such as flexible active-matrix displays or conformable sensors powered by small batteries or solar cells. Thus, the extension of the Grünewald method to transistors with low operating voltages is the objective of the study presented in this chapter. On the one hand, the basic assumptions of the Grünewald method were theoretically evaluated and simplifications were adjusted to meet the requirements of transistors with a thin gate dielectric. On the other hand, the impact of this extension was examined experimentally by applying the original Grünewald method and the extended Grünewald method to measured transfer curves of organic transistors with a thick gate dielectric as well as with a thin gate dielectric. Conclusions were drawn regarding the validity of the methods.

3.1.3 Conclusion

This study deals with the Grünewald method for the extraction of the density and energetic distribution of the trap states in the semiconductor of a transistor from its measured transfer characteristics. An extension of the original Grünewald method to transistors with low operating voltage was developed, explored and its significance experimentally verified. The original Grünewald method makes a critical simplification regarding the potential drop of the applied gate-source voltage: The contribution of the interface potential to the total potential drop (across the semiconductor and the gate dielectric) is neglected. In order to

extend the original Grünewald method and make it applicable to any gate-dielectric thickness and operating voltage, the mathematical formalism of the original Grünewald method was reevaluated and the simplification eliminated, i.e. the contribution of the interface potential to the total potential drop was incorporated correctly. This leads to extended forms of two of the three key equations of the Grünewald method for calculating the trap DOS. As a criterion for which cases this extension becomes relevant the ratio of the gate dielectric capacitance and the capacitance of the charge-accumulation layer was identified. This was transferred into the benchmark that the thickness of the dielectric has to be comparable to the Debye length in the semiconductor. These theoretical considerations were complemented by an experimental study.
In order to test how the developed extension affects the result of the Grünewald method depending on the gate-dielectric thickness, two types of organic transistors were fabricated: One with a thick gate dielectric (110 nm thick) and one with a thin hybrid gate dielectric (5.3 nm thick, which is comparable to the Debye length of approximately 2 nm in the organic semiconductor). The measured transfer curves of each transistor were the basis for the extraction of the trap DOS. For each transfer curve, the original Grünewald method (i.e., with the simplification) and the extended Grünewald method (i.e., without simplification) were employed to extract the trap DOS. Consequently, any deviation between the outcomes of the two methods can be safely ascribed to the simplification. The results show that in the case of the TFT with the thick gate dielectric, the deviation between the trap DOS functions obtained using the original and the extended Grünewald method is extremely small. This outcome confirms that for transistors with high operating voltages, the commonly employed simplification regarding the contribution of the interface potential to the total potential drop is indeed justified. In contrast, the choice of the method has a profound effect on the trap DOS extracted from transistors with low operating voltages, as the simplification that is made in the original Grünewald method leads to an severe overestimation of the DOS compared to the result from the extended Grünewald method. Thus, a reliable extraction of the density of trap states of the semiconductor of a TFT with a thin gate dielectric and low operating voltage is possible only with the extended Grünewald method which was developed in this study. This is particularly important for organic TFTs as they are generally targeting mobile and wearable electronics applications for which low-voltage operation and thin gate dielectrics are thus critical prerequisites.

3.2 Published Article

Quantitative Analysis of the Density of Trap States in Semiconductors by Electrical Transport Measurements on Low-Voltage Field-Effect Transistors

Michael Geiger[1], Lukas Schwarz[1], Ute Zschieschang[1], Dirk Manske[1], Jens Pflaum[2], Jürgen Weis[1], Hagen Klauk[1], R. Thomas Weitz[3,4]

[1] *Max Planck Institute for Solid State Research, Heisenbergstr. 1, 70569 Stuttgart, Germany*
[2] *Experimental Physics IV, Julius Maximilian University, Am Hubland, 97074 Würzburg, Germany*
[3] *AG Physics of Nanosystems, Faculty of Physics, Ludwig Maximilians University, Amalienstr. 54, 80799 München, Germany*
[4] *NanoSystems Initiative Munich (NIM) and Center for NanoScience (CeNS), Ludwig Maximilians University, Schellingstr. 4, 80799 München, Germany*

Physical Review Applied **10, 044023 (2018)**

DOI: 10.1103/PhysRevApplied.10.044023

reprinted on pages 27–40

PHYSICAL REVIEW APPLIED **10,** 044023 (2018)

Quantitative Analysis of the Density of Trap States in Semiconductors by Electrical Transport Measurements on Low-Voltage Field-Effect Transistors

Michael Geiger,[1,*] Lukas Schwarz,[1] Ute Zschieschang,[1] Dirk Manske,[1] Jens Pflaum,[2] Jürgen Weis,[1] Hagen Klauk,[1] and Ralf Thomas Weitz[3,4]

[1] *Max Planck Institute for Solid State Research, Heisenbergstraße 1, 70569 Stuttgart, Germany*

[2] *Experimental Physics VI, Julius Maximilian University, Am Hubland, 97074 Würzburg, Germany*

[3] *AG Physics of Nanosystems, Faculty of Physics, Ludwig Maximilians University, Amalienstraße 54, 80799 München, Germany*

[4] *NanoSystems Initiative Munich (NIM) and Center for NanoScience (CeNS), Ludwig Maximilians University, Schellingstraße 4, 80799 München, Germany*

(Received 24 April 2018; revised manuscript received 8 August 2018; published 9 October 2018)

A method for extracting the density and energetic distribution of the trap states in the semiconductor of a field-effect transistor from its measured transfer characteristics is investigated. The method is based on an established extraction scheme [M. Grünewald *et al*., Phys. Stat. Sol. B 100, K139 (1980)] and extends it to low-voltage thin-film transistors (TFTs). In order to demonstrate the significance of this extension, two types of TFTs are fabricated and analyzed: one with a thick gate dielectric and high operating voltage and one with a thin gate dielectric and low operating voltage. From the measured transfer characteristics of both TFTs, the density of states (DOS) is calculated using both the original and the extended Grünewald method. The results not only confirm the validity of the original Grünewald method for high-voltage transistors, but also indicate the need for the extended Grünewald method for the reliable extraction of the trap DOS in transistors with a thin gate dielectric and low operating voltage.

DOI: 10.1103/PhysRevApplied.10.044023

I. INTRODUCTION

In an ideal crystalline semiconductor, there are no electronic states between the valence-band edge and the conduction-band edge and, therefore, this energy range is called the energy gap [1]. In contrast, the energy gap of polycrystalline or amorphous semiconductors is typically characterized by localized states that arise from structural defects (i.e., static disorder, induced, e.g., by grain boundaries) [2,3]; intentional [4,5] or unintentional [6] impurities; interaction of the charge carriers with polar molecules [7]; and, particularly in van-der-Waals-bonded molecular crystals, from dynamic disorder due to the thermal motion of the molecules [8–10]. These nonidealities lead to localized states in the energy gap of the semiconductor that act as charge-carrier traps. The density and energetic distribution of these localized states [trap density of states (DOS)] strongly influence the electrical characteristics of field-effect transistors based on disordered semiconductors.

When the applied gate-source voltage and, thus, the gate-induced carrier density in the semiconductor are small, most of the charges are trapped deep in the energy gap. When the gate-source voltage is increased, trap states closer to the transport level are gradually filled. The density of trap states therefore affects the subthreshold slope of the transistor, i.e., the slope of the transfer curve in the exponential region below the threshold voltage. For practical applications, this slope should be as steep as possible, ideally close to the room-temperature limit of 58 mV/decade, but a large density of deep trap states will lead to a less steep subthreshold slope. At the same time, as the gate-source voltage is increased, more and more charge carriers reach the transport level where they contribute to the charge transport in the semiconductor.

The origin of the frequently observed electric-field dependence of the effective carrier mobility is often believed to be trap filling and the associated change in the ratio of the densities of localized and delocalized carriers [11,12]. Other field-effect-transistor characteristics affected by the density of trap states are the bias-stress effect [13] and the alignment of the energy levels at the interfaces between the semiconductor and the source and drain contacts [14]. Aside from transistors, the trap DOS also has a critical influence on the charge-transport properties of other electronic devices based on disordered semiconductors, such as organic light-emitting diodes

*m.geiger@fkf.mpg.de

(OLEDs), in which trap states can induce the undesirable nonradiative recombination of electrons and holes [15,16], and photovoltaic cells, in which trap states may be beneficial for the separation of the photo-induced excitons, but also detrimental as they may impede the dissociation of formed charge transfer states or disrupt the transport of the separated carriers to the electrodes [17]. The exact analysis of the density and distribution of traps in disordered semiconductors is, thus, an important task, both from a fundamental perspective and from an application point of view.

While the trap DOS cannot be measured directly, it can be accessed indirectly by means of a number of experimental techniques, including photoemission spectroscopy [18,19], Kelvin-probe force microscopy [20,21], electrical transport measurements [22], photoconductivity measurements [23,24], electron spin resonance spectroscopy [25], and capacitance-voltage measurements [26]. In the 1980s, Grünewald *et al.* developed a method, initially intended for thin-film transistors (TFTs) based on hydrogenated amorphous silicon (a-Si:H), to convert a single transfer curve of a field-effect transistor (i.e., the drain current measured as a function of the applied gate-source voltage) to the underlying density-of-states function [27–29]. Over the past decade, the Grünewald method has been employed with great success to calculate the DOS of TFTs based on a wide range of organic semiconductors and fabricated with a variety of device architectures [30–37].

However, in all these previous reports, the Grünewald method was employed exclusively to TFTs with thick gate dielectrics and high operating gate voltages of a few tens of volts. The reason is that the original Grünewald method requires that the potential drop across the semiconductor layer be negligible compared to the potential drop across the gate dielectric, which significantly simplifies the computation but limits the applicability of the method to TFTs with high operating voltages. Here, we explore an extension of the Grünewald method in which this simplification is removed, thus making the method applicable to low-voltage TFTs with very thin gate dielectrics. This extension is an important upgrade, since organic TFTs are generally targeting mobile and wearable electronics applications in which low-voltage operation and, thus, thin gate dielectrics are critical prerequisites. The formalism for this extension was recently introduced by Jeong *et al.* and applied to inorganic TFTs with a 120-nm-thick gate dielectric, but without analyzing the implications of the extension depending on the thickness of the gate dielectric [38]. In contrast, we apply both the original and the extended Grünewald method to organic TFTs with two different gate-dielectric thicknesses and are, thus, able to show that the original Grünewald method is indeed applicable to high-voltage transistors, but not to low-voltage transistors.

II. EXPERIMENT

A. Device fabrication

All TFTs are fabricated in the bottom-gate, top-contact device structure using boron-doped silicon wafers with an electrical resistivity of 0.005 Ω cm as the substrate [39]. For the TFTs with the thick gate dielectric, the doped silicon wafer also serves as the gate electrode. The thick gate dielectric is a stack of three layers: a 100-nm-thick silicon dioxide (SiO_2) layer grown by thermal oxidation in dry oxygen, an 8-nm-thick aluminum oxide (Al_2O_3) layer deposited by atomic layer deposition, and a 1.7-nm-thick self-assembled monolayer (SAM) of *n*-tetradecylphosphonic acid. This triple-layer gate dielectric has a total thickness of 110 nm and a unit-area capacitance of 34 nF/cm^2 [39]. For the TFTs with the thin gate dielectric, a 30-nm-thick layer of aluminum is deposited onto the silicon substrate by thermal evaporation in vacuum as the gate electrode. The thin gate dielectric consists of a 3.6-nm-thick aluminum oxide (AlO_X) layer obtained by briefly exposing the surface of the aluminum gate electrode to an oxygen plasma and a 1.7-nm-thick *n*-tetradecylphosphonic acid SAM. This double-layer gate dielectric has a total thickness of 5.3 nm and a unit-area capacitance of 700 nF/cm^2 [40].

For both types of TFTs, a 20-nm-thick layer of the small-molecule organic semiconductor 2,9-diphenyl-dinaphtho [2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DPh-DNTT [41,42]) is deposited by thermal sublimation in vacuum. During the semiconductor deposition, the substrate is held at a temperature of 90°C. Finally, a 30-nm-thick layer of gold is deposited through a polyimide shadow mask (CADiLAC Laser, Hilpoltstein, Germany) to define the source and drain contacts, with a channel width of 200 μm and channel lengths ranging from 10 to 100 μm. Figure 1 shows

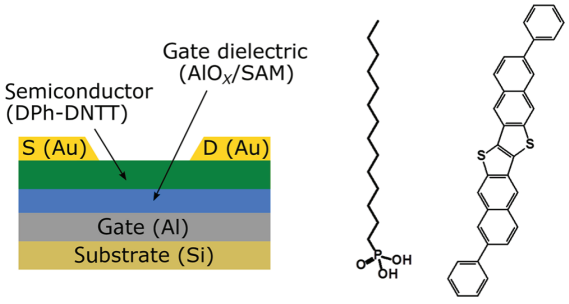


FIG. 1. Schematic cross section of the thin-film transistors with the thin gate dielectric, which consists of a 3.6-nm-thick layer of aluminum oxide (AlO_X) and a 1.7-nm-thick self-assembled monolayer (SAM) of *n*-tetradecylphosphonic acid. The chemical structures of *n*-tetradecylphosphonic acid and of the organic semiconductor 2,9-diphenyl-dinaphtho[2,3-b:2′,3′-f]-thieno[3,2-b]thiophene (DPh-DNTT) are also shown.

the schematic cross section of the TFTs with the thin gate dielectric.

B. Electrical characterization

The current-voltage characteristics of the TFTs are measured in ambient air at room temperature under yellow laboratory light using an Agilent 4156C Semiconductor Parameter Analyzer. The transfer characteristics are measured by applying a drain-source voltage V_{DS} of -2 V to the TFTs with the thick gate dielectric and -0.1 V to the TFTs with the thin gate dielectric and by sweeping the gate-source voltage in steps of -0.75 V (TFTs with the thick gate dielectric) and -50 mV (thin gate dielectric). The drain-source voltages are chosen so that the TFTs are operated in the linear regime.

The effective charge-carrier field-effect mobility μ_{eff} is calculated by fitting the following equation to the measured transfer curve:

$$\mu_{\text{eff}} = \frac{L}{WC_{\text{diel}}V_{\text{DS}}}\frac{\partial I_D}{\partial V_{\text{GS}}}, \tag{1}$$

where I_D is the drain current, L the channel length, W the channel width, C_{diel} the unit-area capacitance of the dielectric and V_{GS} the gate-source voltage.

The subthreshold slope S is calculated by fitting the following equation to the subthreshold region of the measured transfer curve:

$$S = \frac{\partial V_{\text{GS}}}{\partial[\log_{10}(I_D)]}. \tag{2}$$

For the analysis below, the value of the flat-band voltage V_{FB} is required. Following previous publications, we approximate the flat-band voltage as the turn-on voltage V_{on}, i.e., as the gate-source voltage at which the drain current starts to increase sharply above the noise floor when plotted on a logarithmic scale (see Fig. 2) [30].

III. ANALYSIS AND DISCUSSION

A. The original Grünewald method

In the following, a brief summary of the original Grünewald method is provided, including the essential equations and assumptions. More detailed information can be found in the publications by Grünewald *et al.* [27,28] and Kalb *et al.* [30].

The Grünewald method was developed to facilitate the conversion of a single transfer curve of a field-effect transistor recorded in the linear regime of operation (i.e., with a drain-source voltage that is negligibly small compared to the difference between the gate-source voltage and the threshold voltage) to the DOS of the semiconductor. For the original Grünewald method, a number of simplifying assumptions are made:

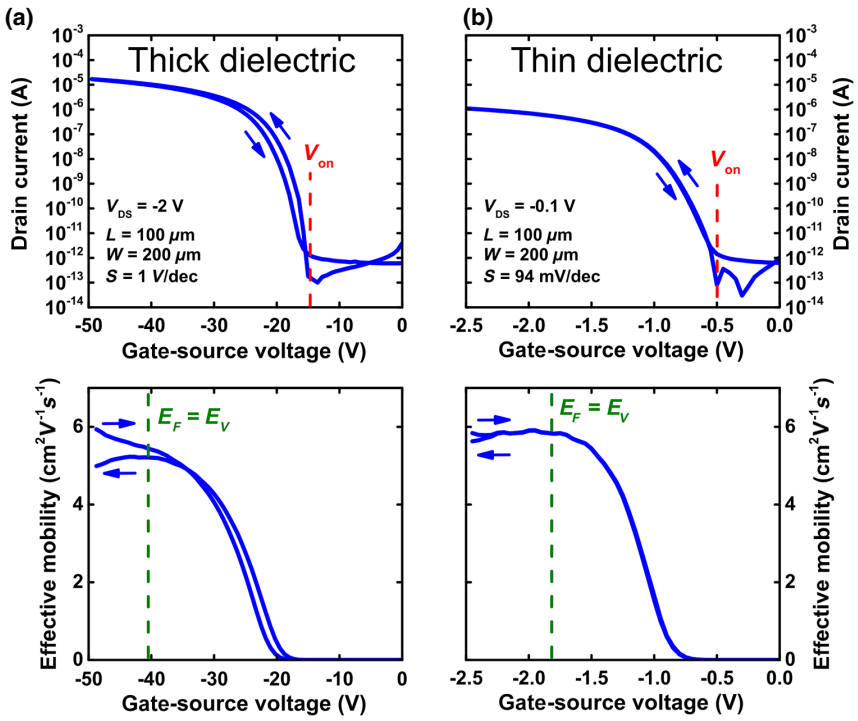


FIG. 2. Transfer curves measured on DPh-DNTT TFTs with a 110-nm-thick gate dielectric (a) and a 5.3-nm-thick gate dielectric (b). The transfer curves are measured in the linear regime of operation. From the transfer curves, the turn-on voltage V_{on} is extracted and taken as the flat-band voltage V_{FB}. The effective carrier mobility μ_{eff} is calculated using Eq. (1) and plotted as a function of gate-source voltage; from this plot, the gate-source voltage at which the mobility saturates is obtained and taken as the gate-source voltage at which $E_F = E_V$, with E_F being the Fermi energy and E_V the valence-band energy. The subthreshold slope S is calculated using Eq. (2).

(1) The gradual channel approximation is valid, i.e., the electric field E_x (created by the gate-source voltage) in the direction perpendicular to the interface between the semiconductor and the gate dielectric is much larger than the electric field E_y (created by the drain-source voltage) parallel to the semiconductor/dielectric interface. This requirement is fulfilled by operating the transistor in the linear regime, i.e., with a small drain-source voltage.

(2) The semiconductor layer is homogeneous in the direction perpendicular to the semiconductor/dielectric interface.

(3) A nonzero flat-band voltage (caused, e.g., by a difference between the work functions of the semiconductor and the gate electrode or by charged states in the gate dielectric) can be taken into account by correcting the applied gate-source voltage for the flat-band voltage: $V_G = V_{GS} - V_{FB}$.

(4) The thickness of the semiconductor layer is larger than the Debye length in the semiconductor, so that the electrostatic potential at the distance d from the semiconductor/dielectric interface (where d is the thickness of the semiconductor layer) is essentially zero.

(5) The potential drop across the thickness of the semiconductor is much smaller than the potential drop across the thickness of the gate dielectric, so that the contribution of the potential drop across the semiconductor layer to the total potential drop of the applied gate-source voltage can be neglected.

(6) The Boltzmann approximation holds for the free charge carriers.

(7) The transfer curve of the transistor is not affected by the contact resistance.

One important advantage of the Grünewald method over other DOS extraction methods is that the Grünewald method does not require any temperature-dependent measurements, as the DOS is calculated from a single transfer curve, which makes it, in principle, possible to investigate the temperature dependence of the DOS [34]. Another advantage of the Grünewald method is that it does not require any abrupt approximations, i.e., it is not necessary to assume that the charge-accumulation layer has a homogeneous charge density or a sharp edge. Instead, the band bending in the semiconductor induced by the gate-source voltage is correctly taken into account. Figure 3 shows a sketch of the band bending in the semiconductor for a gate-source voltage larger than the flat-band voltage. The electrostatic potential at the semiconductor/dielectric interface is called interface potential V_0.

The starting point for the calculation of the gate-induced carrier density is the one-dimensional Poisson equation:

$$\frac{\partial^2 V(x)}{\partial x^2} = \frac{en(x)}{\varepsilon_0 \varepsilon_S}, \tag{3}$$

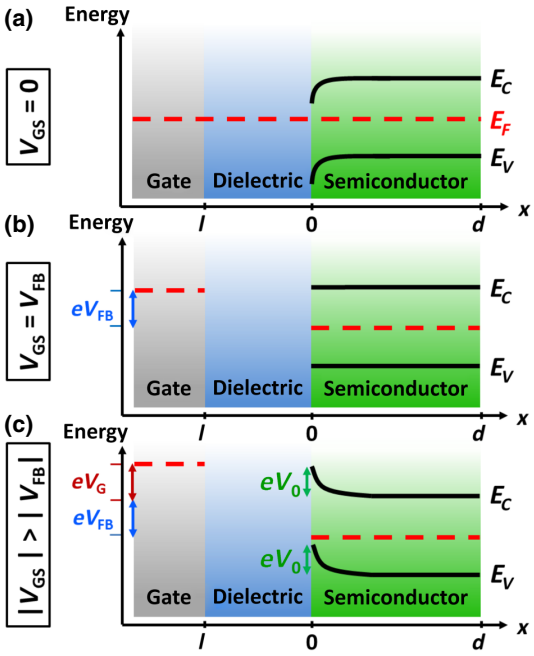


FIG. 3. Schematic cross section of a field-effect transistor showing the relevant energy levels. (a) Initial band bending in the semiconductor in the absence of an applied gate-source voltage. (b) The flat-band voltage V_{FB} is the gate-source voltage necessary to compensate this initial band bending. (c) Applying a gate-source voltage greater than the flat-band voltage ($V_G = V_{GS} - V_{FB}$) induces a band bending in the semiconductor that leads to charge accumulation in the semiconductor in close proximity to the semiconductor/dielectric interface. At this interface, the bands of the semiconductor are shifted by an energy eV_0, with V_0 being the interface potential. E_C and E_V are the conduction- and valence-band energies.

where $V(x)$ is the electrostatic potential at position x, e the elementary charge, $en(x)$ the total charge density (including free and trapped charges as well as ionized acceptors and donors), ε_0 the vacuum permittivity, and ε_S the dielectric constant of the semiconductor. As one of the boundary conditions for the Poisson equation, the following criterion is applied:

$$\varepsilon_0 \varepsilon_{\text{diel}} E_{\text{diel}} = -\varepsilon_0 \varepsilon_S E_S, \tag{4}$$

$$\varepsilon_0 \varepsilon_{\text{diel}} \frac{V_{GS} - V_{FB}}{l} = -\varepsilon_0 \varepsilon_S \frac{\partial V(x)}{\partial x}\bigg|_{x=0}, \tag{5}$$

where E_{diel} (E_S) is the electric field in the gate dielectric (in the semiconductor) at the semiconductor/dielectric interface and oriented perpendicular to the interface, $\varepsilon_{\text{diel}}$ the dielectric constant of the gate dielectric, and l the thickness of the gate dielectric.

For the calculation of the relation between the interface potential and the gate-source voltage, it is assumed that the current that flows in the accumulation channel parallel to the semiconductor/dielectric interface can be written according to the Boltzmann approximation:

$$I = \frac{I_0}{d}\int_0^d \exp\left(\frac{eV(x)}{k_B T}\right) dx, \tag{6}$$

where I_0 is the current at flat-band conditions, d the thickness of the semiconductor layer, k_B the Boltzmann constant, and T the temperature.

By converting Eq. (6) and applying the first boundary condition (5) and the second boundary condition $V(d) = 0$ (see assumption 4 in the list above), the following differential equation for the interface potential V_0 can be derived:

$$\frac{dV_0}{d(V_{\rm GS} - V_{\rm FB})} = \frac{\varepsilon_{\rm diel} d}{\varepsilon_S l}\frac{1}{I_0}\frac{dI}{d(V_{\rm GS} - V_{\rm FB})} \times \frac{V_{\rm GS} - V_{\rm FB}}{\exp\left(\frac{eV_0}{k_B T}\right) - 1}. \tag{7}$$

The form of this differential equation allows a partial integration to be performed, which yields an equation that implicitly contains V_0 as a function of $V_{\rm GS}$:

$$\exp\left(\frac{eV_0}{k_B T}\right) - \frac{eV_0}{k_B T} - 1 = \frac{e}{k_B T}\frac{\varepsilon_{\rm diel} d}{\varepsilon_S l I_0}\left[(V_{\rm GS} - V_{\rm FB}) \times I(V_{\rm GS} - V_{\rm FB}) - \int_0^{V_{\rm GS}-V_{\rm FB}} I(\tilde{V}_{\rm GS}) d\tilde{V}_{\rm GS}\right]. \tag{8}$$

From Eq. (8), the relation $V_0(V_{\rm GS} - V_{\rm FB})$ can be determined numerically, so that for all gate-source voltages, the interface potential V_0 is known. With this knowledge of V_0, a conversion of the Poisson equation (3) using the first boundary condition (5) and the second boundary condition [$V(d) = 0$] leads to an expression for the total carrier density n:

$$n(V_0) = \frac{\varepsilon_{\rm diel}^2 \varepsilon_0}{\varepsilon_S l^2 e}(V_{\rm GS} - V_{\rm FB})\left(\frac{\partial V_0}{\partial(V_{\rm GS} - V_{\rm FB})}\right)^{-1}. \tag{9}$$

Finally, within the zero-temperature approximation (which requires that the Fermi-Dirac function be a step function), the density-of-states function, which is therefore probed at the energy $E_F + eV_0$ (see Fig. 3), can be written as

$$\frac{1}{e}\frac{dn(V_0)}{dV_0} \approx \mathrm{DOS}(E_F + eV_0). \tag{10}$$

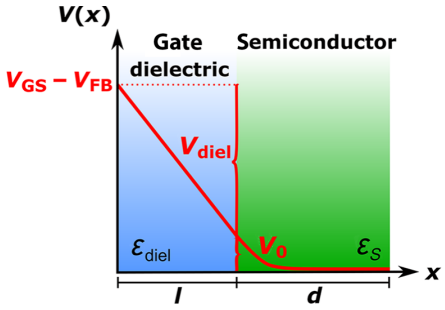


FIG. 4. Sketch of the potential drop across the gate dielectric and the semiconductor layer of the transistor. In the original Grünewald method, it is assumed that $|V_0| \ll |V_{\rm GS}|$ and, hence, V_0 is ignored. In the extended Grünewald method proposed here, this simplification is removed, and the contribution of V_0 is correctly taken into account.

B. Extension of the original Grünewald method

As mentioned in the Introduction, the original Grünewald method makes a critical simplification in the choice of the first boundary condition for the Poisson equation: The contribution of the interface potential V_0 to the total potential drop across the semiconductor and the gate dielectric is neglected (this is assumption 5 in the list above). A schematic of the potential across the semiconductor-gate dielectric stack is shown in Fig. 4. As will be shown, this simplification holds only for transistors with a high operating voltage (i.e., a thick gate dielectric), but not for transistors with a low operating voltage (i.e., with a gate dielectric that is either very thin, as shown here, or has a large permittivity [43]). For low-voltage transistors, the final result of the density-of-states function is greatly affected by the simplification regarding V_0.

For the purpose of this analysis, the gate dielectric can be considered as "thin" if its thickness is no greater than a few times the Debye length in the semiconductor, since in this case the capacitance of the gate dielectric will be similar to the capacitance of the charge-accumulation layer at the flat-band voltage and, thus, the potential drop across the gate dielectric $V_{\rm diel}$ will be similar to the potential drop across the thickness of the semiconductor layer V_0, which implies that the contribution of V_0 to the total voltage drop cannot be neglected [44]. As will be shown later, the average Debye length in the semiconductor is 2 nm, which implies that the gate dielectric with a thickness of 5.3 nm can be considered indeed as thin.

In order to extend the original Grünewald method and make it applicable to any gate-dielectric thickness and operating voltage, we repeated the mathematical derivation of the original Grünewald method, but instead of using Eq. (5), which reflects the simplification

$$V_{\rm GS} = V_{\rm FB} + V_{\rm diel}, \tag{11}$$

we included the term V_0 in this equation in order to properly take into account the contribution of V_0 to the total potential drop:

$$V_{GS} = V_{FB} + V_{diel} + V_0. \tag{12}$$

As a consequence, Eq. (5) transforms into

$$\varepsilon_0\varepsilon_{diel}\frac{V_{GS} - V_{FB} - V_0}{l} = -\varepsilon_0\varepsilon_S\frac{\partial V(x)}{\partial x}\bigg|_{x=0}. \tag{13}$$

This adjustment has profound implications on the subsequent equations. Following the original derivation, the differential equation (7) translates to

$$\frac{dV_0}{d(V_{GS} - V_{FB})} = \frac{\varepsilon_{diel}d}{\varepsilon_S l}\frac{1}{I_0}\frac{dI}{d(V_{GS} - V_{FB})} \times \frac{V_{GS} - V_{FB} - V_0}{\exp\left(\frac{eV_0}{k_BT}\right) - 1}. \tag{14}$$

This differential equation cannot be simplified analytically. However, it is possible to determine the relation $V_0(V_{GS} - V_{FB})$ using numerical methods (e.g., using the ordinary differential equation solver `scipy.integrate.odeint` included in the open-source PYTHON library SciPy [45]). Because the extended boundary condition (13) now includes the term V_0, the equation for the total carrier density must be adjusted as well:

$$n(V_0) = \frac{\varepsilon_{diel}^2\varepsilon_0}{\varepsilon_S l^2 e}(V_{GS} - V_{FB} - V_0) \times \left[\left(\frac{\partial V_0}{\partial(V_{GS} - V_{FB})}\right)^{-1} - 1\right]. \tag{15}$$

All subsequent steps in the analysis are identical to the original Grünewald method.

A general issue of the Grünewald method is that the DOS is calculated as a function of $E_F + eV_0$, i.e., that the energy is referenced to the initial Fermi energy E_F. This may make it difficult to compare the DOS functions of transistors in which the difference between the energy of the transport level and the initial Fermi energy is not the same, e.g., because the transistors are fabricated using different materials. For this reason, it may be more convenient to reference the DOS to the transport level [30,46–48], i.e., to the lowest unoccupied molecular orbital (LUMO) or conduction band edge (E_C) in the case of *n*-channel transistors, and the highest occupied molecular orbital (HOMO) or valence-band edge (E_V) in the case of *p*-channel transistors. One way to accomplish this was recently suggested by Za'aba *et al.* [35]. In their approach, the gate-source voltage at which the measured effective charge-carrier mobility saturates (i.e., no longer increases with increasing gate-source voltage) is translated to the corresponding value for the interface potential V_0 using Eq. (14) and this value is then taken as the energetic position at which the Fermi level crosses the transport level. This approach is adopted here, as illustrated in Fig. 2. We note, however, that this approach produces a reliable result only if the gate-source voltage at which the effective carrier mobility saturates is unambiguously identified, which will usually require that the measurement of the transistors' transfer curve is conducted over a wide range of gate-source voltages.

C. Experimental comparison of the original and extended Grünewald method

In the previous section, we showed how the Grünewald method is extended by eliminating the simplification regarding V_0, which leads to extended forms of two of the three key equations of the Grünewald method, namely, Eqs. (14) and (15). In order to test how this extension affects the result of the Grünewald method depending on the gate-dielectric thickness, we fabricate two types of transistors: one with a thick gate dielectric (110 nm thick) and one with a thin gate dielectric (5.3 nm thick). After device fabrication, the transfer curves (drain current as a function of applied gate-source voltage) of both TFTs are measured in the linear regime of operation, i.e., with a drain-source voltage that is negligible compared to the difference between the gate-source voltage and the threshold voltage (see Fig. 2).

From each of these transfer curves, the DOS of the semiconductor is calculated once using the original Grünewald method [Eqs. (7), (9), and (10)] and once using the extended Grünewald method [Eqs. (14), (15), and (10)]. Consequently, any deviations between the DOS calculated using the original Grünewald method (i.e., with the simplification regarding V_0) and the DOS calculated with the extended Grünewald method (i.e., without this simplification) can be ascribed to the simplification regarding V_0.

In the first step, the relation between the interface potential and the gate-source voltage [$V_0 = f(V_{GS} - V_{FB})$] is calculated numerically using PYTHON, once from Eq. (7) and once from Eq. (14). In the case of the TFT with the thick gate dielectric, the results are essentially identical, as shown in Fig. 5(a). In contrast, for the TFT with the thin gate dielectric, the original differential equation (7) and the extended differential equation (14) produce notably different results [see Fig. 5(b)], because the magnitude of the gate-source voltage is, in this case, comparable to the magnitude of the interface potential V_0 (a few hundred millivolts), so that the latter can no longer be ignored without introducing a significant error.

In the second step, the relation between the total carrier density and the interface potential [$n = f(V_0)$] is calculated, once from Eq. (9) and once from Eq. (15), and

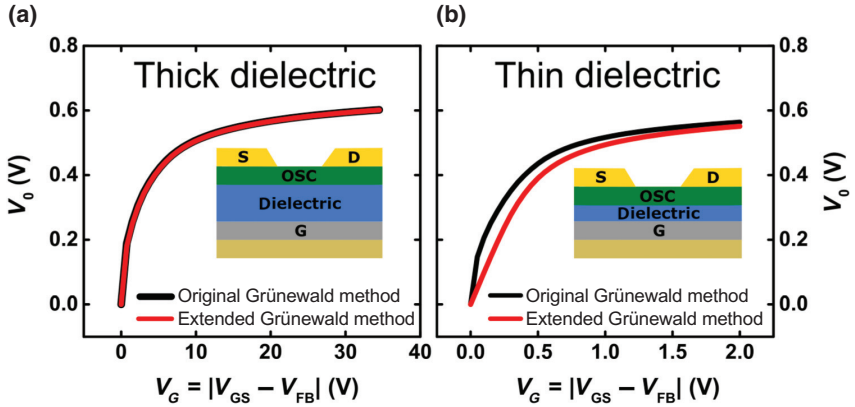


FIG. 5. Results of the first step of the Grünewald method in which the relation between the interface potential and the gate-source voltage is calculated from the measured transfer curves. This calculation is performed once using Eq. (7) (original method, shown with black lines) and once using Eq. (14) (extended method, shown with red lines). (a) For the TFT with the thick gate dielectric, the results show that the simplification in the original Grünewald method is indeed justified. (b) For the TFT with the thin gate dielectric, the original differential equation (7) and the extended differential equation (14) produce notably different results, because the magnitude of the gate-source voltage is, in this case, comparable to the magnitude of the interface potential V_0 (a few hundred millivolts), so that the latter can no longer be ignored without introducing a significant error.

the results are shown in Fig. 6. From the total carrier density, the Debye length in the semiconductor is calculated according to

$$\lambda_D = \sqrt{\frac{\varepsilon_S \varepsilon_0 k_B T}{e^2 n(V_{GS})}}. \tag{16}$$

The average value of the Debye length in the semiconductor over the range of gate-source voltages considered here is 2 nm; only for a narrow range of gate-source voltages just above the flat-band voltage, the Debye length exceeds the thickness of the semiconductor layer (20 nm). This range of gate-source voltages is excluded for the following analysis in order not to violate assumption 4 from the list above and to keep the analysis self-consistent.

In the third step, the trap DOS is calculated using Eq. (10), yielding the DOS as a function of $E_F + eV_0$. In the final step, the DOS is obtained as a function of $E - E_V$ by determining the gate-source voltage at which the carrier mobility saturates and translating it to the corresponding value for the interface potential V_0. This value of V_0 is taken as the energetic position at which the Fermi level crosses the transport level (see Fig. 2).

The results are shown in Fig. 7. As can be seen, in the case of the TFT with the thick gate dielectric, the deviation between the DOS functions obtained using the original and the extended Grünewald method is extremely small, which confirms that, for transistors with high operating voltages, the commonly employed simplification regarding the contribution of the interface potential V_0 to the total potential drop is indeed justified [30–37]. In contrast, the choice of the method has a profound effect on the DOS extracted from transistors with low operating voltages, as the simplification regarding V_0 that is made

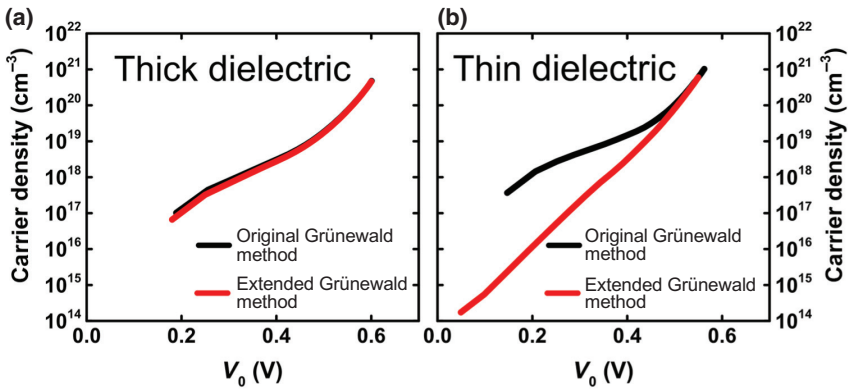


FIG. 6. Results of the second step of the Grünewald method in which the relation between the carrier density and the interface potential is calculated. This calculation is performed once using Eq. (9) (original method, shown with black lines) and once using Eq. (15) (extended method, shown with red lines).

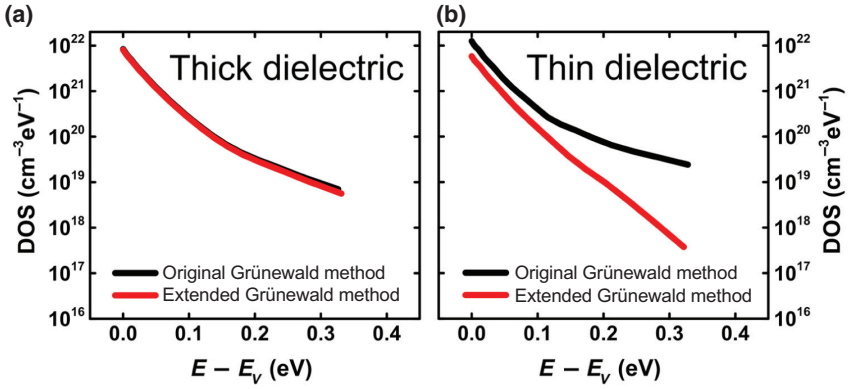


FIG. 7. Results of the final steps of the Grünewald method. Using Eq. (10), the trap DOS is calculated, yielding the DOS as a function of $E_F + eV_0$, which is then converted into the DOS as a function of $E - E_V$ by taking the gate-source voltage at which the carrier mobility saturates (see Fig. 2) as the gate-source voltage at which the Fermi level crosses the transport level E_V. The DOS is calculated once using the results from Eq. (9) (original method, shown with black lines) and once using the results from Eq. (15) (extended method, shown with red lines). (a) For the TFT with the thick gate dielectric, the results show that the simplification in the original Grünewald method does not affect the calculated trap DOS and is thus justified. (b) For the TFT with the thin gate dielectric, the trap DOS functions obtained with and without the simplification deviate substantially, as the original Grünewald method significantly overestimates the trap DOS in this case.

in the original Grünewald method leads to an overestimation of the DOS compared to the result from the extended Grünewald method.

It is important to note that both the original and the extended Grünewald method yield reliable results only if the transfer curve of the transistor is not dominated by the contact resistance, i.e., if the potential drops across the contact resistances are small. To evaluate whether this requirement is fulfilled in the TFTs examined here, we measure the width-normalized contact resistance of both TFTs using the transmission-line method (TLM) [49,50] (for details, see Fig. S3 of the Supplemental Material [51]) and calculated its contribution to the width-normalized total resistance. The results are shown in Fig. 8. As can be seen, in the TFT with the thin gate dielectric, the contribution of the contact resistance to the total TFT resistance is indeed no greater than 10%, which means that the error in the calculation of the DOS in the TFT with the thin gate dielectric is relatively small. In the TFT with the thick gate dielectric, the contribution of the contact resistance to the total TFT resistance is about 20% and will thus introduce a somewhat larger error. On the other hand, Fig. 8 also indicates that the ratio between the contact resistance and the total TFT resistance is essentially independent of the gate-source voltage, which means that the overall shape of the density-of-states function is not significantly affected. One possibility to further reduce the influence of the contact resistance on the extraction of the DOS would be to perform the measurements on TFTs with an even greater channel length [31].

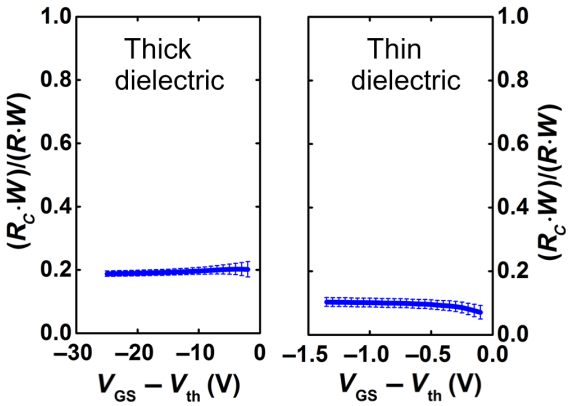


FIG. 8. Ratio between the channel-width-normalized contact resistance ($R_C \cdot W$) and the channel-width-normalized total device resistance ($R \cdot W$) for TFTs with a channel length of 100 μm, measured using the transmission line method (TLM) and plotted as a function of the difference between the gate-source voltage and the threshold voltage. For both types of TFT (thick and thin gate dielectrics), the contact resistance is small compared to the total resistance.

IV. CONCLUSION

We explore an extension of the Grünewald method for the extraction of the density and energetic distribution of the trap states in the semiconductor of a transistor from its measured transfer characteristics to transistors with low operating voltage. The contribution of the interface potential V_0 to the total potential drop of the applied gate-source

voltage is incorporated correctly into the formalism, leading to the extension of two of the three key equations for the Grünewald method. To demonstrate the significance of this extension, we perform the calculation of the trap DOS on TFTs with a thick and with a thin gate dielectric, once using the original Grünewald method and once using the extended Grünewald method. For the TFT with the thick gate dielectric, the original and the extended method yield essentially the same result, which confirms the validity of the original Grünewald method for such transistors. In contrast, for the TFT with the thin gate dielectric, the need for the extended Grünewald method is verified, as in such transistors, the contribution of the interface potential cannot be ignored without introducing a significant error in the calculated trap DOS.

ACKNOWLEDGMENTS

We gratefully acknowledge Kazuo Takimiya (RIKEN Center for Emergent Matter Science, Wako, Saitama, Japan) as well as Koichi Ikeda, Yuichi Sadamitsu, and Satoru Inoue (Nippon Kayaku, Tokyo, Japan) for providing the organic semiconductor DPh-DNTT. We thank Marion Hagel at the Max Planck Institute for Solid State Research for expert technical assistance. This work is partially funded by the German Research Foundation (DFG) under the Grants No. KL 2223/6-1 (SPP FFlexCom), No. KL 2223/7-1, and No. INST 35/1429-1 (SFB 1249).

[1] C. Kittel, *Introduction to Solid State Physics* (Wiley, New York, 2004), 8th ed., p. 163 ff.

[2] W. L. Kalb, S. Haas, C. Krellner, T. Mathis, and B. Batlogg, The trap DOS in small molecule organic semiconductors: A quantitative comparison of thin-film transistors with single crystals, Phys. Rev. B **81**, 155315 (2010).

[3] J. Rivnay, L. H. Jimison, J. E. Northrup, M. F. Toney, R. Noriega, S. Lu, T. J. Marks, A. Facchetti, and A. Salleo, Large modulation of carrier transport by grain-boundary molecular packing and microstructure inorganic thin films, Nat. Mater. **8**, 952 (2009).

[4] O. Tal, Y. Rosenwaks, Y. Preezant, N. Tessler, C. K. Chan, and A. Kahn, Direct Determination of the Hole Density of States in Undoped and Doped Amorphous Organic Films with High Lateral Resolution, Phys. Rev. Lett. **95**, 256405 (2005).

[5] F. Bussolotti, S. Kera, and N. Ueno, Potassium doping of single crystalline pentacene thin film, Phys. Rev. B **86**, 155120 (2012).

[6] J. Pflaum, J. Niemax, and A. K. Tripathi, Chemical and structural effects on the electronic transport in organic single crystals, Chem. Phys. **325**, 152 (2006).

[7] J. Sworakowski, Effect of Dipolar Arrays on the Localization of Charge Carriers in Molecular Materials, IEEE Trans. Dielectr. Electr. Insul. **7**, 531 (2000).

[8] J. P. Sleigh, D. P. McMahon, and A. Troisi, Effect of the intermolecular thermal motions on the tail of the electronic density of states in polyacene crystals, Appl. Phys. A **95**, 147 (2009).

[9] D. P. McMahon and A. Troisi, Organic semiconductors: Impact of disorder at different timescales, ChemPhysChem **11**, 2067 (2010).

[10] S. Fratini, D. Mayou, and S. Ciuchi, The transient localization scenario for charge transport in crystalline organic materials, Adv. Funct. Mater. **26**, 2292 (2016).

[11] D. Venkateshvaran, M. Nikolka, A. Sadhanala, V. Lemaur, M. Zelazny, M. Kepa, M. Hurhangee, A. J. Kronemeijer, V. Pecunia, I. Nasrallah, I. Romanov, K. Broch, I. McCulloch, D. Emin, Y. Olivier, J. Cornil, D. Beljonne, and H. Sirringhaus, Approaching disorder-free transport in high-mobility conjugated polymers, Nature **515**, 384 (2014).

[12] R. Häusermann, K. Willa, B. Blülle, T. Morf, A. Facchetti, Z. Chen, J. Lee, and B. Batlogg, Device performance and density of trap states of organic and inorganic field-effect transistors, Org. Electron. **28**, 306 (2016).

[13] R. Häusermann and B. Batlogg, Gate bias stress in pentacene field-effect-transistors: Charge trapping in the dielectric or semiconductor, Appl. Phys. Lett. **99**, 083303 (2011).

[14] M. Oehzelt, N. Koch, and G. Heimel, Organic semiconductor density of states controls the energy level alignment at electrode interfaces, Nat. Commun. **5**, 4174 (2014).

[15] W. Shockley and W. T. Read, Statistics of the recombinations of holes and electrons, Phys. Rev. **87**, 835 (1952).

[16] M. Kuik, L. J. A. Koster, G. A. H. Wetzelaer, and P. W. M. Blom, Trap-assisted Recombination in Disordered Organic Semiconductors, Phys. Rev. Lett. **107**, 256805 (2011).

[17] R. A. Street, Localized state distribution and its effect on recombination in organic solar cells, Phys. Rev. B **84**, 075208 (2011).

[18] F. Bussolotti, J. Yang, M. Hiramoto, T. Kaji, S. Kera, and N. Ueno, Direct detection of density of gap states in C60 single crystals by photoemission spectroscopy, Phys. Rev. B **92**, 115102 (2015).

[19] J.-P. Yang, F. Bussolotti, S. Kera, and N. Ueno, Origin and role of gap states in organic semiconductor studied by UPS: As the nature of organic molecular crystals, J. Phys. D **50**, 423002 (2017).

[20] S. Yogev, R. Matsubara, M. Nakamura, U. Zschieschang, H. Klauk, and Y. Rosenwaks, Fermi Level Pinning by Gap States in Organic Semiconductors, Phys. Rev. Lett. **110**, 036803 (2013).

[21] V. Palermo, M. Palma, and P. Samori, Electronic characterization of organic thin films by Kelvin probe force microscopy, Adv. Mater. **18**, 145 (2006).

[22] W. L. Kalb and B. Batlogg, Calculating the trap density of states in organic field-effect transistors from experiment: A comparison of different methods, Phys. Rev. B **81**, 035327 (2010).

[23] S. H. Jeong and C. K. Song, Energetic distribution of interface states extracted from photo-conductance of organic thin film transistors, Org. Electron. **15**, 2599 (2014).

[24] K. Lee, M. S. Oh, S. J. Mun, K. H. Lee, T. W. Ha, J. H. Kim, S. H. K. Park, C. S. Hwang, B. H. Lee, M. M. Sung, and S. Im, Interfacial trap density-of-states in pentacene-and ZnO-based thin-film transistors measured via novel photo-excited charge-collection spectroscopy, Adv. Mater. **22**, 3260 (2010).

[25] H. Matsui, A. S. Mishchenko, and T. Hasegawa, Distribution of Localized States from Fine Analysis of Electron Spin Resonance Spectra Inorganic Transistors, Phys. Rev. Lett. **104**, 056602 (2010).

[26] A. Shaw, J. D. Jin, I. Z. Mitrovic, S. Hall, J. S. Wrench, and P. R. Chalker, Extraction of the sub-band gap density of states of Nb doped ZnO thin film transistors using C-V measurements, Microelectron. Eng. **178**, 213 (2017).

[27] M. Grünewald, P. Thomas, and D. Würtz, A Simple Scheme for Evaluating Field Effect Data, Phys. Status Solidi B **100**, K39 (1980).

[28] M. Grünewald, P. Thomas, and D. Würtz, Field effect studies on a-Si:H films, J. Phys. Colloq. **42**, 532 (1981).

[29] K. Weber, M. Grünewald, W. Fuhs, and P. Thomas, Field effect in a-Si:H films, Phys. Status Solidi B **130**, 133 (1982).

[30] W. L. Kalb, F. Meier, K. Mattenberger, and B. Batlogg, Defect healing at room temperature in pentacene thin films and improved transistor performance, Phys. Rev. B **76**, 184112 (2007).

[31] W. L. Kalb, K. Mattenberger, and B. Batlogg, Oxygen-related traps in pentacene thin films: Energetic position and implications for transistor performance, Phys. Rev. B **78**, 035334 (2008).

[32] P. Pattanasattayavong, A. D. Mottram, F. Yan, and T. D. Anthopoulos, Study of the Hole Transport Processes in Solution-Processed Layers of the Wide Bandgap Semiconductor Copper(I)Thiocyanate (CuSCN), Adv. Funct. Mater. **25**, 6802 (2015).

[33] P. J. Diemer, Z. A. Lamport, Y. Mei, J. W. Ward, K. P. Goetz, W. Li, M. M. Payne, M. Guthold, J. E. Anthony, and O. D. Jurchescu, Quantitative analysis of the density of trap states at the semiconductor-dielectric interface in organic field-effect transistors, Appl. Phys. Lett. **107**, 103303 (2015).

[34] S. Hunter, A. D. Mottram, and T. D. Anthopoulos, Temperature and composition-dependent density of states in organic small-molecule/polymerblend transistors, J. Appl. Phys. **120**, 025502 (2016).

[35] N. K. Za'aba, J. J. Morrison, and D. M. Taylor, Effect of relative humidity and temperature on the stability of DNTT transistors: A density of states investigation, Org. Electron. **45**, 174 (2017).

[36] P. Pattanasattayavong, V. Promarak, and T. D. Anthopoulos, Electronic properties of copper(I) thiocyanate (CuSCN), Adv. Electron. Mater. **3**, 1600378 (2017).

[37] P. J. Diemer, A. F. Harper, M. R. Niazi, A. J. Petty, J. E. Anthony, A. Amassian, and O. D. Jurchescu, Laser-printed organic thin-film transistors, Adv. Mater. Technol. **2**, 1700167 (2017).

[38] J. Jeong, J. K. Jeong, J. S. Park, Y. G. Mo, and Y. Hong, Meyer-neldel rule and extraction of density of states in amorphous indium-gallium-zinc-oxide thin-film transistor by considering surface band bending, Jpn. J. Appl. Phys. **49**, 0 (2010).

[39] R. Hofmockel, U. Zschieschang, U. Kraft, R. Rödel, N. H. Hansen, M. Stolte, F. Würthner, K. Takimiya, K. Kern, J. Pflaum, and H. Klauk, High-mobility organic thin-film transistors based on a small-molecule semiconductor deposited in vacuum and by solution shearing, Org. Electron. **14**, 3213 (2013).

[40] U. Zschieschang, F. Ante, M. Schlörholz, M. Schmidt, K. Kern, and H. Klauk, Mixed self-assembled monolayer gate dielectrics for continuous threshold voltage control in organic transistors and circuits, Adv. Mater. **22**, 4489 (2010).

[41] K. Niimi, M. J. Kang, E. Miyazaki, I. Osaka, and K. Takimiya, General synthesis of dinaphtho[2,3- b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) derivatives, Org. Lett. **13**, 3430 (2011).

[42] T. Yokota, K. Kuribara, T. Tokuhara, U. Zschieschang, H. Klauk, K. Takimiya, Y. Sadamitsu, M. Hamada, T. Sekitani, and T. Someya, Flexible low-voltage organic transistors with high thermal stability at 250 °C, Adv. Mater. **25**, 3639 (2013).

[43] P. Ortiz, A. Facchetti, and T. J. Marks, High-k organic, inorganic, and hybrid dielectrics for low-voltage organic field-effect transistors, Chem. Rev. **110**, 205 (2010).

[44] S. Sze and K. Ng, *Physics of Semiconductor Devices* (Wiley, New York, 2006), p. 203 ff.

[45] https://docs.scipy.org/doc/scipy/reference/generated/scipy.integrate.odeint.html, [Online; accessed 18-July-2018].

[46] S. D. Baranovskii, Theoretical description of charge transport in disordered organic semiconductors, Phys. Status Solidi B **251**, 487 (2014).

[47] S. D. Baranovskii, T. Faber, F. Hensel, and P. Thomas, The applicability of the transport-energy concept to various disordered materials, J. Phys. Condens. Matter **9**, 2699 (1997).

[48] H. Sirringhaus, T. Sakanoue, and J. F. Chang, Charge-transport physics of high-mobility molecular semiconductors, Phys. Status Solidi B **249**, 1655 (2012).

[49] H. H. Berger, Contact Resistance and Contact Resistivity, J. Electrochem. Soc. **119**, 507 (1972).

[50] G. K. Reeves and H. B. Harrison, Obtaining the Specific Contact Resistance from Transmission Line Model Measurements, IEEE Electron Device Lett. **3**, 111 (1982).

[51] See Supplemental Material http://link.aps.org/supplemental/10.1103/PhysRevApplied.10.044023 for output characteristics, transfer characteristics in the saturation regime and details on the transmission line method.

Supplemental Material: Quantitative Analysis of the Density of Trap States in Semiconductors by Electrical Transport Measurements on Low-Voltage Field-Effect Transistors

Michael Geiger,[1,*] Lukas Schwarz,[1] Ute Zschieschang,[1] Dirk Manske,[1]
Jens Pflaum,[2] Jürgen Weis,[1] Hagen Klauk,[1,†] and Ralf Thomas Weitz[3,4]

[1] *Max Planck Institute for Solid State Research, Heisenbergstraße 1, 70569 Stuttgart, Germany*

[2] *Experimental Physics VI, Julius Maximilian University, Am Hubland, 97074 Würzburg, Germany*

[3] *AG Physics of Nanosystems, Faculty of Physics, Ludwig Maximilians University, Amalienstraße 54, 80799 München, Germany*

[4] *NanoSystems Initiative Munich (NIM) and Center for NanoScience (CeNS), Ludwig Maximilians University, Schellingstraße 4, 80799 München, Germany*

(Dated: August 22, 2018)

* E-mail address: M.Geiger@fkf.mpg.de

† E-mail address: H.Klauk@fkf.mpg.de

OUTPUT CHARACTERISTICS

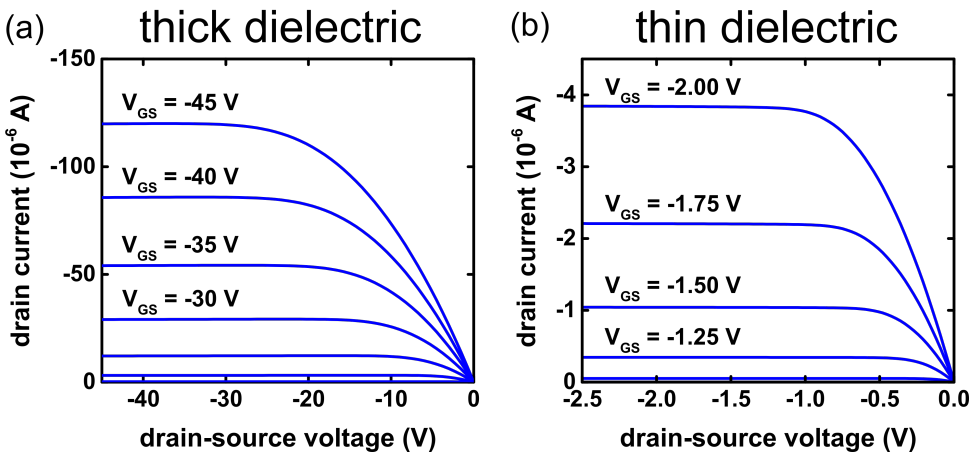


FIG. S1. Measured output characteristics of the transistors with the 110-nm-thick gate dielectric (a) and the 5.3-nm-thick gate dielectric (b).

TRANSFER CHARACTERISTICS IN THE SATURATION REGIME

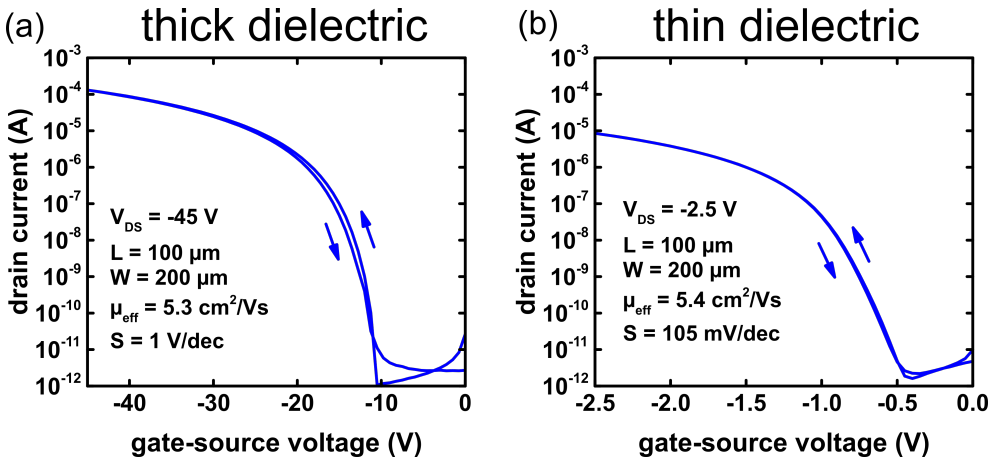


FIG. S 2. Transfer curves measured on the TFTs with a 110-nm-thick gate dielectric (a) and a 5.3-nm-thick gate dielectric (b). The transfer curves were measured in the saturation regime of operation.

TRANSMISSION LINE METHOD

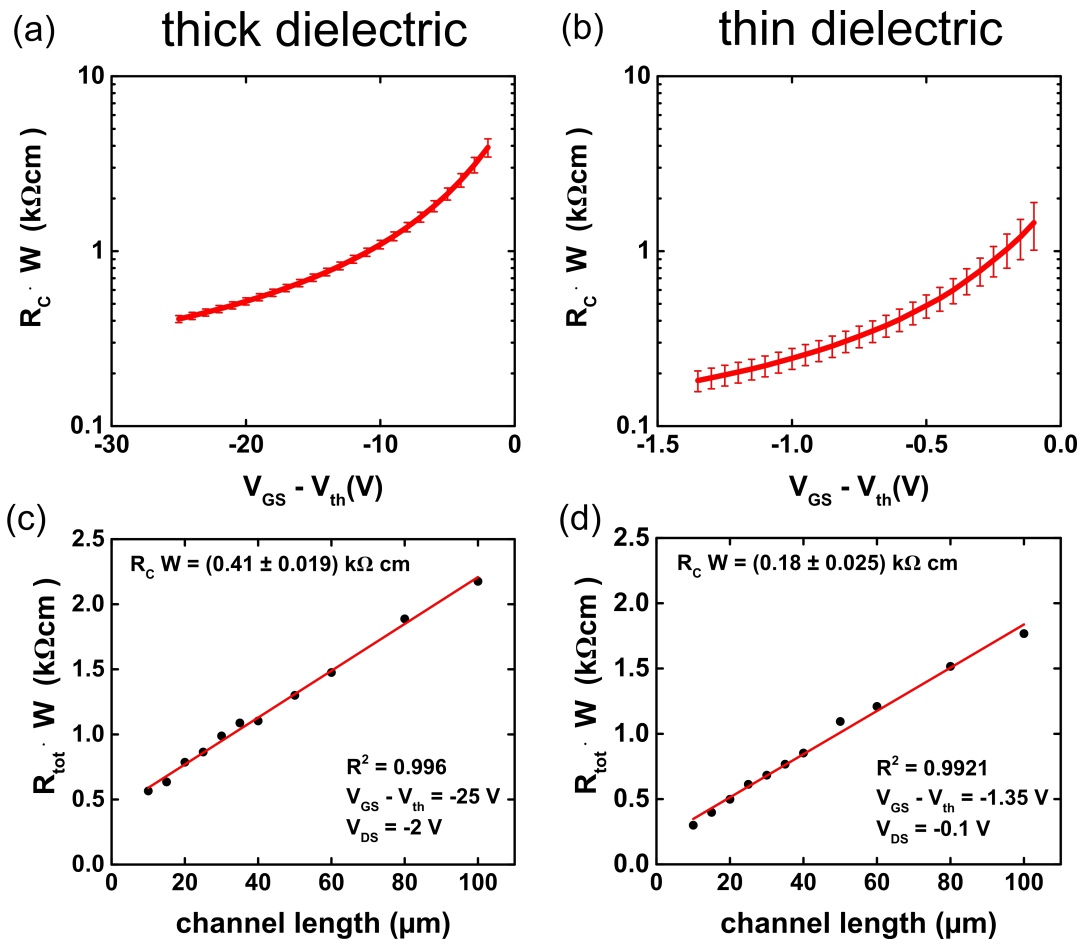


FIG. S3. Channel-width-normalized contact resistance ($R_C \cdot W$) measured using the transmission line method and plotted as a function of the difference between the gate-source voltage and the threshold voltage (V_{GS} - V_{th}) for the TFTs with the 110-nm-thick gate dielectric (a) and the 5.3-nm-thick gate dielectric (b). Exemplary results of the channel-width-normalized total resistance ($R_{tot} \cdot W$) as a function of the channel length for the TFTs with the 110-nm-thick gate dielectric (c) and the 5.3-nm-thick gate dielectric (d).

Chapter 4

Effect of the Degree of the Gate-Dielectric Surface Roughness on the Performance of Bottom-Gate Organic Thin-Film Transistors

4.1 Discussion

4.1.1 State-of-the-Art

The possibility to deposit organic semiconductors at relatively low temperatures (typically below 100 °C) makes it possible to use unconventional substrate materials. A suitable class of substrate materials for future flexible electronics applications are flexible polymeric substrates. Polyethylene naphthalate (PEN) and polyethylene terephthalate (PET) are representative examples and have been established as reliable and robust substrates for flexible organic TFTs.[7,100–102] Moreover, there are a variety of other exotic substrate materials which can be inexpensive, flexible, stretchable, biocompatible, biodegradable or lightweight, typical examples are paper or fabric.[9–12] Employing such exotic substrates offers opportunities for novel applications and implementing electronics in unusual environments, but at the same time the use of such substrate materials is combined with an issue: Typically these unconventional substrate materials exhibit a large degree of surface roughness. Silicon wafers are conventional substrate materials which are virtually unrivaled in terms of surface roughness and can be manufactured to a degree in which the surface is atomically smooth.[103] Also glass substrates for display applications can be manufactured with an outstanding quality and exhibit root-mean-square roughness values of less than 1 nm.[104–106] In contrast, the surface roughness of unconventional flexible substrates is significantly larger, depending on the employed fabrication technique and the characteristic building blocks of the material (e.g. polymer chains, cellulose fibers, or protein filaments). Typically the surface roughness is transmitted through the subsequently deposited layers of the organic TFT and thus affects critical layers such as the semiconductor

layer and the gate dielectric/semiconductor interface. In the past, many reports showed that a large surface roughness of the substrate material can have detrimental effects on the electrical performance of organic TFTs.[60,61,107–111] Usually, to investigate the effect of the surface roughness on the transistor performance, different materials with a different degree of surface roughness were employed. However, the use of different materials does not only affect the roughness values, but typically also affects other materials properties such as the permittivity, the thermal expansion coefficient and the thermal diffusivity (the latter two are especially important if the semiconductor is deposited at elevated temperatures of the substrate). Thus, the disentanglement of all contributing effects and isolating the effect of the surface roughness can be difficult.

4.1.2 Objective

The scope of this work is to contribute to the understanding of the influence of surface roughness on the performance of organic TFTs and gain a deeper understanding of the underlying mechanisms. The basis for this study is the development of a method to tune the degree of the surface roughness of the gate dielectric in organic bottom-gate TFTs in a systematic and and isolated manner for a wide range of roughness values. Keeping all other materials parameters constant is essential, as it is ensured that all observed differences in the TFT performance can be ascribed to effects related to the surface roughness. A special focus in this study lies on the relationship between the surface roughness of the gate dielectric and the morphology of the semiconductor layer.

4.1.3 Conclusion

In this study, a method to vary the degree of the surface roughness of the gate dielectric in bottom-gate organic TFTs was developed. By controlling the substrate temperature during the aluminum deposition it was possible to fabricate aluminum films with varying degrees of surface roughness. Atomic force microscopy (AFM) measurements revealed that the lateral aluminum grain size and the surface roughness of the aluminum film increase with increasing substrate temperature. The root-mean-square roughness was tuned systematically over a range of one order of magnitude and it was shown that the roughness is preserved after exposing the aluminum film to an oxygen plasma and depositing the SAM molecules. This means that the surface roughness of the hybrid AlO_x/SAM gate dielectrics was tuned without using different materials, layer thicknesses or process conditions except the substrate temperature during the deposition of the aluminum gate electrodes. Thus, a suitable model system is developed and any difference in the measured TFT performance can be safely ascribed to effects related solely to the difference in the surface roughness.
Electrical transport measurements on bottom-gate DNTT TFTs based on gate dielectrics with a different degree of surface roughness showed that the effective mobility decreases and the subthreshold swing increases substantially with increasing surface roughness. The application of the extended Grünewald method (developed in Chapter 3) revealed an increase in the trap DOS of the semiconductor with an increased surface roughness of the

dielectric. By means of AFM analysis, the grain density in the DNTT layer was determined and a clear correlation between the surface roughness and the grain density in the DNTT layer was observed. This indicates that the increase in surface roughness hinders the growth of the semiconductor with extended terrace-like structures, but leads to the formation of many small grains and thus to an increase in the density of grain boundaries. In the next step, the density of grain boundaries was disentangled from other types of structural disorder in the semiconductor layer which might be induced by the surface roughness and affect the TFT performance. It was shown that it is possible to tune the grain density in the DNTT layer independent of the surface roughness of the gate dielectric by controlling the substrate temperature during the DNTT deposition. The electrical characteristics of the TFTs in which the grain density of the DNTT was tuned by manipulating the surface roughness of the gate dielectric and the TFTs in which the grain density of the DNTT was tuned by adjusting the substrate temperature during the DNTT deposition coincide remarkably well for both sets of TFTs. Analyzing the results suggests that grain boundaries are indeed the most important type of structural defect which is induced by a large surface roughness. X-ray diffraction (XRD) measurements on DNTT films deposited onto gate dielectrics with a different degree of surface roughness confirmed that the internal morphology of the DNTT grains is not significantly affected by the surface roughness. The presented study indicates that grain boundaries in the semiconductor layer, are the major structural defect induced by the surface roughness of the dielectric and severely diminish lateral charge transport in the semiconductor layer. These results stress the significance of a small surface roughness of the gate dielectric for bottom-gate organic TFTs.

4.2 Published Article

Effect of the Degree of the Gate-Dielectric Surface Roughness on the Performance of Bottom-Gate Organic Thin-Film Transistors

Michael Geiger[1], Rachana Acharya[1], Eric Reutter[1], Thomas Ferschke[2,3], Ute Zschieschang[1], Jürgen Weis[1], Jens Pflaum[2,3], Hagen Klauk[1], R. Thomas Weitz[4,5]

[1] *Max Planck Institute for Solid State Research, Heisenbergstr. 1, 70569 Stuttgart, Germany*
[2] *Experimental Physics IV, Julius Maximilian University, Am Hubland, 97074 Würzburg, Germany*
[3] *Bavarian Center for Applied Energy Research (ZAE Bayern e.V.), Magdalena-Schoch-Str. 3, 97074 Würzburg, Germany*
[4] *AG Physics of Nanosystems, Faculty of Physics, Ludwig Maximilians University, Amalienstr. 54, 80799 München, Germany*
[5] *1st Institute of Physics, Faculty of Physics, University of Göttingen, Friedrich-Hund-Platz 1, 37077 Göttingen, Germany*

***Advanced Materials Interfaces* 7, 1902145 (2020)**

DOI: 10.1002/admi.201902145

reprinted on pages 45–62

FULL PAPER

ADVANCED MATERIALS INTERFACES
www.advmatinterfaces.de

Effect of the Degree of the Gate-Dielectric Surface Roughness on the Performance of Bottom-Gate Organic Thin-Film Transistors

Michael Geiger, Rachana Acharya, Eric Reutter, Thomas Ferschke, Ute Zschieschang, Jürgen Weis, Jens Pflaum, Hagen Klauk,* and Ralf Thomas Weitz*

In organic thin-film transistors (TFTs) fabricated in the inverted (bottom-gate) device structure, the surface roughness of the gate dielectric onto which the organic-semiconductor layer is deposited is expected to have a significant effect on the TFT characteristics. To quantitatively evaluate this effect, a method to tune the surface roughness of a gate dielectric consisting of a thin layer of aluminum oxide and an alkylphosphonic acid self-assembled monolayer over a wide range by controlling a single process parameter, namely the substrate temperature during the deposition of the aluminum gate electrodes, is developed. All other process parameters remain constant in the experiments, so that any differences observed in the TFT performance can be confidently ascribed to effects related to the difference in the gate-dielectric surface roughness. It is found that an increase in surface roughness leads to a significant decrease in the effective charge-carrier mobility and an increase in the subthreshold swing. It is shown that a larger gate-dielectric surface roughness leads to a larger density of grain boundaries in the semiconductor layer, which in turn produces a larger density of localized trap states in the semiconductor.

1. Introduction

Organic thin-film transistors (TFTs) are promising devices to be employed in future flexible, large-area electronics applications, such as active-matrix displays and sensor arrays.[1–3] The possibility to deposit organic semiconductors at relatively low temperatures makes it possible to fabricate organic TFTs on unconventional substrate materials, such as glass,[4,5] plastic foils,[6–8] textiles,[9] or paper.[10,11] The use of these substrate materials offers opportunities for a variety of novel applications, but they are usually characterized by a larger surface roughness than conventional substrate materials, and this can have detrimental effects on the performance of the devices.[12–26]

In this work we study the impact of the surface roughness of the gate dielectric on the electrical performance of bottom-gate organic TFTs. As model organic semiconductor, we employ the small-molecule semiconductor dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT[27]), since its unique combination of electrical performance and long-term stability makes it ideally suited for this investigation.[28–31]

Since the current–voltage characteristics of organic TFTs depend on various parameters other than the surface roughness,[32,33] it is important that the only parameter we vary in our experiments is the surface roughness, as simultaneous changes in other parameters might obscure the effect we intend to investigate. All TFTs were thus fabricated using the same materials, the same layer thicknesses, and the same process conditions, with one exception, namely the substrate temperature during the deposition of the aluminum gate electrodes (in order to analyze the impact of the surface roughness) or the substrate temperature during the deposition of the organic semiconducting layer (in order to disentangle the relations between the surface roughness of the gate dielectric, the grain density of the semiconductor layer, and the density of trap states in the organic-semiconductor layer). By varying the substrate temperature during the aluminum deposition we are able to tune the surface roughness of the gate electrode and thereby the surface roughness of the gate dielectric over approximately one order of magnitude without having to change any other process parameters, so that any differences observed in the TFT

M. Geiger, R. Acharya, E. Reutter, Dr. U. Zschieschang, Prof. J. Weis, Dr. H. Klauk
Max Planck Institute for Solid State Research
Heisenbergstr. 1, Stuttgart 70569, Germany
E-mail: M.Geiger@fkf.mpg.de; H.Klauk@fkf.mpg.de
T. Ferschke, Prof. J. Pflaum
Experimental Physics VI
Julius-Maximilians-University Würzburg
Am Hubland, Würzburg 97074, Germany
Prof. J. Pflaum
Bavarian Center for Applied Energy Research (ZAE Bayern e.V.)
Magdalena-Schoch-Straße 3, Würzburg 97074, Germany
Prof. R. T. Weitz
AG Physics of Nanosystems
Faculty of Physics
Ludwig Maximilians University
Amalienstraße 54, München 80799, Germany
Prof. R. T. Weitz
1st Physical Institute
Faculty of Physics
University of Göttingen
Friedrich-Hund-Platz 1, Göttingen 37077, Germany
The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/admi.201902145.

DOI: 10.1002/admi.201902145

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED MATERIALS INTERFACES
www.advmatinterfaces.de

performance can be safely ascribed to differences in the gate-dielectric surface roughness. By varying the substrate temperature during the DNTT deposition we can control the density of grain boundaries in the DNTT layer independent of the gate-dielectric surface roughness.

2. Results and Discussion

2.1. Gate-Dielectric Surface Roughness

To fabricate TFTs with different degrees of gate-dielectric surface roughness, we prepared a set of eight substrates in which we modified the surface roughness of the aluminum gate electrodes by controlling the substrate temperature during the aluminum deposition. The surface of the aluminum was then oxidized by brief exposure to an oxygen plasma, and the resulting aluminum oxide layer (AlO_X) was then covered with an alkylphosphonic acid self-assembled monolayer (SAM). Due to the fact that the formation of these layers proceeds in a conformal manner, the surface roughness of the aluminum translates directly into the surface roughness of the AlO_X/SAM gate dielectric, as will be shown. A schematic cross section of the TFTs and the chemical structures of *n*-tetradecylphosphonic acid and DNTT are shown in **Figure 1**. The composition of the AlO_X in the gate dielectric is discussed in Section S1, Supporting Information.

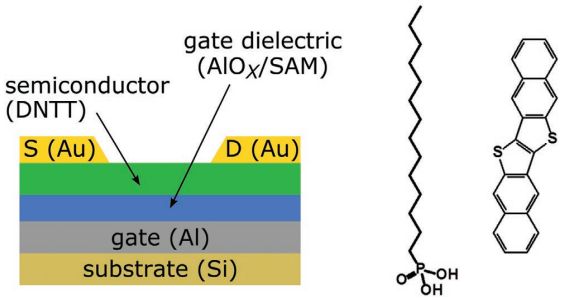


Figure 1. Schematic cross-section of the organic TFTs and chemical structures of *n*-tetradecylphosphonic acid for the gate-dielectric SAM and the organic semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT).

Using atomic force microscopy (AFM), we measured the surface roughness of the aluminum gate electrodes and of the AlO_X/SAM gate dielectrics. **Figure 2**a–c shows AFM images of AlO_X/SAM gate dielectrics fabricated on aluminum gate electrodes deposited at substrate temperatures of 20, 70, and 110 °C. As can be seen, the substrate temperature during the deposition of the aluminum gate electrodes has a significant influence on the morphology of the aluminum films and hence on their root-mean-square surface roughness R_{RMS}. With increasing substrate temperature, both the lateral aluminum grain size and the surface roughness increase. In Figure 2d, the measured surface roughness is plotted as a function of the

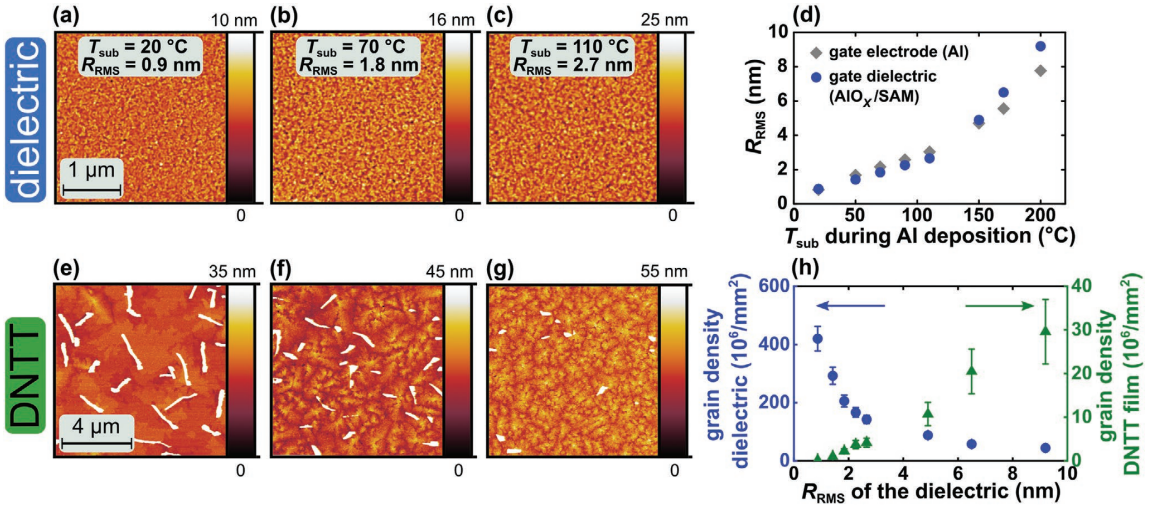


Figure 2. a–c) AFM images of AlO_X/SAM gate dielectrics fabricated on aluminum gate electrodes deposited at substrate temperatures of 20, 70, and 110 °C. d) Root-mean-square surface roughness of aluminum gate electrodes (gray symbols) and AlO_X/SAM gate dielectrics (blue symbols) plotted as a function of the substrate temperature during the aluminum deposition. A higher substrate temperature results in a larger surface roughness of the aluminum which translates directly into a larger gate-dielectric surface roughness. e–g) AFM images of DNTT films deposited onto the gate dielectrics shown in panels (a)–(c) at a substrate temperature of 60 °C. A larger surface roughness of the gate dielectric leads to a terrace structure of strongly reduced terrace size in the DNTT films and a larger grain density. The tall, elongated features seen in the AFM images are crystalline structures with a height of several tens of nanometers that form spontaneously during the organic-semiconductor deposition.[45] h) Grain densities of the aluminum gate electrodes and of the DNTT films plotted as a function of the surface roughness of the gate dielectric. The grain density was determined using the Watershed Algorithm implemented in the AFM analysis software Gwyddion.

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED MATERIALS INTERFACES
www.advmatinterfaces.de

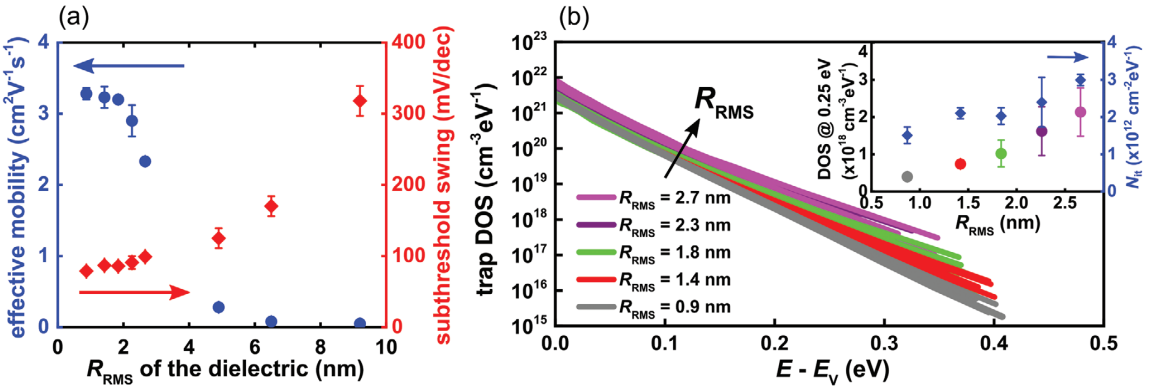


Figure 3. a) Effective charge-carrier mobility extracted in the linear regime of operation and subthreshold swing of the DNTT TFTs plotted as function of the surface roughness of the gate dielectric. b) Density of trap states (trap DOS) in the organic semiconductor plotted as function of the energy above the valence-band energy E_V. The inset shows the value of the trap DOS at an energy of 0.25 eV above the valence-band energy as a function of the surface roughness of the gate dielectric as well as the interface trap density, N_{it}, calculated from the subthreshold swing.

substrate temperature during the aluminum deposition for the complete set of substrates. The gray and blue data points represent the surface roughness R_{RMS} of the aluminum gate electrodes and of the AlO_X/SAM gate dielectrics, respectively. As can be seen, the surface roughness of the gate dielectric is essentially identical to that of the aluminum gate electrode on which the gate dielectric is fabricated, which confirms that the formation of the AlO_X/SAM gate dielectric occurs in a correlated manner. The surface roughness of the gate electrodes and the gate dielectric increases monotonically from 0.9 to 9.2 nm as the substrate temperature during the aluminum deposition is increased from 20 to 200 °C. A similar relation between the surface roughness of aluminum films and the temperature during the aluminum deposition was previously reported by Z. Li et al. during the deposition of significantly thicker aluminum films by electron-beam evaporation for the fabrication of high-quality Echelle gratings.[34]

The observed dependence of the surface roughness of the aluminum films on the substrate temperature during the aluminum deposition can be explained by considering the processes of nucleation and coalescence of the aluminum atoms on the substrate surface. During deposition, the aluminum adatoms rapidly reach thermal equilibrium with the surface, diffuse on the surface, and interact to form immobile polyatomic clusters which will act as seeds for the subsequent formation of the aluminum grains.[35,36] A higher substrate temperature enhances the surface diffusion of the adatoms, which results in the requirement for a larger critical size of the stable nuclei, resulting in a larger surface roughness.[34,37,38] The plasma-generated aluminum oxide layer and the alkylphosphonic acid SAM follow the surface topology of the aluminum films, as is evident from the correlated surface roughness seen in Figure 2d. With this simple approach, the surface roughness can be tuned continuously over approximately an order of magnitude without the need to vary any other process parameters. In particular, it is not necessary to use different materials or to perform any post-process modifications to any of the layers in order to produce different degrees of surface roughness, which is an important benefit, because such modifications might affect the TFT performance in other ways and thereby obscure the surface-roughness effect of interest.

2.2. Electrical TFT Characteristics and Trap-State Density

On each substrate, DNTT TFTs with the same dimensions were fabricated. Their transfer and output characteristics are shown in Figures S2 and S3, Supporting Information. The extracted effective charge-carrier mobilities and subthreshold swings are summarized in **Figure 3**a. With increasing surface roughness, the effective mobility decreases substantially from (3.3 ± 0.8)cm^2 V^{-1} s^{-1} on the smoothest substrate to (0.05 ± 0.01)cm^2 V^{-1} s^{-1} on the roughest substrate. The subthreshold swing increases from (79 ± 3)mV dec^{-1} on the smoothest substrate to (320 ± 21)mV dec^{-1} on the roughest substrate. We have applied the extended Grünewald method to extract the density of trap states (trap DOS) in the organic-semiconductor layer from the measured transfer curves of the TFTs in the linear regime of operation.[39] We were able to apply this method only to the TFTs on the five smoothest substrates, since the TFTs on the three rougher substrates do not meet the criteria for a meaningful extraction of the trap DOS from the transfer curves of the TFTs. The results are summarized in Figure 3b where the trap DOS in the semiconductor is plotted as a function of the energy relative to the valence-band edge for the five smoothest substrates. The characteristic decay of the trap DOS into the band gap is in agreement with other reports on vacuum-deposited films of the organic semiconductor DNTT.[40,41] The results in Figure 3b show a clear correlation between the surface roughness of the gate dielectric and the density of trap states in the organic semiconductor layer. **Figure 4** illustrates the general view of how the roughness of the underlying surface (in this case of the gate dielectric) affects the growth and morphology of the organic semiconductor layer by increasing the degree of structural disorder.

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED MATERIALS INTERFACES
www.advmatinterfaces.de

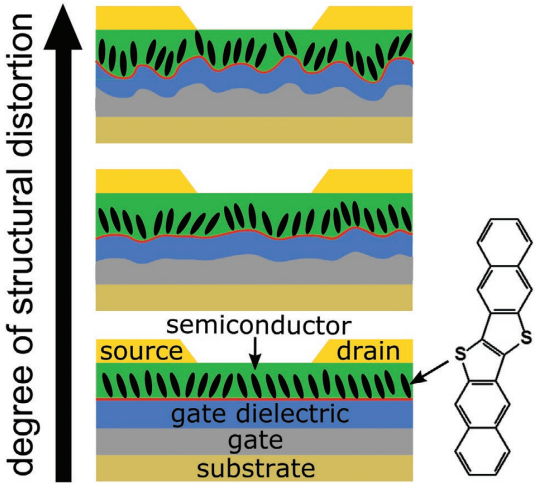


Figure 4. A rough gate electrode correlates with a rough gate dielectric and introduces structural distortion in the semiconductor film. This structural distortion, represented mainly by grain boundaries and their density, leads to the formation of transport barriers and trap states that have a detrimental effect on the electric characteristics of the TFTs.

2.3. Organic-Semiconductor Morphology

As initially proposed by Anderson, among the factors that can cause the localization of charge carriers in a semiconductor is structural disorder.[42] In organic semiconductors, intermolecular interactions are comparatively weak and the transfer integrals are typically small and susceptible to small differences in molecular position or orientation, so these materials are especially prone to the formation of trap states due to structural disorder. One manifestation of the degree of structural disorder in organic semiconductors is the density of grain boundaries. The influence of the gate-dielectric surface roughness on the thin-film morphology and the grain density of the vacuum-deposited DNTT films can be seen in Figure 2e–g: Depositing the DNTT onto a smooth gate dielectric leads to a step-flow growth and thus to an extended terrace-like structure, which is the structure typically reported for many small-molecule organic semiconductors deposited by vacuum sublimation,[43–45] whereas a rough gate dielectric hinders this growth mode and thus induces less extended terrace-like structures correlated with a larger density of smaller domains. This trend is in agreement with observations reported previously for other small-molecule organic semiconductors, such as pentacene, and can be ascribed to a smaller diffusion length of the molecules when deposited onto a rougher surface.[46] The larger grain density in the semiconductor layer observed on rougher surfaces corresponds to a larger density of grain boundaries. In organic semiconductors, grain boundaries are the most important type of structural defect at the micrometer and sub-micrometer length scale. Energy barriers emerging at the grain boundaries and trap states located there are often reported to be a major obstacle for efficient charge transport.[47–51] We have also observed that the effective charge-carrier mobility and the subthreshold swing correlate with the density of grain boundaries imaged by AFM, but it should be noted that AFM reveals only the surface of the organic semiconductor layer, whereas the charge transport occurs mainly in the first molecular monolayer near the interface to the gate dielectric, that is, at a depth that cannot be probed directly by AFM and where structural or chemical inhomogeneities on smaller length scales affecting the charge transport might exist. Due to the weak van der Waals bonding, organic semiconductors are susceptible to imperfect molecular packing and local defects.[52] It has been calculated that even in macroscopically ordered regions of an organic-semiconductor film, local defects induced along the less strongly bound molecular gliding planes lead to the formation of shallow trap states that significantly impede charge transport.[53–56]

In order to disentangle the influence of the density of grain boundaries in the semiconductor layer on the TFT characteristics from the influence of other types of structural disorder, we fabricated a second set of substrates in which we tuned the grain density in the DNTT layer independently of the surface roughness of the gate dielectric. All four substrates in this series were fabricated at the same substrate temperature during the aluminum deposition (20 °C), so that all substrates have the same small gate-dielectric surface roughness. During the DNTT deposition, the substrate was held at a temperature of 20, 40, 60, or 80 °C in order to obtain a different grain density on each substrate. As can be seen in **Figure 5**a, the influence of the substrate temperature during the DNTT deposition on the grain density is quite similar to that of the surface roughness of the gate dielectric. By comparing the electrical characteristics of the TFTs from the first set of substrates (for which the grain density was tuned indirectly by manipulating the surface roughness of the gate dielectric) with those from the second set of substrates (for which the grain density was tuned directly by adjusting the substrate temperature during the DNTT deposition), the importance of the density of grain boundaries relative to other types of disorder induced, for instance, by the gate-dielectric surface roughness can be analyzed in more detail. As seen in Figure 5b,c, the trends and absolute values of the effective mobility and of the subthreshold swing coincide remarkably well for both sets of substrates. We also applied the extended Grünewald method to the TFTs from the second set of substrates to extract the trap DOS. Figure 5d shows that the relation between the grain density and the trap DOS is very similar for the two sets of substrates. These results suggest that the grain boundaries are indeed the most important type of structural defect in DNTT films, regardless of whether they are induced by the surface roughness of the gate dielectric or by the substrate temperature during the DNTT deposition. Contributions by other types of structural imperfections cannot be ruled out, but appear to be less significant.

To quantify the influence of the gate-dielectric surface roughness on the microstructure of the DNTT films in more detail and, complementary to the local AFM analysis, in an integral manner, we have performed X-ray diffraction (XRD) measurements on DNTT films deposited onto AlO_X/SAM gate dielectrics with a surface roughness of 1.0, 2.2, 4.9, and 7.0 nm, respectively. The results are shown in **Figure 6**; Figure S8, Supporting Information. The first-order Bragg peak is located at a reciprocal scattering length of 0.385Å^{-1}, which is in agreement with the value expected for DNTT and its (001) out-of-plane

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED MATERIALS INTERFACES
www.advmatinterfaces.de

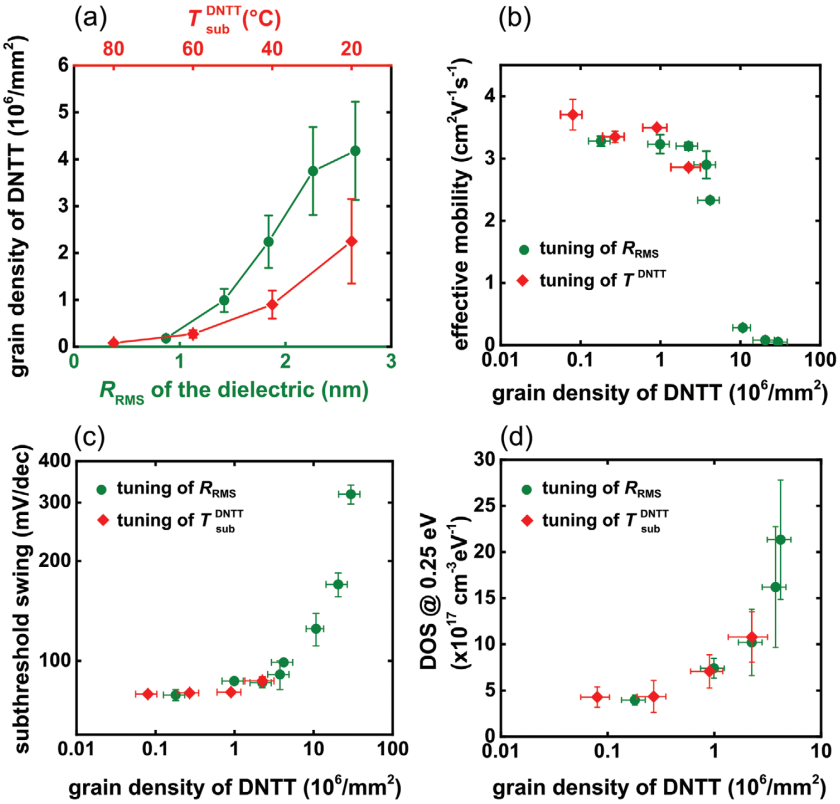


Figure 5. a) Grain densities of DNTT films plotted as a function of the roughness of the gate dielectric and as a function of the substrate temperature during the DNTT deposition. b) Effective carrier mobility and c) subthreshold swing of the TFTs of the two sets of substrates in which the grain density of DNTT was tuned by two different methods. d) Trap DOS at an energy of 0.25 eV above the valence-band edge, determined by the extended Grünewald method. The increase of the trap-state density with increasing grain density is analogous for both sets of substrates.

lattice spacing of 16.19Å.[57] With increasing gate-dielectric surface roughness, the absolute intensity of the first-order Bragg peak decreases monotonically. In order to analyze the influence of the gate-dielectric surface roughness on the angular orientation of the DNTT domains within the DNTT layer, we have evaluated rocking scans of the first-order Bragg reflections. As seen in Figure S8 the rocking scans reveal a sharp specular Bragg intensity at their center and a broad superimposed background originating from diffusive scattering by structural imperfections.[58] The rocking width of the specular Bragg component in the rocking scan is typically associated with the average tilting of the crystalline grains towards the out-of-plane direction, known as mosaicity spread.[57] Hardly any difference in the rocking width of the Bragg peaks is observed in our measurements, suggesting that the surface roughness of the gate dielectric has no measurable influence on the tilting angle of the grains in the vacuum-deposited DNTT layers, which means that the mosaicity spread has no measurable effects on the charge-transport properties. Likewise, there is essentially no variance in the intensity ratio between the area under the Bragg peak and the area under the total spectrum, which suggests that the degree of structural disorder within the grains is not significantly affected by the gate-dielectric surface roughness.[59,60] In summary, the XRD analysis confirms independently that the surface roughness of the gate dielectric does not have a significant impact on the internal morphology of the DNTT grains, which suggests that the TFT characteristics are determined exclusively by the density of grain boundaries along the lateral transport channels within the DNTT layers.

3. Conclusion

In this study we investigated the relation between the surface roughness of the gate dielectric and the electrical characteristics of bottom-gate organic TFTs based on the small-molecule semiconductor DNTT. By controlling the substrate temperature during the deposition of the aluminum gate electrodes, we were able to systematically vary the degree of surface roughness of the gate dielectric over approximately one order of magnitude. We found that the effective charge-carrier mobility decreases and the subthreshold swing increases significantly with increasing surface roughness. We reported a correlation between the gate-dielectric surface roughness and the

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED MATERIALS INTERFACES
www.advmatinterfaces.de

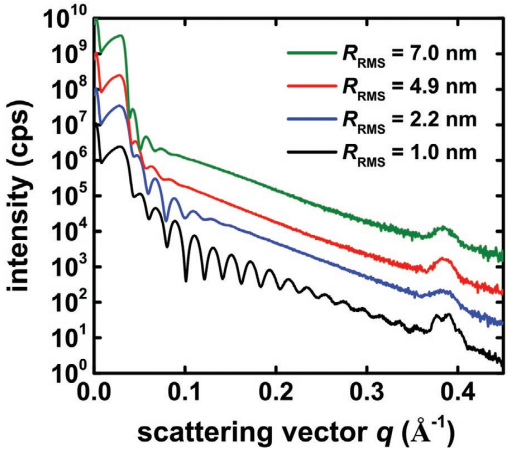


Figure 6. XRD intensities for DNTT films deposited onto gate dielectrics with different surface roughness. The curves are displaced with respect to each other for sake of clarity. The XRD signal from the DNTT film deposited onto the smoothest gate dielectric shows Kiessig oscillations up to high momentum values, which indicates that this DNTT film has a very homogeneous thickness related to the extremely small correlated interface roughness. With increasing roughness the Kiessig fringes are rapidly damped. The (001) Bragg peaks are located at a reciprocal scattering length of 0.385Å^{-1}.

experimentally measured trap density of states in the organic semiconductor. This analysis indicates that grain boundaries, induced by the surface roughness of the gate dielectric, severely hinder charge transport in the organic-semiconductor layer. Our results emphasize the importance of a small surface roughness of the gate dielectric for bottom-gate organic TFTs.

4. Experimental Section

Sample Fabrication: All TFTs were fabricated on doped silicon wafers in the inverted staggered (bottom-gate, top-contact) device structure. As the gate electrode, a 30-nm-thick layer of aluminum was deposited by thermal evaporation in vacuum using a deposition rate of 1.8 nm s^{-1}. The nominal thickness of the metal and organic-semiconductor layers was monitored using a quartz crystal microbalance. For the first part of this study, we fabricated a set of eight substrates in which we tuned the surface roughness of the gate dielectric by performing the aluminum deposition at different substrate temperatures. For this purpose, the substrate was held at a constant temperature T_{sub} of 20, 50, 70, 90, 110, 150, 170, or 200 °C during the aluminum deposition. One substrate was fabricated for each of these eight different substrate temperatures. (In addition, one substrate was prepared on which the aluminum was deposited at a substrate temperature of −24 °C. However, this deposition required the use of a different evaporation system in which the deposition rate is limited to 1Å s^{-1}. At this smaller deposition rate, the aluminum surface roughness is significantly larger.) The aluminum gate electrodes were not patterned. The aluminum surface was briefly exposed to an oxygen plasma to increase the thickness of the native AlO_X layer to 3.6 nm.[61,62] The substrates were then immersed into a 2-propanol solution of *n*-tetradecylphosphonic acid to form a SAM with a thickness of 1.7 nm. The hybrid AlO_X/SAM gate dielectric has a total thickness of 5.3 nm and a unit-area capacitance of 0.7 µF cm^{-2}. Subsequently, a 25-nm-thick layer of the small-molecule semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT; Sigma Aldrich) was deposited by thermal sublimation in vacuum using a deposition rate of 0.03 nm s^{-1}. For the eight substrates employed in the first part of this study, the substrate was held at a constant temperature of 60 °C during the DNTT deposition. For the second part of this study, we fabricated a set of four substrates in which we tuned the microstructure of the DNTT layer by performing the DNTT deposition at different substrate temperatures. On these four substrates, the deposition of the aluminum gate electrodes was performed with a constant substrate temperature of 20 °C in order to obtain the same surface roughness for all four substrates, but during the DNTT deposition, the substrate was held at a temperature of 20, 40, 60, or 80 °C. The final process step for all substrates was the deposition of a 30-nm-thick layer of gold through a polyimide shadow mask (CADiLAC Laser, Hilpoltstein, Germany) to define the source and drain contacts on the surface of the organic-semiconductor layer. The gold was deposited with a rate of 0.03 nm s^{-1}. All TFTs had a channel length of 100 µm and a channel width of 200 µm. The vacuum depositions were performed at a base pressure of 10^{-6} mbar.

Sample Characterization: AFM was performed using a Bruker Dimension Icon system in tapping mode in ambient air. The XRD measurements were carried out with a Seifert/General Electric XRD 3003 T/T diffractometer using monochromatic Cu-Kα_1 radiation with a wavelength of 1.5406 Å. The electrical measurements were performed in ambient air at room temperature using a manual probe station and an Agilent 4156C Semiconductor Parameter Analyzer. The transfer characteristics of the TFTs were measured at a drain-source voltage of −0.1 V and by sweeping the gate-source voltage in steps of −50 mV. The effective charge-carrier mobility was calculated by fitting the following equation to the measured transfer curves:

$$\mu_{eff} = \frac{L}{WC_{diel}V_{DS}} \frac{\partial I_D}{\partial V_{GS}} \quad (1)$$

where L is the channel length, W the channel width, C_{diel} the unit-area capacitance of the gate dielectric, V_{DS} the drain-source voltage, I_D the drain current, and V_{GS} the gate-source voltage. The subthreshold swing was calculated by fitting the following equation to the subthreshold region of the measured transfer curve:

$$S = \frac{\partial V_{GS}}{\partial(\log_{10}(I_D))} \quad (2)$$

The measured subthreshold swing can be used to estimate the trap density at the semiconductor/dielectric interface[63]:

$$N_{it} = \frac{C_{diel}}{e^2}\left[\frac{eS}{k_B T \ln(10)}\right] \quad (3)$$

where e is the elementary charge, T the temperature and k_B the Boltzmann constant.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was partially funded by the German Research Foundation (DFG) under the grants KL 2223/6-1 and KL 2223/6-2 (SPP FFlexCom), KL 2223/7-1, PF 385/11-1, and INST 35/1429-1 (SFB 1249). Funding by the Bavarian State Ministry for Science and the Arts within the collaborative research network "Solar Technologies go Hybrid" (SolTech) is appreciated. The measurement software "SweepMe!" was used for the electrical characterization of the organic transistors (https://sweep-me.net/).

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED MATERIALS INTERFACES
www.advmatinterfaces.de

Conflict of Interest

The authors declare no conflict of interest.

Keywords

grain boundaries, organic thin-film transistors, surface roughness

Received: December 18, 2019
Revised: February 10, 2020
Published online: March 29, 2020

[1] S. R. Forrest, M. E. Thompson, *Chem. Rev.* **2007**, *107*, 923.
[2] X. Ren, K. Pei, B. Peng, Z. Zhang, Z. Wang, X. Wang, P. K. Chan, *Adv. Mater.* **2016**, *28*, 4832.
[3] J. S. Kim, C. K. Song, *Org. Electron.* **2016**, *30*, 45.
[4] H. E. Huitema, G. H. Gelinck, J. B. Van Der Putten, K. E. Kuijk, C. M. Hart, E. Cantatore, D. M. De Leeuw, *Adv. Mater.* **2002**, *14*, 1201.
[5] T. Zaki, F. Ante, U. Zschieschang, J. Butschke, F. Letzkus, H. Richter, H. Klauk, J. N. Burghartz, *IEEE J. Solid-State Circuits* **2012**, *47*, 292.
[6] S. Steudel, K. Myny, S. Schols, P. Vicca, S. Smout, A. Tripathi, B. Van Der Putten, J. L. Van Der Steen, M. Van Neer, F. Schütze, O. R. Hild, E. Van Veenendaal, P. Van Lieshout, M. Van Mil, J. Genoe, G. Gelinck, P. Heremans, *Org. Electron.* **2012**, *13*, 1729.
[7] H. T. Yi, M. M. Payne, J. E. Anthony, V. Podzorov, *Nat. Comm.* **2012**, *3*, 1257.
[8] J. A. Rogers, T. Someya, Y. Huang, *Science* **2010**, *327*, 1603.
[9] K. Cherenack, L. Van Pieterson, *J. Appl. Phys.* **2012**, *112*, 091301.
[10] B. Peng, P. K. L. Chan, *Org. Electron.* **2014**, *15*, 203.
[11] U. Zschieschang, H. Klauk, *Org. Electron.* **2015**, *25*, 340.
[12] S. S. Chang, A. B. Rodríguez, A. M. Higgins, C. Liu, M. Geoghegan, H. Sirringhaus, F. Cousin, R. M. Dalgleish, Y. Deng, *Soft Matter* **2008**, *4*, 2220.
[13] D. Choi, T. K. An, Y. J. Kim, D. S. Chung, S. H. Kim, C. E. Park, *Org. Electron.* **2014**, *15*, 1299.
[14] M. Li, C. An, T. Marszalek, M. Baumgarten, K. Müllen, W. Pisula, *Adv. Mater.* **2016**, *28*, 2245.
[15] S. Lee, F. Li, A. Nathan, *IEEE J. Electron Devices* **2018**, *6*, 653.
[16] M. L. Chabinyc, R. Lujan, F. Endicott, M. F. Toney, I. McCulloch, M. Heeney, *Appl. Phys. Lett.* **2007**, *90*, 88.
[17] Y. Jung, R. Joseph Kline, D. A. Fischer, R. J. Kline, M. Heeney, L. McCulloch, D. M. DeLongchamp, *Adv. Func. Mater.* **2008**, *18*, 742.
[18] S. E. Fritz, T. W. Kelley, C. D. Frisbie, *J. Phys. Chem. B* **2005**, *109*, 10574.
[19] G. Lin, Q. Wang, L. Peng, M. Wang, H. Lu, G. Zhang, G. Lv, L. Qiu, *J. Phys. D: Appl. Phys.* **2015**, *48*, 105103.
[20] A. A. Boampong, J. H. Lee, M. H. Kim, *J. Nanosci. Nanotechnol.* **2018**, *18*, 7132.
[21] K. Shin, S. Y. Yang, C. Yang, H. Jeon, C. E. Park, *Org. Electron.* **2007**, *8*, 336.
[22] S. Steudel, S. De Vusser, S. De Jonge, D. Janssen, S. Verlaak, J. Genoe, P. Heremans, *Appl. Phys. Lett.* **2004**, *85*, 4400.
[23] D. Knipp, R. A. Street, A. R. Völkel, *Appl. Phys. Lett.* **2003**, *82*, 3907.
[24] K. Suemori, S. Uemura, M. Yoshida, S. Hoshino, N. Takada, T. Kodzasa, T. Kamata, *Appl. Phys. Lett.* **2008**, *93*, 1.
[25] P. S. Jo, J. Sung, C. Park, E. Kim, D. Y. Ryu, S. Pyo, H. C. Kim, J. M. Hong, *Adv. Func. Mater.* **2008**, *18*, 1202.
[26] D. Knipp, R. A. Street, B. Krusor, R. Apte, J. Ho, *J. Non-Cryst. Solids* **2002**, *299-302*, 1042.
[27] T. Yamamoto, K. Takimiya, *J. Am. Chem. Soc.* **2007**, *129*, 2224.
[28] K. Takimiya, S. Shinamura, I. Osaka, E. Miyazaki, *Adv. Mater.* **2011**, *23*, 4347.
[29] U. Zschieschang, J. W. Borchert, M. Geiger, F. Letzkus, J. N. Burghartz, H. Klauk, *Org. Electron.* **2018**, *61*, 65.
[30] U. Zschieschang, F. Ante, D. Kälblein, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, J. B. Nimoth, H. Klauk, *Org. Electron.* **2011**, *12*, 1370.
[31] Y. Fujisaki, Y. Nakajima, T. Takei, H. Fukagawa, T. Yamamoto, H. Fujikake, *IEEE Trans. Electron Devices* **2012**, *59*, 3442.
[32] R. Acharya, B. Peng, P. K. L. Chan, G. Schmitz, H. Klauk, *ACS Appl. Mater. Interfaces* **2019**, *11*, 27104.
[33] P. J. Diemer, Z. A. Lamport, Y. Mei, J. W. Ward, K. P. Goetz, W. Li, M. M. Payne, M. Guthold, J. E. Anthony, O. D. Jurchescu, *Appl. Phys. Lett.* **2015**, *107*, 103303.
[34] Z. Li, J. Gao, H. Yang, T. Wang, X. Wang, *Opt. Expresss* **2015**, *23*, 23738.
[35] N. G. Semaltianos, E. G. Wilson, *Thin Solid Films* **2000**, *366*, 111.
[36] D. Smith, *Thin-Film Deposition: Principles and Practice*, McGraw-Hill Education, New York **1995**.
[37] N. G. Semaltianos, *Appl. Surf. Sci.* **2001**, *183*, 223.
[38] S. Fritz, L. Radtke, R. Schneider, M. Weides, D. Gerthsen, *J. Appl. Phys.* **2019**, *125*, 165301.
[39] M. Geiger, L. Schwarz, U. Zschieschang, D. Manske, J. Pflaum, J. Weis, H. Klauk, R. T. Weitz, *Phys. Rev. Appl.* **2018**, *10*, 044023.
[40] N. K. Za'aba, J. J. Morrison, D. M. Taylor, *Org. Electron.* **2017**, *45*, 174.
[41] S. Yogev, R. Matsubara, M. Nakamura, U. Zschieschang, H. Klauk, Y. Rosenwaks, *Phys. Rev. Lett.* **2013**, *110*, 036803.
[42] P. W. Anderson, *Phys. Rev.* **1958**, *109*, 1492.
[43] U. Kraft, K. Takimiya, M. J. Kang, R. Rödel, F. Letzkus, J. N. Burghartz, E. Weber, H. Klauk, *Org. Electron.* **2016**, *35*, 33.
[44] M. Aghamohammadi, R. Rödel, U. Zschieschang, C. Ocal, H. Boschker, R. T. Weitz, E. Barrena, H. Klauk, *ACS Appl. Mater. Interfaces* **2015**, *7*, 22775.
[45] R. Hofmockel, U. Zschieschang, U. Kraft, R. Rödel, N. H. Hansen, M. Stolte, F. Würthner, K. Takimiya, K. Kern, J. Pflaum, H. Klauk, *Org. Electron.* **2013**, *14*, 3213.
[46] W. Shao, H. Dong, L. Jiang, W. Hu, *Chem. Sci.* **2011**, *2*, 590.
[47] I. Vladimirov, M. Kühn, T. Geßner, F. May, R. T. Weitz, *Sci. Rep.* **2018**, *8*, 14868.
[48] B. Rösner, N. Zeilmann, U. Schmidt, R. H. Fink, *Org. Electron.* **2014**, *15*, 435.
[49] J. Chen, C. K. Tee, M. Shtein, J. Anthony, D. C. Martin, *J. Appl. Phys.* **2008**, *103*, 114513.
[50] M. Münch, Strukturelle beeinflussung der elektrischen transporteigenschaften dünner organischer schichten, Ph.D. thesis, University of Stuttgart, **2001**.
[51] T. W. Kelley, C. D. Frisbie, *J. Phys. Chem. B* **2001**, *105*, 4538.
[52] J. Rivnay, S. C. Mannsfeld, C. E. Miller, A. Salleo, M. F. Toney, *Chem. Rev.* **2012**, *112*, 5488.
[53] J. Rivnay, R. Noriega, J. E. Northrup, R. J. Kline, M. F. Toney, A. Salleo, *Phys. Rev. B* **2011**, *83*, 1.
[54] J. H. Kang, D. Da Silva Filho, J. L. Bredas, X. Y. Zhu, *Appl. Phys. Lett.* **2005**, *86*, 1.
[55] R. Noriega, J. Rivnay, K. Vandewal, F. P. V. Koch, N. Stingelin, P. Smith, M. F. Toney, A. Salleo, *Nat. Mater.* **2013**, *12*, 1038.
[56] J. Rivnay, R. Noriega, R. J. Kline, A. Salleo, M. F. Toney, *Phys. Rev. B* **2011**, *84*, 1.
[57] W. Xie, K. Willa, Y. Wu, R. Häusermann, K. Takimiya, B. Batlogg, C. D. Frisbie, *Adv. Mater.* **2013**, *25*, 3478.
[58] B. Nickel, R. Barabash, R. Ruiz, N. Koch, A. Kahn, L. C. Feldman, R. F. Haglund, G. Scoles, *Phys. Rev. B* **2004**, *70*, 125401.

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED MATERIALS INTERFACES
www.advmatinterfaces.de

[59] A. K. Topczak, T. Roller, B. Engels, W. Brüttig, J. Pflaum, *Phys. Rev. B* **2014**, *89*, 201203.
[60] Y. S. Choe, M. H. Yi, J. H. Kim, Y. H. Kim, K. S. Jang, *Phys. Chem. Chem. Phys.* **2016**, *18*, 8522.
[61] T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai, T. Someya, *Science* **2009**, *326*, 1516.
[62] H. Klauk, U. Zschieschang, J. Pflaum, M. Halik, *Nature* **2007**, *445*, 745.
[63] B. Blülle, R. Häusermann, B. Batlogg, *Phys. Rev. Appl.* **2014**, *1*, 034006.

Supporting Information: Effect of the Degree of the Gate-Dielectric Surface Roughness on the Performance of Bottom-Gate Organic Thin-Film Transistors

Michael Geiger, Rachana Acharya, Eric Reutter, Thomas Ferschke, Ute Zschieschang, Jürgen Weis, Jens Pflaum, Hagen Klauk,* and Ralf Thomas Weitz*

1 On the AlO_X in the Gate Dielectric

The AlO_X layer is prepared by exposing the aluminum gate electrode to an RF-generated oxygen plasma with a typical set of parameters (oxygen flow rate: 30 sccm, oxygen partial pressure: 0.01 mbar, RF power: 200 W, duration: 30 s). One advantage of forming the gate oxide by plasma oxidation, rather than by physical or chemical vapor deposition, is that the oxide forms a natural, high-quality interface with the gate metal, thus reducing the possibility of defects at this interface. Another advantage is that, because of the area-selective nature of the plasma-oxidation process, the oxide is formed only where it is required for TFT operation, thus eliminating the need for subtractive patterning. However, due to its small thickness and the fact that it is located directly above a layer of pure aluminum, we are unable to measure its chemical properties, such as the exact composition, i.e. the O/Al ratio, using, e.g., X-ray photoelectron spectroscopy (XPS) or energy dispersive X-ray spectroscopy (EDX). However, based on its dielectric properties, the composition of the AlO_X layer can be speculated within good reason. For aluminum oxide films prepared by other techniques, such as RF magnetron sputtering and solution processing, it has been shown that the conductivity and the permittivity of the oxide are related to its composition.[1,2] For our plasma-produced AlO_X layers, we have measured a leakage current density of no more than 10^{-5} A/cm^2 at an electric field of 5 MV/cm (see Figure S1(a)), and based on its thickness (approximately 4 nm[3,4]) and its capacitance (approximately 1.5 µF/cm^2; see Figure S1(b)), we can estimate its permittivity to be approximately 6.8 ± 1.8, which would suggest its composition to be close to that of stoichiometric Al_2O_3.

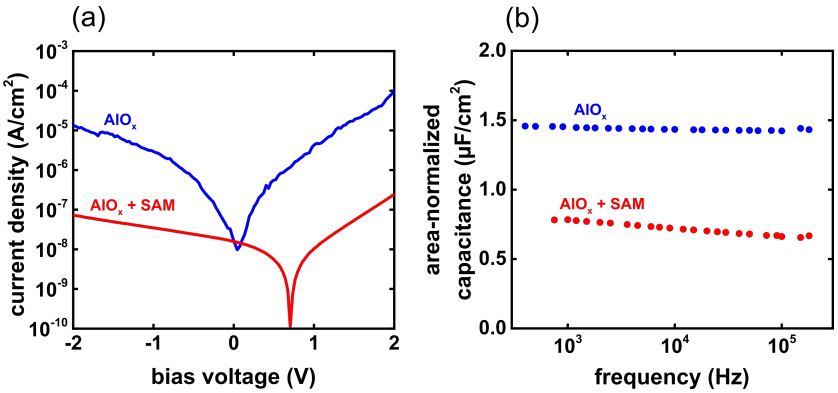


Figure S1. (a) Leakage-current density and (b) area-normalized capacitance of Al/AlO_X/Au capacitors (blue) and Al/AlO_X/SAM/Au capacitors (red).

2 Transfer and Output Characteristics of the TFTs

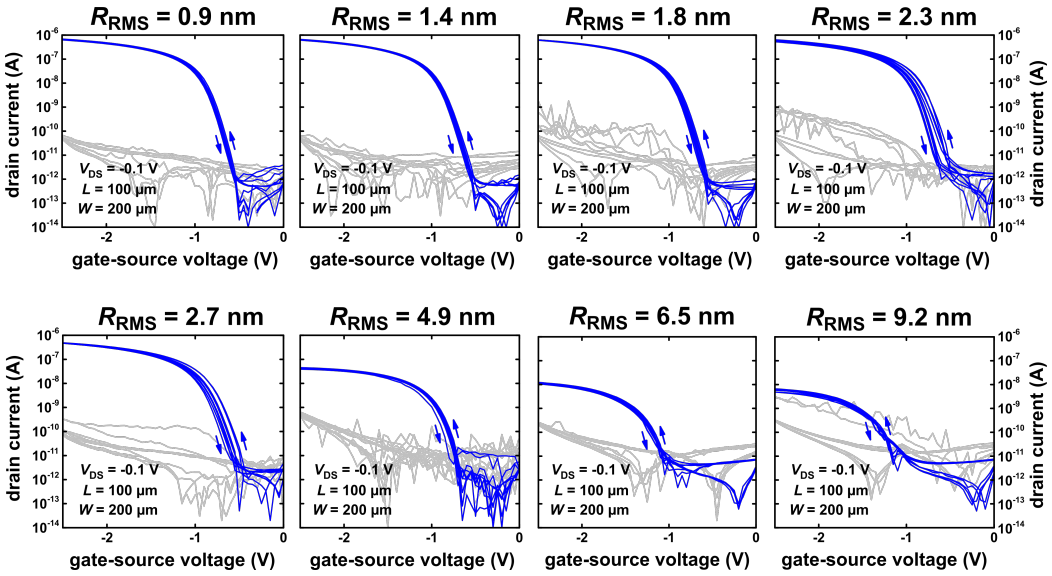


Figure S 2. Measured transfer curves of the TFTs fabricated using gate dielectrics with different degrees of surface roughness.

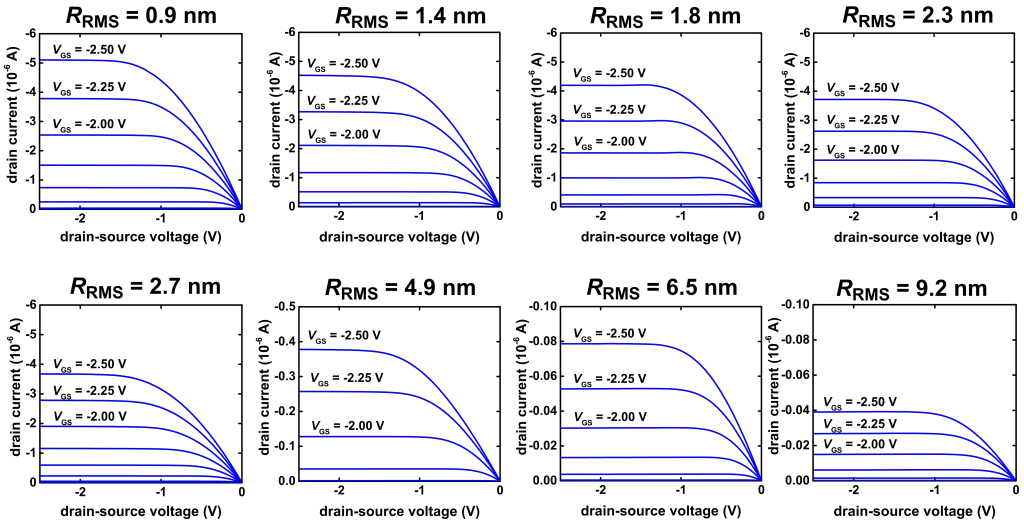


Figure S3. Measured output curves of the TFTs fabricated using gate dielectrics with different degrees of surface roughness.

3 Post-Deposition Heating of the Gate Dielectric

Since the fabrication procedure of the TFTs includes a heating step after the preparation of the gate dielectric (namely the substrate heating during the semiconductor deposition), it is important to show that post-deposition heating does not change the surface roughness of the dielectric. For this purpose, we prepared a substrate with an aluminum layer deposited at a substrate temperature of 20 °C on which the hybrid AlO_X/SAM gate dielectric was then prepared. We then used AFM to measure the surface roughness of the gate dielectric. Then we subjected the substrate to a temperature of 80 °C in vacuum for approximately two hours and then measured the gate-dielectric surface roughness again. The steps of heating the substrate in vacuum and measuring the surface was repeated three more times for temperatures of 100 °C, 150 °C and 200 °C. As can be seen in Figure S4 the post-deposition heating does not have a measurable effect on the R_{RMS} surface roughness of the dielectric, and therefore it is safe to assume that the roughness of the gate dielectric is the same before and after the semiconductor deposition.

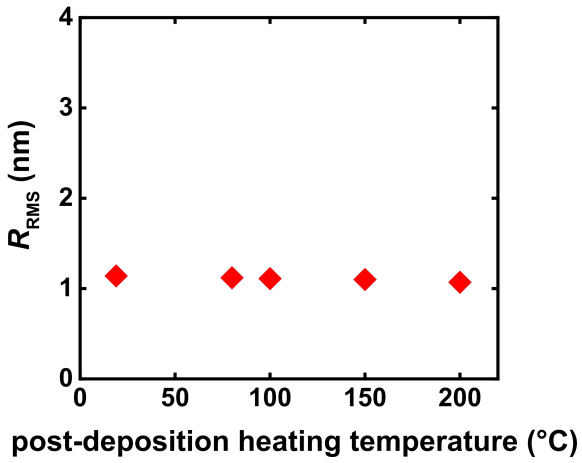


Figure S4. The surface roughness of the hybrid AlO_X/SAM gate dielectric is not affected by heating the gate dielectric up to a temperature of 200 °C in vacuum.

4 Aluminum Film Deposited at $T_{sub} = -24\,°C$

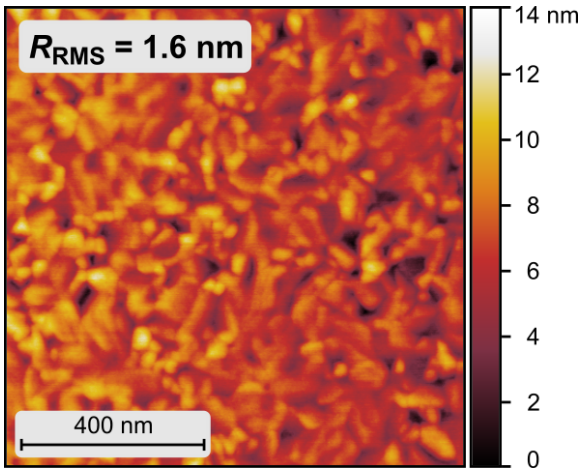


Figure S5. AFM image of a 30-nm-thick layer of aluminum deposited at a substrate temperature of -24 °C. The cooling of the substrate required the use of a different evaporation system in which the deposition rate is limited to 1 Å/s. This deposition rate is much smaller compared to the deposition rate of 18 Å/s used for the deposition of the aluminum films discussed in the main text of the manuscript. This smaller deposition rate results in a larger surface roughness of the aluminum layer.

5 Quantitative Evaluation of Rough Surfaces

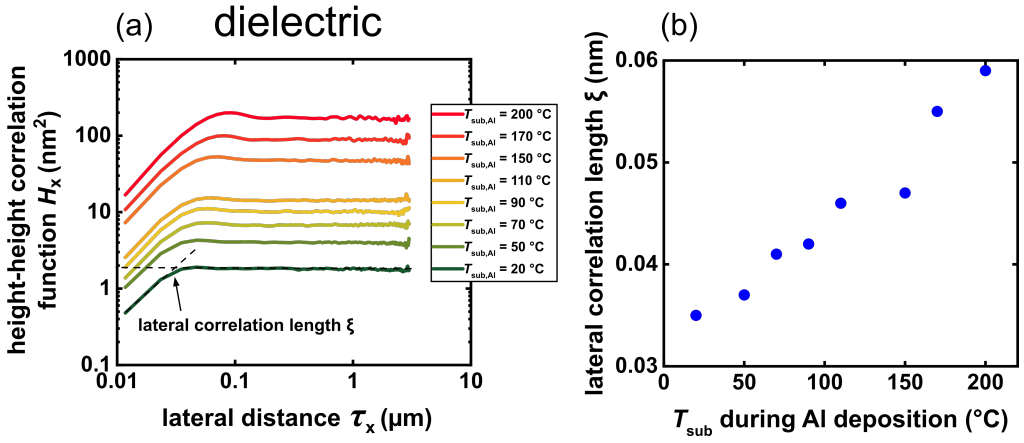


Figure S6. (a) Height-height correlation functions calculated along the fast scanning axis of the AFM of the surface of hybrid AlO_X/SAM gate dielectrics prepared on aluminum layers deposited at substrate temperatures ranging from 20 °C to 200 °C during the aluminum deposition. (b) Extracted lateral correlation lengths of the gate-dielectric surfaces as a function of the substrate temperature during the aluminum deposition.

For the quantitative evaluation of a textured surface, a variety of representative metrics exist. A commonly used quantity is the root-mean-square surface roughness (R_{RMS}). It can be calculated using the following equation:

$$R_{\mathrm{RMS}} = \sqrt{\frac{1}{N}\sum_{j=1}^{N}(z_j - \bar{z})^2}, \tag{1}$$

where N is the number of measurement points, z_j the height of the j-th measurement point and $\bar{z}$ the mean value of the height. The R_{RMS} value contains information about the measured height deviations from a mean line. It is a quantity that is easy to calculate from AFM data and is convenient to report and compare for different surfaces, since it is given as a single value. However, different surfaces can have the same R_{RMS} surface roughness, even though the texture is fundamentally different, e.g. it is conceivable that a sine wave and a step function can produce the same R_{RMS} value. The reason is that characteristic lateral length scales of the surface are not captured by the R_{RMS} value. A more detailed (but also more complicated) approach to represent a surface is the use of second-order quantities which statistically quantify

the mutual relationship between two points on the surface. One such quantity is the height-height correlation function (HHCF), which can be calculated from the AFM data using the following equation:[5]

$$H_x(\tau_x) = \frac{1}{N(M-m)} \sum_{l=1}^{N} \sum_{n=1}^{M-m} (z_{n+m,l} - z_{n,l})^2, \tag{2}$$

where $\tau_x = m\Delta x$ and Δx is the sampling interval along the x direction.

In Figure S6(a) the calculated HHCF for the eight different gate-dielectric surfaces discussed in the main text are shown. Plotted on a double-logarithmic scale, the HHCF displays two distinct regimes. For small distances ($\tau_x < \xi$, where ξ is the lateral correlation length) the HHCF increases linearly, and for large distances ($\tau_x > \xi$) when the heights are no longer correlated, the HHCF saturates. The saturation value $H_\mathrm{x}(\tau_x \gg \xi)$ equals to $2{R_\mathrm{RMS}}^2$.[6] The intersection of the extrapolation of the linear regime and the extrapolation of the saturation plateau is used to extract the lateral correlation length ξ, which is plotted in Figure S6(b) as a function of the substrate temperature during the aluminum deposition. The results summarized in Figure S7 show that the characteristic lateral length scale of the gate-dielectric surface is affected by the substrate temperature during the aluminum deposition in a manner similar to the R_RMS surface roughness. This effect can also be seen in the way that the grain size seen in Figure 2(a)-(c) increases with increasing substrate temperature during the aluminum deposition. The HHCF is therefore a powerful tool to illustrate the impact of the substrate temperature during the aluminum deposition on the grain size, in addition to the analysis of the grain density presented in Figure 2(h).

The same procedure can be applied to demonstrate the impact of the substrate temperature during the DNTT deposition on the grain formation in the DNTT film. Figure S7 shows the HHCF calculated from the AFM data of DNTT films deposited onto gate dielectrics with different degrees of surface roughness and DNTT films which were deposited at different substrate temperatures during the DNTT deposition. Although a reliable quantitative extraction of the lateral correlation lengths is not possible here, the qualitative trend of the HHCF confirms the observations from the grain-density analysis in Figure 2(e)-(h). For a smaller surface roughness of the gate dielectric or a higher substrate temperature during the DNTT deposition, the HHCF levels off at higher distances τ_x, meaning the lateral correlation lengths are larger due

to the fact that the grains in the semiconductor film are larger. Also, the trend and the range of the HHCF curves for the DNTT on the five smoothest gate dielectrics are similar to the HHCF curves of the DNTT deposited at different substrate temperatures, which confirms that the two methods for tuning the grain density in the DNTT film produce similar results.

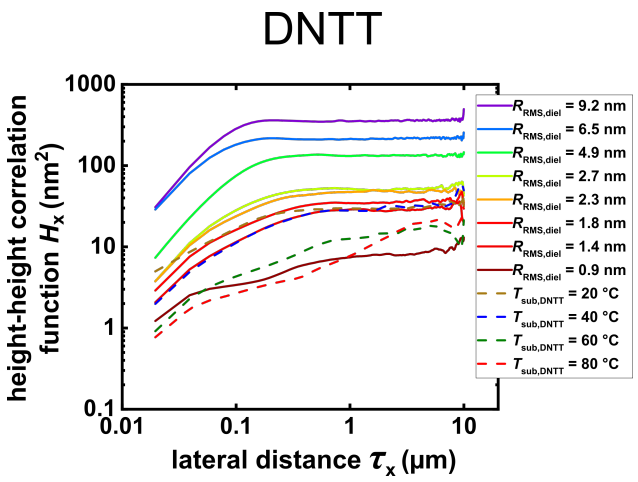


Figure S 7. Calculated height-height correlation functions of DNTT films deposited onto gate dielectrics with different degrees of surface roughness (solid lines) and of DNTT films deposited onto a smooth gate dielectric but at different substrate temperatures during the DNTT deposition (dashed lines).

6 Rocking Scans

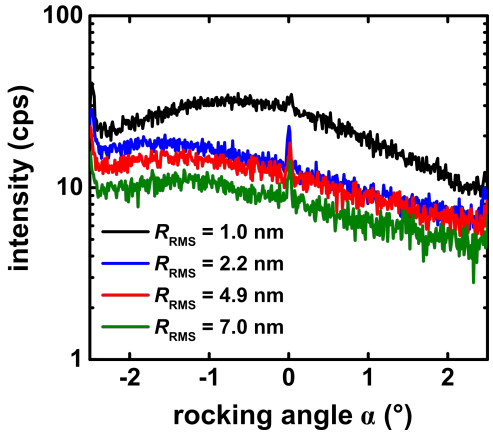


Figure S8. Rocking scans recorded at the position of the first Bragg peak. The DNTT films were deposited onto gate dielectrics with different degrees of surface roughness. The sharp specular Bragg intensity at the center is superimposed by a broad background due to diffusive scattering.

Table S1: Characteristic parameters extracted from the measured rocking scans shown in Figure S8.

R_{RMS} (nm)	1.0	2.2	4.9	7.0
rocking width (°)	0.063	0.035	0.056	0.047
$\mathrm{area}_{\mathrm{peak}}$ (cps°)	3.24	1.70	1.44	1.06
$\mathrm{area}_{\mathrm{total}}$ (cps°)	120.80	61.06	53.04	38.81
$\mathrm{area}_{\mathrm{peak}}/\mathrm{area}_{\mathrm{total}}$	0.03	0.03	0.03	0.03

References

[1] M. Voigt, A. Bergmaier, G. Dollinger, M. Sokolowski, *J. Vac. Sci. Technol. A* **2009**, *27*, 234.

[2] N. Koslowski, S. Sanctis, R. C. Hoffmann, M. Bruns, J. J. Schneider, *J. Mater. Chem.* **2019**, *7*, 1048.

[3] H. Klauk, U. Zschieschang, J. Paum, M. Halik, *Nature* **2007**, *445*, 745.

[4] T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai, T. Someya, *Science* **2009**, *326*, 1516.

[5] P. Klapetek, D. Nečas, C. Anderson, *Gwyddion User Guide* **2009**.

[6] T. Gredig, E. A. Silverstein, M. P. Byrne, *J. Phys.: Conf. Ser.* **2013**, 417, 012069.

Chapter 5

Optimizing the Plasma Oxidation of Aluminum Gate Electrodes for Ultrathin Gate Oxides in Organic Transistors

5.1 Discussion

5.1.1 State-of-the-Art

One area of application for organic transistors can be the implementation in flexible electronic devices such as rollable or bendable active-matrix displays or conformable, wearable or implantable sensors.[112–116] To ensure the portability and safety of the devices, they will be usually be powered by small batteries and consequently the operating voltages of the transistors should be a few volts. The decisive factor for the operating voltage of a transistor is the unit-area capacitance of the gate dielectric. It is dictating how efficiently the applied gate-source voltage is conveyed to the interface potential and thus determines the accumulated charge concentration (as discussed in Chapter 2.2 and Chapter 3).
Approaches for gate dielectrics that provide a large unit-area capacitance for organic TFTs include high-permittivity metal oxides,[108,117] self-assembled nanodielectrics,[118,119] thin films of polymers,[120,121] and hybrid dielectrics composed of a metal oxide in combination with a self-assembled monolayer (SAM) of an organic molecule.[122,123] In addition to a large unit-area capacitance and the correlated operating voltage of the TFT, the gate dielectric plays also an essential role for the subthreshold swing and bias-stress stability of the organic TFTs and governs unwanted charge leakage.[27,124–126] In the case of bottom-gate TFTs, the surface of the gate dielectric has substantial influence on the growth and quality of the organic semiconductor film (as it is also discussed and demonstrated in Chapter 4).[26,46,127]
In the presented study, the approach of an ultrathin hybrid gate dielectric is pursued. The first component of the hybrid gate dielectric is a metal oxide which in principle can be

fabricated by atomic layer deposition,[128–130] electrochemical anodization,[101,131] UV/ozone-assisted oxidation,[132–134] or plasma-assisted oxidation of the surface of the gate electrode.[123] Compared with the fabrication of oxide dielectrics by anodic oxidation or atomic layer deposition, the plasma-oxidation process investigated here has several advantages: (1) It does not require electrical contact to the gate metal during the oxidation (which greatly simplifies the transistor-fabrication process). (2) The oxide is formed only where needed for the transistors (which eliminates the need for subtractive oxide patterning). (3) The native interface between the gate metal and the plasma-grown gate oxide has typically a high quality with a small defect density. The second component of the hybrid gate dielectric is a SAM of an organic molecule. This molecule has an anchor group for the chemisorption on the metal oxide and a tail group which dictates the self-assembly of the molecules and the surface properties of the monolayer.[135–138] Properties of different SAM molecules, the SAM formation process and the relation to the organic TFT performance have been studied in great detail in the past.[27,124,139–145] This work focuses on the metal-oxide component of the hybrid gate dielectric.

5.1.2 Objective

The objective of this study is to investigate how the properties of oxygen-plasma-grown aluminum oxide (AlO_x) dielectrics and hybrid AlO_x/SAM dielectrics are affected by the plasma power and the duration of the plasma exposure. A focus is put on working out the importance of the metal-oxide component in hybrid AlO_x/SAM dielectrics and on finding an optimum combination of plasma parameters which leads to optimum TFT performance. The combination of plasma power and duration was varied systematically and the thickness of the dielectrics, the capacitance of the dielectrics, the leakage currents trough the dielectrics and surface energy as well as surface roughness of the dielectrics were measured and evaluated. Organic TFTs in which these dielectrics served as gate insulator were investigated and the influence of the plasma parameters on the thin-film morphology of the semiconductor and on the TFT characteristics was analyzed.

5.1.3 Conclusion

Cross-sectional transmission electron microscopy (TEM) measurements revealed that the thickness of the aluminum oxide films can be varied between values of 4.3 and 7.3 nm, depending on the plasma parameters. A self-limiting oxide growth was identified, which sets the upper boundary of this range. Analyzing the electrical properties of metal-insulator-metal capacitors in which the plasma-grown AlO_x film served as dielectric revealed a relative permittivity of 8.0 ± 0.2 for the aluminum oxide. The leakage current density through the bare-AlO_x dielectric showed a monotonic dependence on the plasma power and plasma duration and the unit-area capacitance was tuned between values of 1 and 1.6 µF/cm^2. For the hybrid AlO_x/SAM dielectric, the leakage-current densities were reduced by about one order of magnitude and the unit-area capacitance decreased to values between 0.7 and 0.8 µF/cm^2.

The degree of surface roughness of the bare-AlO_x films was significantly affected by the plasma parameters with the trend that increasing plasma power and duration led to a smoother surface. However, for prolonged plasma durations and/or high plasma power the plasma-grown oxide film suffered from surface damage which translated into an unfavorable morphology of the hybrid AlO_x/SAM dielectric.
For DNTT TFTs in which the hybrid AlO_x/SAM dielectric served as gate insulator a range of combinations of plasma parameters was found which promotes high-quality dielectrics and favorable morphology of the DNTT films leading to optimum TFT characteristics. The largest carrier mobility of $2.3\,cm^2/Vs$ was obtained for the combination of a plasma power of 200 W and a plasma duration of 60 s. This study highlights the importance of the metal-oxide component in hybrid AlO_x/SAM dielectrics and the substantial consequences of the plasma process parameters on the properties of the hybrid dielectric and on the performance of low-voltage organic TFTs.

5.2 Published Article

Optimizing the Plasma Oxidation of Aluminum Gate Electrodes for Ultrathin gate Oxides in Organic Transistors

Michael Geiger[1], Marion Hagel[1], Thomas Reindl[1], Jürgen Weis[1], R. Thomas Weitz[2,3], Helena Solodenko[4], Guido Schmitz[4], Ute Zschieschang[1], Hagen Klauk[1], Rachana Acharya[1,4]

[1] *Max Planck Institute for Solid State Research, Heisenbergstr. 1, 70569 Stuttgart, Germany*
[2] *AG Physics of Nanosystems, Faculty of Physics, Ludwig Maximilians University, Amalienstr. 54, 80799 München, Germany*
[3] *1st Institute of Physics, Faculty of Physics, University of Göttingen, Friedrich-Hund-Platz 1, 37077 Göttingen, Germany*
[4] *Institute of Materials Science, University of Stuttgart, Heisenbergstr. 3, 70569 Stuttgart, Germany*

Scientific Reports **11, 6382 (2021)**

DOI: 10.1038/s41598-021-85517-7

reprinted on pages 67–88

www.nature.com/scientificreports

scientific reports

Check for updates

OPEN

Optimizing the plasma oxidation of aluminum gate electrodes for ultrathin gate oxides in organic transistors

Michael Geiger[1]✉, Marion Hagel[1], Thomas Reindl[1], Jürgen Weis[1], R. Thomas Weitz[2,3], Helena Solodenko[4], Guido Schmitz[4], Ute Zschieschang[1], Hagen Klauk[1] & Rachana Acharya[1,4]✉

A critical requirement for the application of organic thin-film transistors (TFTs) in mobile or wearable applications is low-voltage operation, which can be achieved by employing ultrathin, high-capacitance gate dielectrics. One option is a hybrid dielectric composed of a thin film of aluminum oxide and a molecular self-assembled monolayer in which the aluminum oxide is formed by exposure of the surface of the aluminum gate electrode to a radio-frequency-generated oxygen plasma. This work investigates how the properties of such dielectrics are affected by the plasma power and the duration of the plasma exposure. For various combinations of plasma power and duration, the thickness and the capacitance of the dielectrics, the leakage-current density through the dielectrics, and the current–voltage characteristics of organic TFTs in which these dielectrics serve as the gate insulator have been evaluated. The influence of the plasma parameters on the surface properties of the dielectrics, the thin-film morphology of the vacuum-deposited organic-semiconductor films, and the resulting TFT characteristics has also been investigated.

Organic thin-film transistors (TFTs) are being developed for flexible electronics applications, such as rollable or foldable active-matrix displays and conformable sensors[1–5]. To ensure the safe handling and portable nature of these systems, they will typically be powered by small batteries or solar cells and will thus be operating at low voltages of about 2 to 3 V. To enable organic TFTs to operate with low voltages, the gate dielectric should have a large unit-area capacitance. Examples of gate dielectrics suitable for low-voltage organic TFTs include thin insulating polymers[6,7], high-permittivity insulating metal oxides[8,9], self-assembled nanodielectrics[10,11], and ultrathin hybrid dielectrics composed of a thin metal oxide in combination with a molecular self-assembled monolayer (SAM)[12,13]. The thickness of these dielectrics must be sufficiently small to provide a large unit-area capacitance and thereby low-voltage TFT operation[14–17], but sufficiently large to suppress undesirable charge leakage and thus allow for low-power circuit and system operation[18–20]. In addition, the dielectrics should be sufficiently robust to allow the TFTs to be fabricated on unconventional and potentially rough substrates, such as plastics and paper[21–23].

This work focuses on ultrathin hybrid gate dielectrics. The first component of these dielectrics is a thin metal oxide that can be produced by atomic layer deposition[8,24,25], anodic oxidation[26–28], UV/ozone-assisted oxidation[29–31], or plasma-assisted oxidation of the surface of the gate electrode[13]. Among the advantages of the plasma-oxidation process are the fact that it does not require electrical contact to the gate metal during the oxidation process[32] (which greatly simplifies the fabrication process), that the oxide is formed only where needed for the TFTs (which eliminates the need for subtractive patterning to open vias for interconnects[22]) and that the high quality of the native interface between the gate metal and the gate oxide minimizes the hysteresis in the current–voltage characteristics and the subthreshold swing of the TFTs[33,34]. The most popular material combinations for the gate metal and the gate oxide are aluminum/aluminum oxide[15,35] and titanium/titanium oxide[14,27].

The second component of these hybrid dielectrics is a SAM of organic molecules that are composed of an anchor group to facilitate chemisorption on the metal-oxide surface and an aliphatic tail to facilitate the

[1]Max Planck Institute for Solid State Research, Stuttgart, Germany. [2]The 1st Physical Institute, University of Göttingen, Göttingen, Germany. [3]Faculty of Physics, Ludwig-Maximilians-University, München, Germany. [4]Institute of Materials Science, University of Stuttgart, Stuttgart, Germany. ✉email: M.Geiger@fkf.mpg.de; R.Acharya@fkf.mpg.de

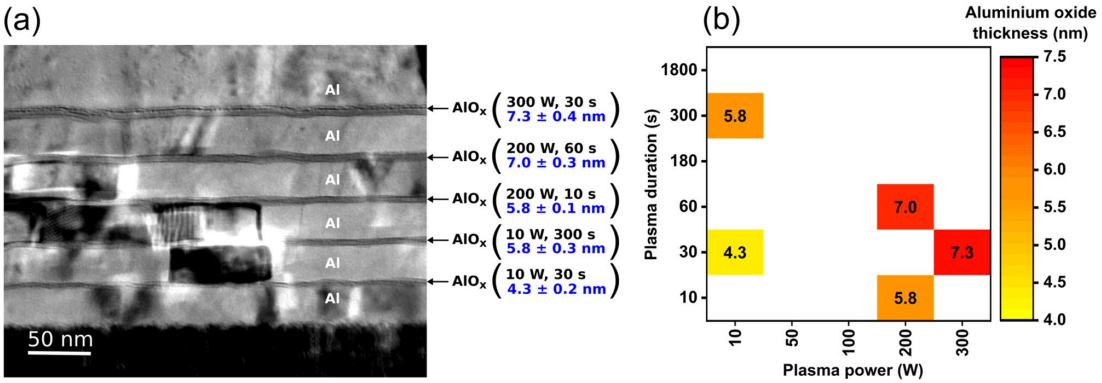


Figure 1. Thickness of plasma-grown aluminum oxide films. (**a**) Cross-sectional TEM image indicating the thicknesses of five AlO_x films produced sequentially by the plasma-assisted surface oxidation of aluminum using five different combinations of plasma power and plasma duration. (**b**) Summary of the results.

self-assembly of a well-ordered molecular monolayer[36]. The preferred anchor group for chemisorption on aluminum oxide is the phosphonic acid[37], while the aliphatic tail can be an alkyl or fluoroalkyl chain[25,38–41]. The effects of the properties of the SAM-forming molecules, such as the alkyl or fluoroalkyl chain length[31,42–44], and the details of the SAM-formation process have been investigated in great detail in the past[45–48]. One result of these studies is that the best TFT performance is often obtained with a medium-chain-length alkylphosphonic acid, such as *n*-tetradecylphosphonic acid, processed from solution.

In this work, we focused on the metal-oxide component of the hybrid dielectric. We prepared thin films of aluminum oxide (AlO_x) by exposing the surface of vacuum-deposited aluminum films to a capacitively coupled radio-frequency (13.56 MHz) plasma in pure, low-pressure oxygen and investigated the extent to which the properties of the resulting AlO_x films can be tuned by adjusting two of the parameters of the plasma-oxidation process, namely the plasma power and the duration of the plasma exposure. We varied the plasma power from 10 to 300 W and the plasma duration from 10 to 1800 s and studied how this affects the properties of the AlO_x films and those of organic TFTs in which these AlO_x films serve either as the gate dielectric or as the first component of a hybrid AlO_x/SAM gate dielectric. The thickness of the plasma-grown AlO_x films was determined by transmission electron microscopy (TEM). For both the bare-AlO_x and the hybrid AlO_x/SAM dielectrics, we measured the unit-area capacitance, the leakage-current density, the surface properties and the current–voltage characteristics of organic TFTs fabricated in the inverted staggered (bottom-gate, top-contact) architecture using the vacuum-deposited small-molecule semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT)[49–51] and analyzed the effects of the plasma parameters on these material and device characteristics.

Results and discussion

Thickness of plasma-grown AlO_x films. Figure 1a shows a cross-sectional TEM image of a specimen prepared on a silicon substrate by repeating the deposition of 30-nm-thick aluminum and the plasma-assisted oxidation of the aluminum surface five times, each time with a different combination of plasma power and plasma duration. During each transfer of the substrate from the metal-deposition system to the plasma system, the aluminum surface was necessarily exposed to ambient air, causing the spontaneous formation of a native oxide film with a thickness of approximately 3 nm on the aluminum surface[52]. The TEM image indicates that after the plasma-assisted oxidation, the aluminum oxide films have a thickness of approximately 4.3 to 7.3 nm, depending on the plasma parameters. (The method of extracting the thickness of the AlO_x films from the TEM image is detailed in Fig. S1).

The lower limit of this thickness range (4.3 nm) is thus larger by approximately 1.3 nm than the thickness of the native oxide. Although this increase in the oxide thickness produced by the plasma process is quite small, it is of critical importance for the proper operation of organic TFTs in which these dielectrics are used as the gate insulator. Figure S2 shows the measured transfer characteristics of DNTT TFTs fabricated using bare-AlO_x and hybrid AlO_x/SAM gate dielectrics based on native aluminum oxide (obtained without plasma process), and as can be seen, these TFTs either do not show a field effect (bare AlO_x) or suffer from prohibitively large gate currents (hybrid AlO_x/SAM dielectric).

The relation between the plasma parameters and the thickness of the plasma-grown AlO_x films extracted from the TEM image is illustrated in Fig. 1b. As expected, both a larger plasma power (by virtue of a higher kinetic energy of the oxygen radicals impinging on the oxide surface) and a longer plasma duration (by virtue of a larger number of incident radicals) result in thicker AlO_x films.

Electrical properties of plasma-grown AlO_x dielectrics. To investigate how the electrical properties of plasma-grown AlO_x dielectrics and of hybrid AlO_x/SAM dielectrics are affected by the plasma parameters, we fabricated metal–insulator–metal capacitors and bottom-gate, top-contact DNTT TFTs with dielectrics prepared using fifteen different combinations of plasma power (ranging from 10 to 300 W) and plasma duration

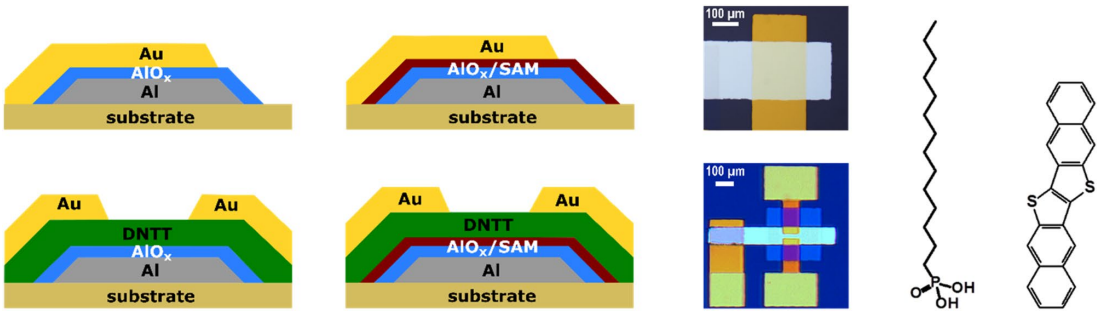


Figure 2. Schematic cross sections and photographs of metal–insulator–metal capacitors and bottom-gate, top-contact TFTs in which the insulator or gate dielectric is either a film of plasma-grown AlO_x or a combination of plasma-grown AlO_x and an *n*-tetradecylphosphonic acid SAM. Also shown are the chemical structure of *n*-tetradecylphosphonic acid and of the organic semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT).

(ranging from 10 to 1800 s). The devices were fabricated on silicon substrates coated with 100-nm-thick silicon dioxide. For the bottom electrode of the capacitors and the gate electrode of the TFTs, aluminum with a thickness of 30 nm and a root-mean-square surface roughness of less than 1 nm (measured by AFM[53]) was deposited by vacuum evaporation. AlO_x was produced by plasma oxidation, SAMs of *n*-tetradecylphosphonic acid were formed from solution, and DNTT was deposited by vacuum sublimation. For the top electrode of the capacitors and the source/drain contacts of the TFTs, gold was deposited by vacuum evaporation. Schematic cross sections and photographs of the capacitors and TFTs and the chemical structures of *n*-tetradecylphosphonic acid and DNTT are shown in Fig. 2.

The measured unit-area capacitance of the capacitors with a bare-AlO_x dielectric is plotted as a function of the plasma power and the plasma duration in Fig. 3a. Depending on these parameters, the unit-area capacitance varies from 1 to 1.6 µF/cm^2, with the general trend of higher power and longer duration producing AlO_x films with smaller capacitance. In Fig. 3b, we plot the unit-area capacitance measured for each of the five plasma-parameter combinations for which the AlO_x thickness was determined by TEM (Fig. 1) as a function of the inverse of that thickness. The error bars reflect the accuracy of the method by which the oxide thickness was extracted from the TEM image (see Fig. S1). By fitting the measurement data with the theoretical relation between the unit-area capacitance C_{ox} and the oxide thickness t_{ox}:

$$C_{ox} = \varepsilon_0 \varepsilon_{ox} \frac{1}{t_{ox}} \tag{1}$$

(where ε_0 is the vacuum permittivity and ε_{ox} the relative permittivity of the plasma-grown oxide) and forcing the linear fit through the origin ($1/t_{ox} = 0$; $C_{ox} = 0$), we obtain a value of 8 ± 0.2 for the relative permittivity of the plasma-grown AlO_x films. This result is in good agreement with the relative permittivity reported in the literature for aluminum oxide films produced by various methods[54–56].

We note that a more elaborate analysis of the relation between the oxide thickness and the oxide capacitance would have included measurements of the oxide thickness for all fifteen combinations of plasma power and plasma duration shown in Fig. 3a, as opposed to selecting only five of these fifteen combinations for the TEM measurements. However, as this was not possible, we deliberately selected for the TEM analysis five plasma-parameter combinations covering both the extremes and the center of the range of thicknesses and capacitances as much as possible.

Closer inspection of Fig. 3a reveals that the influence of the plasma duration on the capacitance is relatively small, as long as the plasma power is at least 50 W and the duration is at least 30 s. For example, for a plasma power of 200 W, a unit-area capacitance of 1 µF/cm^2 is obtained for a plasma duration of one minute and for a plasma duration of half an hour. Combined with the TEM results (Fig. 1), this suggests that the thickness of the plasma-grown AlO_x films saturates at a value of approximately 7 nm after a plasma duration of 30 to 60 s, provided the plasma power is at least 50 W. According to the Cabrera-Mott model[57], this self-limiting oxide-growth behavior results from the low electronic conductivity of aluminum oxide and the small diffusivity of oxygen in aluminum oxide, which prevents oxygen from reaching the metal surface once the oxide thickness has reached a certain value determined mainly by the plasma power[57–59].

Compared with the dependence of the capacitance on the plasma duration, its dependence on the plasma power appears to be more monotonic, but overall, the range over which the capacitance of the plasma-grown AlO_x can be tuned is nevertheless quite small (less than a factor of two). One benefit of this small range of accessible capacitances is that it renders the fabrication process more robust by suppressing the effects of unintended process-parameter variations on the resulting TFT characteristics.

In addition to the capacitance, we also measured the current–voltage characteristics of the capacitors to analyze the influence of the plasma power and duration on the leakage-current density through the dielectrics. The results for the capacitors with a bare-AlO_x dielectric are summarized in Fig. 4a. The general trend is similar

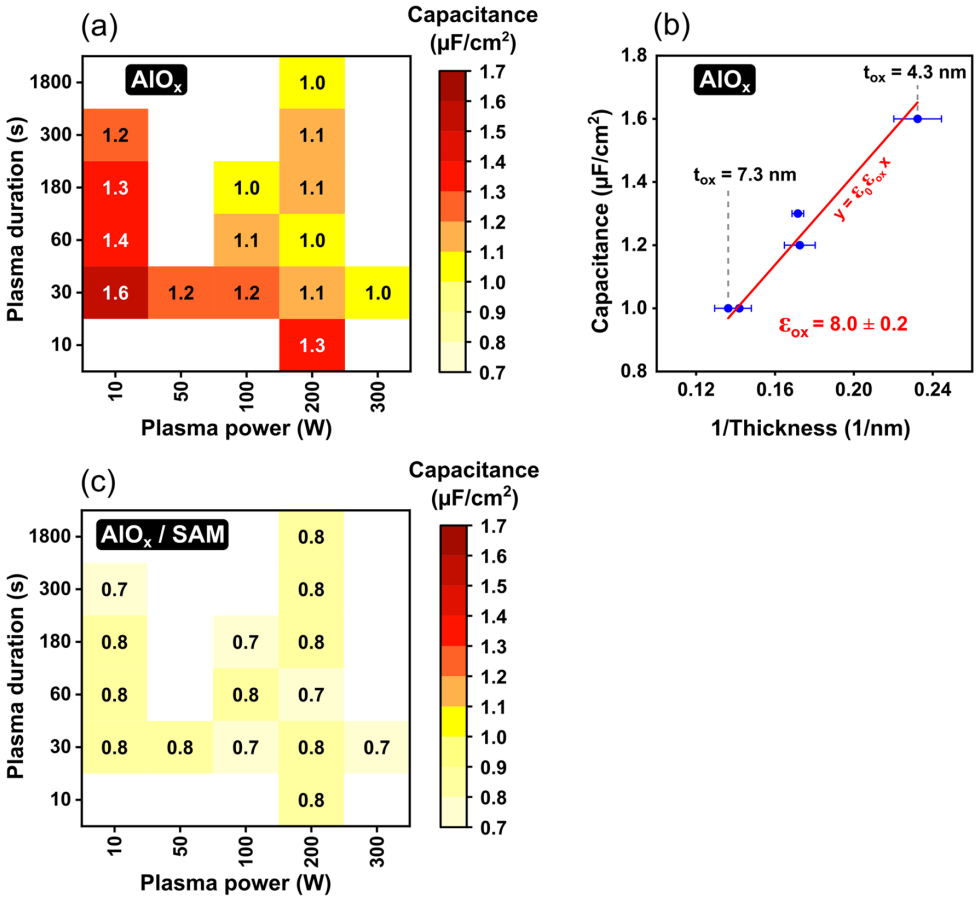


Figure 3. Capacitance of plasma-grown AlO_x and hybrid AlO_x/SAM dielectrics. (**a**) Measured unit-area capacitance of capacitors with a bare-AlO_x dielectric as a function of plasma power and plasma duration. (**b**) Unit-area capacitance of bare-AlO_x dielectrics plotted as a function of the inverse of the AlO_x thickness determined by TEM (Fig. 1) to calculate the relative permittivity of the plasma-grown AlO_x. The red line is a linear fit of Eq. (1) that was forced to pass through the origin ($1/t_{ox} = 0$; $C_{ox} = 0$). (**c**) Measured unit-area capacitance of capacitors with a hybrid AlO_x/SAM dielectric as a function of plasma power and plasma duration.

to the one seen for the capacitance in Fig. 3a and is consistent with the TEM results: a higher plasma power and a longer plasma duration lead to thicker AlO_x films characterized by smaller leakage-current densities.

When the plasma power is smaller than about 50 to 100 W and the plasma duration is shorter than about 30 to 60 s, the leakage-current density through the bare-AlO_x films exceeds 10^{-4} A/cm^2 at ± 3 V. On the other hand, for a plasma power of 200 W and a plasma duration of 60 s, the current density through the bare-AlO_x dielectrics is below 10^{-5} A/cm^2 at ± 3 V. Figure 4a also shows that it is not possible to produce bare-AlO_x dielectrics by plasma oxidation that provide leakage-current densities significantly below 10^{-6} A/cm^2 at ± 3 V.

Electrical properties of hybrid AlO_x/SAM dielectrics. Although it is possible to use the bare, plasma-grown AlO_x films discussed above as the gate dielectric for organic TFTs[40,60,61], the often-preferred option is a hybrid gate dielectric in which the AlO_x is complemented by a phosphonic-acid SAM. This has a number of advantages, including a smaller density of interface trap states[62], a smaller leakage-current density[40], an improved bias-stress stability due to the expulsion of water from the semiconductor-dielectric interface[63], the suppression of Fröhlich polarons due to the low permittivity of the organic SAM[64], the possibility to tune the threshold voltage of the TFTs[15,25,38,65,66], and the possibility to tune the surface energy of the dielectric.

In Fig. 3c, the unit-area capacitance of the capacitors with a hybrid AlO_x/SAM dielectric is plotted as a function of the plasma power and plasma duration. Due to the additional contribution of the SAM, the capacitance of the hybrid AlO_x/SAM dielectric (0.7–0.8 μF/cm^2) is smaller than that of the bare-AlO_x dielectric (1–1.6 μF/cm^2) and shows a notably smaller dependence on the plasma power and duration. From the measured unit-area capacitances of the bare-AlO_x and the hybrid AlO_x/SAM dielectrics, the unit-area capacitance of the SAM can

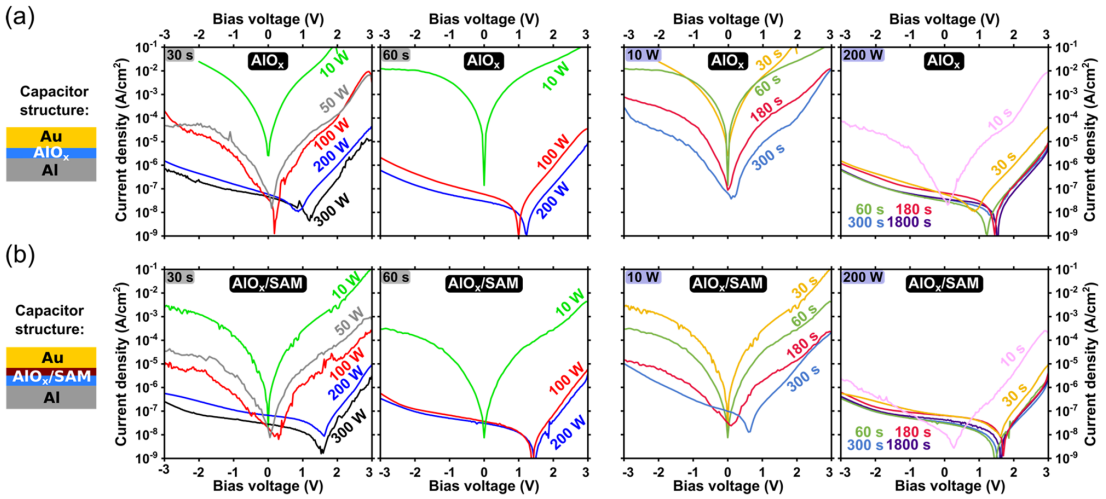


Figure 4. Current density measured as a function of applied voltage through capacitors with a bare-AlO_x dielectric (**a**) and a hybrid AlO_x/SAM dielectric (**b**) for various combinations of plasma power and plasma duration.

be estimated using the equation $1/C_{total} = 1/C_{ox} + 1/C_{SAM}$ (where C_{total}, C_{ox} and C_{SAM} are the unit-area capacitances of the hybrid AlO_x/SAM dielectric, the bare-AlO_x film, and the SAM, respectively), which yields values between approximately 1.7 and 2.1 μF/cm² for the SAM, depending on the set of plasma parameters for which the calculation is performed. However, this does not mean that SAMs formed on AlO_x films produced with different plasma parameters have different capacitances, but merely reflects the uncertainty in the measured capacitances combined with the fact that the influence of variations in the SAM capacitance on the total capacitance is very small. Assuming that the molecules employed for the SAM (*n*-tetradecylphosphonic acid) have an alkyl-chain length of 1.9 nm, as reported previously[13,31], and that the molecules in the SAM have a tilt angle of 20–30° with respect to the surface normal[13], this corresponds to a permittivity between approximately 3.1 and 4.3 for the *n*-tetradecylphosphonic acid SAMs, which is larger by about 25 to 75% than the value of 2.5 that was reported previously for *n*-octadecyltrichlorosilane SAMs[67]. Whether this difference is systematic or not, and if so, how this difference can be explained, is not known.

The results of the measurements of the current density through the hybrid AlO_x/SAM dielectric are summarized in Fig. 4b. As can be seen, the leakage-current density through the hybrid AlO_x/SAM dielectrics is smaller by approximately an order of magnitude than the current density through the bare-AlO_x dielectrics, regardless of the plasma parameters. For a plasma power of 200 W and a duration of 60 s, the leakage-current density through the hybrid AlO_x/SAM dielectric drops below 10^{-6} A/cm². While this confirms the beneficial effect of the SAM in improving the insulating properties of the gate dielectric for low-power organic TFTs, the results in Fig. 4b also clearly demonstrate the critical importance of providing an optimized AlO_x film, even when complementing it with a SAM.

Organic TFTs with bare-AlO_x and hybrid AlO_x/SAM gate dielectrics. On the same substrates as the capacitors discussed above, we also fabricated bottom-gate, top-contact DNTT TFTs with either a bare-AlO_x or a hybrid AlO_x/SAM gate dielectric produced using the same fifteen combinations of plasma power and duration as discussed above. Figure 5 shows the measured transfer characteristics and gate currents of TFTs fabricated with three of these plasma-parameter combinations; the complete set of results is shown in Figs. S3 and S4.

One observation from Figs. 5 and S3 is that a plasma power of 10 W is insufficient to suppress the gate-leakage current to an acceptable level, regardless of the plasma duration and regardless of whether or not the AlO_x is complemented by a SAM. The minimum plasma power required to obtain AlO_x films with sufficient thickness and sufficient quality to limit the gate current to 10^{-11} A over the range of gate-source voltages considered here (0 to −3 V) is 50 W. For a plasma power in the range of 100 to 200 W, both the bare-AlO_x and the hybrid AlO_x/SAM gate dielectric are able to provide gate currents not exceeding 10^{-11} A and on/off current ratios of 10^6. The optimum plasma duration for this range of plasma power is dictated by whether or not the AlO_x is complemented by a SAM: For the bare-AlO_x gate dielectric, the optimum plasma duration is ≥ 300 s, whereas for the hybrid AlO_x/SAM gate dielectric, the optimum plasma duration is in the range of 30 to 60 s (for a plasma power ranging from 100 to 200 W).

In Fig. 6a, the effective charge-carrier mobility extracted from the measured transfer characteristics of the DNTT TFTs with a bare-AlO_x gate dielectric is plotted as a function of the plasma power and the plasma duration. As can be seen, the carrier mobility of these TFTs is rather small, between 0.1 and 0.6 cm²/Vs, which is possibly related to charge trapping and the formation of Fröhlich polarons, due to the fact that the organic semiconductor is in direct contact with the aluminum oxide[64,68].

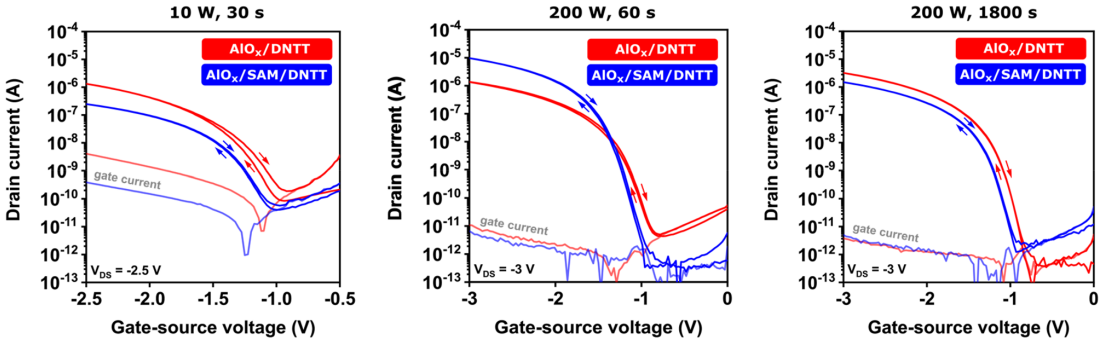


Figure 5. Transfer characteristics and gate currents of DNTT TFTs fabricated using either a bare-AlO_x gate dielectric (red curves) or a hybrid AlO_x/SAM gate dielectric (blue curves) for three combinations of plasma power and plasma duration. (Fig. S3 shows the complete set of results.) The TFTs have a channel length of 20 μm and a channel width of 100 μm.

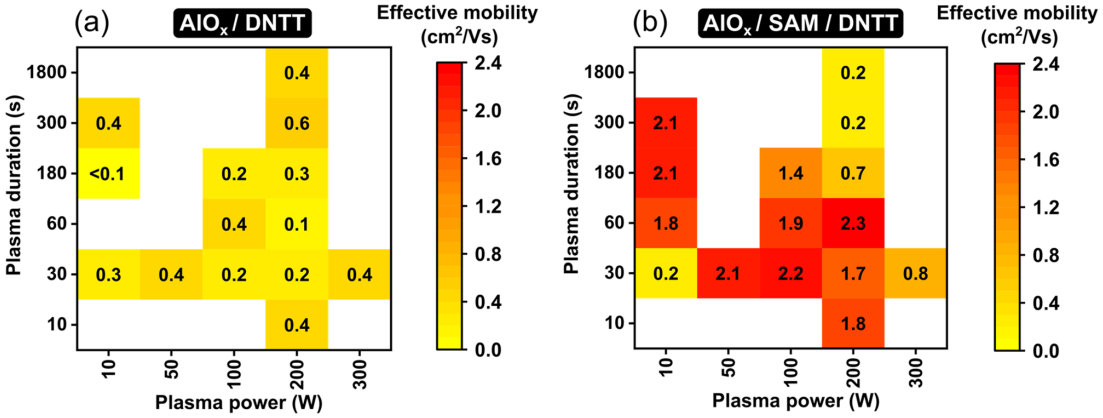


Figure 6. Effective charge-carrier mobilities extracted from the measured transfer characteristics of DNTT TFTs fabricated using either a bare-AlO_x gate dielectric (**a**) or a hybrid AlO_x/SAM gate dielectric (**b**) as a function of plasma power and plasma duration.

The dependence of the carrier mobility of the TFTs with a hybrid AlO_x/SAM gate dielectric on the plasma parameters is summarized in Fig. 6b. The beneficial contribution of the SAM, in providing a hydrophobic surface with a greatly reduced density of water-related trap sites and effective screening of the organic-semiconductor film from the high-permittivity oxide, leads to notably larger carrier mobilities of up to 2.3 cm^2/Vs. Closer inspection of Fig. 6b shows that carrier mobilities of approximately 2 cm^2/Vs are obtained along a track from the upper left to the lower right corner of the graph, i.e., from low-power/long-duration to high-power/short-duration combinations. For parameter combinations outside of this corridor, the carrier mobilities are notably smaller, as small as 0.2 cm^2/Vs. The reasons for this distinctive parameter-dependence pattern will be elucidated in the following section.

Surface properties. The performance of field-effect transistors in general and of organic TFTs in particular is greatly dependent on the properties of the interface between the semiconductor and the gate dielectric[69]. In the case of bottom-gate TFTs, as considered here, this highlights the critical importance of the properties of the gate-dielectric surface. We have thus measured the surface energy and the surface roughness of the bare-AlO_x and the hybrid AlO_x/SAM dielectrics for each of the fifteen combinations of plasma power and plasma duration discussed above.

The surface energies of both the bare-AlO_x and the hybrid AlO_x/SAM dielectrics show only very small variations and no systematic dependence on the plasma parameters (see Fig. S7). The surface energy of the bare-AlO_x dielectric varies between 61 and 71 mJ/m^2, and that of the hybrid AlO_x/SAM dielectric between 23 and 26 mJ/m^2, similar to previous reports[38,43].

The surface roughness, on the other hand, shows a clear correlation with the plasma parameters. Prior to the plasma-oxidation process, the vacuum-deposited aluminum has a root-mean-square (RMS) surface roughness of 0.9 nm[53]. After the plasma-oxidation process, the RMS surface roughness of the bare AlO_x ranges from 0.34 to

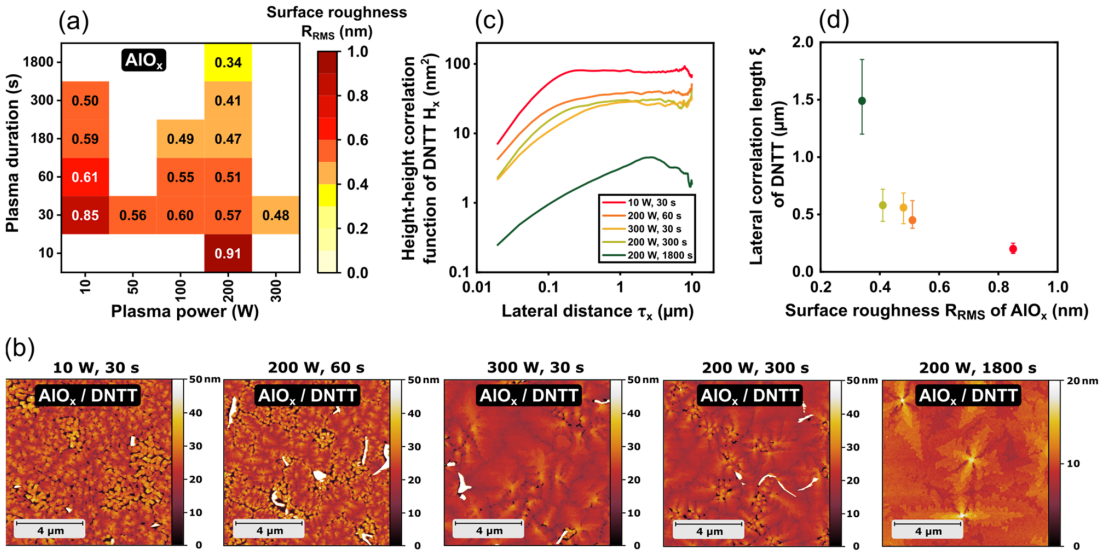


Figure 7. (**a**) Root-mean-square surface roughness of bare-AlO_x dielectrics as a function of plasma power and plasma duration. (**b**) AFM images of DNTT films deposited onto bare-AlO_x dielectrics for five combinations of plasma power and plasma duration. (**c**) Height-height correlation functions (HHCF) of DNTT films deposited onto bare-AlO_x dielectrics for the same five combinations of plasma power and plasma duration. (**d**) Lateral correlation length ξ of the DNTT films as a function of the surface roughness of the bare-AlO_x dielectric.

0.91 nm, depending on the plasma parameters (shown in Fig. 7a). The general trend seen in Fig. 7a is that higher plasma power and longer plasma duration lead to smoother AlO_x films. Given the difference between the RMS surface roughness of the aluminum prior to plasma oxidation (0.9 nm) and the RMS surface roughness of the plasma-grown AlO_x (0.34 to 0.91 nm), it appears that the plasma-oxidation process smoothens the surface, most prominently for sufficiently high plasma powers and sufficiently long durations. This effect was not observed in our previous study[53], in which we measured an almost identical RMS surface roughness of 0.9 nm for both the vacuum-deposited aluminum and the dielectric. However, in this previous study we did not explore the use of high plasma powers or long plasma durations, which might explain why no smoothening was observed.

The degree of the surface roughness of the dielectric affects the properties of the organic-semiconductor film deposited onto it[53]. When DNTT is deposited onto a smooth dielectric, the DNTT film exhibits a pronounced terrace-like structure, whereas deposition onto a rough dielectric results in a notably smaller terrace size. Qualitatively, this can already be seen in the AFM images in Fig. 7b, which show the morphology of DNTT deposited onto bare-AlO_x dielectrics produced using different plasma parameters.

To evaluate the DNTT thin-film morphology in a quantitative manner, we have applied height-height correlation functions (HHCF), calculated from the AFM data using the following equation[70]:

$$H_x(\tau_x) = \frac{1}{N(M-m)} \sum_{l=1}^{N} \sum_{n=1}^{M-m} \left(z_{n+m,l} - z_{n,l}\right)^2 \quad (2)$$

where N and M are the number of measured rows and columns, z is the height of a measurement point, Δx is the sampling interval along the x direction, m an integer ($0 \le m \le M$), and τ_x is the lateral distance ($\tau_x = m\,\Delta x$).

The HHCF has two distinct regimes, as seen in Fig. 7c: over short lateral distances, the heights are correlated and the HHCF increases linearly with distance. Over long distances, the heights are uncorrelated and the HHCF saturates at a value proportional to $2R_{RMS}^2$[71]. The lateral distance at which the crossover between the two regimes occurs is the lateral correlation length ξ. In Fig. 7d, the lateral correlation length determined for each of the DNTT films deposited onto bare AlO_x (Fig. 7b) is plotted as a function of the RMS surface roughness of the AlO_x. As can be seen, the lateral correlation length of the DNTT films shows a monotonic dependence on the AlO_x surface roughness, increasing from 0.2 nm for the largest surface roughness to 1.5 nm for the smoothest surface. However, these trends are not reflected in the measured charge-carrier mobilities of the TFTs in which these bare-AlO_x films serve as the gate dielectric (Fig. 6a), since the carrier mobility in these DNTT films is greatly suppressed, presumably by charge trapping and polaronic effects resulting from the close proximity of the DNTT and the aluminum oxide.

The RMS surface roughness of the hybrid AlO_x/SAM dielectrics as a function of plasma power and duration is shown in Fig. 8a. Comparing Fig. 7a and Fig. 8a shows that the functionalization of the AlO_x surface with the SAM has no measurable effect on the roughness, i.e., the SAM covers the AlO_x surface in a conformal manner, as expected. The extent to which the carrier mobility of the TFTs with the hybrid AlO_x/SAM dielectric correlates

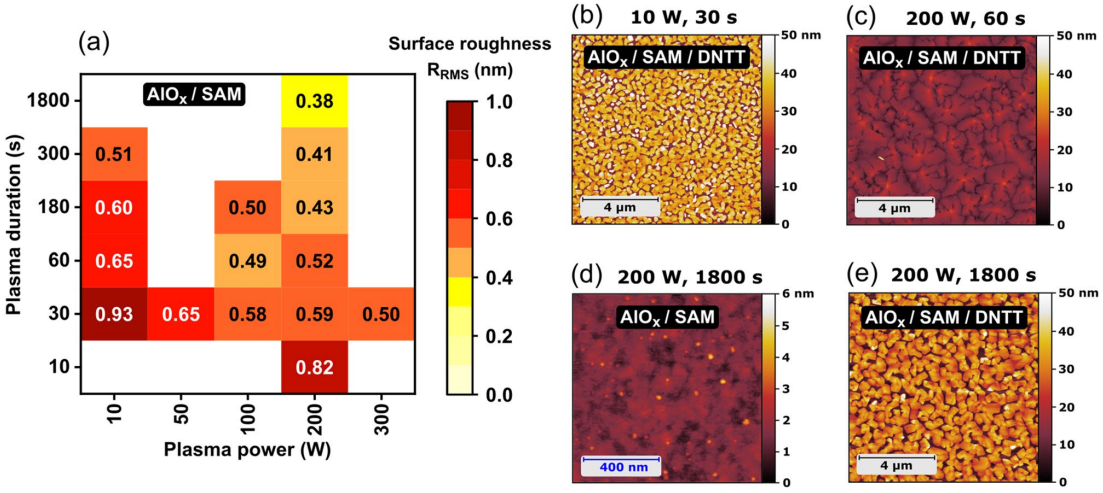


Figure 8. (**a**) Root-mean-square surface roughness of hybrid AlO_x/SAM dielectrics as a function of plasma power and plasma duration. (**b**–**e**) AFM images of representative morphologies on the indicated surfaces with the indicated plasma parameters.

with its surface roughness can be seen by comparing Fig. 6b and Fig. 8a (see also Fig. S5 where these graphs are reproduced and the carrier mobility is plotted as a function of the RMS surface roughness): the largest RMS surface roughness (0.93 nm; obtained with low plasma power/short duration; indicated in grey in Fig. S5) leads to a disordered DNTT film with small grains (Fig. 8b) that shows a very small carrier mobility (0.2 cm^2/Vs), as expected[53]. The largest carrier mobilities (≥ 2 cm^2/Vs) are obtained only when the RMS surface roughness is below approximately 0.65 nm (indicated in green in Fig. S5), so that the DNTT morphology shows a pronounced terrace-like structure (Fig. 8c); this is also in line with expectations. On the other hand, the smallest RMS surface roughness (0.38 nm; obtained with medium power/long duration; indicated in blue in Fig. S5) does not lead to the largest carrier mobility, as one might have expected, but instead to a very small mobility (0.2 cm^2/Vs). The reason for this anomaly is revealed by the AFM image of this dielectric (Fig. 8d), in which a large density of small, tall features can be seen protruding from the surface. These features do not significantly contribute to the calculated RMS surface roughness, but they influence the DNTT morphology in an unfavorable manner, as seen in Fig. 8e. The specifics of these tall features are unknown, but the fact that they appear only for long plasma durations (≥ 300 s) suggests that they mark some form of mechanical damage created on the AlO_x surface by prolonged plasma exposure. AFM images of DNTT films deposited onto hybrid AlO_x/SAM dielectrics for all fifteen combinations of plasma power and plasma duration are collected in Fig. S6.

Organic TFTs and complementary circuits on flexible plastic substrates. The process described above is suitable for the fabrication of organic TFTs on flexible substrates, such as plastics[15] and paper[23]. Figure 9a shows a photograph of organic TFTs and circuits fabricated on a polyethylene naphthalate (PEN) substrate. Based on the findings reported above, a plasma power of 200 W and a plasma duration of 60 s were chosen for the preparation of the aluminum oxide as part of the gate dielectric. Figure 9b and c show the measured transfer and output characteristics of a DNTT TFT, indicating a carrier mobility of 2 cm^2/Vs, an on/off current ratio of 10^7 and a maximum gate current of 10^{-11} A. Results of a bias-stress measurement performed on such a TFT are summarized in Fig. S8.

Figure 10 shows the transfer and output characteristics of p-channel and n-channel organic TFTs and the transfer characteristics of a complementary inverter fabricated on flexible PEN. The AlO_x film was again prepared using a plasma power of 200 W and a duration of 60 s. The organic semiconductors that were used to fabricate these devices are 2,7-diphenyl[1]benzothieno[3,2-b]benzothiophene (DPh-BTBT)[15,72,73] for the p-channel TFTs and N,N'-bis(2,2,3,3,4,4,4-heptafluorobutyl)-1,7-dicyano-perylene-(3,4:9,10)-tetracarboxylic diimide (PTCDI-$(CN)_2$-$(CH_2C_3F_7)_2$; Polyera ActivInk N1100)[74,75] for the n-channel TFTs. The TFTs have effective charge-carrier mobilities of 0.6 cm^2/Vs (DPh-BTBT) and 0.2 cm^2/Vs (N1100). At a supply voltage of 2 V, the complementary inverter has a maximum small-signal gain of 135 and a minimum noise margin of 89% of half the supply voltage, calculated according to Ref.[76]. To our knowledge, this is the largest minimum noise margin reported to date for an organic complementary inverter fabricated on a flexible substrate (see Table 1).

Conclusion

Ultrathin, high-capacitance hybrid gate dielectrics based on oxygen-plasma-grown aluminum oxide films in combination with an alkylphosphonic acid SAM are useful for the realization of low-voltage organic TFTs. Depending on the plasma power and the duration of the plasma exposure, the thickness of the plasma-grown AlO_x films can be tuned to values between approximately 4.3 and 7.3 nm. The lower limit of the range of accessible

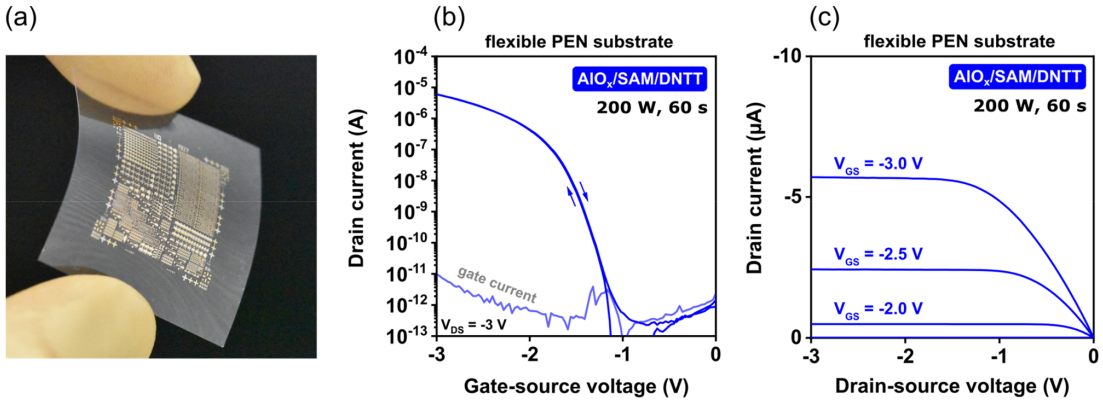


Figure 9. (**a**) Photograph of organic TFTs and circuits fabricated on a flexible polyethylene naphthalte (PEN) substrate. (**b**) Measured transfer and (**c**) output characteristics of a DNTT TFT with a channel length of 20 µm and a channel width of 100 µm on flexible PEN. The effective charge-carrier mobility is 2 cm^2/Vs.

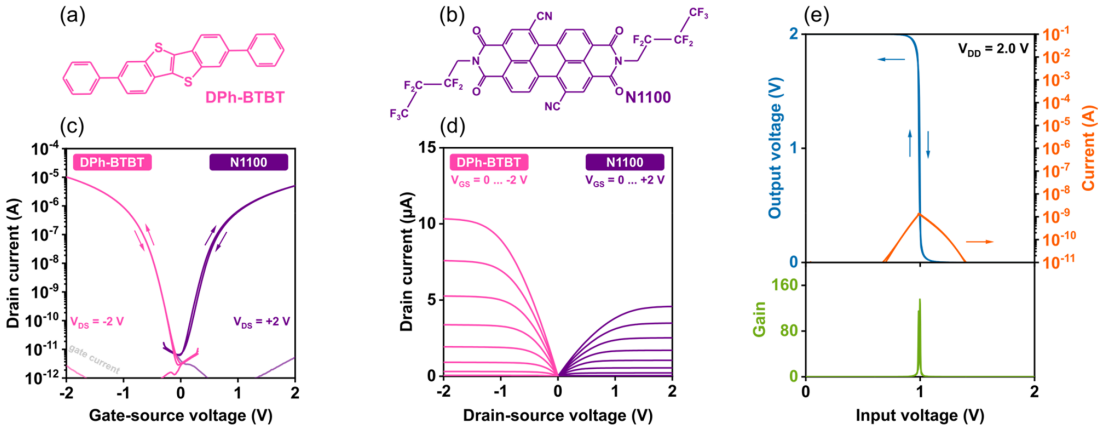


Figure 10. Chemical structures of the organic semiconductors (**a**) 2,7-diphenyl[1]benzothieno[3,2-b] benzothiophene (DPh-BTBT) and (**b**) (PTCDI-$(CN)_2$-$(CH_2C_3F_7)_2$; Polyera ActivInk N1100). (**c**) Transfer and (**d**) output characteristics of a DPh-BTBT p-channel TFT and an N1100 n-channel TFT. The TFTs have a channel length of 40 µm and a channel width of 1000 µm. (**e**) Transfer characteristics of a complementary inverter based on a DPh-BTBT p-channel TFT and an N1100 n-channel TFT fabricated on a flexible PEN substrate.

Reference	Substrate material	Gate-dielectric material	Gate-dielectric capacitance (nF/cm^2)	Small-signal gain	Supply voltage (V)	Voltage-normalized gain (V^{-1})	Noise margin (of V_{DD}/2) (%)	Measurement ambient
[76]	Glass	AlO$_x$/SAM	700	435	2	218	80	Air
[78]	Glass	Anodic Ta_2O_5	140	500	5	100	84	Vacuum
[79]	Glass	AlO$_x$/SAM	700	120	3	40	80	Air
[80]	Glass	AlO$_x$/SAM	700	376	3	125	80	Air
[81]	Glass	Al_2O_3/TMSC	65	500	4	125	92.5	Glove box
[81]	Glass	Al_2O_3/TMSC	65	740	5	148	85	Glove box
[15]	Flexible PEN	AlO$_x$/SAM	700	180	1	180	84	Air
[82]	Flexible PEN	Al_2O_3/PS	26.5	170	5	34	80	Glove box
[83]	Flexible PEN	CVD polymer	70	118	3	39	80	Glove box
This work	Flexible PEN	AlO$_x$/SAM	700	135	2	68	89	Air

Table 1. Summary of organic complementary inverters with a small-signal gain greater than 100 and a minimum noise margin of at least 80% of half the supply voltage (V_{DD}).

thicknesses is dictated by the thickness of the native aluminum oxide (approximately 3 nm) that forms spontaneously when the substrates are exposed to ambient air prior to the plasma-oxidation process, while the upper boundary is set by the inherently self-limiting oxidation kinetics of aluminum oxide. The relative permittivity of the oxygen-plasma-grown AlO_x films is approximately 8 ± 0.2, and the capacitance of the bare-AlO_x films thus falls into the range from 1 to 1.6 $\mu F/cm^2$. By allowing a high-quality monolayer of an alkylphosphonic acid with medium alkyl-chain length to self-assemble on the freshly grown AlO_x surface, a hybrid AlO_x/SAM dielectric is obtained, the capacitance of which varies between 0.7 and 0.8 $\mu F/cm^2$, depending on the plasma parameters. The leakage-current density through the hybrid AlO_x/SAM dielectrics was found to be smaller by about an order of magnitude than the current density through bare-AlO_x dielectrics. For example, for a plasma power of 200 W and a plasma duration of 60 s, the leakage-current density through the hybrid AlO_x/SAM dielectric drops below 10^{-6} A/cm^2 at voltages of $\pm$ 3 V, confirming the beneficial effect of the SAM in improving the insulating properties of the gate dielectric for low-power organic TFTs.

The effective charge-carrier mobility of DNTT TFTs with a bare-AlO_x gate dielectric is no greater than 0.6 cm^2/Vs, and shows little dependence on the plasma parameters. In TFTs with a hybrid AlO_x/SAM dielectric, carrier mobilities ranging from 1.8 to 2.3 cm^2/Vs were obtained for a number of favorable combinations of plasma power and plasma duration that produce AlO_x films with small surface roughness and thus promote the formation of high-quality SAMs and well-ordered DNTT films on these dielectrics. An important finding is that while the properties of the plasma-grown AlO_x films can be tuned over a certain range without negatively affecting the charge-transport properties in the organic-semiconductor films deposited onto them, this is only true as long as the plasma power and the plasma duration do not exceed values beyond which the quality of the plasma-grown oxide films suffers from surface damage. The largest carrier mobility equaling 2.3 cm^2/Vs was obtained for a plasma-parameter combination of 200 W and 60 s.

This work highlights the properties of oxygen-plasma-grown aluminum oxide films as part of high-capacitance gate dielectrics in low-voltage organic transistors and identifies the optimum process parameters for their fabrication.

Experimental section

Fabrication of capacitors and TFTs on silicon substrates. Metal–insulator–metal capacitors and inverted staggered (bottom-gate, top-contact) TFTs were fabricated on silicon substrates coated with 100-µm-thick thermally grown silicon dioxide. For the bottom electrode of the capacitors and the gate electrode of the TFTs, aluminum with a thickness of 30 nm and a root-mean-square surface roughness of less than 1 nm (measured by AFM[53]) was deposited by thermal evaporation in vacuum with a rate of about 20 Å/s. AlO_x films were produced by plasma oxidation in an Oxford Instruments ProLab100 Cobra system in pure oxygen with a partial pressure of 0.01 mbar using the capacitively coupled plasma mode with an excitation frequency of 13.56 MHz. We fabricated substrates with fifteen different combinations of plasma power (ranging from 10 to 300 W) and duration (ranging from 10 to 1800 s). After the plasma oxidation, each substrate was cleaved into two halves. One half was immersed into a 2-propanol solution of *n*-tetradecylphosphonic acid (PCI Synthesis, Newburyport, MA, USA) to form a self-assembled monolayer and hence a hybrid AlO_x/SAM dielectric. The other half remained without SAM (bare-AlO_x dielectric). Onto both halves of each substrate, the small-molecule semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT; Sigma Aldrich) was deposited by thermal sublimation in vacuum with a deposition rate of 0.3 Å/s and with a nominal thickness of 25 nm. During the DNTT deposition, the substrate was held at a constant temperature of 80 °C. For the top electrode of the capacitors and the source/drain contacts of the TFTs, gold with a thickness of 30 nm was deposited by thermal evaporation in vacuum with a rate of 0.3 Å/s. The metals and the DNTT were patterned using polyimide shadow masks (CADiLAC Laser, Hilpoltstein, Germany). The capacitors have an area of 200 µm × 200 µm. The TFTs have a channel length of 20 µm and a channel width of 100 µm. For each of the fifteen combinations of plasma power and plasma duration, capacitors and TFTs were fabricated on the same substrate to minimize the effects of unintentional parameter variations.

Fabrication of TFTs and complementary inverters on flexible substrates. Polyethylene naphthalate (PEN) with a thickness of 125 µm (Teonex Q65 PEN; kindly provided by William A. MacDonald, DuPont Teijin Films, Wilton, U.K.) was used as a flexible substrate. Aluminum gate electrodes (thickness: 30 nm) and AlO_x films (plasma power: 200 W, plasma duration: 60 s) were prepared as on the silicon substrates. For DNTT TFTs, an *n*-tetradecylphosphonic acid SAM was prepared as on the silicon substrates. For TFTs based on the semiconductors 2,7-diphenyl[1]benzothieno[3,2-b]benzothiophene (DPh-BTBT; Sigma Aldrich) and N,N'-bis(2,2,3,3,4,4,4-heptafluorobutyl)-1,7-dicyano-perylene-(3,4:9,10)-tetracarboxylic diimide (PTCDI-$(CN)_2$-$(CH_2C_3F_7)_2$; ActivInk N1100; Polyera Corp., Skokie, IL, U.S.A.), a mixed SAM composed of 25% *n*-octadecylphosphonic acid and 75% 12,12,13,13,14,14,15,15,16,16,17,17,18,18,18-pentadecafluorooctadecylphosphonic acid (synthesized by Matthias Schlörholz, Heidelberg, Germany) was prepared[15]. Source and drain contacts were prepared as on the silicon substrates. The DNTT TFTs have a channel length of 20 µm and a channel width of 100 µm. The DPh-BTBT and N1100 TFTs have a channel length of 40 µm and a channel width of 1000 µm.

TEM characterization. The TEM specimen was prepared on a silicon substrate by repeating the deposition of 30-nm-thick aluminum and the plasma-induced oxidation of its surface five times, each time with a different combination of plasma power and plasma duration. Preparing all five AlO_x films on the same substrate, rather than on five separate substrates, was helpful in minimizing the time required for thinning the specimen in preparation for cross-sectional microscopy. The TEM specimen was fabricated by conventional focused ion beam (FIB) lift-out using a Thermo Fisher Scientific FEI Scios DualBeam instrument equipped with a gallium source.

A platinum strip was deposited to protect the films from ion-beam damage. A lamella with a size of approximately 20 µm × 10 µm was released from the substrate and glued to a copper TEM lift-out grid. The lamella was then thinned to a thickness of less than 100 nm using an acceleration voltage of 30 kV and an ion current of initially 500 pA that was successively decreased to 100 pA. Afterwards, the lamella was cleaned using a low-voltage cleaning step with an acceleration voltage of 5 kV and an ion current of 48 pA to remove gallium-beam damage. The TEM image was recorded in bright-field (BF) mode using a Philips CM-200 FEG TEM operated with an acceleration voltage of 200 kV.

Electrical characterization. All electrical measurements were performed in ambient air at room temperature under yellow laboratory light. The capacitance measurements were performed using a Hameg HM8118 LCR meter by applying an alternating voltage with an amplitude of 0.2 V and a frequency of 1 kHz. The current–voltage measurements were performed using an Agilent 4156C Semiconductor Parameter Analyzer and the measurement software "SweepMe!" (https://sweep-me.net). The effective charge-carrier mobility was calculated by fitting the following equation to the measured transfer curve:

$$\mu_{eff} = \frac{2L}{C_{diel} W} \left(\frac{\partial \sqrt{I_D}}{\partial V_{GS}} \right)^2 \quad (3)$$

where I_D is the drain current, V_{GS} the gate-source voltage, C_{diel} the unit-area capacitance of the gate dielectric, L the channel length and W the channel width.

Surface characterization. AFM images were recorded in air using a Bruker Dimension Icon Atomic Force Microscope in peak force tapping mode (for the DNTT films) or in tapping mode (for the dielectrics). Data processing was performed using the AFM analysis software Gwyddion. Static contact-angle measurements were performed using a Krüss contact angle measurement system. The contact angles of water and hexadecane on the AlO_x dielectrics were measured immediately after the plasma treatment of the aluminum films. The contact angles of water and hexadecane on the AlO_x/SAM hybrid dielectrics were measured immediately after the SAM treatment. The surface energies were calculated using the Owens–Wendt method[77].

Received: 6 November 2020; Accepted: 28 February 2021
Published online: 18 March 2021

References

1. Noda, M. *et al.* An OTFT-driven rollable OLED display. *J. Soc. Inf. Disp.* **19**, 316–322 (2011).
2. Someya, T. *et al.* Conformable, flexible, large-area networks of pressure and thermal sensors with organic transistor active matrixes. *Proc. Natl. Acad. Sci.* **102**, 12321 (2005).
3. Sekitani, T., Zschieschang, U., Klauk, H. & Someya, T. Flexible organic transistors and circuits with extreme bending stability. *Nat. Mater.* **9**, 1015–1022 (2010).
4. Wang, B. *et al.* High-k Gate dielectrics for emerging flexible and stretchable electronics. *Chem. Rev.* **118**, 5690–5754 (2018).
5. Rogers, J. A. *et al.* Paper-like electronic displays: Large-area rubber- stamped plastic sheets of electronics and microencapsulated electrophoretic inks. *Proc. Natl. Acad. Sci.* **98**, 4835–4840 (2001).
6. Yoon, M.-H., Yan, H., Facchetti, A. & Marks, T. J. Low-voltage organic field-effect transistors and inverters enabled by ultrathin cross-linked polymers as gate dielectrics. *J. Am. Chem. Soc.* **127**, 10388–10395 (2005).
7. Yang, S. Y., Kim, S. H., Shin, K., Jeon, H. & Park, C. E. Low-voltage pentacene field-effect transistors with ultrathin polymer gate dielectrics. *Appl. Phys. Lett.* **88**, 173507 (2006).
8. Koo, J. B. *et al.* Low-voltage and high-gain pentacene inverters with plasma-enhanced atomic-layer-deposited gate dielectrics. *Appl. Phys. Lett.* **89**, 033511 (2006).
9. Chang, M. F., Lee, P. T., McAlister, S. P. & Chin, A. Low subthreshold swing HfLaO/pentacene organic thin-film transistors. *IEEE Electron. Dev. Lett.* **29**, 215–217 (2008).
10. Yoon, M.-H., Facchetti, A. & Marks, T. J. σ–π molecular dielectric multilayers for low-voltage organic thin-film transistors. *Proc. Natl. Acad. Sci.* **102**, 4678 (2005).
11. DiBenedetto, S. A., Frattarelli, D., Ratner, M. A., Facchetti, A. & Marks, T. J. Vapor phase self-assembly of molecular gate dielectrics for thin film transistors. *J. Am. Chem. Soc.* **130**, 7528–7529 (2008).
12. Kelley, T. W. *et al.* High-performance OTFTs using surface-modified alumina dielectrics. *J. Phys. Chem. B* **107**, 5877–5881 (2003).
13. Klauk, H., Zschieschang, U., Pflaum, J. & Halik, M. Ultralow-power organic complementary circuits. *Nature* **445**, 745–748 (2007).
14. Jinno, H. *et al.* Low operating voltage organic transistors and circuits with anodic titanium oxide and phosphonic acid self-assembled monolayer dielectrics. *Org. Electron.* **40**, 58–64 (2017).
15. Zschieschang, U., Bader, V. P. & Klauk, H. Below-one-volt organic thin-film transistors with large on/off current ratios. *Org. Electron.* **49**, 179–186 (2017).
16. Haase, K. *et al.* Solution shearing of a high-capacitance polymer dielectric for low-voltage organic transistors. *Adv. Electron. Mater.* **5**, 1900067 (2019).
17. Halik, M. *et al.* Low-voltage organic transistors with an amorphous molecular gate dielectric. *Nature* **431**, 963–966 (2004).
18. Xiong, W., Guo, Y., Zschieschang, U., Klauk, H. & Murmann, B. A 3-V, 6-bit C-2C digital-to-analog converter using complementary organic thin-film transistors on glass. *IEEE J. Solid-State Circuits* **45**, 1380–1388 (2010).
19. Abdinia, S. *et al.* Organic CMOS line drivers on foil. *IEEE J. Disp. Technol.* **11**, 564–569 (2015).
20. Stucchi, E., Dell'Erba, G., Colpani, P., Kim, Y.-H. & Caironi, M. Low-voltage, printed, all-polymer integrated circuits employing a low-leakage and high-yield polymer dielectric. *Adv. Electron. Mater.* **4**, 1800340 (2018).
21. Zschieschang, U. & Klauk, H. Low-voltage organic transistors with steep subthreshold slope fabricated on commercially available paper. *Org. Electron.* **25**, 340–344 (2015).
22. Lei, T. *et al.* Biocompatible and totally disintegrable semiconducting polymer for ultrathin and ultralightweight transient electronics. *Proc. Natl. Acad. Sci.* **114**, 5107–5112 (2017).

23. Kraft, U. *et al.* Low-voltage, high-frequency organic transistors and unipolar and complementary ring oscillators on paper. *Adv. Electron. Mater.* **5**, 1800453 (2019).
24. Borchert, J. W. *et al.* Small contact resistance and high-frequency operation of flexible low-voltage inverted coplanar organic transistors. *Nat. Commun.* **10**, 1119 (2019).
25. Aghamohammadi, M. *et al.* Threshold-voltage shifts in organic transistors due to self-assembled monolayers at the dielectric: Evidence for electronic coupling and dipolar effects. *ACS Appl. Mater. Interfaces* **7**, 22775–22785 (2015).
26. Majewski, L. A., Schroeder, R., Voigt, M. & Grell, M. High performance organic transistors on cheap, commercial substrates. *J. Phys. D* **37**, 3367–3372 (2004).
27. Majewski, L. A., Schroeder, R. & Grell, M. One volt organic transistor. *Adv. Mater.* **17**, 192–196 (2005).
28. Kaltenbrunner, M. *et al.* An ultra-lightweight design for imperceptible plastic electronics. *Nature* **499**, 458–463 (2013).
29. Gupta, S. *et al.* Ozone oxidation methods for aluminum oxide formation: Application to low-voltage organic transistors. *Org. Electron.* **21**, 132–137 (2015).
30. Chinnam, K. C., Gupta, S. & Gleskova, H. Aluminium oxide prepared by UV/ozone exposure for low-voltage organic thin-film transistors. *J. Non. Cryst. Solids* **358**, 2512–2515 (2012).
31. Jedaa, A. *et al.* The impact of self-assembled monolayer thickness in hybrid gate dielectrics for organic thin-film transistors. *Org. Electron.* **10**, 1442–1447 (2009).
32. Kwon, J., Lee, Y., Jo, Y. & Jung, S. Fabrication of ultrathin low-voltage-driven printed organic circuits with anodized gate islands. *Org. Electron.* **62**, 77–81 (2018).
33. Yogev, S. *et al.* Fermi level pinning by gap states in organic semiconductors. *Phys. Rev. Lett.* **110**, 036803 (2013).
34. Borchert, J. W. *et al.* Flexible low-voltage high-frequency organic thin-film transistors. *Sci. Adv.* **6**, 5156 (2020).
35. Leshanskaya, L. I. *et al.* Towards understanding the origin of the hysteresis effects and threshold voltage shift in organic field-effect transistors based on the electrochemically grown AlO_x dielectric. *Thin Solid Films* **649**, 7–11 (2018).
36. Ulman, A. Formation and structure of self-assembled monolayers. *Chem. Rev.* **96**, 1533–1554 (1996).
37. Luschtinetz, R. *et al.* Adsorption of phosphonic and ethylphosphonic acid on aluminum oxide surfaces. *Surf. Sci.* **602**, 1347–1359 (2008).
38. Kraft, U. *et al.* Fluoroalkylphosphonic acid self-assembled monolayer gate dielectrics for threshold-voltage control in low-voltage organic thin-film transistors. *J. Mater. Chem.* **20**, 6416 (2010).
39. Acton, O. *et al.* Simultaneous modification of bottom-contact electrode and dielectric surfaces for organic thin-film transistors through single-component spin-cast monolayers. *Adv. Funct. Mater.* **21**, 1476–1488 (2011).
40. Acharya, R., Peng, B., Chan, P. K. L., Schmitz, G. & Klauk, H. Achieving ultralow turn-on voltages in organic thin-film transistors: Investigating fluoroalkylphosphonic acid self-assembled monolayer hybrid dielectrics. *ACS Appl. Mater. Interfaces* **11**, 27104–27111 (2019).
41. Hirata, I. *et al.* High-resolution spatial control of the threshold voltage of organic transistors by microcontact printing of alkyl and fluoroalkylphosphonic acid self-assembled monolayers. *Org. Electron.* **26**, 239–244 (2015).
42. Fukuda, K. *et al.* Effects of the alkyl chain length in phosphonic acid self-assembled monolayer gate dielectrics on the performance and stability of low-voltage organic thin-film transistors. *Appl. Phys. Lett.* **95**, 203301 (2009).
43. Acton, O. *et al.* Dielectric surface-controlled low-voltage organic transistors via n-alkyl phosphonic acid self-assembled monolayers on high-k metal oxide. *ACS Appl. Mater. Interfaces* **2**, 511–520 (2010).
44. Hannah, S. *et al.* Interplay between vacuum-grown monolayers of alkylphosphonic acids and the performance of organic transistors based on Dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene. *ACS Appl. Mater. Interfaces* **8**, 25405–25414 (2016).
45. Gleskova, H., Gupta, S. & Šutta, P. Structural changes in vapour-assembled n-octylphosphonic acid monolayer with post-deposition annealing: Correlation with bias-induced transistor instability. *Org. Electron.* **14**, 3000–3006 (2013).
46. Gupta, S. & Gleskova, H. Dry growth of n-octylphosphonic acid monolayer for low-voltage organic thin-film transistors. *Org. Electron.* **14**, 354–361 (2013).
47. Hauffman, T., Hubin, A. & Terryn, H. Study of the self-assembling of n-octylphosphonic acid layers on aluminum oxide from ethanolic solutions. *Surf. Interface Anal.* **45**, 1435–1440 (2013).
48. Bauer, T. *et al.* Phosphonate-and carboxylate-based self-assembled monolayers for organic devices: A theoretical study of surface binding on aluminum oxide with experimental support. *ACS Appl. Mater. Interfaces* **5**, 6073 (2013).
49. Yamamoto, T. & Takimiya, K. Facile synthesis of highly π-extended heteroarenes, dinaphtho[2,3-b: 2',3'-f]chalcogenopheno[3,2-b] chalcogenophenes, and their application to field-effect transistors. *J. Am. Chem. Soc.* **129**, 2224–2225 (2007).
50. Zschieschang, U. *et al.* Dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) thin-film transistors with improved performance and stability. *Org. Electron.* **12**, 1370–1375 (2011).
51. Milvich, J. *et al.* Flexible low-voltage organic phototransistors based on air-stable dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT). *Org. Electron.* **20**, 63–68 (2015).
52. Evertsson, J. *et al.* The thickness of native oxides on aluminum alloys and single crystals. *Appl. Surf. Sci.* **349**, 826–832 (2015).
53. Geiger, M. *et al.* Effect of the degree of the gate-dielectric surface roughness on the performance of bottom-gate organic thin-film transistors. *Adv. Mater. Interfaces* **7**, 1902145 (2020).
54. Harman, A. K., Ninomiya, S. & Adachi, S. Optical constants of sapphire (α-Al_2O_3) single crystals. *J. Appl. Phys.* **76**, 8032–8036 (1994).
55. Groner, M. D., Fabreguette, F. H., Elam, J. W. & George, S. M. Low-temperature Al_2O_3 atomic layer deposition. *Chem. Mater.* **16**, 639–645 (2004).
56. Acharya, J., Wilt, J., Liu, B. & Wu, J. Probing the dielectric properties of ultrathin Al/Al_2O_3/Al trilayers fabricated using in situ sputtering and atomic layer deposition. *ACS Appl. Mater. Interfaces* **10**, 3112–3120 (2018).
57. Cabrera, N. & Mott, N. F. Theory of the oxidation of metals. *Rep. Prog. Phys.* **12**, 163–184 (1949).
58. Cai, N., Zhou, G., Müller, K. & Starr, D. E. Tuning the limiting thickness of a thin oxide layer on Al(111) with oxygen gas pressure. *Phys. Rev. Lett.* **107**, 035502 (2011).
59. Baran, J. D., Grönbeck, H. & Hellman, A. Mechanism for limiting thickness of thin oxide films on aluminum. *Phys. Rev. Lett.* **112**, 146103 (2014).
60. Kim, K. D. & Song, C. K. Low voltage pentacene thin film transistors employing a self-grown metal-oxide as a gate dielectric. *Appl. Phys. Lett.* **88**, 233508 (2006).
61. Kang, H., Han, K.-K., Park, J.-E. & Lee, H. H. High mobility, low voltage polymer transistor. *Org. Electron.* **8**, 460–464 (2007).
62. Chua, L.-L. *et al.* General observation of n-type field-effect behaviour in organic semiconductors. *Nature* **434**, 194–199 (2005).
63. Kettner, M., Zhou, M., Brill, J., Blom, P. W. M. & Weitz, R. T. Complete suppression of bias-induced threshold voltage shift below 273 K in solution-processed high-performance organic transistors. *ACS Appl. Mater. Interfaces* **10**, 35449–35454 (2018).
64. Hulea, I. N. *et al.* Tunable Fröhlich polarons in organic single-crystal transistors. *Nat. Mater.* **5**, 982–986 (2006).
65. Chung, Y. *et al.* Controlling electric dipoles in nanodielectrics and its applications for enabling air-stable n-channel organic transistors. *Nano Lett.* **11**, 1161–1165 (2011).

66. Pernstich, K. P. *et al.* Threshold voltage shift in organic field effect transistors by dipole monolayers on the gate insulator. *J. Appl. Phys.* **96**, 6431–6438 (2004).
67. Fontaine, P. *et al.* Octadecyltrichlorosilane monolayers as ultrathin gate insulating films in metal-insulator-semiconductor devices. *Appl. Phys. Lett.* **62**, 2256–2258 (1993).
68. Li, J., Du, J., Xu, J., Chan, H. L. W. & Yan, F. The influence of gate dielectrics on a high-mobility n-type conjugated polymer in organic thin-film transistors. *Appl. Phys. Lett.* **100**, 033301 (2012).
69. Chen, H., Zhang, W., Li, M., He, G. & Guo, X. Interface engineering in organic field-effect transistors: Principles, applications, and perspectives. *Chem. Rev.* **120**, 2879–2949 (2020).
70. Klapetek, P., Nečas, D., Anderson, C., Necas, D. & Anderson, C. *Gwyddion User Guide* (Springer, 2013).
71. Gredig, T., Silverstein, E. A. & Byrne, M. P. Height-height correlation function to determine grain size in iron phthalocyanine thin films. *J. Phys. Conf. Ser.* **417**, 012069 (2013).
72. Takimiya, K. *et al.* 2,7-Diphenyl[1]benzothieno[3,2-b]benzothiophene, a new organic semiconductor for air-stable organic field-effect transistors with mobilities up to 2.0 $cm^2 V^{-1} s^{-1}$. *J. Am. Chem. Soc.* **128**, 12604–12605 (2006).
73. Moon, H., Cho, H., Kim, M., Takimiya, K. & Yoo, S. Towards colorless transparent organic transistors: Potential of benzothieno[3,2-b]benzothiophene-based wide-Gap semiconductors. *Adv. Mater.* **26**, 3105–3110 (2014).
74. Jones, B. A. *et al.* High-mobility air-stable n-type semiconductors with processing versatility: Dicyanoperylene-3,4:9,10-bis(dicarboximides). *Angew. Chem. Int. Ed.* **43**, 6363–6366 (2004).
75. Soeda, J. *et al.* High electron mobility in air for N, N′-1H,1H- perfluorobutyldicyanoperylene carboxydi-imide solution-crystallized thin-film transistors on hydrophobic surfaces. *Adv. Mater.* **23**, 3681–3685 (2011).
76. Zschieschang, U. *et al.* Mixed self-assembled monolayer gate dielectrics for continuous threshold voltage control in organic transistors and circuits. *Adv. Mater.* **22**, 4489–4493 (2010).
77. Owens, D. K. & Wendt, R. C. Estimation of the surface free energy of polymers. *J. Appl. Polym. Sci.* **13**, 1741–1747 (1969).
78. Tatemichi, S., Ichikawa, M., Kato, S., Koyama, T. & Taniguchi, Y. Low-voltage, high-gain, and high-mobility organic complementary inverters based on N, N′-ditridecyl-3,4,9,10-perylenetetracarboxylic diimide and pentacene. *Phys. Stat. Sol. RRL* **2**, 47–49 (2008).
79. Zschieschang, U., Halik, M. & Klauk, H. Microcontact-printed self-assembled monolayers as ultrathin gate dielectrics in organic thin-film transistors and complementary circuits. *Langmuir* **24**, 1665 (2008).
80. Martens, S. C., Zschieschang, U., Wadepohl, H., Klauk, H. & Gade, L. H. Tetrachlorinated tetraazaperopyrenes (TAPPs): Highly fluorescent dyes and semiconductors for air-stable organic n-channel transistors and complementary circuits. *Chem. Eur. J.* **18**, 3498 (2012).
81. Petritz, A. *et al.* Cellulose-derivative-based gate dielectric for high-performance organic complementary inverters. *Adv. Mater.* **27**, 7645 (2015).
82. Zhang, X., Potscavage, W. J., Choi, S. & Kippelen, B. Low-voltage flexible organic complementary inverters with high noise margin and high dc gain. *Appl. Phys. Lett.* **94**, 043312 (2009).
83. Seong, H. *et al.* Organic inverters: A low-voltage organic complementary inverter with high operation stability and flexibility using an ultrathin iCVD polymer dielectric and a hybrid encapsulation layer. *Adv. Electron. Mater.* **2**, 1500385 (2016).

Acknowledgements
This work is partially funded by the German Research Foundation (DFG) under the Grants KL 2223/6-2 (SPP FFlexCom), KL 2223/7-1, and INST 35/1429-1 (SFB 1249).

Author contributions
M.G., H.K. and R.A. devised the experimental details of the study. M.G., U.Z. and R.A. fabricated the devices and samples and performed electrical measurements and surface characterization. M.H, T.R. and J.W. supervised the Oxford Instruments ProLab100 Cobra system and gave technical assistance. H.S. and G.S. performed the TEM characterization and gave technical assistance. M.G., H.K. and R.A. wrote the manuscript. R.T.W., G.S., H.K., G.S. and R.A. supervised the project. All the authors discussed the results and contributed to the development of the final manuscript.

Funding
Open Access funding enabled and organized by Projekt DEAL.

Competing interests
The authors declare no competing interests.

Additional information
Supplementary Information The online version contains supplementary material available at https://doi.org/10.1038/s41598-021-85517-7.

Correspondence and requests for materials should be addressed to M.G. or R.A.

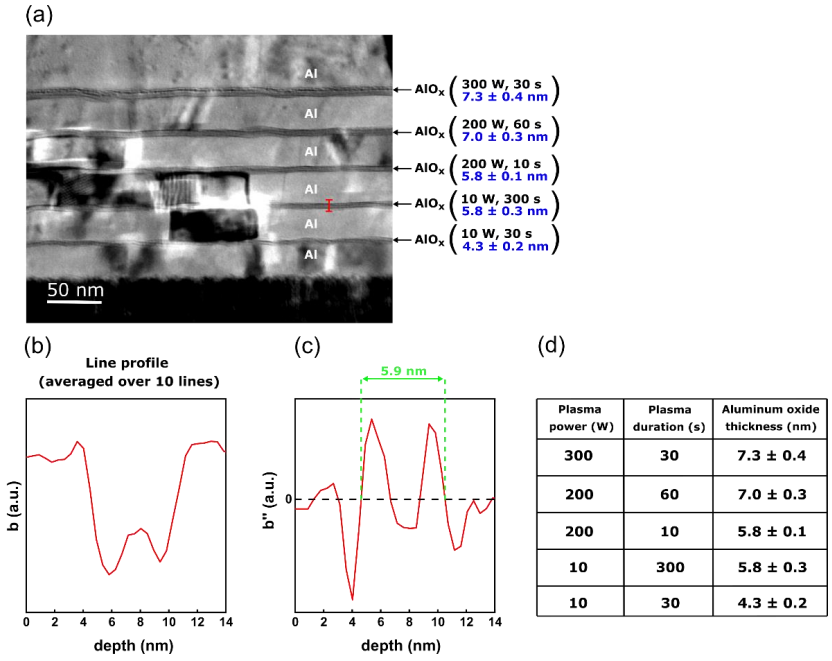
Reprints and permissions information is available at www.nature.com/reprints.

Publisher's note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Supplementary Information

Optimizing the plasma oxidation of aluminum gate electrodes for ultrathin gate oxides in organic transistors

Michael Geiger, Marion Hagel, Thomas Reindl, Jürgen Weis,
R. Thomas Weitz, Helena Solodenko,
Guido Schmitz, Ute Zschieschang, Hagen Klauk, Rachana Acharya



Plasma power (W)	Plasma duration (s)	Aluminum oxide thickness (nm)
300	30	7.3 ± 0.4
200	60	7.0 ± 0.3
200	10	5.8 ± 0.1
10	300	5.8 ± 0.3
10	30	4.3 ± 0.2

Figure S1: Analysis of the cross-sectional TEM image to extract the thicknesses of the AlO_x films produced using five different combinations of plasma power and plasma duration. From the digital data representing the TEM image (a), a depth profile (having a line width of 10 pixels) through the AlO_x film (starting and ending a few nanometers above and below the Al/AlO_x interfaces) representing the average pixel brightness (denoted as "b") was extracted using the image software Gwyddion (b). In the depth profile, the materials Al and AlO_x are distinguished by larger and smaller values of the pixel brightness b, respectively. The second derivative of b with respect to the depth was calculated and plotted as a function of depth to identify the points of inflection (b" = 0) in the depth profile, and the distance between these points was measured as the thickness of the AlO_x film (c). For each of the five AlO_x films, this process was repeated 10 times in various locations across the TEM image, and the averaged results were tabulated (d).

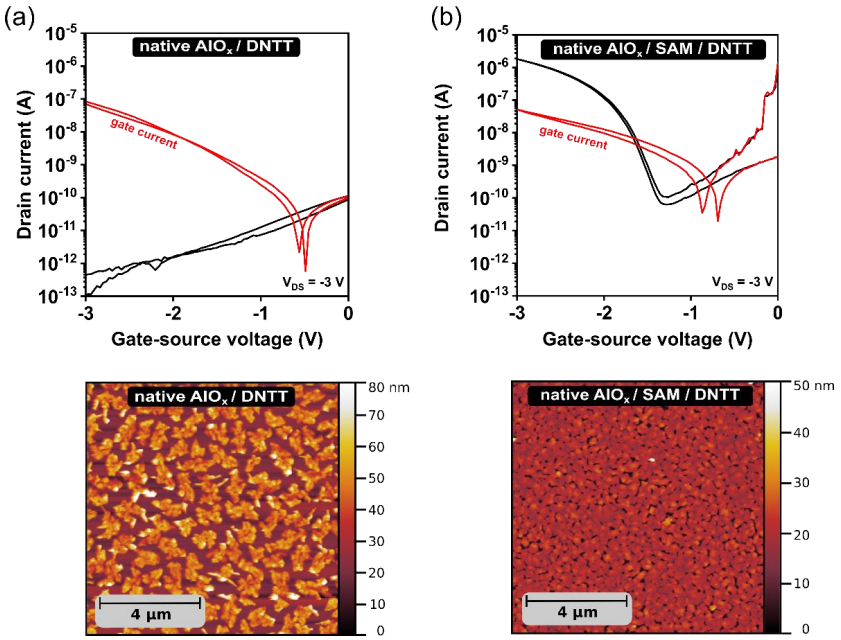


Figure S2: Transfer characteristics and gate currents of DNTT TFTs fabricated using native aluminum oxide (obtained without plasma process) either as the gate dielectric (a) or as part of a hybrid AlO_x/SAM gate dielectric (b). As can be seen, the native aluminum oxide alone is insufficient as a gate dielectric, as the TFTs either do not show a field effect (a) or suffer from gate currents exceeding 10 nA at a gate-source voltage of -2 V. AFM images of DNTT films deposited onto the bare native AlO_x and the hybrid AlO_x/SAM gate dielectric are also shown.

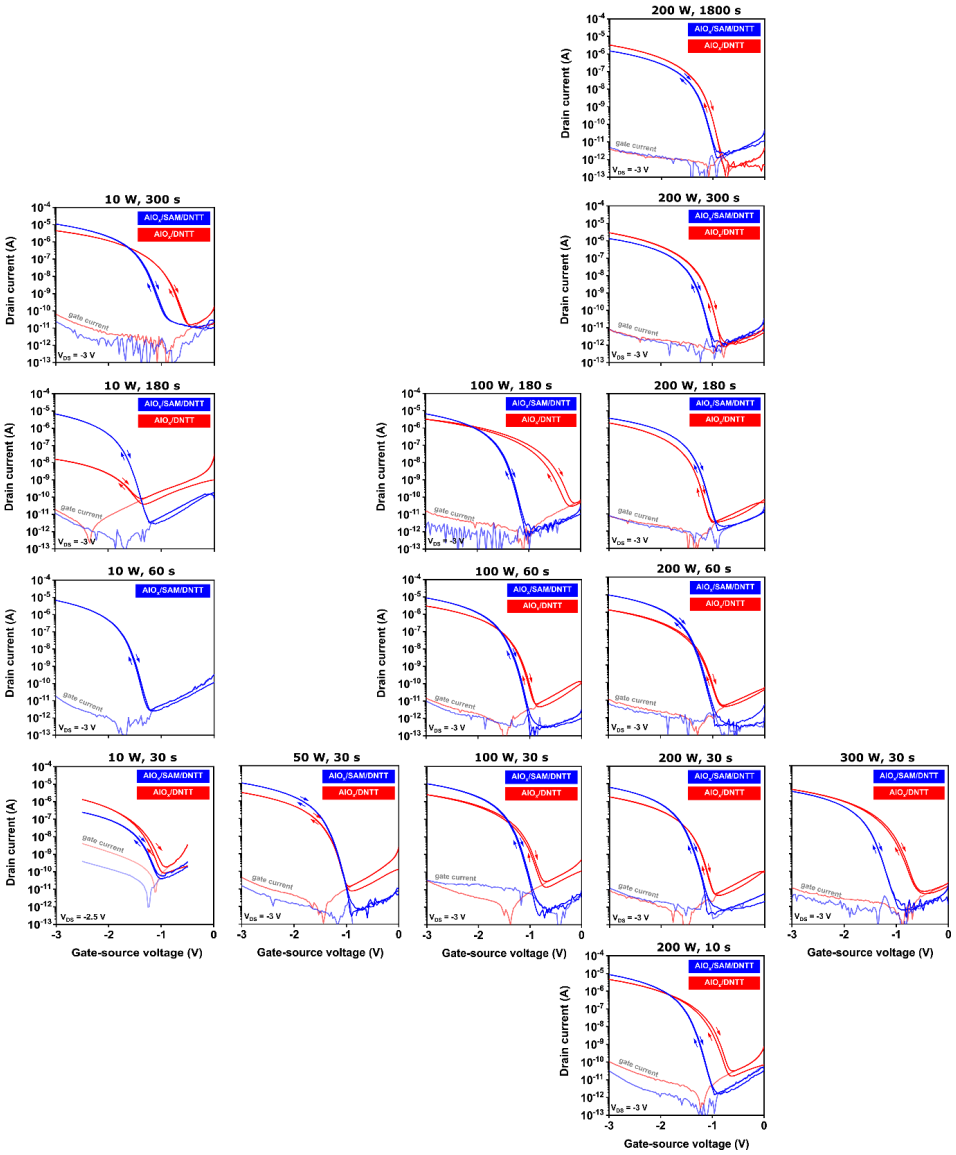


Figure S3: Transfer characteristics and gate currents of DNTT TFTs fabricated using either a bare-AlO_x gate dielectric (red curves) or a hybrid AlO_x/SAM gate dielectric (blue curves) for all fifteen combinations of the plasma power and plasma duration.

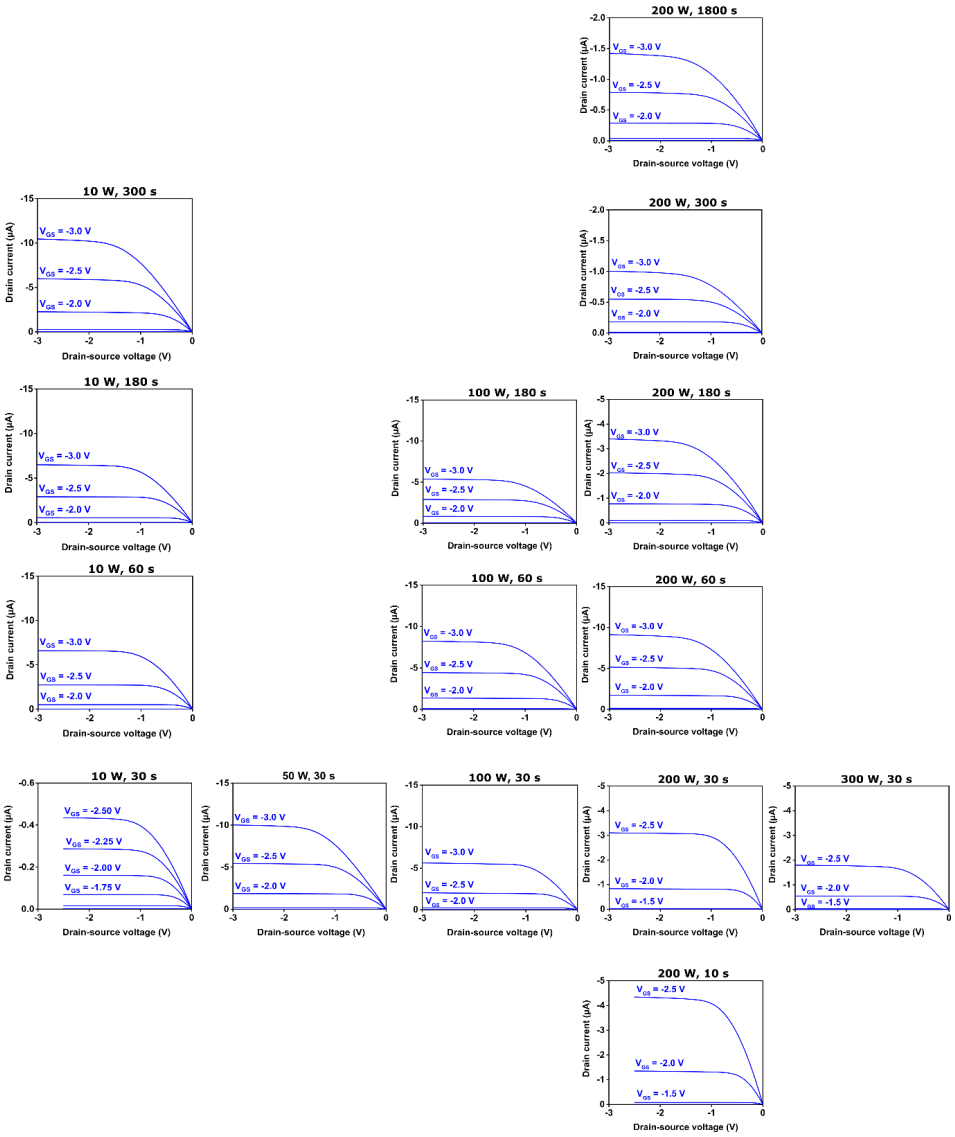


Figure S4: Output characteristics of DNTT TFTs fabricated using a hybrid AlO_x/SAM gate dielectric for all fifteen combinations of plasma power and plasma duration.

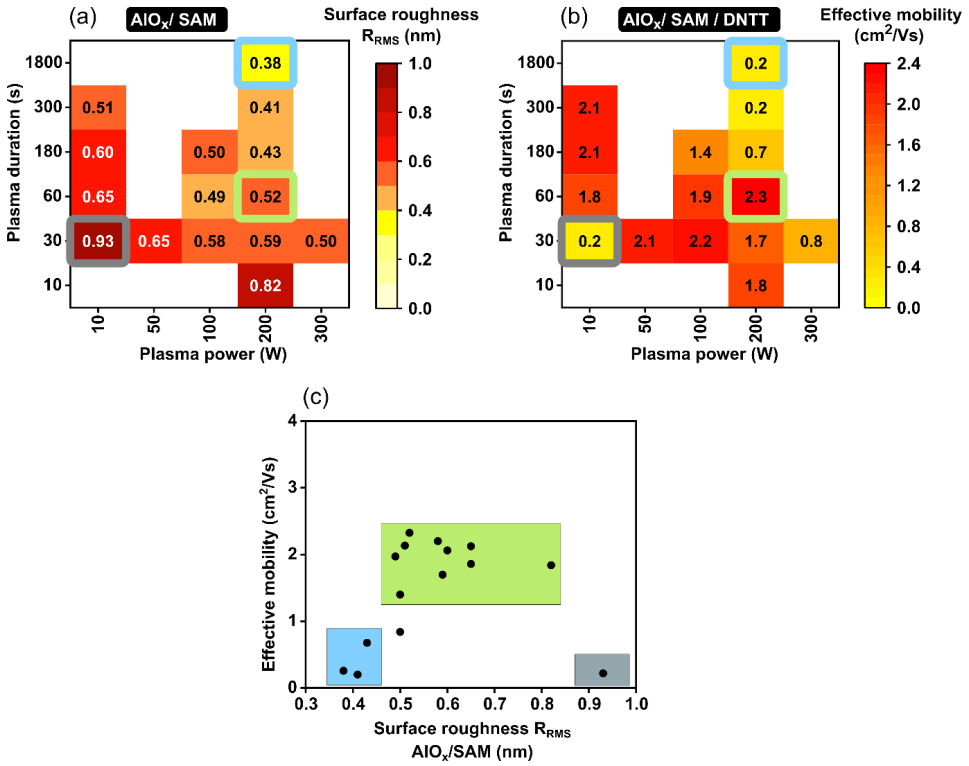


Figure S5: (a) Root-mean-square surface roughness of hybrid AlO_x/SAM dielectrics as a function of plasma power and plasma duration. (b) Carrier mobilities extracted from the measured transfer characteristics of DNTT TFTs fabricated using a hybrid AlO_x/SAM gate dielectric as a function of plasma power and plasma duration. (c) Carrier mobility plotted as a function of the RMS surface roughness.

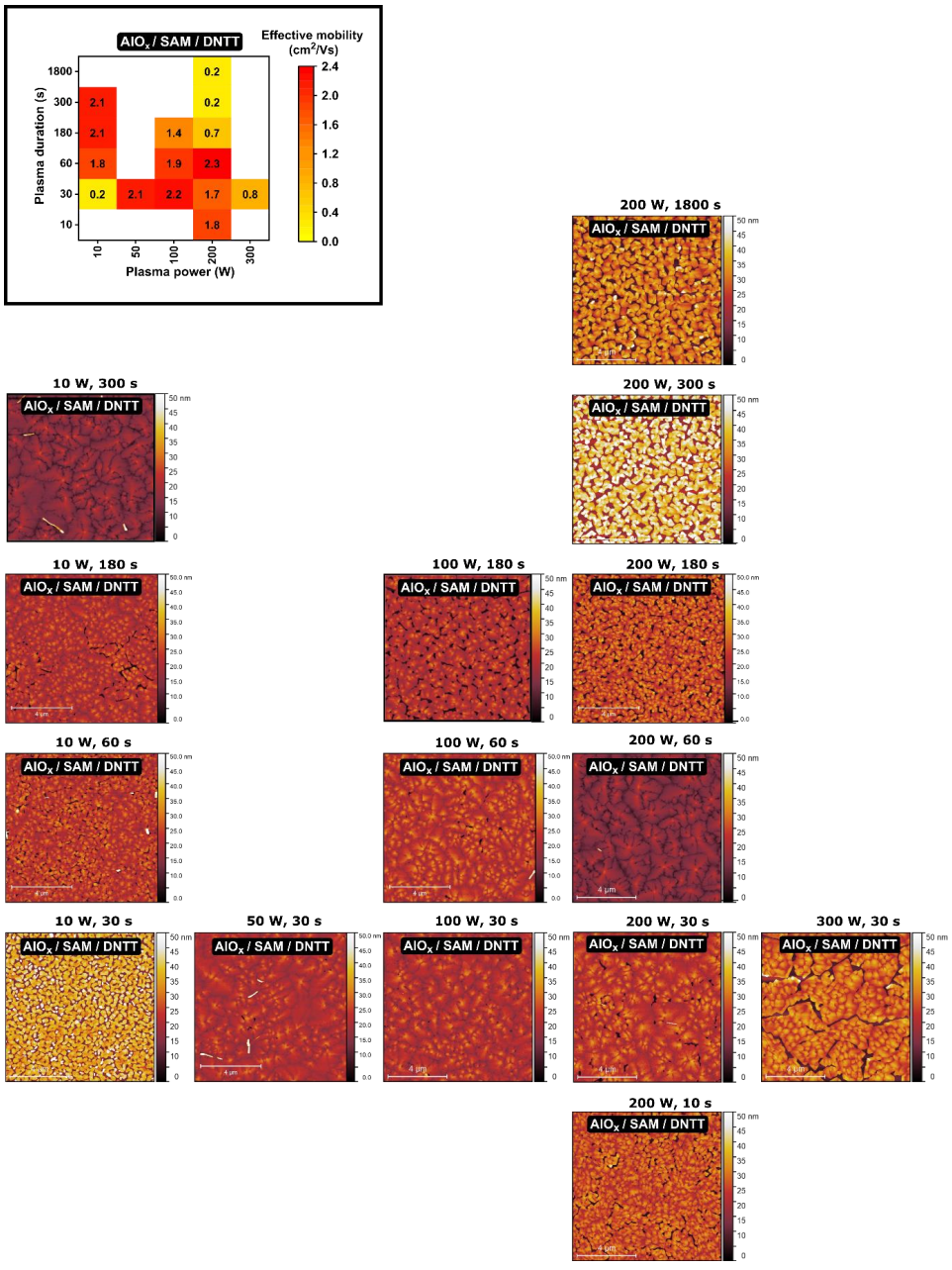


Figure S6: AFM images of DNTT films deposited onto hybrid AlO_x/SAM dielectrics for all fifteen combinations of plasma power and plasma duration.

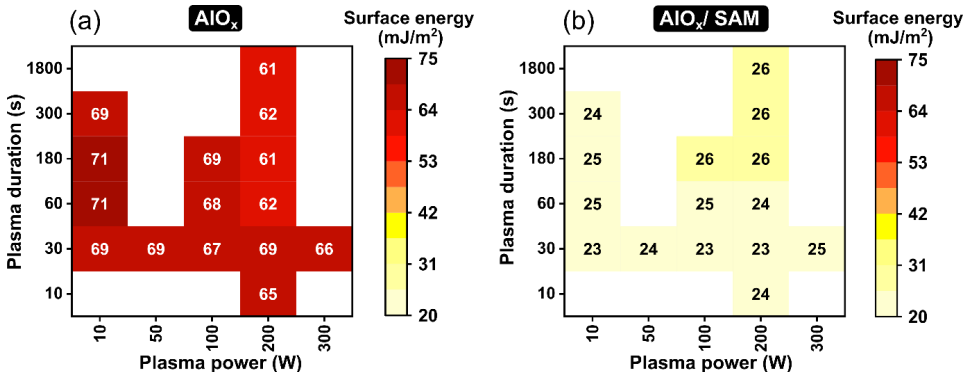


Figure S7: Surface energy of bare-AlO_x dielectrics (a) and hybrid AlO_x/SAM dielectrics as a function of plasma power and plasma duration.

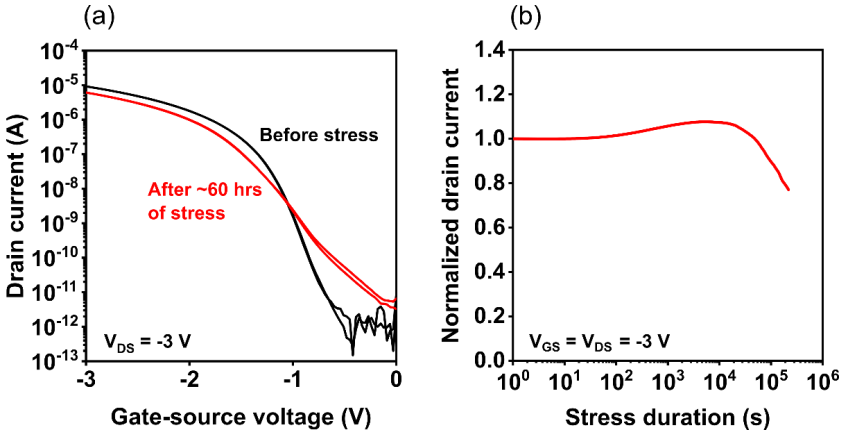


Figure S8: (a) Transfer characteristics of a DNTT TFT measured before and after bias stress. (b) Drain current measured continuously over a period of 60 hours during bias stress with gate-source and drain-source voltages of -3 V.

Chapter 6

Subthreshold Swing of 59 mV/decade in Nanoscale Flexible Ultralow-Voltage Organic Transistors

6.1 Discussion

6.1.1 State-of-the-Art

A successful approach for high-capacitance gate dielectrics for low-voltage organic TFTs is a hybrid dielectric consisting of an insulating thin metal oxide and a SAM. The combination of an aluminum gate electrode and plasma-grown aluminum oxide complemented with an aliphatic phosphonic acid has been studied intensively (see also Chapter 5) and many high-quality organic TFTs and circuits based on this gate stack have been fabricated.[7,22,24,128,146,147] As pointed out in Chapter 5, the plasma-assisted oxidation of the surface of metal gate electrodes brings several advantages compared to the fabrication of metal-oxide dielectrics by anodic oxidation or atomic layer deposition. However, apart from aluminum oxide there have been no reports on high-quality plasma-grown metal oxides for the use as gate dielectrics in organic TFTs by now.
Majewski et al. and Jinno et al. have demonstrated that titanium oxide (TiO_x), grown by anodic oxidation on the surface of titanium gate electrodes, can be employed in hybrid TiO_x/SAM dielectrics.[148–150] In these reports, a unit-area capacitance close to $1\,\mu F/cm^2$ was achieved which allowed organic TFTs to be operated with very low voltages of about 1 V. In typical inorganic dielectrics the permittivity is inversely proportional to the band gap.[116,151] Thus, it is challenging to obtain small leakage currents and large on/off current ratios in TFTs in which titanium oxide is employed as part of the gate dielectric.

6.1.2 Objective

The objective of this study is to fabricate high-quality hybrid TiO_x/SAM dielectrics by combining the advantages of the plasma-assisted oxidation process of the gate metal with

the beneficial material properties of titanium oxide. The fabrication process as well as the surface and electrical properties of the bare-TiO_x films and the hybrid TiO_x/SAM dielectrics are investigated and optimized in terms of a high capacitance and yet low charge leakage. The use of plasma-grown TiO_x films as the first component in hybrid TiO_x/SAM dielectrics for flexible ultralow-voltage organic TFTs and circuits is explored and evaluated.

6.1.3 Conclusion

In this study, it was shown that it is possible to deposit thin titanium films on flexible PEN substrates by thermal evaporation in vacuum. The surface roughness of the resulting titanium films is just as small as the surface roughness of the PEN substrates. Analysis of cross-sectional TEM measurements of titanium oxide films, grown by plasma-assisted oxidation of the surface of titanium films, yielded thickness values of the TiO_x films ranging from 4.7 to 6.7 nm, depending on the duration of the plasma exposure. A value for the permittivity of the plasma-grown titanium oxide of 14 ± 1 was extracted.
Hybrid TiO_x/SAM dielectrics composed of an optimized titanium oxide film complemented with an *n*-tetradecylphosphonic acid SAM exhibited leakage-current densities close to $10^{-6}\,A/cm^2$ at a voltage of $-1\,V$ and a unit-area capacitance of $1.1\,\mu F/cm^2$. These values represent a remarkable combination of high unit-area capacitance and low charge leakage for gate dielectrics.
Flexible ultralow-voltage DPh-BTBT TFTs with the novel hybrid TiO_x/SAM gate dielectric showed excellent electrical performance for a wide range of channel lengths as small as 0.7 µm including a subthreshold swing of (59 ± 1) mV/decade (which is within the measurement error of the theoretical limit), a width-normalized transconductance of 0.6 S/m and an on/off current ratio of 10^7 for a gate-source-voltage range of 1 V. Flexible TFTs with the hybrid TiO_x/SAM gate dielectric based on the organic semiconductor DPh-DNTT exhibited a width-normalized contact resistance of $(15 \pm 5)\,\Omega$cm and a threshold-voltage shift of 10 mV after continuous bias stress for 72 hours.
The combination of DPh-DNTT TFTs with a Ti/TiO_x/SAM gate stack (normally-on TFT) and with an Al/AlO_x/SAM gate stack (normally-off TFT) made the fabrication of zero-V_{GS} inverters possible. These inverters showed small-signal gains ranging from 180 at a supply voltage of 0.4 V to 1900 at a supply voltage of 1 V. At a supply voltage of 1 V the inverters had a noise margin as large as 79 % of half the supply voltage. The results of this study demonstrate that the use of plasma-grown titanium oxide in a hybrid TiO_x/SAM dielectric can provide both high capacitance and low charge leakage and promotes excellent electrical performance in flexible ultralow-voltage organic TFTs and circuits.

6.2 Published Article

Subthreshold Swing of 59 mV/decade in Nanoscale Flexible Ultralow-Voltage Organic Transistors

Michael Geiger[1], Robin Lingstädt[1], Tobias Wollandt[1], Julia Deuschle[1], Ute Zschieschang[1], Florian Letzkus[2], Joachim N. Burghartz[2], Peter A. van Aken[1], R. Thomas Weitz[3], Hagen Klauk[1]

[1] *Max Planck Institute for Solid State Research, Heisenbergstr. 1, 70569 Stuttgart, Germany*
[2] *Institute for Microelectronics Stuttgart (IMS CHIPS), Allmandring 30A, 70569 Stuttgart, Germany*
[3] *1st Institute of Physics, Faculty of Physics, University of Göttingen, Friedrich-Hund-Platz 1, 37077 Göttingen, Germany*

***Advanced Electronic Materials*, 2101215 (2022)**

DOI: 10.1002/aelm.202101215

reprinted on pages 92–110

RESEARCH ARTICLE

ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

Subthreshold Swing of 59 mV decade^{-1} in Nanoscale Flexible Ultralow-Voltage Organic Transistors

Michael Geiger, Robin Lingstädt, Tobias Wollandt, Julia Deuschle, Ute Zschieschang, Florian Letzkus, Joachim N. Burghartz, Peter A. van Aken, R. Thomas Weitz, and Hagen Klauk**

Organic thin-film transistors (TFTs) that provide subthreshold swings near the theoretical limit together with large on/off current ratios at very low operating voltages require high-capacitance gate dielectrics with a vanishingly small defect density. A promising approach to the fabrication of such dielectrics at temperatures sufficiently low to allow TFT fabrication on polymeric substrates are hybrid dielectrics consisting of a thin metal oxide layer in combination with a molecular self-assembled monolayer (SAM). Here, the electrical and surface properties of titanium oxide produced by the plasma-assisted oxidation of the surface of vacuum-deposited titanium gate electrodes and its use as the first component of a hybrid TiO_x/SAM gate dielectric in flexible organic TFTs are investigated. These transistors have a gate-dielectric capacitance of about 1 μF cm^{-2}, a subthreshold swing of 59 mV decade^{-1} (within measurement error of the physical limit at room temperature) for a wide range of channel lengths as small as 0.7 μm, and an on/off current ratio of 10^7 for a gate-source-voltage range of 1 V.

1. Introduction

Organic thin-film transistors (TFTs) can typically be fabricated at substantially lower temperatures than transistors based on inorganic semiconductors, making them potentially useful for the realization of flexible active-matrix displays, wearable sensors and low-power integrated circuits.[1–4] A key component of organic TFTs for such advanced technologies is the gate dielectric.[5] Among the prerequisites enabling low-voltage TFT operation is a large unit-area gate-dielectric capacitance, which can be achieved by implementing either ultrathin and/or high-permittivity dielectrics.[6–8] The gate dielectric is also critical in determining the threshold voltage, the subthreshold swing and the bias-stress stability of the TFTs.[9–12] For organic TFTs fabricated in the inverted (bottom-gate) device architecture, the surface properties of the gate dielectric have a pronounced influence on the growth and the quality of the organic-semiconductor film.[13–15] Overall, the gate dielectric has essential and far-reaching impact on the performance and stability of field-effect transistors in general and organic TFTs in particular.

A possible limitation of aluminum oxide as the gate oxide in field-effect transistors is its relatively small permittivity, which limits the unit-area capacitance of low-leakage hybrid AlO_x/SAM dielectrics to about 0.7 μF cm^{-2}.[24] Majewski et al. and Jinno et al. thus introduced titanium oxide, grown by anodic oxidation on the surface of titanium gate electrodes, and demonstrated hybrid TiO_x/SAM dielectrics with a unit-area capacitance close to 1 μF cm^{-2} and organic TFTs capable of operating in the saturation regime with gate-source and drain-source voltages of just 1 V.[25–27] This represents an important achievement, as it fulfills a critical requirement for low-voltage electronic systems that are to be powered by small batteries, solar cells or energy-harvesting devices, or which are to be in direct contact with human tissue.[28–30] A challenge that arises from using titanium oxide is its smaller bandgap that makes it more difficult to achieve small gate currents, large on/off current ratios and small subthreshold swings. In the TFTs reported by Majewski et al. and Jinno et al., the gate currents exceeded 10^{-11} A, the on/off current ratios were no greater than 10^5, and the subthreshold swings were above 100 mV decade^{-1}.

Here we show that the formation of ultrathin titanium oxide dielectrics by plasma-assisted oxidation, rather than anodization, leads to ultralow-voltage organic TFTs on plastic substrates that set a number of organic-TFT-performance records, including a subthreshold swing of 59 mV decade^{-1} (i.e., close to the physical limit at room temperature) for TFTs with channel lengths as small as 0.7 μm and an on/off current ratio of 10^7 for a gate-source-voltage range of 1 V. In addition, we also fabricated unipolar inverters that display a small-signal gain of 1900 in combination with a noise

M. Geiger, R. Lingstädt, T. Wollandt, J. Deuschle, U. Zschieschang, P. A. van Aken, H. Klauk
Max Planck Institute for Solid State Research
Heisenbergstr. 1, 70569 Stuttgart, Germany
E-mail: M.Geiger@fkf.mpg.de; H.Klauk@fkf.mpg.de
F. Letzkus, J. N. Burghartz
Institute for Microelectronics Stuttgart (IMS CHIPS)
Allmandring 30A, 70569 Stuttgart, Germany
R. T. Weitz
1st Institute of Physics
Faculty of Physics
University of Göttingen
Friedrich-Hund-Platz 1, 37077 Göttingen, Germany
The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/aelm.202101215.

DOI: 10.1002/aelm.202101215

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

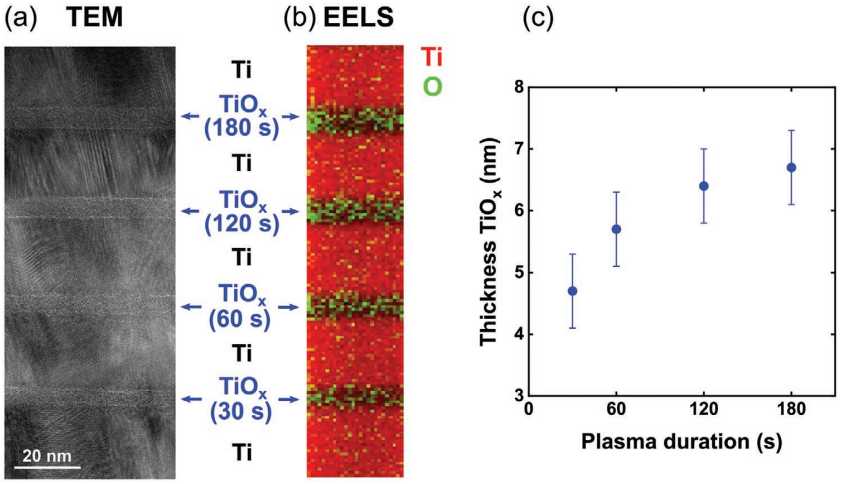


Figure 1. a) Cross-sectional transmission electron microscopy (TEM) image of titanium oxide films (TiO_x) produced sequentially by the plasma-assisted surface oxidation of vacuum-deposited titanium films. Surface oxidation was performed using a plasma power of 200 W and plasma durations of 30, 60, 120, and 180 s. b) Elemental mapping of titanium and oxygen obtained from the Ti-$L_{2,3}$ and O-K edges of the electron energy loss spectroscopy (EELS) spectra. c) Thickness of the TiO_x films determined from the TEM image plotted as a function of the plasma duration.

margin of 79% of half the supply voltage at a supply voltage of 1 V. This is the best combination of small-signal gain and noise margin reported to date for organic-TFT-based unipolar inverters operating with supply voltages of less than 20 V.

2. Results and Discussion

2.1. Thickness of Plasma-Grown TiO_x Films

Figure 1a shows a cross-sectional transmission electron microscopy (TEM) image of a specimen prepared on a silicon substrate by depositing a 25-nm-thick film of titanium by thermal evaporation in vacuum, followed by exposing the titanium surface to a radio-frequency-generated oxygen plasma to form a thin layer of titanium oxide (TiO_x). These two process steps were repeated four times on the same specimen, each time using a different duration for the plasma-oxidation process (30, 60, 120, and 180 s). To be able to unambiguously identify and distinguish the metal and oxide layers in the cross-sectional image, electron energy loss spectroscopy (EELS) was performed. The elemental distribution was obtained by mapping the Ti-$L_{2,3}$ and O-K edges of the recorded spectra (see Figure 1b).

The TEM analysis indicates that the thickness of the plasma-grown titanium oxide films ranges from 4.7 nm for the shortest plasma duration (30 s) to 6.7 nm for the longest duration (180 s). Figure 1c shows the experimentally determined relation between the plasma duration and the thickness of the TiO_x films. The range of TiO_x thicknesses obtained here is similar to the range of thicknesses reported previously for plasma-grown AlO_x films.[24]

2.2. Electrical and Surface Properties of Plasma-Grown TiO_x and Hybrid TiO_x/SAM Dielectrics

To investigate the electrical properties of plasma-grown TiO_x and hybrid TiO_x/SAM dielectrics, we fabricated metal-insulator-metal capacitors on flexible polyethylene naphthalate (PEN) substrates. For the bottom electrode, titanium with a thickness of 25 nm was deposited by thermal evaporation in vacuum. The TiO_x films were obtained by plasma-assisted oxidation of the titanium surface with plasma durations of 30, 60, 120, or 180 s. For the hybrid TiO_x/SAM dielectrics, a monolayer of *n*-tetradecylphosphonic acid or *n*-octadecylphosphonic acid was allowed to self-assemble from solution on the TiO_x surface.[31] For the top electrode, gold with a thickness of 30 nm was deposited by vacuum evaporation. The electrodes were patterned using silicon stencil masks.[32] In **Figure 2**a,b, schematic cross sections of capacitors with a bare-TiO_x dielectric or a hybrid TiO_x/SAM dielectric are shown.

An important prerequisite for minimizing the charge leakage through ultrathin gate dielectrics in TFTs fabricated in the inverted (bottom-gate) device architecture is a small surface roughness of the gate electrodes. Figure S1 (Supporting Information) shows atomic force microscopy (AFM) images of a bare PEN substrate and of nominally 25-nm-thick titanium and aluminum films deposited by thermal evaporation onto PEN. Analysis of the AFM images indicates that all three surfaces (PEN, Ti on PEN, Al on PEN) have essentially the same root-mean-square surface roughness of (1.6 ± 0.1) nm, confirming that the surface roughness of vacuum-deposited titanium is just as small as that of vacuum-deposited aluminum and that both metals cover the PEN surface in a conformal manner.

Obtaining a favorable thin-film morphology of the vacuum-deposited small-molecule organic semiconductor greatly benefits from a small surface energy of the underlying gate dielectric. For hybrid TiO_x/SAM dielectrics based on plasma-grown titanium oxide, we have measured water contact angles of (109 ± 2)° with *n*-tetradecylphosphonic acid SAMs and (108 ± 2)° with *n*-octadecylphosphonic acid SAMs, essentially identical to hybrid AlO_x/SAM dielectrics[33] and confirming that plasma-grown, SAM-functionalized gate oxides provide very small

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

surface energies. While gate dielectrics with small surface energies are beneficial for TFTs based on vacuum-deposited organic semiconductors, they often present problems if the semiconductor deposition is to be performed from solution, due to poor wetting of the semiconductor solution on low-energy surfaces. However, Wöbkenberg et al. previously demonstrated that the solution-deposition of organic semiconductors on hybrid oxide/SAM gate dielectrics with very low surface energy is in fact possible, provided the use of specifically tailored organic semiconductors with compatible surface properties.[34]

The current-voltage characteristics of the metal-insulator-metal capacitors were measured to analyze the influence of the plasma duration on the leakage-current density through the dielectrics. For the bare-TiO_x dielectrics, the leakage-current density is smaller for longer plasma durations, which is consistent with the growth of thicker TiO_x films with longer plasma duration, as confirmed by the TEM investigation. Nevertheless, as seen in Figure 2c, bare-TiO_x dielectrics exhibit overall high leakage-current densities, indicating poor insulating properties. Due to the small bandgap of about 3.5 eV, thermionic emission is a serious concern for bare-TiO_x dielectrics.[35,36]

However, when the TiO_x films are complemented by an alkylphosphonic acid SAM, the leakage-current densities are significantly smaller, i.e., below 10^{-5} A cm^{-2} at a voltage of –1 V for the *n*-tetradecylphosphonic acid SAM and below 10^{-6} A cm^{-2} at a voltage of –1 V for the *n*-octadecylphosphonic acid SAM and for plasma durations of at least 120 s (see Figure 2d,e). These leakage-current densities are not significantly larger than those measured previously in hybrid AlO_x/SAM dielectrics.[24]

In Figure 2f–h, the measured unit-area capacitance is shown for different plasma durations as a function of the measurement frequency. The unit-area capacitance of the bare-TiO_x dielectrics ranges from 1.1 to 3.0 μF cm^{-2} with a clear dependence on the plasma duration. The additional contribution of the SAM decreases the capacitance of the hybrid TiO_x/SAM dielectric and leads to a much less pronounced dependence on the plasma duration (1.1 to 1.4 μF cm^{-2} for the n-tetradecylphosphonic acid SAM; 0.7 to 0.8 μF cm^{-2} for the n-octadecylphosphonic acid SAM).

Figure 2j shows the measured unit-area capacitance of the bare-TiO_x dielectrics plotted as a function of the inverse of the TiO_x thickness, as determined by TEM. By fitting the theoretical relation between the unit-area oxide capacitance C_{ox} and the oxide thickness t_{ox}:

$$C_{ox} = \varepsilon_0 \varepsilon_{ox} \frac{1}{t_{ox}} \quad (1)$$

where ε_0 is the vacuum permittivity, a value for the permittivity of the plasma-grown titanium oxide of $\varepsilon_{ox} = 14 \pm 1$ is obtained. (See Figure S2 (Supporting Information) for details on the error calculation.) This value falls into the range of permittivities reported for titanium oxide in literature.[34,37–41]

In summary, the results of the measurements of the electrical properties of the plasma-grown TiO_x and hybrid TiO_x/SAM dielectrics show that a plasma duration of 120 s is sufficient to minimize the charge leakage through hybrid TiO_x/SAM dielectrics. Taking this as a prerequisite, the unit-area capacitance of the hybrid TiO_x/SAM dielectric is 1.1 μF cm^{-2} for the *n*-tetradecylphosphonic acid SAM and 0.7 μF cm^{-2} for the *n*-octadecylphosphonic acid SAM. Together with the results of the surface-roughness and contact-angle measurements, the hybrid TiO_x/SAM dielectric meets the general requirements for low-voltage organic TFTs.

2.3. Organic TFTs

Organic TFTs with a hybrid TiO_x/SAM gate dielectric were fabricated on flexible PEN substrates in the inverted coplanar (bottom-gate, bottom-contact) device architecture without encapsulation. For the gate electrodes, a 25-nm-thick film of titanium was deposited by thermal evaporation in vacuum. The titanium surface was exposed to an oxygen plasma, and the substrates were then immersed into a solution of *n*-tetradecylphosphonic acid or *n*-octadecylphosphonic acid. For the source and drain contacts, gold with a thickness of 30 nm was deposited and functionalized with a monolayer pentafluorobenzenethiol (PFBT) to minimize the contact resistance.[21,22] As the semiconductor, either 2,7-diphenyl[1]benzothieno[3,2-b][1]benzothiophene (DPh-BTBT) or 2,9-diphenyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DPh-DNTT) was deposited by thermal sublimation in vacuum.[6,10,42] The metals and the organic-semiconductor layers were patterned using silicon stencil masks.[32] The highest process temperature is the temperature at which the substrate is held during the deposition of the organic semiconductor, i.e., 100°C for the DPh-BTBT TFTs and 90°C for the DPh-DNTT TFTs. All electrical measurements were performed in ambient air at room temperature (293 K).

DPh-BTBT, whose chemical structure is shown as part of **Figure 3**a, is a commercially available small-molecule semiconductor developed by Kazuo Takimiya.[43] DPh-BTBT TFTs fabricated with a hybrid AlO_x/SAM gate dielectric and a fluoroalkylphosphonic acid SAM have previously shown a turn-on voltage of exactly 0 V,[10] which can be of great value for the efficient design of low-voltage, low-power digital integrated circuits.[6]

Figure 3a,b shows a schematic cross section of a TFT with a hybrid TiO_x/SAM dielectric and a photograph of a PEN substrate with arrays of TFTs and circuits. A scanning electron microscopy (SEM) image of a DPh-BTBT TFT with a channel length of 0.7 μm and the measured transfer and output characteristics of this TFT are shown in Figure 3c–e. The small channel length is helpful in achieving a large channel-width-normalized transconductance of 0.6 S m^{-1} at a gate-source voltage of –1 V. Owing to the exceptional combination of large unit-area gate-dielectric capacitance and insignificant gate leakage, an on/off current ratio of 10^7 is obtained for the gate-source-voltage range from 0 to –1 V. To our knowledge, these are the largest width-normalized transconductance and the largest on/off current ratio reported to date for flexible organic TFTs for a gate-source-voltage range of 1 V or less.[6]

The subthreshold swing of the DPh-BTBT TFTs is determined to be (59 ± 1) mV decade^{-1} for a drain-source voltage of –0.1 V and (62 ± 2) mV decade^{-1} for a drain-source voltage of –0.7 V (see Figure 3f–h). To our knowledge, this is the first time that a subthreshold swing below 66 mV decade^{-1} is reported for a submicron-channel-length organic transistor.[22,47,48] The

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

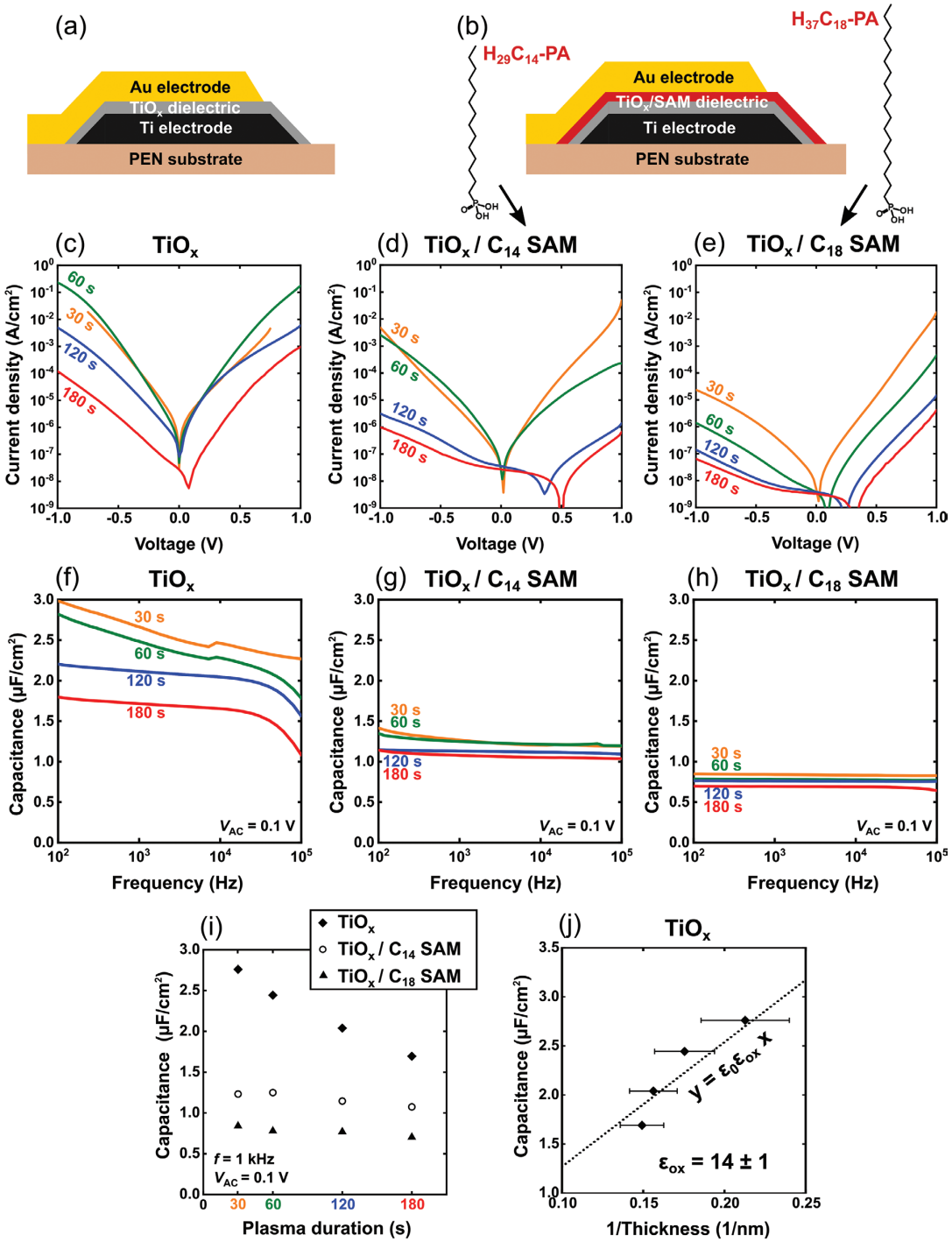


Figure 2. Schematic cross sections of metal-insulator-metal capacitors based on a) bare plasma-grown TiO_x as the dielectric and b) a hybrid dielectric consisting of plasma-grown TiO_x and an *n*-tetradecylphosphonic acid or *n*-octadecylphosphonic acid self-assembled monolayer (SAM). c–e) Measured leakage current density and f–i) unit-area capacitance. j) Unit-area capacitance of capacitors based on bare plasma-grown TiO_x plotted as a function of the inverse of the TiO_x thickness, as determined by TEM, to calculate the relative permittivity of the plasma-grown titanium oxide.

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

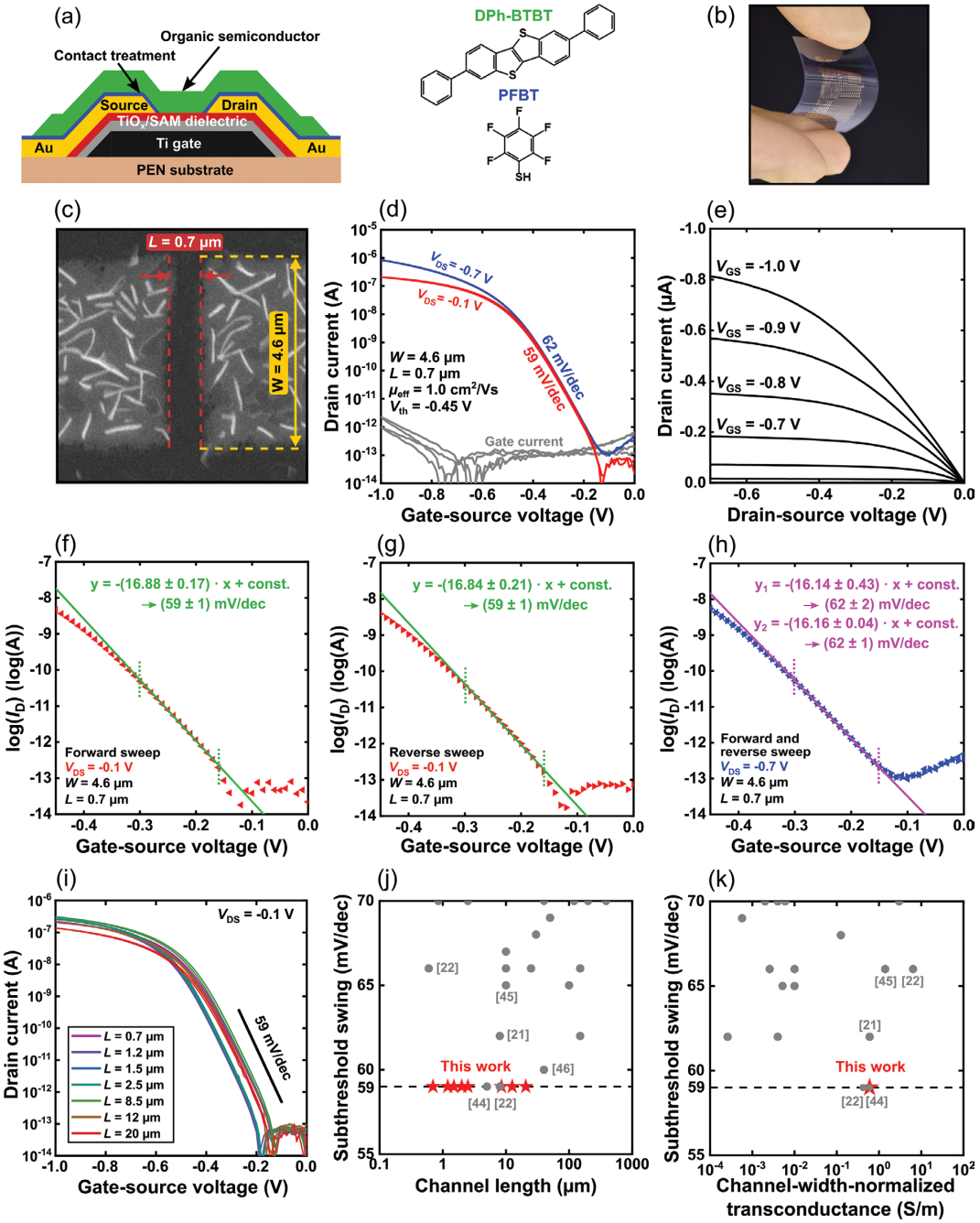


Figure 3. a) Schematic cross section of organic thin-film transistors (TFT) with a hybrid TiO_x/SAM gate dielectric, and molecular structures of the organic semiconductor 2,7-diphenyl-[1]benzothieno[3,2-b][1]benzothiophene (DPh-BTBT) and of the molecule pentafluorobenzenethiol (PFBT) employed to functionalize the gold source and drain contacts with a chemisorbed monolayer to minimize the contact resistance. b) Photograph of a flexible PEN substrate with arrays of organic TFTs and circuits. c) Scanning electron microscopy (SEM) image of a flexible DPh-BTBT TFT with a channel length of 0.7 µm. d) Measured transfer and e) output characteristics of a flexible DPh-BTBT TFT having a channel length of 0.7 µm. f–h) Extraction of the subthreshold swing from the transfer characteristics. i) Measured transfer characteristics of flexible DPh-BTBT TFTs with a Ti/TiO_x/SAM gate stack and channel lengths ranging from 0.7 to 20 µm. j) Literature summary of organic TFTs with subthreshold swings of 70 mV decade^{-1} or less, plotted versus the channel length, and k) plotted versus the channel-width-normalized transconductance of the transistors.

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

subthreshold swing of 59 mV decade^{-1} was measured here in flexible TFTs with channel lengths ranging from 0.7 to 20 µm (see Figure 3i,j).

For the temperature at which these measurements were performed (T = 293 K), the subthreshold swing of (59 ± 1) mV decade^{-1} is within the measurement error of the theoretical minimum of 58.1 mV decade^{-1}, given as $\ln(10)k_BT/q$, where k_B is the Boltzmann constant and q is the elementary charge.[49] This confirms that it is possible to fabricate nanoscale organic TFTs with minimum subthreshold swing on flexible substrates, provided an optimized combination of materials and techniques for film formation and patterning is employed for all transistor components, including high-fidelity lithography and a native interface between the gate metal and the gate oxide that is characterized by a vanishingly small defect density.

One drawback of DPh-BTBT TFTs is their relatively large contact resistance. Using the transmission line method (TLM) in the linear regime of operation, we determined a channel-width-normalized contact resistance of (142 ± 37) Ω cm for flexible DPh-BTBT TFTs with a hybrid TiO_x/SAM dielectric (see **Figure 4**a–c). Notably smaller contact resistances can be expected by replacing DPh-BTBT with DPh-DNTT (chemical structure shown in **Figure 5**a), which was also developed by Kazuo Takimiya[50] and for which a contact resistance of 29 Ω cm (also determined by TLM in the linear regime of operation) was recently obtained in flexible TFTs with a hybrid AlO_x/SAM gate dielectric.[21]

Figure 5b,c shows the measured transfer and output characteristics of a flexible DPh-DNTT TFT with a hybrid TiO_x/SAM gate dielectric having a channel length of 2.4 µm. The DPh-DNTT TFTs have an on/off current ratio of 10^7 within a gate-source-voltage range of 1 V (similar to the DPh-BTBT TFTs) and a subthreshold swing of (63 ± 1) mV dec^{-1} for a drain-source voltage of –0.1 V and (66 ± 1) mV dec^{-1} for a drain-source voltage of –0.6 V (see Figure 5d).

To probe the bias-stress stability of these TFTs, gate-source and drain-source voltages of –0.6 V were applied continuously for a duration of 72 h in ambient air. In Figure 5e, the normalized drain current is plotted as a function of bias-stress duration, and Figure 5f shows the transfer characteristics of the TFT measured before and after the bias-stress test. The 72 h bias-stress test caused a threshold-voltage shift of –0.01 V and a drain-current reduction of 6%. Considering that the TFTs were fabricated on a plastic substrate without encapsulation and that the bias stress was applied in ambient air and for a duration of three days, the bias-stress stability reported here is on par with the best results reported in literature (see **Table 1**). This further confirms the excellent quality of hybrid TiO_x/SAM gate dielectrics based on plasma-grown titanium oxide.[51]

Figure 6 shows the transfer characteristics of DPh-DNTT TFTs with a Ti/TiO_x/SAM gate stack in comparison to those of DPh-DNTT TFTs with an Al/AlO_x/SAM gate stack. The only noteworthy difference between the transfer curves is the threshold voltage, which has values of –0.07 V for the TFTs with the Ti/TiO_x/SAM gate stack and –0.53 V for the TFTs with the Al/AlO_x/SAM gate stack. The threshold voltage of organic TFTs can be approximated as:[56]

$$V_{th} = \frac{Q_{sc} - Q_{diel}}{C_{diel}} + \Phi_{ms} \quad (2)$$

where Q_{sc} is the density of free charge carriers in the semiconductor at equilibrium (i.e., no voltages applied), Q_{diel} is the density of charges in the gate dielectric or at the semiconductor-dielectric interface, C_{diel} is the unit-area gate-dielectric capacitance and Φ_{ms} is the difference between the workfunction of the metal and the semiconductor. The difference between the workfunctions of titanium (4.33 eV)[57] and aluminum (4.23 to 4.32 eV)[58,59] is too small to explain the observed difference between the threshold voltages in Figure 6 (0.46 V). It thus appears that there is a significant difference in the density of charges in the semiconductor (Q_{sc}) and/or in the gate dielectric and/or at the semiconductor-dielectric interface (Q_{diel}) that is responsible for the observed difference in the threshold voltages of the TFTs. It will certainly be useful to investigate the exact origin(s) and location(s) of these charges and the question how these relate to the materials properties of plasma-grown titanium oxide and aluminum oxide, but such investigations are beyond the scope of the present study.

In addition to a steep subthreshold swing, a large on/off current ratio and good bias-stress stability, organic TFTs also need to have a small contact resistance. Figure 4d–i shows results of a TLM analysis of flexible DPh-DNTT TFTs with the two different gate stacks (Ti/TiO_x/SAM and Al/AlO_x/SAM). The width-normalized contact resistance at the highest gate overdrive voltage (difference between gate-source voltage and threshold voltage) is (15 ± 5) Ω cm for the TFTs with the titanium gates (long-term stability of the contact resistance shown in Figure S3: Supporting Information) and (12 ± 2) Ω cm for the TFTs with the aluminum gates. These are the smallest contact resistances reported to date for organic TFTs in the linear regime of operation, aside from the contact resistances of 1 Ω cm reported by Braga et al. and 3 Ω cm reported by Lenz et al. for an electrolyte-gated polymer TFTs in which the contact resistance benefits greatly from the extremely large charge-carrier density induced by the electrolyte[60,61] For DPh-DNTT TFTs operated in the saturation regime, Borchert et al. recently reported a contact resistance of 10 Ω cm extracted from scattering-parameter measurements.[22]

The intrinsic channel mobility extracted from the TLM analysis in Figure 4 is about 30% smaller in the DPh-DNTT TFTs with the titanium gates (3.0 cm^2 V^{-1} s^{-1}) than in the DPh-DNTT TFTs with the aluminum gates (4.6 cm^2 V^{-1} s^{-1}). This difference in intrinsic channel mobility is possibly related to the formation of Fröhlich polarons,[14,62] which is known to be more prominent for a larger gate-oxide permittivity (TiO_x: 14 ± 1; AlO_x: 8.0 ± 0.2).[24] The compromise between the gate-dielectric permittivity and the charge-carrier mobility is a general problem for organic TFTs, and the smaller mobility we have found here for the TFTs with the Ti/TiO_x/SAM gate stack is an obvious drawback in comparison to TFTs with an Al/AlO_x/SAM gate stack.

Also shown in Figure 4 is the analysis of the contact resistance according to the formulation developed by Luan and Neudeck, in which the contact resistance R_CW is modeled as the sum of two terms, one that decreases with increasing gate-source voltage and one that represents a minimum contact resistance $R_{C,0}W$ that is independent of the gate-source voltage:[63]

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

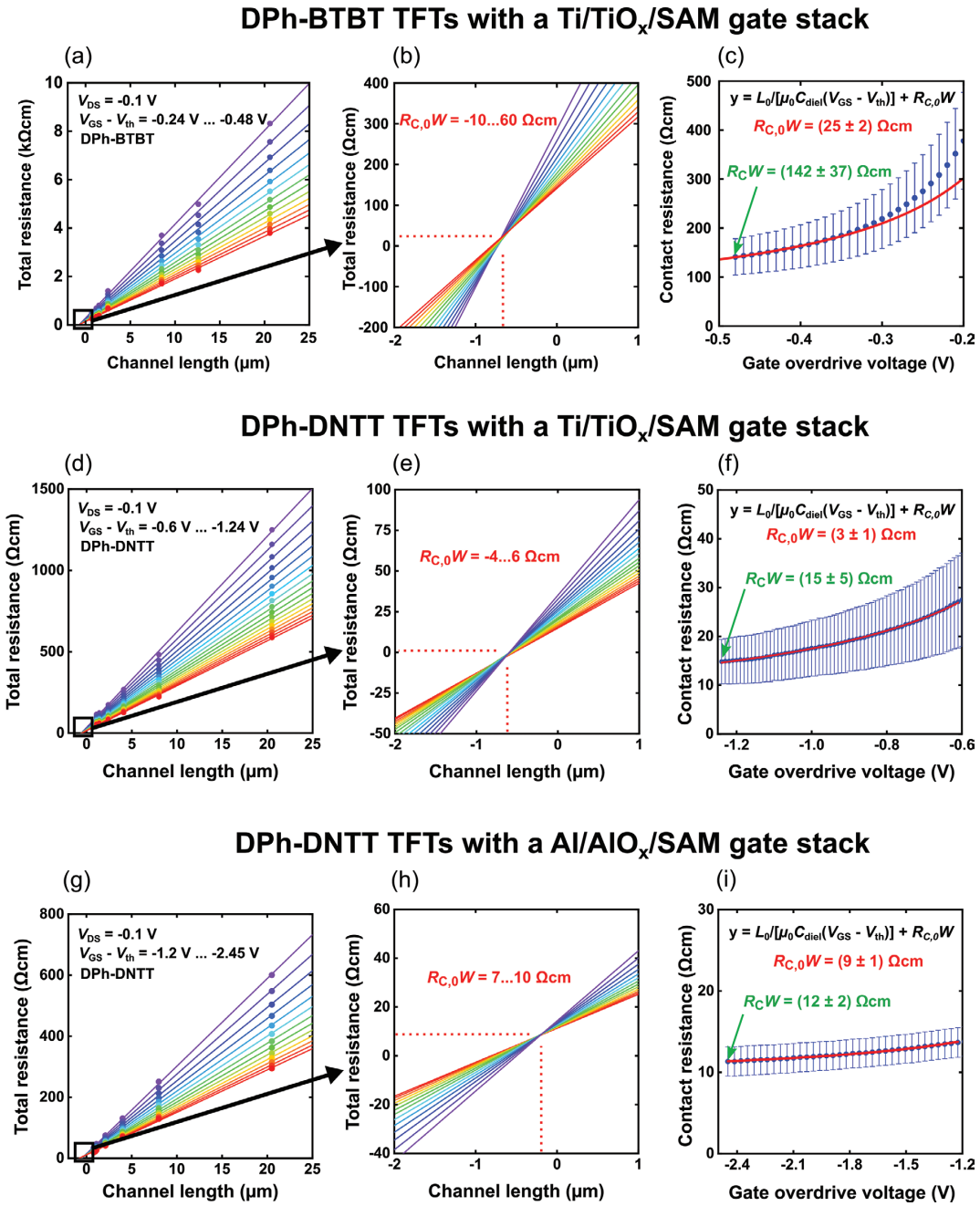


Figure 4. a) Transmission line method (TLM) analysis of flexible DPh-BTBT TFTs with a Ti/TiO_x/SAM gate stack. b) The gate-source-voltage-independent minimum contact resistance $R_{C,0}W$ can be estimated from the intercept of the individual fit lines in the plot of the total device resistance RW versus the channel length L. c) Channel-width-normalized contact resistance plotted as a function of the gate overdrive voltage. For the largest gate overdrive voltage (V_{GS}-V_{th} = –0.48 V), a width-normalized contact resistance R_CW of (142 ± 37) Ω cm is extracted. Fitting Equation (1) to the R_CW = f(V_{GS}-V_{th}) data yields a value for $R_{C,0}W$ of (25 ± 2) Ω cm. d) TLM analysis of flexible DPh-DNTT TFTs with an Ti/TiO_x/SAM gate stack. e) Extrapolation of the fit lines to estimate $R_{C,0}W$. f) Width-normalized contact resistance plotted as a function of the gate overdrive voltage, yielding R_CW = (15 ± 5) Ω cm for the largest gate overdrive voltage (V_{GS}-V_{th} = –1.24 V) and $R_{C,0}W$ = (3 ± 1) Ω cm. g) TLM analysis of flexible DPh-DNTT TFTs with an Al/AlO_x/SAM gate stack. h) Extrapolation of the fit lines. i) Width-normalized contact resistance plotted as a function of the gate overdrive voltage, yielding R_CW = (12 ± 2) Ω cm for the largest gate overdrive voltage (V_{GS}-V_{th} = –2.45 V) and $R_{C,0}W$ = (9 ± 1) Ω cm.

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

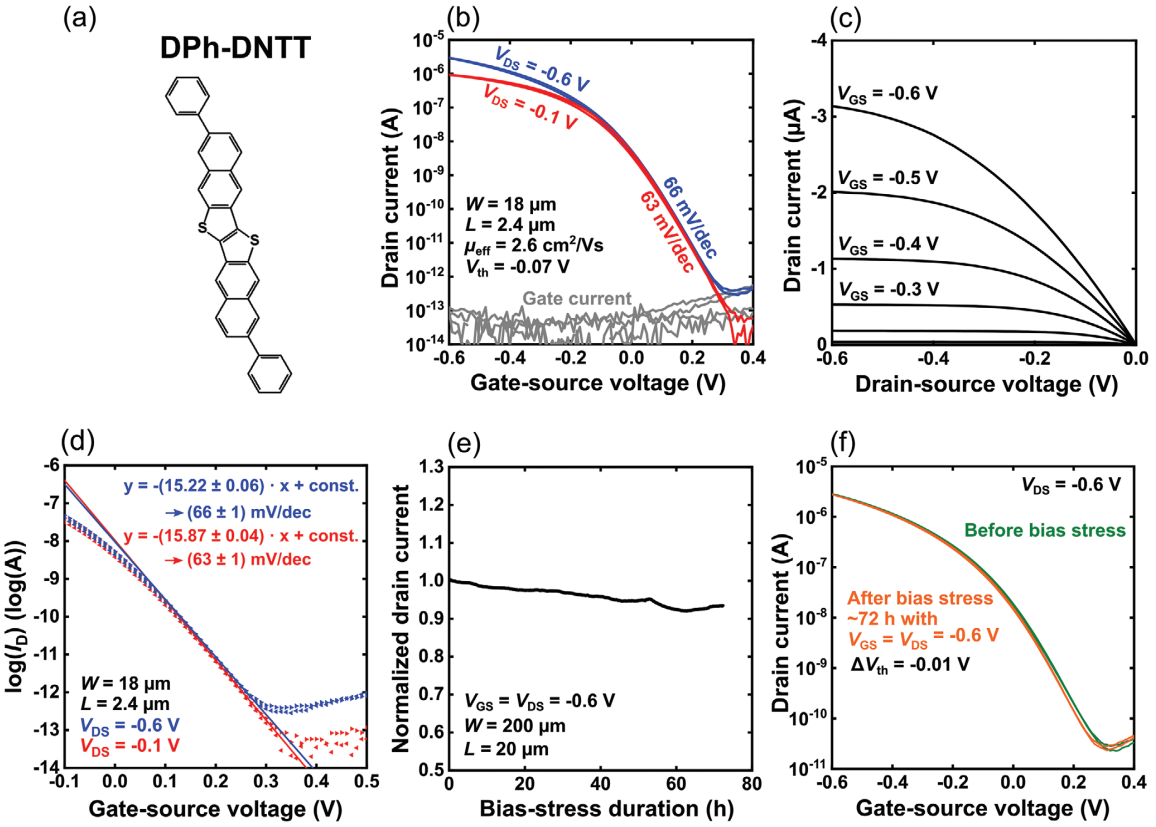


Figure 5. a) Molecular structure of the organic semiconductor 2,9-diphenyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DPh-DNTT). b) Measured transfer and c) output characteristics of a flexible DPh-DNTT TFT with a hybrid TiO_x/SAM gate dielectric having a channel length of 2.4 µm. d) Extraction of the subthreshold swing from the transfer characteristics. e) Evolution of the drain current of a flexible DPh-DNTT TFT with a hybrid TiO_x/SAM gate dielectric during a bias stress. f) Transfer characteristics of the same TFT measured before and after bias stress for a duration of 72 h.

$$R_C W = \frac{L_0}{\mu_0 C_{diel}(V_{GS} - V_{th})} + R_{C,0} W \quad (3)$$

where μ_0 is the intrinsic channel mobility, V_{GS} is the gate-source voltage, V_{th} is the threshold voltage, W is the channel width, and L_0 is a characteristic contact length. The values of L_0 and $R_{C,0}W$ can be extracted from the intercept of the individual fit lines in the plot of the total device resistance RW versus the channel length L (see Figure 4e,h), and alternatively by fitting the above equation to the plot of the contact resistance $R_C W$ versus the gate overdrive voltage V_{GS}-V_{th} (see Figure 4f,i). Values for $R_{C,0}W$ of (3 ± 1) Ω cm and (9 ± 1) Ω cm were found

Table 1. Comparison of the bias-stress stability of the flexible low-voltage DPh-DNTT TFTs in Figure 5e,f with the bias-stress stability of organic TFTs reported by Kalb et al. in 2007, by Jia et al. in 2018, and by Iqbal et al. in 2021. The parameter N_{trap}/N_{init} was calculated using Equation (2) in ref. [52].

Ref.	C_{diel} [nF cm^{-2}]	V_{GS} [V]	$C_{diel}(V_{GS}$-$V_{th})$ [C cm^{-2}]	Substrate	Measurement ambient	Encapsulation	Semiconductor	Bias-stress duration [h]	ΔV_{th} [V]	N_{trap}/N_{init} [%]
[53]	3.5	–70	$2.5 \cdot 10^{-7}$	Glass	Helium	None	Single-crystalline Rubrene	2	–0.18	0.3
[54]	40.8	–10	$3.3 \cdot 10^{-7}$	Glass	Nitrogen	None	Solution-deposited TIPS- pentacene/PTAA	163	–0.04	0.5
[55]	17.3	–35	$4.3 \cdot 10^{-7}$	Si wafer	Air	Parylene N	Solution-deposited IDT-BT	8	+0.1	0.4
This work	1100	–0.6	$5.8 \cdot 10^{-7}$	Flexible PEN	Air	None	Vacuum-deposited DPh-DNTT	72	–0.01	1.8

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

Table 2. Summary of the parameters of the TFTs with the Ti/TiO_x/SAM gate stack from Figure 3d, of the DPh-DNTT TFTs with the Ti/TiO_x/SAM gate stack from Figure 5b, and of the DPh-DNTT TFTs with the Al/AlO_x/SAM gate stack from Figure 6.

Substrate	Gate stack	Semi-conductor	L [µm]	S [mV dec^{-1}]	on/off ratio	V_{th} [V]	$R_C W$ [Ω cm]	$R_{C,0} W$ [Ω cm]	μ_0 [cm^2 V^{-1} s^{-1}]	g_m/W [S m^{-1}]
PEN	Ti/TiO_x/SAM	DPh-BTBT	0.7	59 mV dec^{-1}	10^7	–0.45	142 ± 37	25 ± 2	1.8	0.6
PEN	Ti/TiO_x/SAM	DPh-DNTT	2.4	63 mV dec^{-1}	10^7	–0.07	15 ± 5	3 ± 1	3.0	0.6
PEN	Al/AlO_x/SAM	DPh-DNTT	2.4	71 mV dec^{-1}	10^7	–0.53	12 ± 2	9 ± 1	4.6	0.5

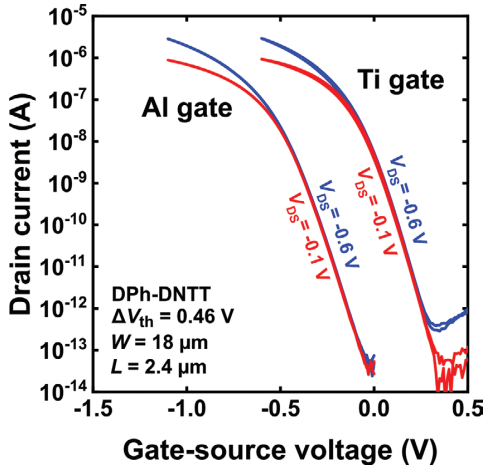


Figure 6. Measured transfer characteristics of flexible DPh-DNTT TFTs with an Al/AlO_x/SAM gate stack (left) and a Ti/TiO_x/SAM gate stack (right). The TFTs with the Al/AlO_x/SAM gate stack have a negative turn-on voltage, while the TFTs with the Ti/TiO_x/SAM gate stack have a positive turn-on voltage. The difference between the threshold voltages is 0.46 V.

for the DPh-DNTT TFTs with the Ti/TiO_x/SAM gate stack and the Al/AlO_x/SAM gate stack, respectively. These results suggest that further optimization of the materials and/or device architecture might lead to a contact resistance of about 1 Ω cm or perhaps even below 1 Ω cm in organic TFTs with ultrathin, high-capacitance gate dielectrics.

Table 2 summarizes the parameters of the DPh-BTBT TFTs with the Ti/TiO_x/SAM gate stack from Figure 3d, of the DPh-DNTT TFTs with the Ti/TiO_x/SAM gate stack from Figure 5b, and of the DPh-DNTT TFTs with the Al/AlO_x/SAM gate stack from **Figure 6**.

2.4. Zero-V_{GS} Inverters Based on a Normally-On Load and a Normally-Off Drive TFT

The fact that DPh-DNTT TFTs have a positive turn-on voltage when fabricated with a Ti/TiO_x/SAM gate stack but a negative turn-on voltage when fabricated with an Al/AlO_x/SAM gate stack (see Figure 6) can be exploited for the fabrication of zero-V_{GS} inverters with a normally-on ("depletion-mode") load and a normally-off ("enhancement-mode") drive transistor. The circuit schematic of the zero-V_{GS} inverter is shown in **Figure 7**a. There are numerous reports of organic-TFT-based zero-V_{GS} inverters,[28,30,44,64] but in most of these reports, the inverters were based on two normally-off or two normally-on transistors. However, the optimum design of zero-V_{GS} inverters utilizes a normally-off drive transistor to provide a switching voltage close to half the supply voltage (and thus noise margins close to 100% of half the supply voltage) and a normally-on load transistor to facilitate rapid discharging of the output node when the drive transistor is non-conducting.[65–68] Properly designed zero-V_{GS} inverters are advantageous in comparison to other unipolar inverter styles, as they provide a larger small-signal gain and larger noise margins than diode-load and biased-load inverters, and a smaller TFT count and shorter signal delays than pseudo-CMOS inverters.[69,70] We fabricated zero-V_{GS} inverters with a

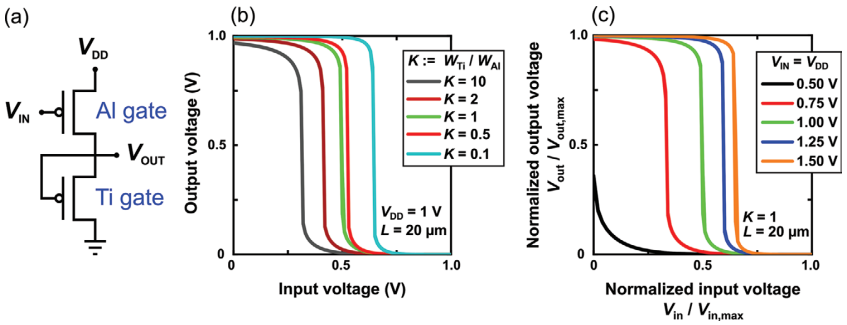


Figure 7. a) Circuit schematic of a zero-V_{GS} inverter, here based on a normally-on load TFT (Ti/TiO_x/SAM gate stack) and a normally-off drive TFT (Al/AlO_x/SAM gate stack). Both TFTs utilize the same organic semiconductor (DPh-DNTT). b) Measured transfer characteristics of zero-V_{GS} inverters with different channel-width ratios ($K = W_{load}/W_{drive}$). c) Transfer characteristics of a zero-V_{GS} inverter with a channel-width ratio $K = 1$ measured for supply voltages V_{DD} ranging from 0.5 to 1.5 V.

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

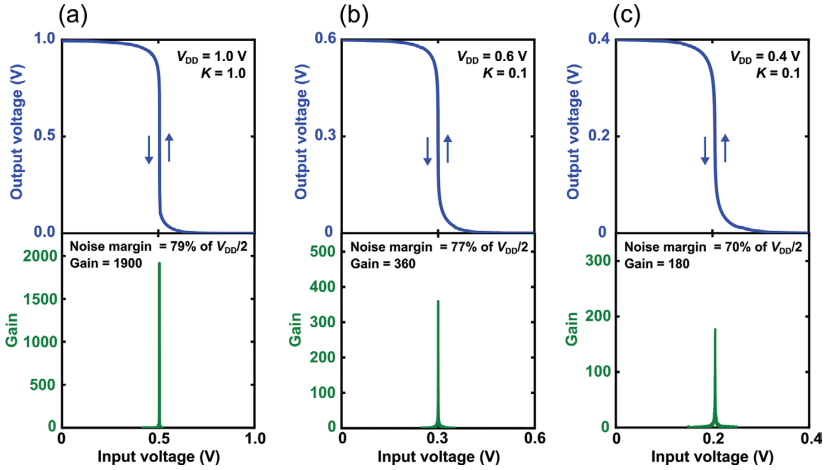


Figure 8. Measured transfer characteristics of zero-V_{GS} inverters based on DPh-DNTT TFTs with Ti/TiO_x/SAM and Al/AlO_x/SAM gate stacks for the load and drive TFTs, respectively.

normally-on load TFT (Ti gate electrode) and a normally-off drive TFT (Al gate electrode) on a flexible PEN substrate.

Figure 7b,c illustrates the dependence of the switching voltage of the zero-V_{GS} inverters on the channel-width ratio ($K = W_{load}/W_{drive}$) and the supply voltage (V_{DD}). For the optimum channel-width ratio K, the deviation of the switching voltage from its optimum value (i.e., from half the supply voltage, $V_{DD}/2$) ranges from 1 to 10 mV (or from 0.2% to 2.8%), depending on the supply voltage. All else being equal, a smaller deviation of the switching voltage from $V_{DD}/2$ will lead to larger noise margins. The optimized zero-V_{GS} inverters reported here have noise margins as large as 79% of $V_{DD}/2$ (determined using the method described in reference 33).

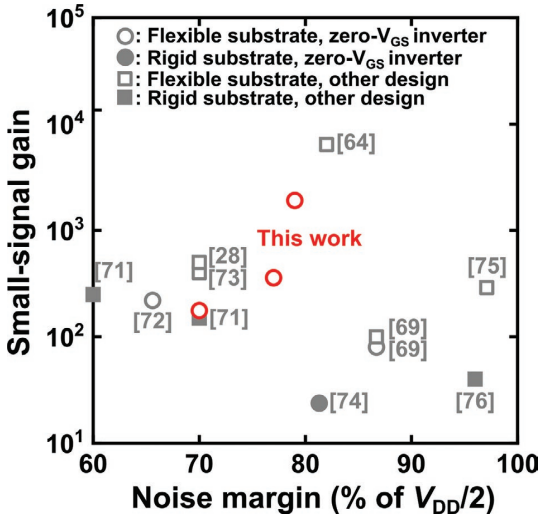


Figure 9. Literature summary of organic-TFT-based unipolar inverters with a small-signal gain of at least 10 and a noise margin of at least 60% of half the supply voltage.

Compared with diode-load and biased-load inverters, zero-V_{GS} inverters provide significantly larger small-signal gains.[69] The small-signal gains of the zero-V_{GS} inverters in **Figure 8** range from 180 at a supply voltage of 0.4 V to 1900 at a supply voltage of 1.0 V. **Figure 9** and Table S1 (Supporting Information) illustrate that the combination of low operating voltage, large noise margin and large small-signal gain of the inverters reported here compares very favorably with the performance of organic-TFT-based unipolar inverters reported in literature.

3. Conclusions

In summary, we have shown that it is possible to fabricate gate dielectrics with both high capacitance and low charge leakage by using plasma-grown titanium oxide in a hybrid TiO_x/SAM dielectric for use in flexible ultralow-voltage organic TFTs. We have presented flexible DPh-BTBT TFTs with a Ti/TiO_x/SAM gate stack and channel lengths as small as 0.7 µm that exhibit record organic-TFT-performance, including a channel-width-normalized transconductance of 0.6 S m^{-1} and an on/off current ratio of 10^7 for a gate-source-voltage range from 0 to –1 V, and a subthreshold swing at the room-temperature limit of 59 mV $decade^{-1}$.

In addition, we demonstrated unipolar inverters by combining DPh-DNTT TFTs with a Ti/TiO_x/SAM gate stack (normally-on load transistor) and an Al/AlO_x/SAM gate stack (normally-off drive transistor). These inverters combine large small-signal gains and large noise margins at ultra-low supply voltages of 1 V or less. The DPh-DNTT TFTs have channel-width normalized contact resistances as low as (12 ± 2) Ω cm, which is the smallest contact resistance reported to date for flexible organic TFTs in the linear regime of operation.

4. Experimental Section

Device Fabrication: All capacitors, TFTs and inverters were fabricated on flexible polyethylene naphthalate (PEN) with a thickness

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

of 125 µm (Inabata Europe GmbH, Düsseldorf, Germany). For the bottom electrodes of the capacitors and the gate electrodes of the TFTs, titanium with a thickness of 25 nm was deposited by thermal evaporation in vacuum (10^{-7} mbar) with a deposition rate of 1 to 2 nm s^{-1}. The TiO_x dielectric was produced by exposing the titanium surface to a capacitively coupled radio-frequency (13.56 MHz) plasma in pure oxygen (partial pressure 0.01 mbar) for a duration of 30, 60, 120, or 180 s at a plasma power of 200 W.[24] To produce a hybrid TiO_x/SAM dielectric, the substrate was then immersed into a 2-propanol solution of either *n*-tetradecylphosphonic acid or *n*-octadecylphosphonic acid (PCI Synthesis, Newburyport, MA, USA) to form a self-assembled monolayer. For the top electrode of the capacitors and the source and drain contacts of the TFTs, gold with a thickness of 30 nm was deposited by thermal evaporation in vacuum with a rate of 0.03 nm s^{-1}. To functionalize the source and drain contacts of the TFTs with a monolayer of pentafluorobenzenethiol (PFBT; TCI Deutschland GmbH, Eschborn, Germany), the substrate was immersed into a 0.01 M solution of PFBT in ethanol for 1 h.[21] As the semiconductor, a nominally 35-nm-thick layer of either 2,7-diphenyl[1]benzothieno[3,2-b][1]benzothiophene (DPh-BTBT; Sigma Aldrich) or 2,9-diphenyl-dinaphtho[2,3-b:2′,3′-f] thieno[3,2-b]thiophene (DPh-DNTT; Nippon Kayaku, kindly provided by K. Ikeda) was deposited by thermal sublimation in vacuum (10^{-7} mbar) with a deposition rate of 0.03 nm s^{-1}. During the semiconductor deposition, the substrate was held at a constant temperature of 100 °C for DPh-BTBT and 90°C for DPh-DNTT. Gate electrodes, source/drain contacts and organic-semiconductor layers were patterned using silicon stencil masks. These masks were fabricated from silicon-on-insulator (SOI) wafers by a combination of electron-beam lithography and deep reactive-ion etching of 20-µm-thick silicon membranes,[77,78] a process developed originally for ion-projection lithography.[79] Mask alignment was performed manually under an optical microscope.

Electrical Characterization: The capacitance measurements were performed using a Hameg HM8118 LCR meter, and the current-voltage measurements were performed using an Agilent 4156C Semiconductor Parameter Analyzer, both controlled using the software "SweepMe!" (https://sweep-me.net). All measurements were performed in ambient air at room temperature under yellow laboratory light.

Surface Characterization: The AFM images were recorded using a Bruker Dimension Icon Atomic Force Microscope in peak force tapping mode. Water contact-angle measurements were performed using a Krüss contact angle measurement system. A Zeiss Merlin Scanning electron microscope was used to perform the SEM investigations.

TEM Characterization: The TEM specimen was prepared by focused ion beam (FIB) in situ lift-out using a FEI Scios DualBeam instrument. The TEM image was recorded using a JEOL JEM ARM200F image-corrected atomic-resolution microscope and an acceleration voltage of 200 kV. Spatially resolved electron energy-loss spectroscopy for elemental mapping was conducted in scanning mode by raster-scanning the focused electron probe across the area of interest while acquiring energy-loss spectra for each spatial pixel.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The authors gratefully acknowledge Kazuo Takimiya (RIKEN Center for Emergent Matter Science, Wako, Saitama, Japan) as well as Koichi Ikeda, Yuichi Sadamitsu, and Satoru Inoue (Nippon Kayaku, Tokyo, Japan) for providing the organic semiconductor DPh-DNTT. The authors thank Sebastian Riesel for excellent assistance in the lab. This work is partially funded by the German Research Foundation (DFG) under the grants KL 2223/6-2 (SPP FFlexCom), KL 2223/7-1, and INST 35/1429-1 (SFB 1249). This project has received funding from the European Union's Horizon 2020 research and innovation program under grant agreement No. 823717 – ESTEEM3.

Open access funding enabled and organized by Projekt DEAL.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

gate dielectric, low-voltage operation, organic transistor, subthreshold swing

Received: November 9, 2021
Revised: December 9, 2021
Published online:

[1] M. Noda, N. Kobayashi, M. Katsuhara, A. Yumoto, S. Ushikura, R. Yasuda, N. Hirai, G. Yukawa, I. Yagi, K. Nomoto, T. Urabe, *J. Soc. Inf. Disp.* **2011**, *19*, 316.
[2] T. Someya, Y. Kato, T. Sekitani, S. Iba, Y. Noguchi, Y. Murase, H. Kawaguchi, T. Sakurai, *Proc. Natl. Acad. Sci. USA* **2005**, *102*, 12321.
[3] J. A. Rogers, T. Someya, Y. Huang, *Science* **2010**, *327*, 1603.
[4] T. Sekitani, U. Zschieschang, H. Klauk, T. Someya, *Nat. Mater.* **2010**, *9*, 1015.
[5] A. Facchetti, M. H. Yoon, T. J. Marks, *Adv. Mater.* **2005**, *17*, 1705.
[6] U. Zschieschang, V. P. Bader, H. Klauk, *Org. Electron.* **2017**, *49*, 179.
[7] K. Haase, J. Zessin, K. Zoumboulis, M. Müller, M. Hambsch, S. C. B. Mannsfeld, *Adv. Electron. Mater.* **2019**, *5*, 1900067.
[8] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, C. Dehm, M. Schütz, S. Maisch, F. Effenberger, M. Brunnbauer, F. Stellacci, *Nature* **2004**, *431*, 963.
[9] K. Fukuda, T. Hamamoto, T. Yokota, T. Sekitani, U. Zschieschang, H. Klauk, T. Someya, *Appl. Phys. Lett.* **2009**, *95*, 203301.
[10] R. Acharya, B. Peng, P. K. L. L. Chan, G. Schmitz, H. Klauk, P. K. L. Chan, G. Schmitz, H. Klauk, *ACS Appl. Mater. Interfaces* **2019**, *11*, 27104.
[11] K. P. Pernstich, S. Haas, D. Oberhoff, C. Goldmann, D. J. Gundlach, B. Batlogg, A. N. Rashid, G. Schitter, *J. Appl. Phys.* **2004**, *96*, 6431.
[12] M. F. Chang, P. T. Lee, S. P. McAlister, A. Chin, *IEEE Electron Device Lett.* **2009**, *30*, 133.
[13] S. Y. Yang, K. Shin, C. E. Park, *Adv. Funct. Mater.* **2005**, *15*, 1806.
[14] I. N. Hulea, S. Fratini, H. Xie, C. L. Mulder, N. N. Iossad, G. Rastelli, S. Ciuchi, A. F. Morpurgo, *Nat. Mater.* **2006**, *5*, 982.
[15] M. Geiger, R. Acharya, E. Reutter, T. Ferschke, U. Zschieschang, J. Weis, J. Pflaum, H. Klauk, R. T. Weitz, *Adv. Mater. Interfaces* **2020**, *7*, 1902145.
[16] T. W. Kelley, L. D. Boardman, T. D. Dunbar, D. V. Muyres, M. J. Pellerite, T. P. Smith, *J. Phys. Chem. B* **2003**, *107*, 5877.
[17] O. Acton, G. G. Ting, P. J. Shamberger, F. S. Ohuchi, H. Ma, A. K. Y. Jen, *ACS Appl. Mater. Interfaces* **2010**, *2*, 511.
[18] H. Klauk, U. Zschieschang, J. Pflaum, M. Halik, *Nature* **2007**, *445*, 745.

ADVANCED SCIENCE NEWS
www.advancedsciencenews.com

ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

[19] A. Jedaa, M. Burkhardt, U. Zschieschang, H. Klauk, D. Habich, G. Schmid, M. Halik, *Org. Electron.* **2009**, *10*, 1442.
[20] L. I. Leshanskaya, N. N. Dremova, S. Y. Luchkin, I. S. Zhidkov, S. O. Cholakh, E. Z. Kurmaev, K. J. Stevenson, P. A. Troshin, *Thin Solid Films* **2018**, *649*, 7.
[21] J. W. Borchert, B. Peng, F. Letzkus, J. N. Burghartz, P. K. L. L. Chan, K. Zojer, S. Ludwigs, H. Klauk, *Nat. Commun.* **2019**, *10*, 1119.
[22] J. W. Borchert, J. W. Borchert, U. Zschieschang, F. Letzkus, M. Giorgio, M. Giorgio, R. T. Weitz, R. T. Weitz, R. T. Weitz, M. Caironi, J. N. Burghartz, S. Ludwigs, H. Klauk, *Sci. Adv.* **2020**, *6*, eaaz5156.
[23] M. Kaltenbrunner, T. Sekitani, J. Reeder, T. Yokota, K. Kuribara, T. Tokuhara, M. Drack, R. Schwödiauer, I. Graz, S. Bauer-Gogonea, S. Bauer, T. Someya, *Nature* **2013**, *499*, 458.
[24] M. Geiger, M. Hagel, T. Reindl, J. Weis, R. T. Weitz, H. Solodenko, G. Schmitz, U. Zschieschang, H. Klauk, R. Acharya, *Sci. Rep.* **2021**, *11*, 6382.
[25] L. A. Majewski, R. Schroeder, M. Grell, *Adv. Funct. Mater.* **2005**, *15*, 1017.
[26] L. A. Majewski, R. Schroeder, M. Grell, *Adv. Mater.* **2005**, *17*, 192.
[27] H. Jinno, T. Yokota, N. Matsuhisa, M. Kaltenbrunner, Y. Tachibana, T. Someya, *Org. Electron.* **2017**, *40*, 58.
[28] T. Sekitani, T. Yokota, K. Kuribara, M. Kaltenbrunner, T. Fukushima, Y. Inoue, M. Sekino, T. Isoyama, Y. Abe, H. Onodera, T. Someya, *Nat. Commun.* **2016**, *7*, 11425.
[29] N. K. Elumalai, A. Uddin, *Energy Environ. Sci.* **2016**, *9*, 391.
[30] M. Kondo, T. Uemura, T. Matsumoto, T. Araki, S. Yoshimoto, T. Sekitani, *Appl. Phys. Express* **2016**, *9*, 061602.
[31] J. P. Folkers, C. B. Gorman, P. E. Laibinis, S. Buchholz, G. M. Whitesides, R. G. Nuzzo, *Langmuir* **1995**, *11*, 813.
[32] T. Zaki, R. Rodel, F. Letzkus, H. Richter, U. Zschieschang, H. Klauk, J. N. Burghartz, *IEEE Electron Device Lett.* **2013**, *34*, 520.
[33] U. Zschieschang, F. Ante, M. Schlörholz, M. Schmidt, K. Kern, H. Klauk, *Adv. Mater.* **2010**, *22*, 4489.
[34] P. H. Wöbkenberg, J. Ball, F. B. Kooistra, J. C. Hummelen, D. M. De Leeuw, D. D. C. Bradley, T. D. Anthopoulos, *Appl. Phys. Lett.* **2008**, *93*, 013303.
[35] S. A. Campbell, D. C. Gilmer, X. C. Wang, M. T. Hsieh, H. S. Kim, W. L. Gladfelter, J. Yan, *IEEE Trans. Electron Devices* **1997**, *44*, 104.
[36] S. A. Campbell, H.-S. Kim, D. C. Gilmer, B. He, T. Ma, W. L. Gladfelter, *IBM J. Res. Dev.* **1999**, *43*, 383.
[37] T. Fuyuki, H. Matsunami, *Jpn. J. Appl. Phys.* **1986**, *12*, 1288.
[38] N. Rausch, E. P. Burte, *J. Electrochem. Soc.* **1993**, *140*, 145.
[39] J. Yan, D. C. Gilmer, S. A. Campbell, W. L. Gladfelter, P. G. Schmid, *J. Vac. Sci. Technol., B Microelectron. Nanometer. Struct.* **1996**, *14*, 1706.
[40] M. Bareiß, D. Kälblein, C. Jirauschek, A. Exner, I. Pavlichenko, B. Lotsch, U. Zschieschang, H. Klauk, G. Scarpa, B. Fabel, W. Porod, P. Lugli, *Appl. Phys. Lett.* **2012**, *101*, 083113.
[41] J. Robertson, *Eur. Phys. J.: Appl. Phys.* **2004**, *28*, 265.
[42] U. Kraft, K. Takimiya, M. J. Kang, R. Rödel, F. Letzkus, J. N. Burghartz, E. Weber, H. Klauk, *Org. Electron.* **2016**, *35*, 33.
[43] K. Takimiya, H. Ebata, K. Sakamoto, T. Izawa, T. Otsubo, Y. Kunugi, *J. Am. Chem. Soc.* **2006**, *128*, 12604.
[44] Z. Luo, B. Peng, J. Zeng, Z. Yu, Y. Zhao, J. Xie, R. Lan, Z. Ma, L. Pan, K. Cao, Y. Lu, D. He, H. Ning, W. Meng, Y. Yang, X. Chen, W. Li, J. Wang, D. Pan, X. Tu, W. Huo, X. Huang, D. Shi, L. Li, M. Liu, Y. Shi, X. Feng, P. K. L. Chan, X. Wang, *Nat. Commun.* **2021**, *12*, 1928.
[45] S. H. Kim, I. Kang, Y. G. Y. H. Kim, H. R. Hwang, Y. G. Y. H. Kim, S. K. Kwon, J. Jang, *J. Mater. Chem. C* **2013**, *1*, 2408.
[46] C. Jiang, H. W. Choi, X. Cheng, H. Ma, D. Hasko, A. Nathan, *Science* **2019**, *363*, 719.
[47] F. Ante, D. Kälblein, U. Zschieschang, T. W. Canzler, A. Werner, K. Takimiya, M. Ikeda, T. Sekitani, T. Someya, H. Klauk, *Small* **2011**, *7*, 1186.
[48] U. Zschieschang, J. W. Borchert, M. Giorgio, M. Caironi, F. Letzkus, J. N. Burghartz, U. Waizmann, J. Weis, S. Ludwigs, H. Klauk, *Adv. Funct. Mater.* **2020**, *30*, 1903812.
[49] S. Sze, K. K. Ng, in *Physics of Semiconductor Devices*, John Wiley & Sons, New York **2007**, pp. 314–316.
[50] K. Niimi, M. J. Kang, E. Miyazaki, I. Osaka, K. Takimiya, *Org. Lett.* **2011**, *13*, 3430.
[51] W. H. Lee, H. H. Choi, D. H. Kim, K. Cho, *Adv. Mater.* **2014**, *26*, 0935.
[52] M. Kettner, Z. Mi, D. Kälblein, J. Brill, P. W. M. M. Blom, R. T. Weitz, *Adv. Electron. Mater.* **2019**, *5*, 1900295.
[53] W. L. Kalb, T. Mathis, S. Haas, A. F. Stassen, B. Batlogg, *Appl. Phys. Lett.* **2007**, *90*, 092104.
[54] X. Jia, C. Fuentes-Hernandez, C. Y. Wang, Y. Park, B. Kippelen, *Sci. Adv.* **2018**, *4*, eaao1705.
[55] H. F. Iqbal, Q. Ai, K. J. Thorley, H. Chen, I. McCulloch, C. Risko, J. E. Anthony, O. D. Jurchescu, *Nat. Commun.* **2021**, *12*, 2352.
[56] G. Horowitz, R. Hajlaoui, H. Bouchriha, R. Bourguiga, M. Hajlaoui, *Adv. Mater.* **1998**, *10*, 923.
[57] J. R. Rumble, in *CRC Handbook of Chemistry and Physics*, Vol. *102*, CRC Press, Boca Raton, FL **2021**, p. 12.
[58] M. Uda, A. Nakamura, T. Yamamoto, *J. Electron Spectros. Relat. Phenom.* **1998**, *88–91*, 643.
[59] G. N. Derry, M. E. Kern, E. H. Worth, *J. Vac. Sci. Technol., A* **2015**, *33*, 060801.
[60] D. Braga, M. Ha, W. Xie, C. D. Frisbie, *Appl. Phys. Lett.* **2010**, *97*, 193311.
[61] J. Lenz, F. Giudice, F. R. Geisenhof, F. Winterer, R. T. Weitz, *Nat. Nanotechnol.* **2019**, *14*, 579.
[62] J. Li, J. Du, J. Xu, H. L. W. Chan, F. Yan, *Appl. Phys. Lett.* **2012**, *100*, 033301.
[63] S. Luan, G. W. Neudeck, *J. Appl. Phys.* **1992**, *72*, 766.
[64] D. Raiteri, P. Van Lieshout, A. Van Roermund, E. Cantatore, **2014**, *49*, 524.
[65] M. Spijkman, E. C. P. Smits, P. W. M. Blom, D. M. De Leeuw, Y. Bon Saint Cône, S. Setayesh, E. Cantatore, *Appl. Phys. Lett.* **2008**, *92*, 143304.
[66] I. Nausieda, K. K. Ryu, D. Da He, A. I. Akinwande, V. Bulović, C. G. Sodini, *IEEE Trans. Electron Devices* **2010**, *57*, 3027.
[67] Q. Cui, R. A. Sporea, W. Liu, X. Guo, *IEEE Trans. Electron Devices* **2014**, *61*, 3838.
[68] L. Feng, Q. Cui, J. Zhao, W. Tang, X. Guo, *IEEE Trans. Electron Devices* **2014**, *61*, 2220.
[69] M. Elsobky, M. Elattr, G. Alavi, F. Letzkus, H. Richter, U. Zschieschang, M. Strecker, H. Klauk, J. N. Burghartz, *Org. Electron.* **2017**, *50*, 491.
[70] Z. Yao, T. J. Chang, D. Wentzlaff, B. P. Rand, *Synth. Met.* **2021**, *278*, 116825.
[71] K. Fukuda, T. Sekitani, T. Yokota, K. Kuribara, T. Huang, T. Yamamoto, K. Takimiya, K. Cheng, T. Someya, *IEEE Electron Device Lett.* **2011**, *32*, 1448.
[72] A. Petritz, M. Krammer, E. Sauter, M. Gärtner, G. Nascimbeni, B. Schrode, A. Fian, H. Gold, A. Cojocaru, E. Karner-Petritz, R. Resel, A. Terfort, E. Zojer, M. Zharnikov, K. Zojer, B. Stadlober, *Adv. Funct. Mater.* **2018**, *28*, 1804462.
[73] T. Yokota, T. Sekitani, T. Tokuhara, N. Take, U. Zschieschang, H. Klauk, K. Takimiya, T. C. Huang, M. Takamiya, T. Sakurai, T. Someya, *IEEE Trans. Electron Devices* **2012**, *59*, 3434.
[74] X. Fang, J. Shi, X. Zhang, X. Ren, B. Lu, W. Deng, J. Jie, X. Zhang, *Adv. Funct. Mater.* **2021**, *31*, 2100237.
[75] N. Matsuhisa, M. Kaltenbrunner, T. Yokota, H. Jinno, K. Kuribara, T. Sekitani, T. Someya, *Nat. Commun.* **2015**, *6*, 7461.
[76] R. Janneck, T. S. Nowack, F. De Roose, H. Ali, W. Dehaene, P. Heremans, J. Genoe, C. Rolin, *Org. Electron.* **2019**, *67*, 64.
[77] J. Butschke, A. Ehrmann, B. Höfflinger, M. Irmscher, R. Käsmaier, F. Letzkus, H. Löschner, J. Mathuni, C. Reuter, C. Schomburg, R. Springer, *Microelectron. Eng.* **1999**, *46*, 473.
[78] F. Letzkus, J. Butschke, B. Höfflinger, M. Irmscher, C. Reuter, R. Springer, A. Ehrmann, J. Mathuni, *Microelectron. Eng.* **2000**, *53*, 609.
[79] J. Melngailis, *J. Vac. Sci. Technol., B* **1998**, *16*, 927.

ADVANCED ELECTRONIC MATERIALS

Supporting Information

for *Adv. Electron. Mater.,* DOI: 10.1002/aelm.202101215

Subthreshold Swing of 59 mV decade^{-1} in Nanoscale Flexible Ultralow-Voltage Organic Transistors

Michael Geiger, Robin Lingstädt, Tobias Wollandt, Julia Deuschle, Ute Zschieschang, Florian Letzkus, Joachim N. Burghartz, Peter A.van Aken, R. Thomas Weitz, and Hagen Klauk**

Supporting Information

Subthreshold Swing of 59 mV/decade in Nanoscale Flexible Ultralow-Voltage Organic Transistors

Michael Geiger, Robin Lingstädt, Tobias Wollandt, Julia Deuschle, Ute Zschieschang, Florian Letzkus, Joachim N. Burghartz, Peter A. van Aken, R. Thomas Weitz, Hagen Klauk

Contents

1. Surface roughness

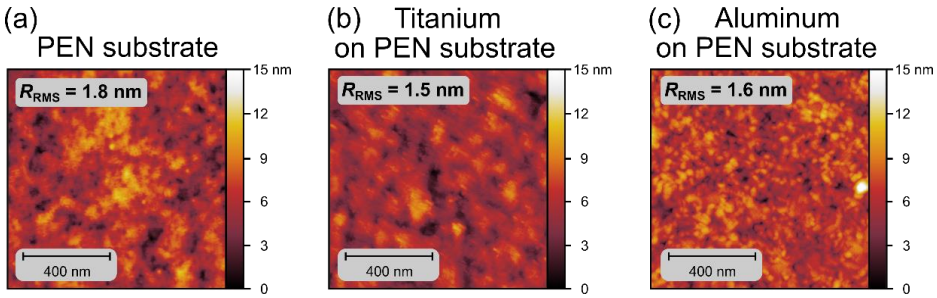


Figure S1. Atomic force microscopy (AFM) images and root-mean-square surface roughness of (a) the surface of a PEN substrate, (b) a 25-nm-thick vacuum-deposited titanium film on PEN, and (c) a 25-nm-thick vacuum-deposited aluminum film on PEN.

2. Error calculation for the permittivity of TiO_x

For calculating the permittivity of the oxide, the following theoretical relation between the unit-area oxide capacitance and the oxide thickness is fitted to the measurement data:

$$C_{\mathrm{ox}} = \varepsilon_0 \varepsilon_{\mathrm{ox}} \frac{1}{t_{\mathrm{ox}}}$$

As a consequence, the linear fit in the $C_{ox}(1/t_{ox})$-plot must go through the origin ($1/t_{ox} = 0$, $C_{ox} = 0$). This boundary condition significantly narrows the range of reasonable fit lines compared to what might have been expected from looking at the data points and their error bars with bare eyes. To illustrate this, we have plotted in the two graphs below the fit lines which correspond to $\varepsilon = 13$ and $\varepsilon = 15$ (i.e., $\varepsilon = 14 \pm 1$; Figure S2(a)) and to $\varepsilon = 12$ and $\varepsilon = 16$ (i.e., $\varepsilon = 14 \pm 2$; Figure S2(b)). By fitting the theoretical formula to the data (using the "Orthogonal Distance Regression" algorithm)[S1] and taking into account the error bars, we obtain an error of 0.6 for the permittivity. We have rounded this value up and report a permittivity of 14 ± 1 for the TiO_x.

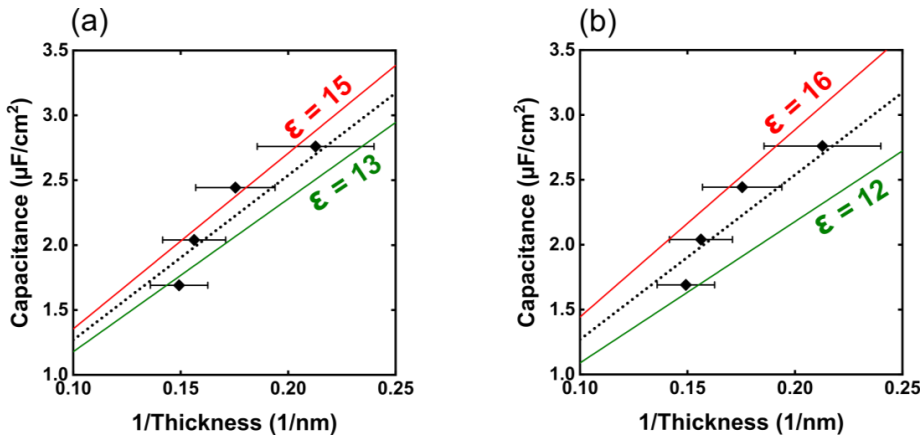


Figure S2. (a) Measured unit-area capacitance of capacitors based on bare plasma-grown TiO_x plotted as a function of the inverse of the TiO_x thickness, as determined by TEM, to calculate the relative permittivity of the plasma-grown titanium oxide. Shown is the fit which yields the total least squares of the orthogonal distance regression (black dashed line) and fit lines which correspond to $\varepsilon = 13$ and $\varepsilon = 15$ (i.e., $\varepsilon = 14 \pm 1$). (b) Fit lines which correspond to $\varepsilon = 12$ and $\varepsilon = 16$ (i.e., $\varepsilon = 14 \pm 2$).

3. Temporal evolution of the width-normalized contact resistance

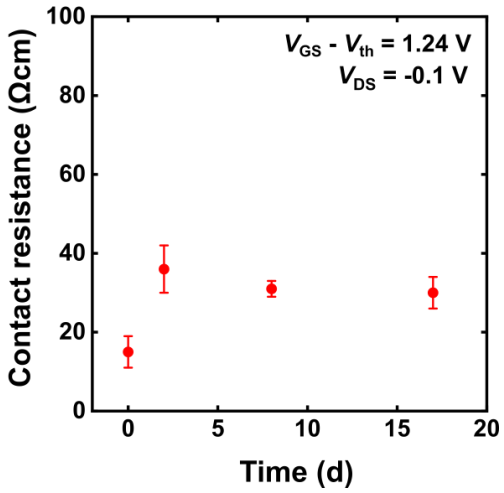


Figure S3. Evolution of the width-normalized contact resistance of flexible DPh-DNTT TFTs with a Ti/TiO_x/SAM gate stack over a period of 17 days after fabrication while being stored in ambient air with a relative humidity of about 40%.

4. Summary of unipolar inverters

Table S1. Summary of the parameters of the unipolar inverters from Figure 9.

Ref.	Substrate	Circuit design	# of TFTs	Supply voltage (V)	Small-signal gain	Noise margin (% of V_{DD}/2)
[28]	Flexible PEN	Pseudo-CMOS	2	2	500	70
[64]	Flexible PEN	Level-shift	4	20	6400	82
[69]	Flexible PI/BCB	Zero-V_{GS}	2	3	80	87
[69]	Flexible PI/BCB	Pseudo-D	2	3	100	87
[71]	Glass	Pseudo-CMOS	4	1	150	70
[71]	Glass	Pseudo-CMOS	4	1.5	250	60
[72]	Flexible PC	Zero-V_{GS}	2	4	220	66
[73]	Flexible PI	Pseudo-CMOS	4	2	400	70
[74]	Si wafer	Zero-V_{GS}	2	20	24	82
[75]	Flexible PI	Pseudo-CMOS	4	3	290	97
[76]	Si wafer	Pseudo-CMOS	4	20	40	96
This work	Flexible PEN	Zero-V_{GS}	2	1	1900	79
This work	Flexible PEN	Zero-V_{GS}	2	0.6	360	77
This work	Flexible PEN	Zero-V_{GS}	2	0.4	180	70

5. Implementation of the TFT-fabrication process in a manufacturing environment

The process for the fabrication of the organic TFTs described here is in principle similar to the process for the fabrication of organic light-emitting diodes in commercially manufactured active-matrix organic light-emitting diode (AMOLED) displays. All of the functional materials (gate electrodes, source/drain contacts, and organic semiconductor in the case of the organic TFTs; red, green and blue organic emitters in the case of AMOLED displays) are sequentially deposited by thermal evaporation or sublimation in a vacuum cluster system and patterned using stencil masks. This process avoids the use of resists, solvents and irradiation, all of which are potentially harmful to organic semiconductors, as well as the costs associated with the disposal of potentially toxic, carcinogenic and/or environmentally harmful chemicals often used in solution processing. The main difference between the TFT-fabrication process described here and the commercial OLED-fabrication process is that the display industry utilizes substrates with a size on the order of 1 square-meter and stencil masks made from invar metals[S2,S3] (fine-metal mask; FMM) that are aligned using automated vision systems and which provide a resolution on the order of 10 µm, whereas the TFT process described here is limited to a substrate size of a few square-centimeters and manual mask alignment, while providing a resolution of about 1 µm. Implementing this TFT process in a commercial manufacturing environment would thus make it possible to take advantage of rapid automatic mask alignment, but will likely lead to a compromise in terms of the TFT channel length (by using the larger-area commercial metal masks instead of the silicon masks employed here), unless the metal-mask resolution can be further improved. The plasma-oxidation process described here for the growth of the TFTs' gate oxide would require the addition of a plasma chamber to the cluster tool in which the depositions of the organic and inorganic materials are performed in commercial AMOLED display manufacturing. The formation of the thiol and phosphonic acid monolayers for the contact treatment and the gate dielectric, respectively, which in the work described here were carried out by immersing the substrates into ethanol or 2-propanol solutions, can alternatively be accomplished by a combination of vacuum deposition and thermal treatment,[S4] which are processes that can also be integrated into existing commercial cluster-tool process flows.

References

[S1] P. T. Bogs, R.H. Byrd, R.B. Schnabel, *SIAM J. Sci. and Stat. Comput.* **1987**, 8, 1052.
[S2] J.-J. Lih, C.-I. Chao, C.-C. Lee, *J. Soc. Inf. Display* **2007**, 15, 3.
[S3] S.-K. Hong, J.-H. Sim, I.-G. Seo, K.-C. Kim, S.-I. Bae, H.-Y. Lee, N.-Y. Lee, J. Jang, *J. Display Technol.* **2010**, 6, 601.
[S4] S. Gupta, H. Gleskova, *Org. Electron.* **2013**, 14, 354.

Chapter 7

Summary and Outlook

Organic TFTs are promising candidates for the realization of novel future electronic systems, in particular for flexible and/or large-area applications. Organic TFTs have undergone steady improvements during the last decades. However, they have not yet reached a sufficient level to be fully commercialized and are subject to ongoing research. A central element of organic TFTs is the gate dielectric which is determinative for the TFT performance in many respects. In the presented thesis, the approach of a hybrid gate dielectric consisting of a thin metal-oxide layer complemented by a molecular self-assembled monolayer was pursued. Various aspects of the dielectric in terms of its intrinsic properties as well as the effects on the characteristics of organic TFTs were investigated with the objective to gain a deeper understanding of the relevant material properties and processes and to finally improve the performance of organic TFTs.

One important benefit of a hybrid dielectric is the fact that a large unit-area capacitance can be achieved. This is a prerequisite for low-voltage TFTs which are particularly interesting for mobile and wearable electronics applications. Chapter 3 dealt with the consequences of an ultrathin hybrid gate dielectric (and thus low-voltage operation of the TFT) on the extraction of the trap DOS in organic TFTs. The work in this chapter is based on the Grünewald method which makes it possible to extract the trap DOS from a single measured transfer curve of a TFT. The theoretical model of the original Grünewald method contains a simplification which limits its application to TFTs with high operating voltages of several tens of volts. The goal of this study was to extend the applicability of the Grünewald method to state-of-the-art low-voltage TFTs with an ultrathin hybrid gate dielectric. Therefore, the basic theoretical assumptions of the original model were reevaluated and its simplifications regarding the thickness of gate dielectric removed. To demonstrate the significance of this extension, the calculation of the trap DOS was performed on TFTs with a thick and with a thin gate dielectric, once using the original Grünewald method and once using the novel extended Grünewald method. For the TFT with the thick gate dielectric, the original and the extended method yield virtually the same result, which confirms the validity of the original Grünewald method for high-voltage

TFTs. In contrast, for the TFT with the thin gate dielectric, the original method significantly overestimated the resulting trap DOS. This demonstrates the need of the newly developed extended Grünewald method to reliably extract the trap DOS in low-voltage TFTs.

For the performance of organic TFTs not only the electrical properties of the gate dielectric are relevant but also its surface properties, such as the surface roughness. Surface roughness plays a special role in organic TFTs as they can be manufactured on unconventional substrates which are typically characterized by an increased degree of surface roughness compared to conventional substrates. In Chapter 4 the relation between the surface roughness of a hybrid AlO_x/SAM gate dielectric and the performance of organic bottom-gate TFTs was investigated with the goal of gaining a deeper insight into the underlying mechanisms. In order to create a model system in which all observed differences in TFT performance can safely be ascribed to effects which are related to the surface roughness, a method was developed to exclusively tune the degree of surface roughness of the gate dielectric. It was found that by controlling the substrate temperature during the aluminum deposition, the degree of surface roughness of a hybrid AlO_x/SAM gate dielectric can be systematically tuned over a wide range. Electrical transport measurements on bottom-gate TFTs showed that with increasing surface roughness of the gate dielectric the effective mobility decreases and the subthreshold swing increases substantially. The results of applying the extended Grünewald method (developed in Chapter 3) revealed a clear correlation between the surface roughness of the gate dielectric and the density of trap states in the semiconductor layer. The analysis of electrical transport measurements as well as AFM and XRD studies indicated the same finding which is the key result of this study: Grain boundaries in the semiconductor layer are the major structural defect induced by the surface roughness of the gate dielectric. These grain boundaries severely hinder charge transport in the semiconductor layer and thus diminish the TFT performance. The results of this study emphasize the importance of a small surface roughness of the gate dielectric for high-performance bottom-gate organic TFTs.

In the next two chapters a primary focus was put on the metal-oxide component of the hybrid gate dielectric. Chapter 5 dealt with the fabrication and optimization of ultrathin aluminum oxide films by plasma oxidation of the surface of vacuum-deposited aluminum films. It was investigated to which extend the properties of the resulting AlO_x dielectrics and hybrid AlO_x/SAM dielectrics can be tuned by adjusting two of the parameters of the plasma-oxidation process, namely the plasma power and the duration of the plasma exposure. The results showed that the thickness and the capacitance of the dielectrics, the leakage-current density through the dielectrics, the surface morphology of the dielectrics and the current-voltage characteristics of the organic TFTs in which these dielectrics serve as the gate insulator can be tuned over a wide range by controlling the plasma power and the plasma duration. This study reveals the optimum range of plasma parameters that yield the highest transistor performance and clearly demonstrates the critical importance of providing an optimized AlO_x film, even when complementing it with a SAM.

Finally, in Chapter 6 the use of plasma-grown titanium oxide films as the first component in hybrid TiO_x/SAM gate dielectrics for flexible ultralow-voltage organic TFTs and circuits

was developed and explored. The optimized hybrid TiO_x/SAM dielectrics provided a favorable combination of low charge leakage and high unit-area capacitance. Flexible organic TFTs with the novel Ti/TiO_x/SAM gate stack showed excellent electrical performance and set a number of performance records for organic TFTs including a subthreshold swing of (59 ± 1) mV/decade for channel lengths as small as 0.7 µm, a width-normalized transconductance of 0.6 S/m at a gate-source voltage of -1 V, an on/off current ratio of 10^7 for a gate-source-voltage range of 1 V, a width-normalized contact resistance of (15 ± 5) Ωcm and a threshold-voltage shift of 10 mV after continuous bias stress for 72 hours. By combing organic TFTs with an Al/AlO_x/SAM gate stack and a Ti/TiO_x/SAM gate stack, unipolar zero-V_{GS} inverters were demonstrated. These inverters combined large small-signal gains and large noise margins at ultra-low supply voltages of 1 V or less.

In summary, the results of this thesis highlight the far-reaching effects of the gate dielectric properties on the characteristics of low-voltage organic TFTs. Especially the significance of the plasma-grown metal-oxide component in ultrathin hybrid gate dielectrics is revealed. This thesis contributes to the advance of organic electronics by investigating the underlying mechanisms for the fabrication of high-quality gate dielectrics and by developing a novel hybrid TiO_x/SAM dielectric for the use in flexible ultralow-voltage organic TFTs.

In the future, it will be interesting to pursue the approach of the demonstrated zero-V_{GS} inverters and use them as building blocks for more complex unipolar circuits such as NAND gates or NOR gates. The minimum channel length of 0.7 µm which was achieved in the presented work is close to the minimum of what is possible by the use of high-resolution silicon stencil masks.[152–154] To address the dynamic performance of TFTs and circuits, the dimensions of the TFTs have to be reduced, in particular the channel length and the gate-to-contact-overlap.[155,156] A powerful approach is the use of electron-beam lithography for pattering the TFTs.[156] If it is feasible to manufacture the presented TFTs and unipolar inverters by means of electron-beam lithography, while maintaining their excellent electrical properties (i.e. the small subthreshold swing, the small width-normalized contact resistance and the long-term stability), organic TFTs and circuits with a remarkable dynamic performance will be possible.

References

[1] Bardeen, J. & Brattain, W. H. The Transistor, A Semi-Conductor Triode. *Physical Review* **74**, 230–231 (1948).

[2] Shockley, W. The theory of p-n junctions in semiconductors and p-n junction transistors. *The Bell System Technical Journal* **28**, 435–489 (1949).

[3] Handy, J. How Many Transistors Have Ever Shipped? *Forbes* (2014).

[4] Jones, S. TSMC and Samsung 5 nm Comparison (2019). URL: https://semiwiki.com/semiconductor-manufacturers/samsung-foundry/8157-tsmc-and-samsung-5nm-comparison/ (retrieved 21.10.2021).

[5] Klauk, H. Organic thin-film transistors. *Chemical Society Reviews* **39**, 2643–2666 (2010).

[6] Paterson, A. F. *et al.* Recent Progress in High-Mobility Organic Transistors: A Reality Check. *Advanced Materials* **30**, 1801079 (2018).

[7] Borchert, J. W. *et al.* Flexible low-voltage high-frequency organic thin-film transistors. *Science Advances* **6**, eaaz5156 (2020).

[8] Pope, M. & Swenberg, C. *Electronic Processes in Organic Crystals and Polymers* (Oxford University Press, New York, 1999).

[9] Zschieschang, U. & Klauk, H. Organic transistors on paper: a brief review. *Journal of Materials Chemistry C* (2019).

[10] Cherenack, K. & Van Pieterson, L. Smart textiles: Challenges and opportunities. *Journal of Applied Physics* **112**, 091301 (2012).

[11] Irimia-Vladu, M., Głowacki, E. D., Voss, G., Bauer, S. & Sariciftci, N. S. Green and biodegradable electronics. *Materials Today* **15**, 340–346 (2012).

[12] Matsuhisa, N. *et al.* Printable elastic conductors with a high conductivity for electronic textile applications. *Nature Communications* **6**, 7461 (2015).

[13] Ebata, H. *et al.* Highly Soluble [1]Benzothieno[3,2-b]benzothiophene (BTBT) Derivatives for High-Performance, Solution-Processed Organic Field-Effect Transistors. *Journal of the American Chemical Society* **129**, 15732–15733 (2007).

[14] Minder, N. A. *et al.* Tailoring the molecular structure to suppress extrinsic disorder in organic transistors. *Advanced Materials* **26**, 1254–1260 (2014).

[15] Henson, Z. B., Müllen, K. & Bazan, G. C. Design strategies for organic semiconductors beyond the molecular formula. *Nature Chemistry* **4**, 699 (2012).

[16] Takimiya, K., Shinamura, S., Osaka, I. & Miyazaki, E. Thienoacene-based organic semiconductors. *Advanced Materials* **23**, 4347–4370 (2011).

[17] Tsumura, A., Koezuka, H. & Ando, T. Macromolecular electronic device: Field-effect transistor with a polythiophene thin film. *Applied Physics Letters* **49**, 1210–1212 (1986).

[18] Horowitz, G., Fichou, D., Peng, X., Xu, Z. & Garnier, F. A field-effect transistor based on conjugated alpha-sexithienyl. *Solid State Communications* **72**, 381–384 (1989).

[19] Takimiya, K., Yamamoto, T., Ebata, H. & Izawa, T. Design strategy for air-stable organic semiconductors applicable to high-performance field-effect transistors. *Science and Technology of Advanced Materials* **8**, 273–276 (2007).

[20] Okamoto, T. *et al.* Robust, high-performance n-type organic semiconductors. *Science Advances* **6**, eaaz0632 (2020).

[21] Yamamoto, T. & Takimiya, K. Facile synthesis of highly π-extended heteroarenes, dinaphtho[2,3-b:2′,3′-f]chalcogenopheno[3,2-b]chalcogenophenes, and their application to field-effect transistors. *Journal of the American Chemical Society* **129**, 2224–2225 (2007).

[22] Zschieschang, U. *et al.* Dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) thin-film transistors with improved performance and stability. *Organic Electronics* **12**, 1370–1375 (2011).

[23] Kang, M. J. *et al.* Alkylated Dinaphtho-[2,3-b:2′,3′-f]thieno[3,2-b]thiophene-f] (Cn-DNTTs): Organic Semiconductors for High-Performance Thin-Film Transistors. *Advanced Materials* **23**, 1222–1225 (2011).

[24] Kraft, U. *et al.* Detailed analysis and contact properties of low-voltage organic thin-film transistors based on dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) and its didecyl and diphenyl derivatives. *Organic Electronics* **35**, 33–40 (2016).

[25] Kalb, W. L., Mathis, T., Haas, S., Stassen, A. F. & Batlogg, B. Organic small molecule field-effect transistors with cytop™ gate dielectric: Eliminating gate bias stress effects. *Applied Physics Letters* **90**, 092104 (2007).

[26] Yang, S. Y., Shin, K. & Park, C. E. The effect of gate-dielectric surface energy on pentacene morphology and organic field-effect transistor characteristics. *Advanced Functional Materials* **15**, 1806–1814 (2005).

[27] Fukuda, K. *et al.* Effects of the alkyl chain length in phosphonic acid self-assembled monolayer gate dielectrics on the performance and stability of low-voltage organic thin-film transistors. *Applied Physics Letters* **95**, 203301 (2009).

[28] Sze, S. M. & Ng, K. K. *Physics of Semiconductor Devices* (John Wiley & Sons, Ltd, 2006).

[29] Hunklinger, S. *Festkörperphysik* (De Gruyter Oldenbourg, 2017).

[30] Stallinga, P. *Electrical Characterization of Organic Electronic Materials and Devices* (John Wiley & Sons, Ltd, 2009).

[31] Klauk, H. Lecture: Organische Transistoren (2017). University of Stuttgart, Faculty of Computer Science, Electrical Enineering and Information Technology.

[32] Weis, J. Lecture: Semiconducor Physics (2016). University of Stuttgart, Faculty of Mathematics and Physics.

[33] Kittel, C. *Introduction to Solid State Physics* (John Wiley & Sons, Ltd, 2004).

[34] Kopitzki, K. & Herzog, P. *Einführung in die Festkörperphysik* (Springer Spektrum, 2017).

[35] Wilson, A. H. & Dirac, P. A. M. The theory of electronic semi-conductors. *Proceedings of the Royal Society of London* **133**, 458–491 (1931).

[36] Brotherton, S. *Introduction to Thin Film Transistors* (Springer International Publishing, 2013), 1 edn.

[37] Fick, A. Ueber diffusion. *Annalen der Physik* **170**, 59–86 (1855).

[38] Brews, J. A charge-sheet model of the MOSFET. *Solid-State Electronics* **21**, 345–355 (1978).

[39] Vollhardt, K. P. C. & Schore, N. E. *Organische Chemie* (Wiley-VCH, Weinheim, 2000).

[40] Park, S. K., Jackson, T. N., Anthony, J. E. & Mourey, D. A. High mobility solution processed 6,13-bis(triisopropyl-silylethynyl) pentacene organic thin film transistors. *Applied Physics Letters* **91**, 063514 (2007).

[41] Niimi, K., Kang, M. J., Miyazaki, E., Osaka, I. & Takimiya, K. General synthesis of dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) derivatives. *Organic Letters* **13**, 3430–3433 (2011).

[42] Coropceanu, V. *et al.* Charge transport in organic semiconductors. *Chemical Reviews* **107**, 926–952 (2007).

[43] Kang, J. H., Da Silva Filho, D., Bredas, J. L. & Zhu, X. Y. Shallow trap states in pentacene thin films from molecular sliding. *Applied Physics Letters* **86**, 152115 (2005).

[44] Willa, K. *et al.* From organic single crystals to solution processed thin-films: Charge transport and trapping with varying degree of order. *Journal of Applied Physics* **113**, 133707 (2013).

[45] Häusermann, R. *et al.* Device performance and density of trap states of organic and inorganic field-effect transistors. *Organic Electronics* **28**, 306–313 (2016).

[46] Hulea, I. N. *et al.* Tunable Fröhlich polarons in organic single-crystal transistors. *Nature Materials* **5**, 982–986 (2006).

[47] Kim, C., Facchetti, A. & Marks, T. J. Gate dielectric microstructural control of pentacene film growth mode and field-effect transistor performance. *Advanced Materials* **19**, 2561–2566 (2007).

[48] Brütting, W. & Adachi, C. *Physics of Organic Semiconductors* (Wiley-VCH, Berlin, 2013).

[49] Dunlap, W. C. & Watters, R. L. Direct measurement of the dielectric constants of silicon and germanium. *Physical Review* **92**, 1396–1397 (1953).

[50] Rivnay, J., Noriega, R., Kline, R. J., Salleo, A. & Toney, M. F. Quantitative analysis of lattice disorder and crystallite size in organic semiconductor thin films. *Physical Review B* **84**, 045203 (2011).

[51] Rivnay, J., Mannsfeld, S. C., Miller, C. E., Salleo, A. & Toney, M. F. Quantitative determination of organic semiconductor microstructure from the molecular to device scale. *Chemical Reviews* **112**, 5488–5519 (2012).

[52] Ciuchi, S. & Fratini, S. Electronic transport and quantum localization effects in organic semiconductors. *Physical Review B* **86**, 245201 (2012).

[53] Fratini, S., Mayou, D. & Ciuchi, S. The transient localization scenario for charge transport in crystalline organic materials. *Advanced Functional Materials* **26**, 2292–2315 (2016).

[54] Fratini, S., Nikolka, M., Salleo, A., Schweicher, G. & Sirringhaus, H. Charge transport in high-mobility conjugated polymers and molecular semiconductors. *Nature Materials* **19**, 491–502 (2020).

[55] Kettner, M., Zhou, M., Brill, J., Blom, P. W. & Weitz, R. T. Complete Suppression of Bias-Induced Threshold Voltage Shift below 273 K in Solution-Processed High-Performance Organic Transistors. *ACS Applied Materials and Interfaces* **10**, 35449 (2018).

[56] Zuo, G., Linares, M., Upreti, T. & Kemerink, M. General rule for the energy of water-induced traps in organic semiconductors. *Nature Materials* **18**, 588–593 (2019).

[57] Kirova, N. & Bussac, M. N. Self-trapping of electrons at the field-effect junction of a molecular crystal. *Physical Review B* **68**, 235312 (2003).

[58] Houili, H., Picon, J. D., Zuppiroli, L. & Bussac, M. N. Polarization effects in the channel of an organic field-effect transistor. *Journal of Applied Physics* **100**, 023702 (2006).

[59] Haneef, H. F., Zeidell, A. M. & Jurchescu, O. D. Charge carrier traps in organic semiconductors: A review on the underlying physics and impact on electronic devices. *Journal of Materials Chemistry C* **8**, 759–787 (2020).

[60] Steudel, S. *et al.* Influence of the dielectric roughness on the performance of pentacene transistors. *Applied Physics Letters* **85**, 4400–4402 (2004).

[61] Fritz, S. E., Kelley, T. W. & Frisbie, C. D. Effect of dielectric roughness on performance of pentacene TFTs and restoration of performance with a polymeric smoothing layer. *Journal of Physical Chemistry B* **109**, 10574–10577 (2005).

[62] Gilles Horowitz, R. H. & Delannoy, P. Temperature Dependence of the Field-Effect Mobility of Sexithiophene. Determination of the Density of Traps. *Journal de Physique III* **5**, 355–371 (1995).

[63] Horowitz, G., Hajlaoui, M. E. & Hajlaoui, R. Temperature and gate voltage dependence of hole mobility in polycrystalline oligothiophene thin film transistors. *Journal of Applied Physics* **87**, 4456–4463 (2000).

[64] Mehraeen, S., Coropceanu, V. & Brédas, J. L. Role of band states and trap states in the electrical properties of organic semiconductors: Hopping versus mobility edge model. *Physical Review B* **87**, 195209 (2013).

[65] Tessler, N., Preezant, Y., Rappaport, N. & Roichman, Y. Charge transport in disordered organic materials and its relevance to thin-film devices: A tutorial review. *Advanced Materials* **21**, 2741–2761 (2009).

[66] Miller, A. & Abrahams, E. Impurity Conduction at Low Concentrations. *Physical Review* **120**, 745–755 (1960).

[67] Bässler, H. Localized states and electronic transport in single component organic solids with diagonal disorder. *Physica Status Solidi (B)* **107**, 9–54 (1981).

[68] Vissenberg, M. C. J. M. & Matters, M. Theory of the field-effect mobility in amorphous organic transistors. *Physical Review B* **57**, 12964–12967 (1998).

[69] Baranovskii, S. D. Theoretical description of charge transport in disordered organic semiconductors. *Physica Status Solidi (b)* **251**, 487–525 (2014).

[70] Bussolotti, F. *et al.* Direct detection of density of gap states in C60 single crystals by photoemission spectroscopy. *Physical Review B* **92**, 115102 (2015).

[71] Yang, J.-P., Bussolotti, F., Kera, S. & Ueno, N. Origin and role of gap states in organic semiconductor studied by UPS: as the nature of organic molecular crystals. *Journal of Physics D* **50**, 423002 (2017).

[72] Palermo, V., Palma, M. & Samori, P. Electronic characterization of organic thin films by Kelvin probe force microscopy. *Advanced Materials* **18**, 145 (2006).

[73] Yogev, S. *et al.* Fermi level pinning by gap states in organic semiconductors. *Physical Review Letters* **110**, 036803 (2013).

[74] Zhang, Y., Ziegler, D. & Salmeron, M. Charge trapping states at the sio2–oligothiophene monolayer interface in field effect transistors studied by kelvin probe force microscopy. *ACS Nano* **7**, 8258–8265 (2013).

[75] Lee, K. *et al.* Interfacial trap density-of-states in pentacene- and ZnO-based thin-film transistors measured via novel photo-excited charge-collection spectroscopy. *Advanced Materials* **22**, 3260 (2010).

[76] Jeong, S. H. & Song, C. K. Energetic distribution of interface states extracted from photo-conductance of organic thin film transistors. *Organic Electronics* **15**, 2599 (2014).

[77] Matsui, H., Mishchenko, A. S. & Hasegawa, T. Distribution of localized states from fine analysis of electron spin resonance spectra in organic transistors. *Physical Review Letters* **104**, 056602 (2010).

[78] Jang, J. *et al.* Extraction of the sub-bandgap density-of-states in polymer thin-film transistors with the multi-frequency capacitance-voltage spectroscopy. *Applied Physics Letters* **100**, 133506 (2012).

[79] Wu, W. J. *et al.* Analytical Extraction Method for Density of States in Metal Oxide Thin-Film Transistors by Using Low-Frequency Capacitance-Voltage Characteristics. *Journal of Display Technology* **12**, 888–891 (2016).

[80] Shaw, A. *et al.* Extraction of the sub-band gap density of states of Nb doped ZnO thin film transistors using C-V measurements. *Microelectronic Engineering* **178**, 213 (2017).

[81] Kalb, W. L. & Batlogg, B. Calculating the trap density of states in organic field-effect transistors from experiment: A comparison of different methods. *Physical Review B* **81**, 035327 (2010).

[82] Powell, M. J. & Pritchard, J. The effect of surface states and fixed charge on the field effect conductance of amorphous silicon. *Journal of Applied Physics* **54**, 3244–3248 (1983).

[83] Lang, D. V., Chi, X., Siegrist, T., Sergent, A. M. & Ramirez, A. P. Amorphouslike density of gap states in single-crystal pentacene. *Physical Review Letters* **93**, 086802 (2004).

[84] Kalb, W. L., Mattenberger, K. & Batlogg, B. Oxygen-related traps in pentacene thin films: Energetic position and implications for transistor performance. *Physical Review B* **78**, 035334 (2008).

[85] Kalb, W. L., Haas, S., Krellner, C., Mathis, T. & Batlogg, B. The trap DOS in small molecule organic semiconductors: A quantitative comparison of thin-film transistors with single crystals. *Physical Review B* **81**, 155315 (2010).

[86] Iqbal, H. F., Waldrip, M., Chen, H., McCulloch, I. & Jurchescu, O. D. Elucidating the role of water-related traps in the operation of polymer field-effect transistors. *Advanced Electronic Materials* **7**, 2100393 (2021).

[87] Hunter, S., Mottram, A. D. & Anthopoulos, T. D. Temperature and composition-dependent density of states in organic small-molecule/polymer blend transistors. *Journal of Applied Physics* **120**, 025502 (2016).

[88] Grünewald, M., Thomas, P. & Würtz, D. A Simple Scheme for Evaluating Field Effect Data. *Physica Status Solidi (B)* **100**, K39 (1980).

[89] Grünewald, M., Thomas, P. & Würtz, D. Field effect studies on a-Si:H films. *Journal de Physique Colloques* **42**, 532–526 (1981).

[90] Weber, K., Grünewald, M., Fuhs, W. & Thomas, P. Field Effect in a-Si:H Films. *Physica Status Solidi (B)* **133**, 133–142 (1982).

[91] Kalb, W. L., Meier, F., Mattenberger, K. & Batlogg, B. Defect healing at room temperature in pentacene thin films and improved transistor performance. *Physical Review B* **76**, 184112 (2007).

[92] Pattanasattayavong, P., Mottram, A. D., Yan, F. & Anthopoulos, T. D. Study of the Hole Transport Processes in Solution-Processed Layers of the Wide Bandgap Semiconductor Copper(I) Thiocyanate (CuSCN). *Advanced Functional Materials* **25**, 6802–6813 (2015).

[93] Diemer, P. J. *et al.* Quantitative analysis of the density of trap states at the semiconductor-dielectric interface in organic field-effect transistors. *Applied Physics Letters* **107**, 103303 (2015).

[94] Diemer, P. J. *et al.* Laser-Printed Organic Thin-Film Transistors. *Advanced Materials Technologies* **2**, 1700167 (2017).

[95] Pattanasattayavong, P., Promarak, V. & Anthopoulos, T. D. Electronic Properties of Copper(I) Thiocyanate (CuSCN). *Advanced Electronic Materials* **3**, 1600378 (2017).

[96] Za'aba, N. K., Morrison, J. J. & Taylor, D. M. Effect of relative humidity and temperature on the stability of DNTT transistors: A density of states investigation. *Organic Electronics* **45**, 174–181 (2017).

[97] Wei, P. *et al.* Dopant/Semiconductor/Electret Trilayer Architecture for High-Performance Organic Field-Effect Transistors. *Advanced Electronic Materials* **4**, 1800339 (2018).

[98] Iqbal, H. F., Holland, E. K., Anthony, J. E. & Jurchescu, O. D. Real-time monitoring of trap dynamics reveals the electronic states that limit charge transport in crystalline organic semiconductors. *Materials Horizons* **7**, 2390–2398 (2020).

[99] Goetz, K. P. *et al.* Organic single crystals of charge-transfer complexes: model systems for the study of donor/acceptor interactions. *Materials Horizons* (2021).

[100] Zardetto, V., Brown, T. M., Reale, A. & Di Carlo, A. Substrates for flexible electronics: A practical investigation on the electrical, film flexibility, optical, temperature, and solvent resistance properties. *Journal of Polymer Science Part B: Polymer Physics* **49**, 638–648 (2011).

[101] Kaltenbrunner, M. *et al.* An ultra-lightweight design for imperceptible plastic electronics. *Nature* **499**, 458–463 (2013).

[102] Leydecker, T. *et al.* Flexible non-volatile optical memory thin-film transistor device with over 256 distinct levels based on an organic bicomponent blend. *Nature Nanotechnology* **11**, 769–775 (2016).

[103] Teichert, C. *et al.* Comparison of surface roughness of polished silicon wafers measured by light scattering topography, soft-x-ray scattering, and atomic-force microscopy. *Applied Physics Letters* **2346**, 2346 (1995).

[104] Crawford, G. P. *Flexible Flat Panel Displays* (John Wiley and Sons, 2005).

[105] Garner, S., Glaesemann, S. & Li, X. Ultra-slim flexible glass for roll-to-roll electronic device fabrication. *Applied Physics A* **116** (2014).

[106] Data Sheet: Corning Willow Glass (2019). URL: https://www.corning.com/media/worldwide/Innovation/documents/WillowGlass/CorningWillowGlassFactSheets August2019.pdf (retrieved 29.11.2021).

[107] Knipp, D., Street, R. A., Krusor, B., Apte, R. & Ho, J. Polycrystalline pentacene thin films for large area electronic applications. *Journal of Non-Crystalline Solids* **299-302**, 1042–1046 (2002).

[108] Chang, S. S. *et al.* Control of roughness at interfaces and the impact on charge mobility in all-polymer field-effect transistors. *Soft Matter* **4**, 2220–2224 (2008).

[109] Jung, Y. *et al.* The effect of interfacial roughness on the thin film morphology and charge transport of high-performance polythiophenes. *Advanced Functional Materials* **18**, 742–750 (2008).

[110] Lin, G. *et al.* Impact of the lateral length scales of dielectric roughness on pentacene organic field-effect transistors. *Journal of Physics D: Applied Physics* **48** (2015).

[111] Lee, S. *et al.* Influence of Surface Energy and Roughness on Hole Mobility in Solution-Processed Hybrid Organic Thin Film Transistors. *IEEE Journal of the Electron Devices Society* **6**, 653–657 (2018).

[112] Noda, M. *et al.* An OTFT-driven rollable OLED display. *Journal of the Society for Information Display* **19**, 316–322 (2011).

[113] Someya, T. *et al.* Conformable, flexible, large-area networks of pressure and thermal sensors with organic transistor active matrixes. *Proceedings of the National Academy of Sciences* **102**, 12321–12325 (2005).

[114] Rogers, J. A., Someya, T. & Huang, Y. Materials and Mechanics for Stretchable Electronics. *Science,* **327**, 1603–1607 (2010).

[115] Sekitani, T., Zschieschang, U., Klauk, H. & Someya, T. Flexible organic transistors and circuits with extreme bending stability. *Nature materials* **9**, 1015–1022 (2010).

[116] Wang, B. *et al.* High-k gate dielectrics for emerging flexible and stretchable electronics. *Chemical Reviews* **118**, 5690–5754 (2018).

[117] Koo, J. B. *et al.* Low-voltage and high-gain pentacene inverters with plasma-enhanced atomic-layer-deposited gate dielectrics. *Applied Physics Letters* **89**, 033511 (2006).

[118] Yoon, M.-h. H., Facchetti, A. & Marks, T. J. σ-π molecular dielectric multilayers for low-voltage organic thin-film transistors. *Proceedings of the National Academy of Sciences* **102**, 4678–4682 (2005).

[119] DiBenedetto, S. A., Frattarelli, D., Ratner, M. A., Facchetti, A. & Marks, T. J. Vapor phase self-assembly of molecular gate dielectrics for thin film transistors. *Journal of the American Chemical Society* **130**, 7528–7529 (2008).

[120] Yoon, M. H., Yan, H., Facchetti, A. & Marks, T. J. Low-voltage organic field-effect transistors and inverters enabled by ultrathin cross-linked polymers as gate dielectrics. *Journal of the American Chemical Society* **127**, 10388–10395 (2005).

[121] Yang, S. Y., Kim, S. H., Shin, K., Jeon, H. & Park, C. E. Low-voltage pentacene field-effect transistors with ultrathin polymer gate dielectrics. *Applied Physics Letters* **88**, 173507 (2006).

[122] Kelley, T. W. *et al.* High-performance OTFTs using surface-modified alumina dielectrics. *Journal of Physical Chemistry B* **107**, 5877–5881 (2003).

[123] Klauk, H., Zschieschang, U., Pflaum, J. & Halik, M. Ultralow-power organic complementary circuits. *Nature* **445**, 745–748 (2007).

[124] Acharya, R. *et al.* Achieving Ultra-Low Turn-On Voltages in Organic Thin-Film Transistors : Investigating Fluoroalkyl-Phosphonic Acid Self-Assembled Monolayer Hybrid Dielectrics. *ACS Applied Materials and Interfaces* **11**, 27104–27111 (2019).

[125] Pernstich, K. P. *et al.* Threshold voltage shift in organic field effect transistors by dipole monolayers on the gate insulator. *Journal of Applied Physics* **96**, 6431–6438 (2004).

[126] Chang, M. F., Lee, P. T., McAlister, S. P. & Chin, A. Small-subthreshold-swing and low-voltage flexible organic thin-film transistors which use HfLaO as the gate dielectric. *IEEE Electron Device Letters* **30**, 133–135 (2009).

[127] Geiger, M. *et al.* Effect of the Degree of the Gate-Dielectric Surface Roughness on the Performance of Bottom-Gate Organic Thin-Film Transistors. *Advanced Materials Interfaces* 1902145 (2020).

[128] Borchert, J. W. *et al.* Small contact resistance and high-frequency operation of flexible low-voltage inverted coplanar organic transistors. *Nature Communications* **10**, 1119 (2019).

[129] Acharya, J., Wilt, J., Liu, B. & Wu, J. Probing the Dielectric Properties of Ultrathin $Al/Al_2O_3/Al$ Trilayers Fabricated Using in Situ Sputtering and Atomic Layer Deposition. *ACS Applied Materials and Interfaces* **10**, 3112–3120 (2018).

[130] Aghamohammadi, M. *et al.* Threshold-Voltage Shifts in Organic Transistors Due to Self-Assembled Monolayers at the Dielectric: Evidence for Electronic Coupling and Dipolar Effects. *ACS Applied Materials and Interfaces* **7**, 22775–22785 (2015).

[131] Leshanskaya, L. I. *et al.* Towards understanding the origin of the hysteresis effects and threshold voltage shift in organic field-effect transistors based on the electrochemically grown AlO_2 dielectric. *Thin Solid Films* **649**, 7–11 (2018).

[132] Chinnam, K. C., Gupta, S. & Gleskova, H. Aluminium oxide prepared by UV/ozone exposure for low-voltage organic thin-film transistors. *Journal of Non-Crystalline Solids* **358**, 2512–2515 (2012).

[133] Gupta, S. *et al.* Ozone oxidation methods for aluminum oxide formation: Application to low-voltage organic transistors. *Organic Electronics* **21**, 132–137 (2015).

[134] Jedaa, A. *et al.* The impact of self-assembled monolayer thickness in hybrid gate dielectrics for organic thin-film transistors. *Organic Electronics* **10**, 1442–1447 (2009).

[135] Luschtinetz, R. *et al.* Adsorption of phosphonic and ethylphosphonic acid on aluminum oxide surfaces. *Surface Science* **602**, 1347–1359 (2008).

[136] Kraft, U. *et al.* Fluoroalkylphosphonic acid self-assembled monolayer gate dielectrics for threshold-voltage control in low-voltage organic thin-film transistors. *Journal of Materials Chemistry* **20** (2010).

[137] Acton, O. *et al.* Dielectric surface-controlled low-voltage organic transistors via n-alkyl phosphonic acid self-assembled monolayers on high-k metal oxide. *ACS Applied Materials and Interfaces* **2**, 511–520 (2010).

[138] Acton, O. *et al.* Simultaneous modification of bottom-contact electrode and dielectric surfaces for organic thin-film transistors through single-component spin-cast monolayers. *Advanced Functional Materials* **21**, 1476–1488 (2011).

[139] Hutchins, D. O. *et al.* Effects of self-assembled monolayer structural order, surface homogeneity and surface energy on pentacene morphology and thin film transistor device performance. *Journal of Materials Chemistry C* **1**, 101–113 (2013).

[140] Hirata, I. *et al.* High-resolution spatial control of the threshold voltage of organic transistors by microcontact printing of alkyl and fluoroalkylphosphonic acid self-assembled monolayers. *Organic Electronics* **26**, 239–244 (2015).

[141] Hannah, S. *et al.* Interplay between Vacuum-Grown Monolayers of Alkylphosphonic Acids and the Performance of Organic Transistors Based on Dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene. *ACS Applied Materials and Interfaces* **8**, 25405–25414 (2016).

[142] Gleskova, H., Gupta, S. & Šutta, P. Structural changes in vapour-assembled n-octylphosphonic acid monolayer with post-deposition annealing: Correlation with bias-induced transistor instability. *Organic Electronics* **14**, 3000–3006 (2013).

[143] Gupta, S. & Gleskova, H. Dry growth of n-octylphosphonic acid monolayer for low-voltage organic thin-film transistors. *Organic Electronics* **14**, 354–361 (2013).

[144] Hauffman, T., Hubin, A. & Terryn, H. Study of the self-assembling of n-octylphosphonic acid layers on aluminum oxide from ethanolic solutions. *Surface and Interface Analysis* **45**, 1435–1440 (2013).

[145] Bauer, T. *et al.* Phosphonate-and Carboxylate-Based Self-Assembled Monolayers for Organic Devices: A Theoretical Study of Surface Binding on Aluminum Oxide with Experimental Support. *ACS Applied Materials and Interfaces* **5**, 6073 (2013).

[146] Kraft, U. *et al.* Flexible low-voltage organic complementary circuits: Finding the optimum combination of semiconductors and monolayer gate dielectrics. *Advanced Materials* **27**, 207–214 (2015).

[147] Zschieschang, U., Bader, V. P. & Klauk, H. Below-one-volt organic thin-film transistors with large on/off current ratios. *Organic Electronics* **49**, 179–186 (2017).

[148] Majewski, L. A., Schroeder, R. & Grell, M. One volt organic transistor. *Advanced Materials* **17**, 192–196 (2005).

[149] Majewski, L. A., Schroeder, R. & Grell, M. Low-voltage, high-performance organic field-effect transistors with an ultra-thin TiO_2 layer as gate insulator. *Advanced Functional Materials* **15**, 1017–1022 (2005).

[150] Jinno, H. *et al.* Low operating voltage organic transistors and circuits with anodic titanium oxide and phosphonic acid self-assembled monolayer dielectrics. *Organic Electronics* **40**, 58–64 (2017).

[151] Campbell, S. A. *et al.* MOSFET transistors fabricated with high permitivity TiO_2 dielectrics. *IEEE Transactions on Electron Devices* **44**, 104–109 (1997).

[152] Zaki, T. *et al.* S-parameter characterization of submicrometer low-voltage organic thin-film transistors. *IEEE Electron Device Letters* **34**, 520–522 (2013).

[153] Zschieschang, U. *et al.* Megahertz operation of flexible low-voltage organic thin-film transistors. *Organic Electronics* **14**, 1516–1520 (2013).

[154] Zschieschang, U. *et al.* Stencil lithography for organic thin-film transistors with a channel length of 300 nm. *Organic Electronics* **61**, 65–69 (2018).

[155] Klauk, H. Will We See Gigahertz Organic Transistors? *Advanced Electronic Materials* **4**, 1700474 (2018).

[156] Zschieschang, U. *et al.* Roadmap to Gigahertz Organic Transistors. *Advanced Functional Materials* **30**, 1903812 (2020).

List of acronyms

a-Si:H	Hydrogenated amorphous silicon
AFM	Atomic force microscopy
AlO_x	Aluminum oxide
AMLCD	Active-matrix liquid-crystal display
AMOLED	Active-matrix organic light-emitting diode
BF	Bright field
C_{10}-DNTT	Didecyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene
CB	Conduction band
CMOS	Complementary metal-oxide-semiconductor
CVD	Chemical vapor deposition
DNTT	Dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene
DPh-BTBT	Diphenyl-[1]benzothieno[3,2-b][1]benzothiophene
DPh-DNTT	Diphenyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene
DOS	Density of states
EDX	Energy dispersive X-ray spectroscopy
EELS	Electron energy loss spectroscopy
FET	Field-effect transistor
FIB	Focused ion beam
FMM	Fine-metal mask
HHCF	Height-height correlation function
HOMO	Highest occupied molecular orbital
LUMO	Lowest unoccupied molecular orbital

MOSFET	Metal-oxide-semiconductor field-effect transistor
MPI	Max Planck Institute
N1100	N,N'-bis(2,2,3,3,4,4,4-heptafluorobutyl)-1,7-dicyano-perylene-(3,4:9,10)-tetracarboxylic diimide
OLED	Organic light-emitting diode
PECVD	Plasma-enhanced chemical-vapor deposition
PEN	Polyethylene naphthalate
PET	Polyethylene terephthalate
PFBT	Pentafluorobenzenethiol
RIE	Reactive ion etching
RMS	Root mean square
SOI	Silicon-on-insulator
TEM	Transmission electron microscopy
TLM	Transmission-line method
TFT	Thin-film transistor
TiO_x	Titanium oxide
TIPS	Tri-isopropylsilyl-ethynyl
SAM	Self-assembled monolayer
SEM	Scanning electron microscopy
UV	Ultraviolet
VB	Valence band
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction

Acknowledgments

My deep gratitude goes to Dr. Hagen Klauk who gave me the opportunity to perform my work in his research group. Thank you for the steady support and guidance I received and at the same time for giving me the freedom to realize my ideas. I appreciate all the things I have learned on a scientific and also personal level.
I am also very thankful to Prof. Thomas Weitz for taking the responsibility for being my main examiner, for the continuous support, the scientific discussions we had and the warm welcomes in München and Göttingen. I especially thank Dr. Ute Zschieschang for teaching me everything I know in the lab and showing all the big and small tricks to fabricate transistors and for creating such a familiar atmosphere in the group.
I am very thankful to my colleagues Dr. James Borchert, Dr. Rachana Acharya, Vera Bader, Dr. Mélanie Brouillard, Tobias Wollandt and Sabrina Steffens for the shared time we have spent with many scientific projects and discussions and for several leisure time activities.
Further I would like to thank:
Prof. Jürgen Weis for being my external adviser at the MPI. I acknowledge the help of him and Marion Hagel and Thomas Reindl in the Nanostructuring lab and the support I received, especially with the RIE system.
Prof. Dirk Manske and Lukas Schwarz for helping me with their expertise in solving equations numerically.
Prof. Jens Pflaum and Thomas Ferschke for performing the XRD measurements and all helpful discussions.
Prof. Guido Schmitz and Helena Solodenko for performing the TEM characterization of the aluminum oxide films.
Prof. Peter van Aken, Dr. Julia Deuschle and Robin Lingstädt for characterizing the titanium oxide films by means of TEM and EELS measurements.
Dr. Axel Fischer for his support with his measurement software SweepMe!.
Prof. Louis Giraudet for the nice stay in Reims and teaching me a lot about capacitance measurements.
I also thank Nicolas Zuber, Robin Lingstädt, Jonathan Bauch, Robert Sittig, Patrick Kreissl and Sebastian Weber who have accompanied me through my studies.
I am deeply thankful to Patricia for reading my whole thesis and for scientific discussions at home.
Finally, my special thanks goes to my sister Lena and my parents Sabine and Wolfgang for their support and sympathy at all times and in all respects.