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# Charge Transport in Organic Semiconductors at the Nanoscale

Jakob Lenz

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# Zusammenfassung

Die Verwendung organischer Materialien in elektronischen Bauteilen bietet enormes Potential in Bezug auf Kostenreduzierung, einem geringeren technologischen Aufwand bei der Herstellung sowie bei der Verwendung flexibler Substrate. Dabei werden nicht nur fortlaufend neue Anwendungsfelder erschlossen, sondern mehr und mehr auch anorganische Halbleiter in bestehenden Technologien ersetzt. Jedoch ist der Ladungstransport in organischen Halbleitern durch eine vergleichsweise kompliziertere Morphologie, verschiedenen Fallenzuständen, Korngrenzen sowie ein höheres Maß an Unordnung verglichen mit anorganischen Halbleitern bis heute nicht vollständig verstanden.

Diese kumulativ verfasste Arbeit befasst sich mit der Untersuchung des Ladungstransportes verschiedener organischer Halbleiter als auch einzelner Kohlenstoffnanoröhren auf nanoskopischen Größenskalen unter Zuhilfenahme verschiedener Feldeffekttransistor-Geometrien und Gate-Konfigurationen.

Zunächst wurden verschiedene Polymerhalbleiter in einer vertikal angeordneten Kontaktgeometrie elektrisch charakterisiert, wobei sich zwischen den übereinanderliegenden Elektroden ein Isolator befindet. Dabei kann die Kanallänge durch die Dicke des Isolators zwischen den Elektroden mit Nanometer-Präzision kontrolliert werden. In dieser neu entwickelten Transistorstruktur wird die obere Elektrode abhängig vom Material des Isolators mittels Trocken- oder Nassätzen unterätzt. Die empfindlichen organischen Halbleiter werden im letzten Schritt aufgebracht. Dabei bleiben die intrinsischen Eigenschaften des organischen Halbleiters optimal erhalten und können durch nachfolgende Prozessschritte nicht verändert werden. Abhängig von der Wahl des Isolator-Materials können Kanallängen bis zu 2.4 Nanometer realisiert werden. Um trotz dieser kurzen Kanallängen eine ausreichende Kontrolle der Ladungsträgerkonzentration zu gewährleisten, wird als Gate der vertikalen organischen Transistoren eine ionische Flüssigkeit als Elektrolyt mit vergleichsweise hohen Kapazitäten verwendet. Vor dem Aufbringen der ionischen Flüssigkeit wird der organische Halbleiter mittels reaktiven Ionenätzen isotrop geätzt, wobei die obere Elektrode als Ätzmaske dient. Dadurch wird ein optimaler seitlicher Zugang der Ionen des flüssigen Elektrolyten zu dem ausschließlich zwischen den Elektroden vorhandenen organischen Halbleiter gewährleistet. Insgesamt werden drei verschiedene Polymerhalbleiter und drei verschiedene Isolator-Materialien untersucht. Bei der Verwendung von  $\text{SiO}_2$  als Isolator führt die Kombination von Kanallängen bis zu 40 Nanometer mit den hohen Kapazitäten des flüssigen Elektrolyten als Gate zu Rekordstromdichten von bis zu  $3 \text{ MA cm}^{-2}$ , Transkonduktanzen von bis zu  $5000 \text{ S m}^{-1}$  und on-off Verhältnissen von bis zu  $10^8$ . Bei hexagonalem Bornitrid als Isolator mit Kanallängen bis zu 2.4 Nanometer kann mit  $65 \text{ mV dec}^{-1}$  ein

Unterschwellanstieg nahe dem Raumtemperatur-Limit von  $60 \text{ mV dec}^{-1}$  realisiert werden. Zusätzlich können diese vertikalen organischen Transistoren bei sehr niedrigen Spannungen von bis zu  $10 \mu\text{V}$  betrieben werden.

Ein weiteres mögliches Anwendungsfeld ist die Verwendung als neuromorphes Bauteil in hardware-basierten künstlichen neuronalen Netzwerken. Bei der Verwendung flüssiger Elektrolyte als Gate können Transistoren als synaptischer Speicher fungieren, da die Ionen nach Anlegen einer Gate-Spannung dazu neigen, innerhalb des organischen Halbleiters zu verweilen. Bei aufeinanderfolgenden Gate-Pulsen hängt die Leitfähigkeit der Transistoren demnach vom vorherigen Zustand ab. Hier kann ein Schalten der Leitfähigkeit über fünf Größenordnungen demonstriert werden.

Im zweiten Teil der Arbeit werden einzelne Kohlenstoffnanoröhren mit Kanallängen von nur 10 Nanometern mittels ionischer Flüssigkeit als Gate elektrisch charakterisiert und die Ergebnisse mit einem auf dem Landauer-Büttiker Formalismus basierten Modell verglichen. Die hohen Kapazitäten des flüssigen Elektrolyten ermöglichen auf den Durchmesser normierte Stromdichten von bis zu  $2.57 \text{ mA } \mu\text{m}^{-1}$ , on-off Verhältnisse von bis zu  $10^4$  und einen Unterschwellanstieg von bis zu  $100 \text{ mV dec}^{-1}$ . Vergleicht man Messungen zu Beginn mit denen nach längerer Lagerung in Vakuum wird deutlich, dass das Einfangen von Elektronen die gleiche Art Hysterese verursacht wie die für ionische Flüssigkeiten charakteristische limitierte Diffusionsgeschwindigkeit der Ionen innerhalb des Elektrolyten.

Der letzte Teil der Arbeit befasst sich mit der Untersuchung des Ladungstransports in einzelnen Polymerfasern im Bereich unter 50 Nanometern unter Zuhilfenahme zweier verschiedener Gate-Konfigurationen, einem Oxid mit einer Phosphonsäure basierten selbst organisierten Monolage sowie hexagonales Bornitrid auf Graphit. Temperaturabhängige Messungen geben erste Hinweise auf einen band-artigen Ladungstransport. Die auftretenden Coulomb Oszillationen mit deutlich erkennbaren Coulomb Diamanten sind ein Beweis für die Bildung einer Reihe von Quantenpunkten bei cryogenen Temperaturen, wobei Ladungsträger nur über diskrete Energieniveaus fließen können. Im differentiellen Stabilitätsdiagramm sind zusätzlich angeregte Zustände in der Form von parallel zum Rand der Coulomb Diamanten verlaufenden Linien zu erkennen. Die Energieskala der gemessenen angeregten Zustände stimmt dabei gut mit Raman Messungen vergleichbarer Moleküle überein.

Die hier erzielten Ergebnisse sollen zum Verständnis des Ladungstransports organischer Halbleiter auf der Nanoskala beitragen.

# Abstract

The application of organic materials in electronic devices offers huge potential in terms of cost reduction, ease of processability as well as the usage of flexible substrates. Indeed nowadays organic semiconductors (OSCs) not only open new fields of application, but also replace more and more their inorganic counterparts in existing technologies. However due to a substantial amount of conformational freedom resulting in complex morphologies, the presence of traps, grain boundaries and a larger degree of disorder compared to inorganic semiconductors, charge transport processes of organic semiconductors are still not fully understood.

In this cumulative thesis, charge transport properties of different organic semiconductors as well as single walled carbon nanotubes (SWCNTs) are investigated at nanoscopic dimensions. For this purpose, different types of field-effect transistor (FET) geometries as well as gate configurations have been utilized.

First, several polymeric semiconductors were electrically characterized in a vertical contact geometry. Here, the staggered electrodes are separated by an insulating spacer. One advantage of this configuration is that the channel length, given by the spacer thickness, can be controlled with sub-nanometer precision. The main idea of this new developed vertical transistor structure lies in an underetched top contact, where both wet and dry etching can be applied depending on the spacer material. The deposition of the fragile organic semiconductor is the last manufacturing step. In this way the intrinsic OSC properties can be optimally maintained and remain uninfluenced by the successive process steps. Depending on the spacer material, channel lengths down to 2.4 nanometers can be realized. To guarantee a sufficient charge carrier density control via the gate electrode despite such short channel lengths, the vertical organic transistors (VOT) are gated via ionic liquids (IL) as electrolytes which exhibit very high capacitances. To enable an optimal lateral access of ions within the IL to the active channel, the organic semiconductor is isotropically etched via reactive ion etching prior to the IL gate deposition with the top electrode serving as an etching mask. This results in a well-defined OSC channel between the two electrodes. In total three different polymers as well as three different spacer materials are investigated. The combination of channel lengths in the nanometer region together with the high capacitances of electrolyte gates enable record on-current densities of up to  $3 \text{ MA cm}^{-2}$ , transconductances of up to  $5000 \text{ S m}^{-1}$  and on-off ratios of up to  $10^8$  with  $\text{SiO}_2$  as insulating spacer. When using hexagonal boron nitride (hBN) as spacer material, a steep subthreshold swing of  $65 \text{ mV dec}^{-1}$  could be realized, which approaches the room temperature limit of  $60 \text{ mV dec}^{-1}$ . Furthermore these devices can be operated at ultra-low bias voltages down to  $10 \text{ } \mu\text{V}$ .

Another potential field of application of electrolyte-gated VOTs is the usage as neuromorphic devices in hardware-based artificial neural networks. When gating with electrolytes, transistors can be used as a synaptic memory, as ions tend to remain in the semiconducting bulk after gate bias application. Hence when applying consecutive gate pulses, the device conductivity depends on its previous state. Here a record conductivity switching for neuromorphic systems over five orders of magnitude can be realized.

In the second part of this thesis, single walled carbon nanotubes with channel lengths down to 10 nanometers are electrically characterized using ILs as a gate and compared to a developed model based on the Landauer–Büttiker formalism. The high capacitances of ILs enables diameter-normalized current densities of up to  $2.57 \text{ mA } \mu\text{m}^{-1}$ , on-off ratios of up to  $10^4$  and a subthreshold swing of up to  $100 \text{ mV dec}^{-1}$ . By comparing initial measurements and measurements after long vacuum storage, additionally to the well-established polarization effects with limited ion diffusion velocity being responsible for hysteretic behavior in the electrolyte gated devices, electron trapping is identified to cause the same type of hysteresis.

In the last part, charge transport mechanisms of single polymer fiber transistors with channel lengths in the sub 50 nanometers regime are investigated. In this study, two different solid dielectric gate configurations, a hybrid oxide/phosphonic acid self-assembled monolayer (SAM) and a graphite/hBN gate has been used. Temperature dependent measurements indicate a regime of band-like transport. The occurring Coulomb oscillations with clearly observable Coulomb diamonds proves the formation of a series of quantum dots within a single polymer fiber at cryogenic temperatures. Here, charges can only be transported over discrete energy levels. In the differential stability diagram, also excited states in the form of lines running parallel to the Coulomb diamond edge are verified. The energy scale of the measured excited states compares well to Raman measurements of comparable molecules.

The results achieved within this thesis should contribute to the understanding of charge transport mechanism of OSCs at the nanoscale.

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# 1 Introduction

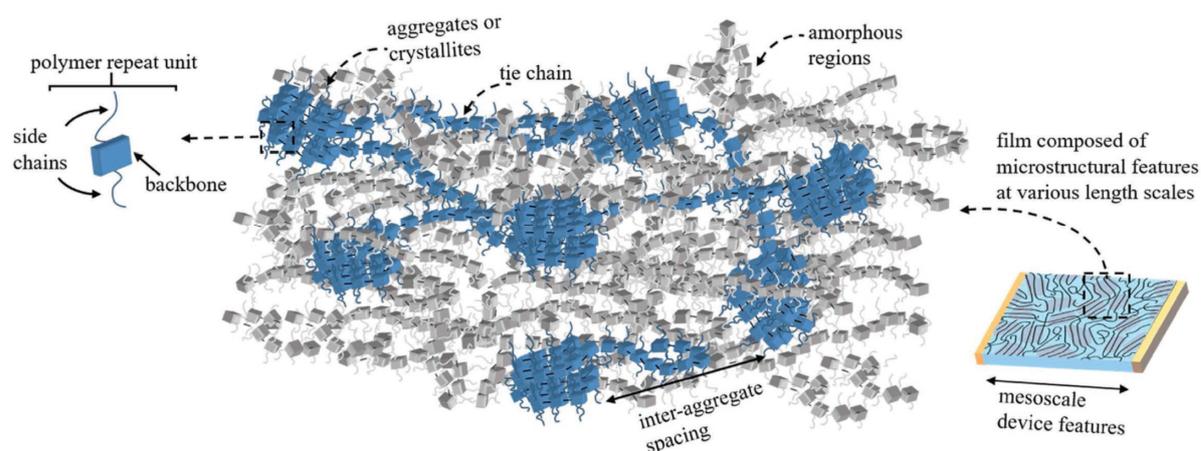
Since the discovery of electrically conducting polymers by Heeger, MacDiarmid and Shirakawa in 1977<sup>2</sup>, huge progress has been made both in the development of new organic semiconducting materials as well as OSC devices. Compared to inorganic semiconductors, their advantages of low-cost, large-scale and easy solution based processability already led to the commercialization of e.g. organic light emitting diodes (OLEDs) and organic solar cells. Furthermore big steps has been made for other future applications as e.g. sensors<sup>3,4</sup>, organic light emitting transistors (OLETs)<sup>5,6</sup>, organic laser diodes<sup>7,8</sup> and also artificial synapses<sup>9,10</sup> as a basis for hardware based artificial neural networks. One of the most versatile field, however, are organic field-effect transistors (OFETs), which could function as the fundamental building block of wearable electronics<sup>11</sup>, flexible and foldable displays<sup>12</sup> or integrated circuits<sup>13</sup>. Nowadays, due to the discovery of novel OSC materials as well as device optimization, OFETs exceed the device performance in terms of mobility compared to their inorganic counterpart as e.g. amorphous silicon<sup>14</sup>. However, to access the whole potential of organic materials and to further improve existing and future device concepts, a full understanding of individual charge transport processes is inevitable.

In the last couple of years it has become increasingly clear that there is no uniform model to describe, predict and compare the charge transport mechanism over the full range of OSCs. In fact, different theories have been successfully applied to different OSC systems according to morphology and microstructure

*The following part is adapted from the Manuscript in section 2.7.*

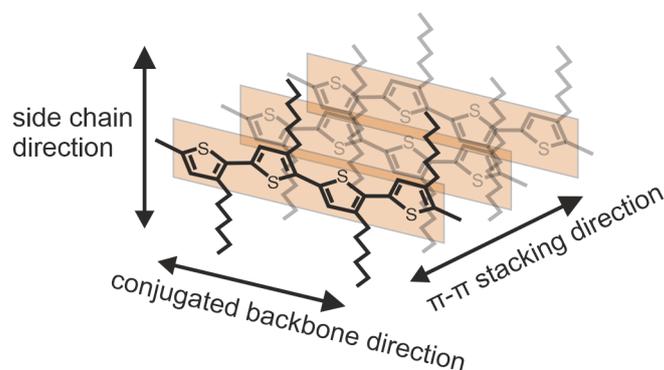
In general, the basis of charge transport in OSCs are delocalized electrons in the  $\pi$ -molecular orbital of linked carbon atoms, where a larger  $\pi$ -orbital overlap between individual molecules is favorable, since it improves charge delocalization. In molecular OSCs the well-defined crystalline morphology facilitates a theoretical understanding of charge transport mechanisms. In polymeric OSCs however the solid-state microstructure is determined by weak van-der-Waals forces between single polymer chains, which results in a large variety of intermolecular packing due to the conformational freedom of the polymer chains. In the schematic in Figure 1.1, two types of ordered phases exist, namely crystallites or aggregates. While aggregates reveal order solely in the  $\pi$ -stacking direction, crystallites display additional order in the alkyl-stacking direction<sup>15</sup> (see Figure 1.2). In these ordered regions the most efficient charge transport occurs at the shortest length scales (typically a few nanometers) within femto- to picoseconds<sup>1</sup> along the polymer backbone within single polymer chains (intrachain).

# 1 Introduction



**Figure 1.1 Schematic of the microstructure of conjugated polymers illustrating different length scales.** The mesoscale of a polymer film comprises ordered and amorphous regions. Ordered regions (blue), either consisting of crystallites (long-range order) or aggregates (short-range order), can be interconnected via tie chains. Adapted from ref<sup>1</sup>.

This ordered regions are very efficiently connected via intercrystalline chains, called tie chains. At longer length scales within ordered regions, charge transport is dominated by interchain hopping, which is two to three orders of magnitude slower compared to intrachain transport<sup>16</sup>. Charge transport via the typically non-conjugated side-chains is almost negligible<sup>17</sup> and they e.g. define the polymer's solubility as well as the relative stacking of chains. Finally, charge transport in the amorphous regions is very inefficient due to a lack of  $\pi$ -stacking order. All together the different length scales in the mesoscale of a polymer film lead to the presence of multiple charge transport processes. This implies that transport at the typical transistor channel lengths in the micrometer range needs to be regarded as a multiscale process and is usually limited by transport through amorphous regions. As a result, the theoretical and experimental characterization is very complex and optimization of the microstructures of polymer films is difficult. This becomes even clearer



**Figure 1.2 Schematic of possible charge transport exemplary shown for polythiophenes along the  $\pi$ - $\pi$  direction, the conjugated backbone and the isolating alkyl side chain direction.**

considering that contrary to the general expectation that a higher degree of crystallinity is accompanied by an improved charge transport, it has been shown that in specific cases less crystalline donor-acceptor (D-A) copolymers consisting of alternating electron-rich and electron-deficient units along the polymer backbone exhibit an improved charge transport behavior<sup>18-20</sup>. The high performance of these quasi-amorphous polymers is related to a minimized energetic disorder and a facilitated charge transport along the almost torsion-free, planar and rigid polymer backbone. From the above description it becomes clear that to obtain a more unified picture of charge transport in polymer thin films, it would be advantageous to be able to address the described individual charge transport processes occurring at each specific length scale separately. While several general works describing transport at ultrashort length scales in molecular break junctions<sup>21-23</sup> and macroscopic devices<sup>14,24</sup> are available, the focus of this work lies on the investigation of charge transport in the hard-to-probe scale of crystalline aggregates or few molecular chains. To this end, polymeric OSCs as well as SWCNTs are electrically characterized using various FET structures with nanoscopic device dimensions and different gate configurations. Specifically, the newly developed IL gated vertical OFET structure exhibit continuous on-state current densities of more than  $1 \text{ MA cm}^{-1}$ , which brings organic and inorganic semiconductors on the same level in this respect. Additionally the usage of these devices as artificial synapses is demonstrated. Neuromorphic devices are the building blocks for artificial neural networks, which can be used to emulate the learning process in human brains. Hence, they would allow to solve not completely deterministic problems via parallel instead of sequential processing (as in conventional computers). The origin of conductance memory behavior lies in the electrochemical doping of the OSC bulk, where ions remain in the channel after applying  $V_{GS}$  pulses. In the last part of the thesis, electrical transport in single polymer fibers is investigated. At cryogenic temperatures, Coulomb effects and size quantization is demonstrated in the form of Coulomb oscillations and Coulomb diamonds in the differential stability diagram. These findings provide novel insights of charge transport over discrete energy levels in nanoscopic organic systems.

This cumulative thesis is organized as follows. In chapter 2, the theoretical foundations in addition to the review manuscript M1 are briefly introduced. After a short general discussion of OSCs, the electrical characteristics of OFETs context of metal-oxide-semiconductor field-effect transistors (MOSFETs) are derived. Thereafter, different effects that might lead to deviations for short channel length devices are introduced. In the next part, the mechanism of using electrolytes as a gate is presented. In the last two sections, first different concepts of vertical organic transistors are introduced, and second the underlying theory of Coulomb blockade to describe the results of single polymer fiber transistors at cryogenic temperature is described. The third chapter comprises all device fabrication and characterization steps that are not covered by the attached publications. In chapter 4 results of electrolyte-gated VOFETs beyond the associated publications are shown. Chapter 5 is dedicated to the results and discussion of single polymer fiber transistors using two different gate

## 1 Introduction

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configurations. While in the first part, electrical measurements at room temperature are shown, the second part discusses temperature dependent measurements. In the last part, Coulomb blockade oscillation with the formation of well-defined Coulomb diamonds at cryogenic temperatures are presented. The thesis concludes with a summary of the work and outlook in chapter 6.

# 2 Theoretical Foundations

*In this chapter the fundamental principles and theories that are not covered by the manuscript M1 are presented. The article is attached as full text in section 2.7. First, the fundamentals of organic semiconductors are briefly presented. Since charge transport is solely investigated with the aid of different field-effect transistor structures, the theoretical derivation is given in the second section, followed by a detailed discussion of vertical organic transistors. In the next section, IL gating as an alternative to solid dielectrics, is discussed. Finally charge transport dominated by Coulomb effects and size quantization occurring for nanostructures at low temperatures is presented.*

## 2.1 Fundamentals of organic semiconductors

Here, in addition to the manuscript M1 in section 2.7, the basic concepts of organic semiconductors are discussed, following the references<sup>25,26</sup>. The term “organic” implies that the basis of these materials is built by carbon and hydrogen atoms. In general, organic semiconductors can be classified in two groups, small molecules and polymers. The fact that organic materials are able to transport charge carriers stems from the ability of carbon to form hybridized states, i.e. a mixed state of different orbitals. The most favorable  $sp^2$  hybridization results in three in plane  $\sigma$ -bonds and one out of plane  $\pi$ -bond. The electrons in  $\sigma$ -bonds are localized and cannot contribute to charge transport. The delocalized electrons in the  $\pi$ -molecular orbital of linked carbon atoms with alternating single and double bonds in conjugated chains or aromatic rings build the basis of charge transport in organic materials. In inorganic semiconductors, the band structure is characterized by the formation of a periodic lattice potential due to the crystal nature of covalently bonded atoms, resulting in valence and conduction bands. In organic semiconductors, the molecular orbitals are filled up with electrons up to the highest binding  $\pi$ -state, referred to as highest occupied molecular orbital (HOMO), which compares to the conduction band. The next empty molecular orbital, the lowest antibinding  $\pi^*$ -state, referred to as the lowest unoccupied molecular orbital (LUMO), can be considered as the conduction band and is separated from the HOMO by an energy gap, i.e. the band gap. Depending on the relative values of the HOMO and LUMO levels in respect to the work function of the source and drain material, OSCs can transport holes (p-type) and electrons (n-type).

Due to complex morphologies, large conformational freedom, different trap states (e.g. grain boundaries or impurities) and a larger degree of disorder compared to inorganic semiconductors, there is no uniform model to describe the charge transport mechanism over the full range of organic

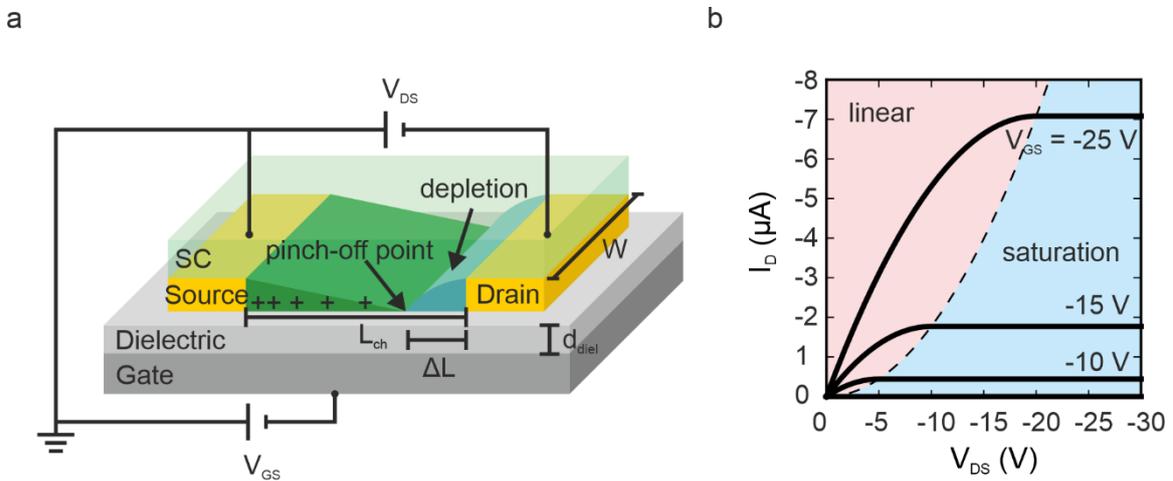
## 2 Theoretical Foundations

semiconductors. An overview of the most prominent models is given in the manuscript M1.

### 2.2 Electrical characteristics of field-effect transistors

Throughout this thesis charge transport properties of organic semiconductors at the nanoscale were investigated using different FET geometries. In general, FETs are three-terminal devices with a gate electrode separated from the semiconductor (SC) by a dielectric and the source and drain electrode in direct contact with the SC (see Figure 2.1 a)). The theoretical description in addition to the FET section in the manuscript M1 is following the textbook of S. M. Sze<sup>27</sup> for MOSFETs assuming the following conditions:

- No interface traps or mobile charges in the dielectric
- Charge transport is caused by drift current
- Gradual channel approximation: the transversal electric field (controlled by the gate source voltage  $V_{GS}$ ) is much larger than the longitudinal electric field between the source and drain electrode (controlled by the drain source voltage  $V_{DS}$ )
- A uniform doping throughout the SC channel



**Figure 2.1 p-type FET.** a) Schematic illustration with bottom-gate bottom contact architecture in saturation mode. The characteristic length scales channel length  $L_{ch}$ , channel width  $W$  and insulator thickness  $d_{diel}$  are indicated. b) Idealized output characteristics with the linear regime marked in red and the saturation regime in blue.

## 2.2 Electrical characteristics of field-effect transistors

Applying a bias  $V_{GS}$  between gate and source electrode accumulates charges at the semiconductor dielectric interface, also referred to as conducting channel, according to a capacitor model with capacitance  $\hat{C}$ , the vacuum permittivity  $\epsilon_0$  and the dielectric constant  $\epsilon_r$  and thickness  $d_{diel}$  of the dielectric layer:

$$\hat{C} = \epsilon_0 \epsilon_r / d_{diel}. \quad (2.1)$$

The current flow of these accumulated charges can be controlled by applying a voltage between the drain and the source electrode  $V_{DS}$ . Based on the number of induced charge carriers  $Q(x)$  at a point  $x$  in the conductive channel with

$$Q(x) = \hat{C}(V_{GS} - V_{th} - V(x)) \quad (2.2)$$

and the threshold voltage  $V_{th}$  (see manuscript M1), a general expression for the drain current  $I_D$  can be derived:

$$I_D = \frac{W}{L_{ch}} \mu \hat{C} \left[ (V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]. \quad (2.3)$$

with the channel width and length  $W$  and  $L_{ch}$  (see Figure 2.1 a)) and the charge-carrier mobility  $\mu$ . The operation of FETs can be differentiated in the subthreshold, linear and saturation regime. In the subthreshold regime with  $V_{GS} < V_{th}$ , where charge carriers begin to accumulate without a continuous conducting channel,  $I_D$  increases exponentially with  $V_{GS}$ . In this regime, charge transport is dominated by diffusion and the derivation of equation 2.2 is not valid. This region, quantified by the subthreshold swing  $SS$ , with

$$SS = \frac{\partial V_{GS}}{\partial \log(I_D)} = \frac{k_B T}{q} \ln(10) \left( 1 + \frac{q N_{it}}{\hat{C}} \right) \quad (2.4)$$

characterizes, how sharply a FET can be turned on by varying  $V_{GS}$ . With the Boltzmann constant  $k_B$  and the elementary charge  $q$ , the  $SS$  strongly depends on the deep interface trap density  $N_{if}$  at the semiconductor dielectric interface.

In the linear regime, where  $V_{GS} - V_{th} > V_{DS}$  with a uniform charge-carrier density across the conductive channel,  $I_D$  increases linearly with  $V_{DS}$  and equation 2.2 can be simplified to:

$$I_{D,lin} = \mu_{lin} \frac{W}{L} \hat{C} (V_{GS} - V_{th}) V_{DS}. \quad (2.5)$$

Once  $V_{DS} = V_{GS} - V_{th}$ , all charge carriers near the drain are collected by the drain electrode and the channel is disrupted (transition from the linear to the saturation regime). This so-called pinch-off point is moving from the drain to the source electrode with increasing  $V_{DS}$ , whereby also the depletion

## 2 Theoretical Foundations

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zone at the drain electrode increases (see Figure 2.1 a)). As the potential at the pinch-off point is constantly  $V_{GS} - V_{th}$ ,  $I_D$  becomes  $V_{DS}$  independent and saturates according to equation 2.2. to

$$I_{D,sat} = \mu_{sat} \frac{W\hat{C}}{2L} (V_{GS} - V_{th})^2. \quad (2.6)$$

Figure 2.1 b) shows the simulated drain current according to equations 2.5 and 2.6 with the transition between linear and saturation regime at  $V_{DS} = V_{GS} - V_{th}$  (dotted line).

The mobilities for the different regimes are given by

$$\mu_{lin} = \frac{L}{\hat{C}WV_{DS}} \frac{\partial I_{DS,lin}}{\partial V_{GS}} \quad (2.7)$$

and

$$\mu_{sat} = \frac{2L}{W\hat{C}} \left( \frac{\partial \sqrt{I_{D,sat}}}{\partial V_{GS}} \right)^2. \quad (2.8)$$

Although the operation mode of OFETs (accumulation) differs from that of standard MOSFETs (inversion), it is still valid in good approximation to describe the electrical characteristics by the derived formalism<sup>28</sup>. Here the following additional conditions have to be fulfilled:

- The conductive channel resistance must be substantially larger than the contact resistances at the source and drain electrodes
- The channel length  $L_{ch}$  has to be significantly smaller than the channel width  $W$
- The mobility  $\mu$  has to be charge-carrier density independent (i.e.  $V_{GS}$ -independent)

In general, the mobility is the figure of merit to classify and compare the device performance of OFETs<sup>29</sup>. However, it has been shown that a lot of groups presented overestimated mobility values in the past. The hurdles and criteria that have to be fulfilled for a valid mobility extraction can be found in ref.<sup>30</sup> and have also been addressed in an own section in the manuscript M1.

### 2.3 Deviations from ideal FETs

This thesis mainly focuses on organic transistors with channel lengths in the nanometer regime. Here, various so-called short-channel effects as well as an increasing influence of contact resistances have to be considered.

### 2.3.1 Contact resistance

In any type of electronic device used to investigate charge transport, special care has to be taken to distinguish material-specific properties from device-related effects. One of the most prominent influences arises from non-negligible contact resistances at the metal semiconductor interface, where charge carriers are in- and ejected. One assumption of the derivation in section 2.2 for OFETs is that the total resistance is dominated by the channel resistance with negligible contact resistances, i.e. the OSC is the limiting factor of charge flow. In contrast to the case of e.g. silicon transistors with highly doped regions as source and drain contacts and hence almost no contact resistances, the contacts in OFETs are realized by direct metal semiconductor interfaces. This interface is described by a Mott-Schottky model, where the barrier height is given by the difference between the OSC HOMO or LUMO level (for holes and electrons) and the work function of the metal electrode<sup>24</sup>. Ohmic-like behavior can be achieved by choosing metals with work functions close to the HOMO or LUMO level, in order to avoid high barriers which might lead to reduced overall currents and a superlinear current increase in the linear regime in the output characteristics. As the channel resistance scales with  $L_{ch}$ , contact resistances in short channel devices can reach the same magnitude as the channel resistance and the FET is operated in the contact-limited regime.

To assess the intrinsic properties of the OSC under investigation by FET measurements, the influence of contact resistances should, if possible, always be characterized by e.g. four-point probe measurements<sup>31</sup> or the transfer line method<sup>32</sup>.

### 2.3.2 Short-channel effects

Short-channel effects always arise when the dimensions of FETs are scaled down in a way that the gradual channel approximation is not valid, i.e. when the lateral drain source field is comparable to the vertical gate source field<sup>27</sup>. As a consequence, the potential distribution in the channel becomes two dimensional, which results in deviations from the ideal FET characteristics. An overview about the existing short-channel effects in OFETs can be found in ref.<sup>33</sup>. One effect that is frequently observed when reducing  $L_{ch}$  is an absence of saturation in the output characteristics above the pinch-off point. As explained above, increasing  $V_{DS}$  in the saturation regime shifts the pinch-off point from the drain to the source electrode. Hence,  $L_{ch}$  is reduced by the length of the depletion region  $\Delta L$  (see Figure 2.1 a)), resulting in an effective channel length  $L_{eff} = L_{ch} - \Delta L$ . This effect, which is called channel-length modulation, always occurs and can be neglected for long channel length devices where  $\Delta L \ll L_{ch}$ . However, when the size of the depletion region becomes comparable to the channel length, the effective channel length reduces with increasing  $V_{DS}$ , i.e. becomes  $V_{DS}$  dependent. According to equation 2.6, this results in increasing drain currents for increased  $V_{DS}$  in the saturation regime<sup>28</sup>. Another short-channel effect that has been observed in the course of this thesis is drain-induced barrier-lowering (DIBL), which is characterized by a reduction of  $V_{th}$  with increasing  $V_{DS}$ <sup>34,35</sup>. Speaking

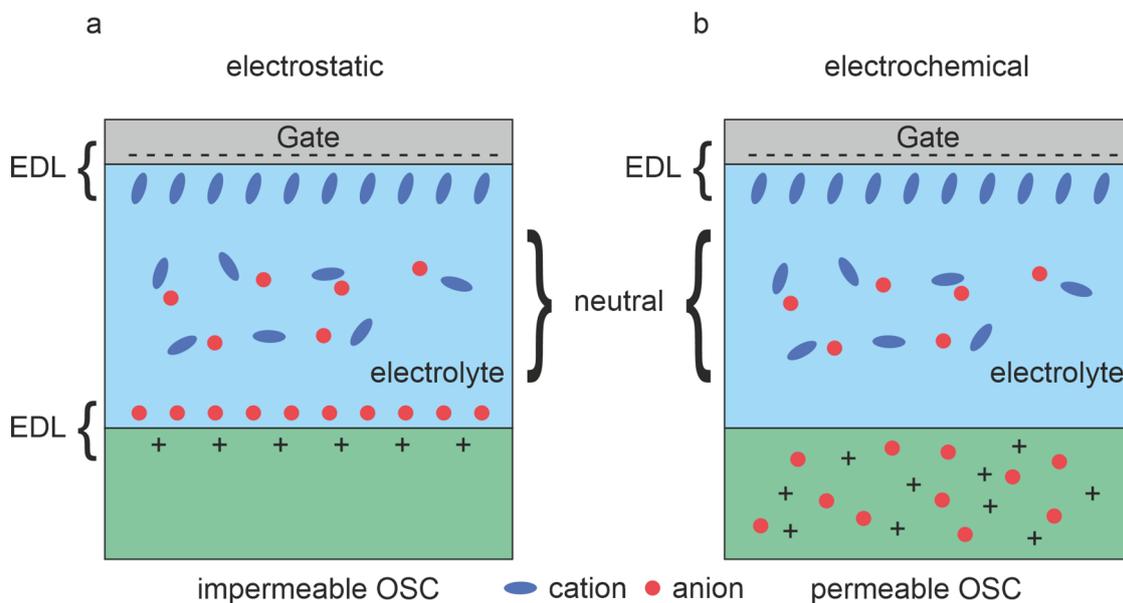
## 2 Theoretical Foundations

in the picture of MOSFETs, the drain bias can reduce the barrier at the source electrode when the depletion region of the drain reaches the source due to channel length modulation. As a consequence, for higher  $V_{DS}$  more charge carriers can be injected, the transistor is turned on prematurely and  $V_{th}$  reduces<sup>27</sup>.

Short-channel effects can be avoided to a certain extent by scaling down all device dimensions so that the gradual channel approximation still holds true. However, when decreasing e.g. the dielectric thickness, increasing leakage currents and tunneling have to be considered. Another possibility to realize sufficient gate coupling is the usage of ILs with very large capacitances, as will be explained in the next section.

### 2.4 Ionic liquid gating

In order to stay within the gradual channel approximation, when decreasing the channel length also the gate capacity has to increase. In recent years, the high capacity of  $1 - 10 \mu\text{F cm}^{-2}$ <sup>36</sup> of ILs, i. e. liquid salts, has been utilized to fabricate high-performance electrolyte-gated OFETs<sup>37-39</sup>, whereby the ion-conducting and electronically-insulating electrolyte works as a gate insulator. Here, either the IL itself, or a solid gel composed of an IL is embedded in a polymer matrix, can be used. The following derivation regards p-type OSCs and is schematically shown in Figure 2.2, whereby n-type OSCs can be treated analogously. Without an external potential, the ions within the IL are randomly distributed. By applying a negative voltage at the gate electrode, cations are attracted and form an electric double



**Figure 2.2 Schematic illustration of electrolyte gating for p-type OSCs.** a) Electrostatic gating with the formation of an EDL for impermeable OSCs and b) electrochemical doping for permeable OSCs. Note: The gate potential is applied to the reference grounded source electrode.

## 2.5 Vertical organic transistors

layer (EDL) at the electrolyte gate-electrode interface. OSCs can be either impermeable (Figure 2.2 a)) or permeable (Figure 2.2 b)) to ions of the IL<sup>40</sup>. If the OSC is ion impermeable, the applied gate voltage induces an accumulation of anions at the electrolyte-OSC interface, which in turn leads to an accumulation of holes in the OSC. The formed EDL can be seen as a capacitor with a thickness of only  $2\text{ nm}$ <sup>41,42</sup>. The resulting high capacitances according to equation 2.1 lead to very high carrier densities and hence to very high currents at low voltages (see equations 2.5 and 2.6). As almost the whole applied gate potential drops across the two EDLs in quasi-static operation, the electrolyte bulk is electrically neutral<sup>43</sup>. For ion-permeable OSCs, an applied gate voltage again results in the formation of an EDL at the electrolyte gate-electrode interface, whereas anions at the electrolyte OSC interface can penetrate and accumulate holes in the whole bulk of the OSC. This mechanism is also called electrochemical doping and mostly occurs for polymeric OSC systems<sup>44</sup>. As both ions, cations and anions, might diffuse into the OSC bulk upon changing the gate-bias potential, the OSC bulk can also be depleted and the whole process of electrochemical doping is reversible<sup>45,46</sup>. The theoretical description of this three dimensional capacity more sophisticated<sup>47,48</sup> and still an important area of research. Other advantages of electrolyte-gating aside from high capacitances are reduced contact resistances<sup>49</sup> and the possibility to print solid electrolytes<sup>39,43,50</sup>. However, due to the limited ion-diffusion velocity, the switching frequency of electrolyte-gated devices are currently limited to the kHz regime and will probably not exceed a few MHz<sup>51</sup>. To ensure a stable operation special care has to be taken to stay within the electrochemical window, i.e. the anodic and cathodic limits, which are defined as the difference between the reduction and oxidation potential of anions and cations. Exceeding this window results in irreversible reduction and oxidation of anions and cations, respectively.

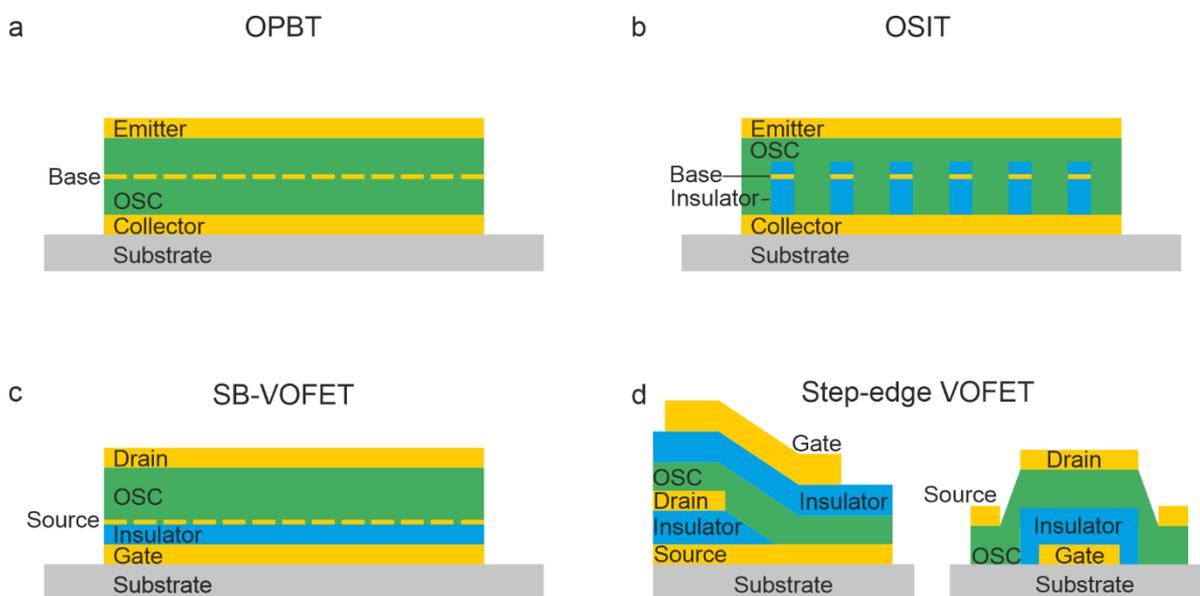
In the course of this thesis solely the IL 1-Ethyl-3-methylimidazolium-bis(trifluoromethylsulfonyl)imid [EMIM][TFSI], provided by BASF SE, was used. Depending on the water content, whereby a higher amount of water molecules within the hydrophilic ILs results in narrowing of the electrochemical window at both the anodic and cathodic limits, most likely caused by water electrolysis<sup>52</sup>, different anodic ( $1.7 - 2\text{ V}$ ) and cathodic ( $-2 - -2.4\text{ V}$ ) limits for [EMIM][TFSI] can be found in literature<sup>53,54</sup>.

## 2.5 Vertical organic transistors

Compared to conventional OFETs with a planar structure, the source and drain electrodes in VOTs are stacked vertically on top of one another. Since the first VOT presented by Yang and Heeger in 1994<sup>55</sup>, huge progress was made in improving the device performance. Nowadays VOTs exceeds the performance of lateral OFETs with current densities in the  $\text{MA cm}^{-2}$  regime<sup>56</sup> and a record transition frequency (the highest frequency where the transistor is still able to amplify electrical signals) of  $40\text{ MHz}$ <sup>57</sup>. With limited mobilities as a material specific parameter of the currently available materials, a promising way to improve the device performance is to shorten the channel length  $L_{ch}$ , as the

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transition frequency scales with  $\approx \mu L_{ch}^{-2}$ <sup>58</sup> and the saturation current with  $\mu L_{ch}^{-1}$  (see equation 2.6). Downscaling of the channel length in lateral devices is very challenging and demands high-resolution structuring techniques which would contradict the entitlement of low-cost, large-area and easy to fabricate organic electronic devices. In contrast, by a vertical alignment of the source and drain electrodes with a channel length determined solely by the sandwiched organic semiconductor layer respectively a thin isolating spacer, short-channel devices in the sub 100 nanometer regime can be easily realized. The arising obstacle of preventing the source and drain electrode from screening the gate field resulted in a huge variety of VOT device concepts, which can be roughly categorized into organic permeable base transistors (OPBTs), organic static induction transistors (OSITs), Schottky barrier vertical organic field-effect transistors (SB-VOFETs) and vertical organic field-effect transistors (VOFETs) (see Figure 2.3). The following overview is guided by refs.<sup>59–61</sup>. The operation principle and device architecture of OPBTs and OSITs with a nearly pure vertical and negligible lateral charge transport can be compared to the concept of a vacuum triode. Nowadays OPBTs are one of the most promising types of vertical organic transistors due to large current densities, reasonable on-off ratios and record switching behavior<sup>62–64</sup>. OPBTs comprise of a staggered charge-carrier injecting (emitter) and extraction (collector) electrode with the OSC layer in between, whereby the carrier-injection is controlled by applying an emitter-collector bias  $V_{CE}$ . The thin metal electrode (base) embedded in the OSC, is used to control the current flow from the emitter to the collector by a potential difference  $V_{BE}$  between the emitter and the base. Hence, the base electrode in OPBTs has to be highly transparent (permeable) for charge carriers to let them pass, and also sufficiently insulating, in order to keep



**Figure 2.3 Schematic illustration of different vertical organic transistor concepts.** a) Organic permeable base transistor, b) organic static induction transistor, c) Schottky barrier VOFETs and d) two exemplary types of step-edge VOFETs.

## 2.5 Vertical organic transistors

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leakage currents into the base as small as possible, which can e.g. be realized by thin native oxide layers,. Typical base electrodes are very thin metal films with nanometer sized pinholes<sup>65</sup> or porous metal films<sup>66</sup>.

OSITs are a special version of OPBTs, where in contrast to the rather self-assembled base electrode of OPBTs, the base electrode of OSITs is fabricated prior to OSC deposition by conventional structuring techniques<sup>67,68</sup>. This additional degree of freedom enables a more flexible device control of the most delicate part of these types of transistors. Moreover, insulating layers might be applied to reduce the off-current.

In SB-VOFETs, which can be regarded as organic Schottky diodes with an additional gate electrode, the OSC is sandwiched between vertically aligned source and drain electrodes. The gate electrode, separated by an insulator, lies below the source electrode. An effective charges-transport control can only be guaranteed if the gate electric field is not fully screened by the source electrode. This can be realized e.g. by perforated source electrodes<sup>69,70</sup> or porous networks of nanowires<sup>71</sup> or carbon nanotubes<sup>72</sup>. In the off state, charge-carrier injection is limited by the Schottky barrier at the source-semiconductor interface. The height of the Schottky barrier can be modulated by the applied gate potential. Hence, instead of tuning the charge-carrier density in the OSC, the working principle is related to a change of the contact resistance at the source electrode.

Aside from the above presented vertical organic transistor concepts and the electrolyte-gated VOFETs in publication A1 and A3, both attached as full text in the appendix, all of them exhibiting truly vertical channels, there are a lot of proposals covering both lateral and vertical transport<sup>73-76</sup>. These so called step-edge VOFETs with vertically displaced source and drain electrodes and a gate-bias modulated charge-carrier density are the most similar representatives of VOTs compared to conventional OFETs in terms of structure and operation. The main difference is that charge transport is not limited anymore to the small accumulation layer at the semiconductor insulator interface.

Although the best vertical organic transistors already outperform the best lateral transistors, direct comparison between lateral and vertical devices is very delicate and well described in ref.<sup>59</sup>. Especially the charge-carrier mobility  $\mu$  as the figure of merit in planar devices is much more challenging to calculate. Due to different working principles of the presented vertical device concepts as well as a potential superposition of lateral and vertical charge transport, the derivation in section 2.2 not necessarily holds true. Furthermore, in vertical transistors charge transport is not limited to a nanometer-thick accumulation layer at the dielectric semiconductor interface, as has been widely demonstrated for planar OFETs<sup>77-79</sup>. In fact the whole OSC bulk is contributing to charge transport. In summary, the detailed operation mechanism of vertical organic transistors is still poorly understood and different device concepts have to be treated individually. Instead of the mobility, different parameters such as current density, on-off ratio, *SS* value or transition frequency can be used to evaluate the device performance.

The intention of all types of vertical organic transistors is to find an easy way to fabricate short-

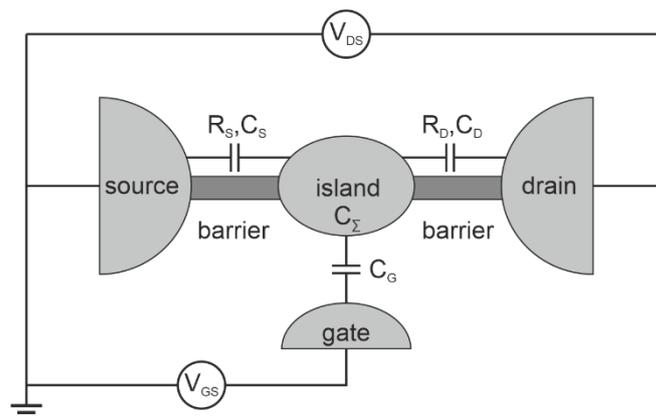
## 2 Theoretical Foundations

channel devices with improved performances. Here, the inherently accompanied increasing influence of short-channel effects and contact resistances has to be considered.

### 2.6 Coulomb blockade

In order to address charge transport in highly ordered regions of polymeric semiconductors, single polymer fibers with nanoscopic dimensions has been fabricated. Here, especially at low temperatures, one has to consider size quantization as well as Coulomb interactions. These effects occur in nanostructures with sizes in the range of the Fermi wavelength (i.e. the de Broglie-wavelength of electrons at the Fermi level). From the first evidence in 1968<sup>80</sup> Coulomb effects have been demonstrated for a variety of systems such as e.g. single walled carbon nanotubes<sup>81,82</sup>, metals<sup>83</sup>, and semiconducting nanowires<sup>84,85</sup>, 2D materials as graphene<sup>86</sup> or MoS2<sup>87</sup>, single molecules<sup>88,89</sup> and even single atoms<sup>90</sup>. In the field of OSCs, Coulomb interaction was shown for polymer fibers in two-terminal devices<sup>91,92</sup>, for molecular OFETS<sup>93,94</sup> and for single molecule transistors<sup>95,96</sup>. The following derivation is guided by refs.<sup>97-100</sup>. Whenever decreasing the extension of a structure, simplified from here as island, in at least one dimension, the number of charges on this island is quantized ( $Q = ne$ ,  $n \in \mathbb{N}$ ). If this nanostructure comprises the channel of a FET, the charging behavior of such systems can be treated with the picture of a single electron transistor, depicted in Figure 2.4. The island with a total capacitance of  $C_{\Sigma}$  is coupled via tunnel barriers to electron reservoirs, which can be referred to as source (drain) with resistance  $R_S$  and capacitance  $C_S$  ( $R_D$ ,  $C_D$ ). Additionally, the island is coupled to a gate with capacitance  $C_G$ .

In contrast to metallic islands with a comparably large electron density, in semiconducting islands aside from charge-quantization effects also quantum-confinement effects have to be considered. In such systems the transport can be described with the constant interaction model<sup>101</sup>. As the islands



**Figure 2.4** Schematic illustration of a single-electron transistor. The island is coupled via tunnel barriers to the source and drain electrode.

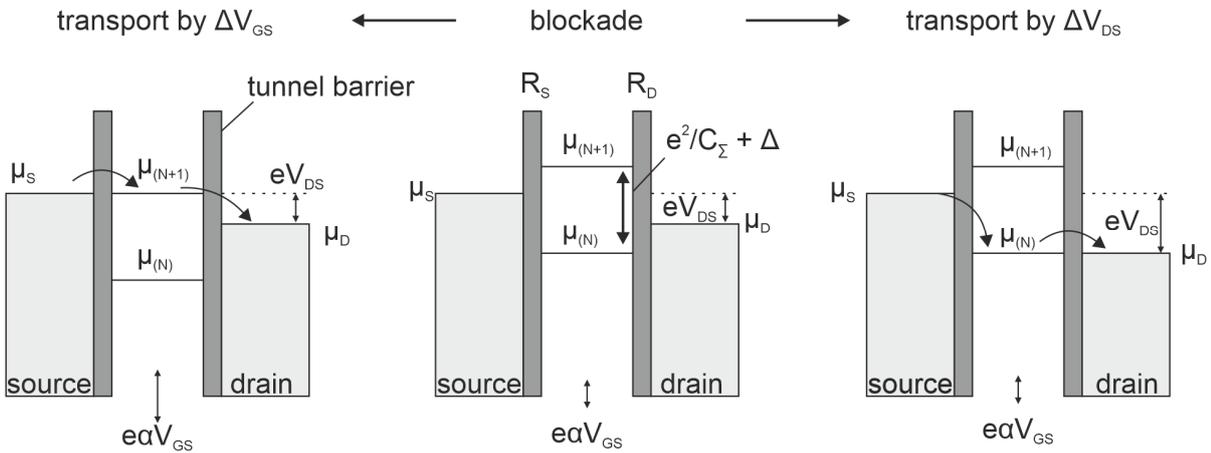
## 2.6 Coulomb blockade

usually comprises of quantum dots, from here these terms are used analogously. The energy needed to add an electron to the island  $E_{add}$  can be derived from the difference between two neighboring energy levels, represented by the chemical potentials:

$$E_{add} = \mu_{(N+1)} - \mu_{(N)} = \frac{e^2}{C_\Sigma} + E_{(N+1)} - E_{(N)} \quad (2.9)$$

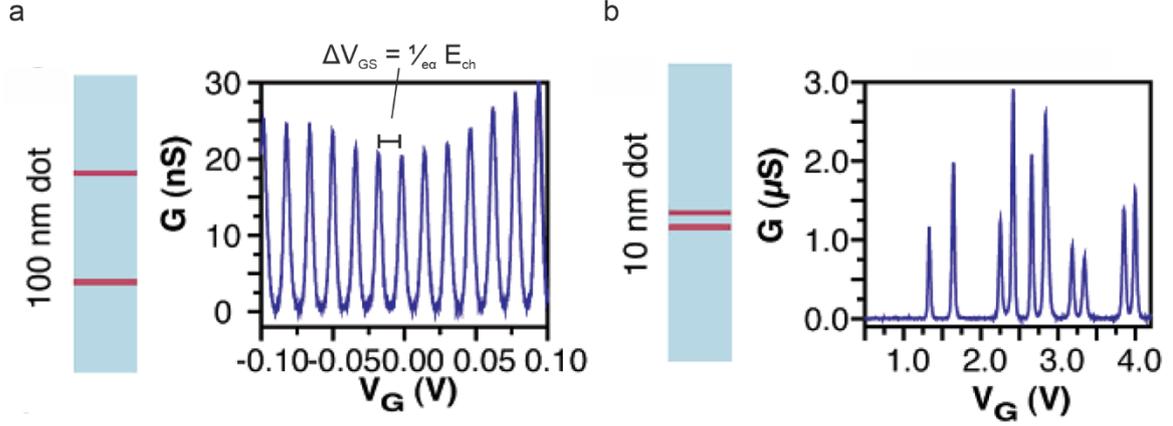
with  $E_{ch} = e^2/C_\Sigma$  being the charging energy of the island and  $\Delta = E_{(N+1)} - E_{(N)}$  the single-particle energy-splitting due to quantum confinement. For metallic or large semiconductor quantum dots the splitting energy is negligible.

At small  $V_{DS}$  and sufficiently small temperatures, the energy needed to add an extra electron to the island can be larger than the thermal energy ( $k_B T \ll e^2/C_\Sigma + \Delta$ ). The current through the island can be illustrated by the energy diagrams of a double tunnel barrier configuration, depicted in Figure 2.5. In the case, where the number of charges on the island  $N$  is fixed, the potentials of the source and drain electrode, represented by  $\mu_S$  and  $\mu_D$ , lie in between two energy levels  $\mu_{(N)}$  and  $\mu_{(N+1)}$  of the island (middle of Figure 2.5). This regime, where no charges can flow through the island, is called Coulomb blockade. By tuning  $V_{GS}$ , the ladder of the chemical potential  $\mu_i$  inside the island can be shifted in a way, that e.g.  $\mu_{(N+1)}$  aligns with  $\mu_S$ . An additional electron can now tunnel through the barrier  $R_S$ . The gate coupling factor  $\alpha = C_G / C_\Sigma$  denotes the relationship between the intrinsic energy scale of the island and the distance of two experimentally observed consecutive conductance peaks by tuning  $V_{GS}$ . If also  $\mu_S \geq \mu_D$ , the number of charges on the island fluctuates between  $N$  and  $N+1$  and current can flow from source to drain, which is experimentally addressable as a peak in conductance (left of



**Figure 2.5 Energy diagram for a quantum-dot transistor.** Two tunnel barriers connect the source and drain electrode to the quantum dot. Middle: The transport is blocked with a fixed number of  $N$  electrons on the quantum dot, if the source and drain chemical potentials are in between two states of the quantum dot  $\mu_{(N)}$  and  $\mu_{(N+1)}$ . Left: An additional electron ( $N+1$ ) can tunnel through the barriers  $R_S$  or  $R_D$  by shifting the ladder of the chemical potential via  $V_{GS}$ , which results in a conductance peak. Right: Transport through the quantum dot by changing  $V_{DS}$ .

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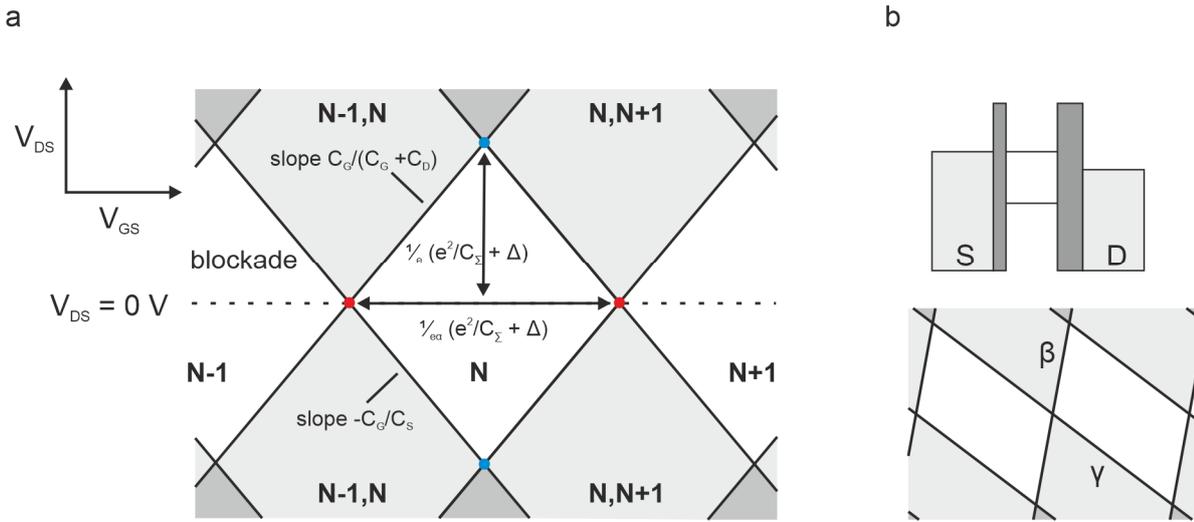


**Figure 2.6 Coulomb peaks for different quantum dot sizes.** a) Periodic oscillations for a dot size of 100 nm. b) Irregularly spaced oscillations for a dot size of 10 nm, where the single particle spacing  $\Delta$  due to quantum confinement is non-negligible. Adapted from ref.<sup>70</sup>.

Figure 2.5). By continuously varying  $V_{GS}$ , the conductance peaks occur every time when the number of charges on the island is not fixed and current can flow from source to drain. The resulting Coulomb blockade oscillations are illustrated in Figure 2.6 with two scenarios for different quantum dot sizes. For comparably large sizes, the splitting energy  $\Delta$  is negligible and the conductance peaks exhibit regular spacing. When decreasing the size of the quantum dot in Figure 2.6 b),  $\Delta$  exceeds the charging energy  $E_{ch}$ , which results in irregularly spaced oscillations. The same argumentation holds true when tuning the height of  $\mu_D$  respective  $\mu_S$  by applying a source drain bias  $V_{DS}$  (right of Figure 2.5). In the  $(V_{GS}, V_{DS})$ -conductance map, each of the resonances at specific  $V_{GS}$  and  $V_{DS}$  values causes two straight lines that separates regions where current is blocked and allowed (see Figure 2.7). The white diamond shaped areas mark the blockade regime and are referred to as Coulomb blockade diamonds with a fixed number of electrons. Note that for the sake of simplicity the Coulomb diamond plots are drawn for large quantum dots with negligible  $\Delta$ . Considering  $\Delta$  for small sized dots would lead to different sized Coulomb diamonds. In the light grey regions, the number of electrons can fluctuate by 2, i.e. two electrons can tunnel simultaneously through the barriers and the island. In the dark grey regions, more than two electrons can tunnel through the dot. At  $V_{DS} = 0$  V, the chemical potentials of  $\mu_{(N)}$  and  $\mu_{(N+1)}$  align at the crossing points, marked by red circles in Figure 2.7 a). The spacing  $\Delta V_{GS}$  between these two points is according to equation 2.9:

$$\Delta V_{GS} = \frac{1}{e \alpha} \left( \frac{e^2}{C_{\Sigma}} + \Delta \right). \quad (2.10)$$

Here, the gate coupling factor  $\alpha = C_G / C_{\Sigma}$  denotes the relationship between the intrinsic energy scale of the island and the distance of two consecutive conductance peaks. The upper vertex of the diamond, which is given by the crossing point where  $\mu_S = \mu_{(N)}$  and  $\mu_D = \mu_{(N-1)}$  (vice versa for the lower

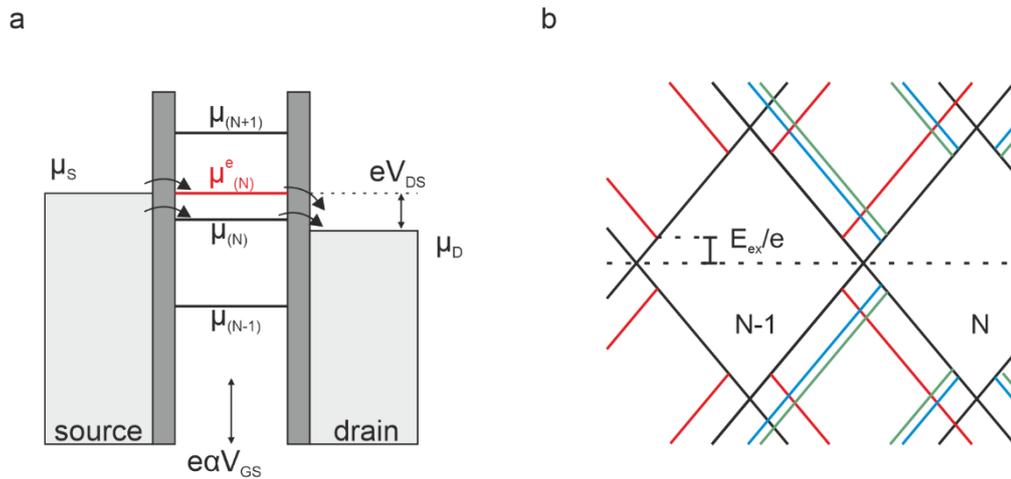


**Figure 2.7 Sketch of Coulomb blockade diamonds (stability diagram) with negligible  $\Delta$ .** a) Current as a function of  $V_{GS}$  and  $V_{DS}$  with symmetric coupling of source and drain to the island. The current is blocked in white diamond shaped areas with a constant number of electrons (e.g.  $N-1$ ,  $N$ ,  $N+1$ ). In the light grey regions, 2 electrons and in the dark grey region more than 2 electrons can tunnel through the dot b) Asymmetric coupling with a larger tunnel barrier at the drain contact results in sheared diamond with different slopes  $\beta$  and  $\gamma$ .

vertex), marked by blue circles in Figure 2.7 a), is defined by  $\Delta V_{DS} = 1/e (e^2/C_S + \Delta)$ . Hence,  $\alpha$  can be directly extracted by comparing the upper or lower vertex of the diamond with  $\Delta V_{GS}$ . The slopes of the two lines of the diamond,  $\beta = C_G/(C_G + C_D)$  and  $\gamma = -C_G/C_S$ , represent the coupling of the source and drain electrode to the island. Another possibility to extract  $\alpha$  stems from the relation  $1/\alpha = 1/\beta + 1/\gamma$ . In Figure 2.7 a) similar tunnel barriers and hence symmetric coupling is assumed, which results in symmetric and straight Coulomb diamonds with similar slopes ( $1/\beta = 1/\gamma = 1/2\alpha$ ). Asymmetric coupling, frequently observed in literature<sup>102–104</sup> and illustrated in Figure 2.7 b), leads to sheared Coulomb diamonds. To facilitate data analysis, usually the differential conductance  $\partial I_D/\partial V_{GS}$  is used. Here, every conductance change is illustrated as a peak in the  $(V_{GS}, V_{DS})$ -map.

Up to now, only the ground state configuration with a specific number of electrons on the island was considered. However, once an electronic or vibrational excited state  $\mu_e^{(N)}$  (Figure 2.8 a)), is aligned with  $\mu_S$  (or  $\mu_D$ ), an additional transport channel is accessible, resulting in a current increase through the dot. This increase in turn appears as parallel lines to the Coulomb diamond edges in the differential stability diagram, schematically depicted in Figure 2.8 b). Hence, the excitation energy  $E_{ex} = V_{DS} \cdot e$  can be extracted from the crossing point of the Coulomb diamond edge and the excitation line. For electronic excitations,  $E_{ex}$  corresponds to the difference between the ground and first excited

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**Figure 2.8 Excited states in quantum dots with negligible  $\Delta$ .** a) Energy diagram of a quantum dot with three energy levels (black) and one excited state  $\mu_{(N)}^e$  (red). b) Differential stability diagram with the presence of excited states. The colored lines mark the positions where excited states contribute to charge transport. The excited states appear as parallel lines (red, blue, green) to the edge of the blocked regions in non-blocked regions.

state and is within the constant interaction model equivalent to the splitting energy. Details for vibrational excitations can be found in ref.<sup>100</sup>. As explained above, the prerequisite to observe quantum and charge-quantization effects is a smaller thermal energy  $k_B T$  compared to the addition energy in equation 2.9. This condition can already be fulfilled at room temperature for very small quantum dots<sup>105,106</sup>. In general, the full width at half maximum of the conductance peaks is decreasing for smaller temperatures<sup>107</sup>, because for higher temperatures more and more charges are in the thermal energy range of  $E_{odd}$  and can tunnel through the dot.

## 2.7 Manuscript M1: Charge transport in semiconducting polymers at the nanoscale

Jakob Lenz and R. Thomas Weitz

*In preparation*

### **Abstract**

In highly ordered crystalline small molecule based organic semiconductors the interplay between the charge transport mechanism and the molecular structure of the organic lattice is nowadays comparably well understood due to the clearly defined morphology. Charge transport in polymeric semiconductors on the other hand is rather complex for example due to the substantial amount of conformational freedom of the polymer chains. In macroscopic devices, charge transport is characterized by alternating ordered and disordered phases with varying interconnections and structural defects which implies that the influence of molecular weight and side-chains, polymer fiber alignment and backbone rigidity has to be considered, since different transport mechanisms at various length scales from single chains to the macroscale can overlap. To fully understand transport in these systems, ideally each length scale would be addressed individually before different processes can be joined in a macroscopic picture. In this perspective we focus on charge transport properties of polymeric semiconductors at the shortest possible length scales still accessible by charge transport experiments.

### **Contribution**

The first draft of the manuscript was written entirely by me and I produced the final version. All figures were designed by me.

### Charge transport at the nanoscale in semiconducting polymers

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#### Abstract

In highly ordered crystalline small molecule based organic semiconductors the interplay between the charge transport mechanism and the molecular structure of the organic lattice is nowadays comparably well understood due to the clearly defined morphology. Charge transport in polymeric semiconductors on the other hand is rather complex for example due to the substantial amount of conformational freedom of the polymer chains. In macroscopic devices, charge transport is characterized by alternating ordered and disordered phases with varying interconnections and structural defects which implies that the influence of molecular weight and side-chains, polymer fiber alignment and backbone rigidity has to be considered, since different transport mechanisms at various length scales from single chains to the macroscale can overlap. To fully understand transport in these systems, ideally each length scale would be addressed individually before different processes can be joined in a macroscopic picture. In this perspective we focus on charge transport properties of polymeric semiconductors at the shortest possible length scales still accessible by charge transport experiments.

## 2.7 Manuscript M1: Charge transport in semiconducting polymers at the nanoscale

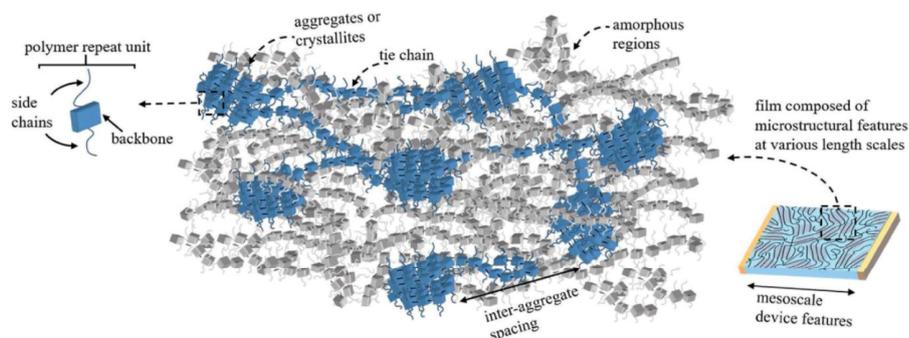
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### Introduction

In molecular organic semiconductors (OSCs) the well-defined crystalline morphology facilitates a theoretical description of the experimental and theoretical understanding of charge transport mechanism. In polymeric OSCs however the solid-state microstructure is characterized by weak van der Waals forces between single polymer chains, which results in a large variety of intermolecular packing due to conformational freedom of the polymer chains. In the cartoon representation in Figure 1.1, two types of ordered phases exist, namely crystallites or aggregates. While aggregates reveal order solely in the  $\pi$ -stacking direction, crystallites display additional order in the alkyl-stacking direction [1]. In these ordered regions the most efficient charge transport occurs at the shortest length scales (typically a few nanometers) within femto- to picoseconds [2] along the polymer backbone within single polymer chains (intrachain). At longer length scales within ordered regions, charge transport is dominated by interchain hopping, which is two to three orders of magnitude slower compared to intrachain transport [3]. Charge transport via the typically non-conjugated side-chains is almost negligible [4] and they e.g. define the polymer's solubility as well as the relative stacking of chains. Finally, in the amorphous regions charge transport is very inefficient due to a lack of  $\pi$ -stacking order. All together the different length scales in the mesoscale of a polymer film lead to the presence of multiple charge transport processes. This implies that transport at longer length scales of typical transistor channel lengths ( $> \mu\text{m}$ ) needs to be regarded as a multiscale process [3,5,6] and is usually limited by transport through amorphous regions. However, transport can be drastically increased by interconnecting crystallites or aggregates via the mentioned of tie chains [7,8]. If an optimum amount of interconnectivity can be ensured charge transport is limited by interchain hopping processes within ordered phases [3,9]. Different charge transport mechanisms dominating at different length scales illustrate the complexity in theoretical and experimental characterization, understanding and in a next step optimization of the microstructures of polymer films. The complexity becomes even clearer considering that contrary to the general expectation that a higher degree of crystallinity is accompanied by an improved charge transport, it has been shown that in specific cases comparably less crystalline donor-acceptor (D-A) copolymers consisting of alternating electron-rich and electron-deficient units along the polymer backbone exhibit an improved charge transport behaviour [10–12]. The high performance of these quasi-amorphous polymers is related to a minimized energetic disorder and a facilitated charge transport along the almost torsion-free, planar and rigid polymer backbone.

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**Figure 1. Cartoon representation of the microstructure of conjugated polymers illustrating different length scales.** The mesoscale of a polymer film can be distinguished in ordered and amorphous regions. Ordered regions (blue), either consisting of crystallites (long-range order) or aggregates (short-range order), can be interconnected via tie chains. Figure reproduced with permission from ref. [2]. Copyright 2018, John Wiley & Sons, Inc.

From the above description it becomes clear that to obtain a more unified picture of charge transport in polymer thin films, it would be advantageous to be able to address the described individual charge transport processes occurring at each specific length scale separately. While several general works describing transport at ultrashort lengthscales in single molecular breakjunctions [13–15] and macroscopic devices [16,17] are available, we aim here to give a perspective how the gap between macroscopic and local, namely in the hard-to-probe scale of crystalline aggregates or few molecular chains can be probed by charge transport. The upper limit of intrachain transport within single chains can be estimated using high frequency non-contact measurements [18,19] where mobilities of up to  $600 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  [19] have been reported without external influences present in organic field-effect transistors (OFETs) as e.g. contact resistances, short channel effects or interfacial trap states. Here we address how charge transport can be probed experimentally at lower frequencies by charge transport. This perspective is organized as follows: First, we give an overview of the most prominent charge transport mechanism in polymeric OFETs starting with a theoretical derivation of the electrical characteristics of FETs. In the next part we summarize different structural influences as side chain engineering or the molecular on the charge transport behaviour in OFETs. The following section elucidates the superior charge transport along a proper aligned polymer backbone. The last part of this perspective is dedicated to the transport dynamics in nanoscopic devices.

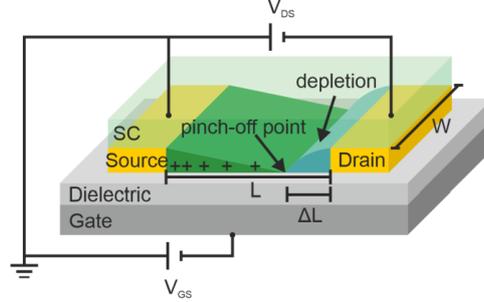
### Charge transport in OFETs

In the last couple of years it has become increasingly obvious that there is no uniform model and no generalized understanding to describe, predict and compare the charge transport mechanism over the full range of organic semiconductors. In fact different theories according to morphology and microstructure have been successfully applied to different experiments. In this part we want to summarize the most prominent existing models of microscopic charge transport mechanisms and their specific fields of application. To this end we first want to introduce the fundamental working principles of field-effect transistors (FETs) with corresponding device parameters. The mobility as figure of merit will be explained followed by a short discussion of short channel and contact resistance effects in short channel OFETs.

### FET

Transistors in general and specifically FETs are the most commonly used devices for charge transport investigations of semiconductors due to the large number of turning knobs available, as e.g. size tunability, different geometries regarding the arrangement of electrodes, selection of different electrode and gate materials, to name a few. In that way, different lengths scales within the OSC, transport properties at varying charge carrier concentrations as well as the influence of the interface of the OSC to the electrode or dielectric material, can be separately addressed and characterized. Figure 2 illustrates a schematic FET cross section with bottom gate bottom contact configuration. More extensive explanations of the working principles of OFETs can be found in several excellent reviews [17,20]. Usually FETs comprise a substrate, a gate electrode separated by a dielectric from the organic semiconductor, and the source drain electrodes. The basic model to derive the equations that describe the working principle of an ideal FET is the gradual channel approximation originally derived for metal-oxide-semiconductor FETs (MOSFETs) [21,22]. The gradual channel approximation is based on the assumption that the gate electric field (controlled by the gate-source voltage  $V_{GS}$ ) is much greater than the longitudinal electric field between source and drain electrodes (controlled by the drain-source voltage  $V_{DS}$ ). Furthermore charge transport is dominated by drift current and it is assumed charge carrier mobility is constant within the conducting channel. The following deviation is similar for electrons and holes. Corresponding to the picture of a capacitor, applying a gate voltage  $V_{GS}$  between gate and source electrode induces a few nm accumulation layer [23,24] of charge carriers at the OSC dielectric interface, usually referred to as conducting channel. With an additional applied source drain voltage  $V_{DS}$  the conductivity of the semiconductor as function of the charge carrier density can be investigated. Based on the number of induced charge carriers in the conductive channel, a general expression for the drain current  $I_D$  can be derived with the channel width  $W$ , channel length  $L$  (see Figure 2), the capacitance per unit area  $C_i$  of the dielectric and the charge carrier mobility  $\mu$ .

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**Figure 2. Schematic device structure of a p-type OFET with bottom gate and bottom contact configuration in saturation mode.** The characteristic length scales channel length  $L$  and channel width  $W$  are indicated

$$I_D = \frac{W}{L_{ch}} \mu \hat{C} \left[ (V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad (1)$$

The empirical threshold voltage  $V_{th}$  is characterized by the minimum gate voltage that has to be applied in order to induce a strong inversion of charges. Since methods for controlled doping of OSCs are just emerging [25,26], the materials are usually used in their as-synthesized form [17]. Hence the devices are predominantly driven in accumulation mode [27]. Here,  $V_{th}$  is defined by the difference between the Fermi level of the S/D contact and the HOMO respective LUMO level of organic material [28], which will be explained at later parts. This leads to a charge transfer resulting in a dipole and a band bending in the semiconductor. Additionally, there may be deep traps present in the organic semiconductor or at the OSC - dielectric interface, which need to be filled first before the channel is fully conductive.

In the linear regime where  $V_{GS}$  is larger than  $V_{th}$  and very large compared to  $V_{DS}$  the drain current  $I_{D,lin}$  is given by [21]

$$I_{D,lin} = \mu_{lin} \frac{W}{L} C_i (V_{GS} - V_{th}) V_{DS} \quad (2)$$

Once  $V_{DS}$  exceeds  $V_{DS,sat} = V_{GS} - V_{th}$ , the conductive channel is disrupted at the drain electrode since the influence of  $V_{GS}$  is neutralized by  $V_{DS}$  close to the drain contact. This so called "pinch-off" effect is characterized by an absence of free charge carriers and hence high resistance close to the drain. Here  $I_D$  becomes  $V_{DS}$  independent and saturates according to equation 1.

$$I_{D,sat} = \mu_{sat} \frac{WC_i}{2L} (V_{GS} - V_{th})^2 \quad (3)$$

The mobilities for the different regimes are given by:

$$\mu_{lin} = \frac{L}{C_i W V_{DS}} \frac{\partial I_{D,lin}}{\partial V_{GS}} \quad (4)$$

and

$$\mu_{sat} = \frac{2L}{WC_t} \left( \frac{\partial \sqrt{I_{D,sat}}}{\partial V_{GS}} \right)^2. \quad (5)$$

A further increase of  $V_{DS}$  leads to a slight shift of the pinch-off point away from the drain electrode towards the source electrode leading to a reduced effective channel length  $\tilde{L} = L - \Delta L$ . This effect becomes increasingly relevant for the overall transistor operation with decreasing channel lengths in short channel devices. Here according to equation (3) for increasing  $V_{DS}$  and hence decreasing  $\tilde{L}$ ,  $I_{D,sat}$  starts to deviate (or more specifically  $I_D$  increases) from the ideal behaviour resulting in the absence of saturation in extreme cases [29], which is one of the most prominent short channel effects.

### Mobility as figure of merit

For experimental investigation of not only organic but also inorganic and hybrid semiconductors the important figures of merit,  $\mu_{lin}$  and  $\mu_{sat}$  are usually calculated by extracting the slope of  $I_{D,lin}$  and  $I_{D,sat}^{1/2}$  versus  $V_{GS}$  at constant  $V_{DS}$  in the linear and the saturation regime, respectively. The aforementioned derived Equations (4) and (5) only hold true within the gradual channel approximation fulfilling the prerequisites of a much larger transversal gate electric field compared to the longitudinal source-drain electric field and a charge carrier density independent mobility [21]. Using Equations (4) and (5) to calculate the mobility  $\mu$  is only valid for linear transfer characteristics [30], i. e.  $I_D(V_{GS})$  in the linear regime and  $|I_D|^{1/2}(V_{GS})$  in the saturation regime has to be linear in an extended  $V_{GS}$  range. This becomes one of the major hurdles for realizing devices with channel lengths in the nanometre region. To stay within the gradual channel approximation, very thin materials with sufficient dielectric strengths, high-k dielectrics or the high capacity of ionic liquids can be utilized. It is obvious that using points with high curvatures in nonlinear transfer characteristics might lead to overestimated  $\mu$  values according to equations 4 and 5. Instead of extracting the mobility with the maximum of the derivative of  $I_D$  with respect to  $V_{GS}$  one should use a constant region which corresponds to linear transfer characteristics. Another requirement is the avoidance of the inherently increasing contact resistances compared to the channel resistance [31,32] for decreasing device dimensions. Since four-probe measurements, which would overcome contact resistance influences, require more complicated device architectures and fabrication steps (especially for short channel devices) as well as more sophisticated measurement setups, attention is typically attributed to minimizing the effects of contact resistances in the commonly used two-probe configurations. The most common methods to reduce contact resistances is the use of thiol monolayers to tune the metal work function [33] or contact doping [34]. To avoid data misinterpretation and to estimate the mobility in a correct way we refer to the guidelines given by Choi and coworkers [35]. For a detailed understanding which factors determine the mobility and

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other device parameters a theoretical description of the specific charge transport mechanism is inevitable.

### Charge transport mechanism

Charge transport physics in molecular and polymeric OSCs has been widely discussed in several excellent reviews [36–39]. Depending on the materials and crystallinity, the most frequently used theories to describe charge transport in OSCs include the transient localization picture, band transport, multiple-trap and release and variable range hopping. While the theoretical description for small molecular single crystals is more straightforward, charge transport dynamics in weakly bonded conjugated polymers with microstructures varying from amorphous to crystalline is far from being fully understood. Since the length of electronic devices typically exceeds the dimension of a single polymer chains, the measured macroscopic mobility is characterized by multiscale processes and usually dominated by intermolecular charge transfer. The degree of overlap between delocalized  $\pi$ -orbitals of adjacent molecules or crystalline polymers determines the intermolecular charge carrier transfer rate. For an ideal organic crystal in analogy to inorganic semiconductors as e.g. Si, the highest occupied molecular orbital (HOMO) can be regarded as the valence-band edge and the lowest unoccupied molecular orbital (LUMO) as the bottom of the conduction band [40]. To differentiate between charge transport mechanisms in OSCs one test is to measure the temperature dependence of the mobility. Since charge localization in polarons, in impurity and structurally induced electronic traps hinders freely propagating charges, a prerequisite for band or band-like transport are almost disorder-free OSCs. Band or band-like transport is usually proven by a negative temperature dependence of the mobility. Here by freezing out the effects of vibrations and impurities, the mobility increases for decreasing temperature. This sought after regime was presented both for specific small molecules [41–43] and polymers [44–46].

In polycrystalline OSCs with a low extent of structural disorder, charge transport can be described by the multiple trap and release (MRT) model or the mobility edge (ME) model, which is well established to describe charge transport in amorphous silicon [47]. In polycrystalline polymers with a short range order, where crystalline aggregates are separated by defects, grain boundaries and disordered regions, charges are temporarily trapped in localized states. Above a characteristic energy in the DOS, the so called mobility edge, trapped charges can become temporarily mobile e.g. by thermal excitation and delocalized in ordered regions until they are retrapped. The MRT and ME model have been successfully used to describe charge transport in polymeric OFETs in several studies [48–50].

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The most widely applied charge transport model for rather low-mobility OSCs on the other hand is the variable range hopping (VRH) model [51–54]. For truly amorphous materials with an absence of any long range order, charge transport is limited by hopping due to thermally activated tunnelling between localized states in a broad DOS with an energetically disordered landscape of sites. Both variable range hopping and MRT (ME) model exhibit a thermally activated mobility with an increased charge carrier delocalization with increasing temperature.

The huge variation of the different models and their limitations for different materials, morphologies and microstructures makes a direct comparison of OSCs regarding charge transport properties very challenging. To circumvent this fundamental problem Liu et al.[55] presented the generalized Einstein relation (GER) which unifies various validated theories as a generalized charge transport model treating OSCs with different morphologies. The model phenomenologically takes into account morphologies ranging from single crystal to amorphous by changing the variance of the density of states (DOS)  $\Delta E$ , which can be regarded as a signature of energetic disorder, and delocalization degree  $\Delta D$  in a Gaussian-distributed DOS. Like this, the GER can quantify most temperature and charge carrier mobility dependencies. Based on three characteristics of OSCs in FETs, weak bonding of neighboring molecules, a degenerate state induced Fermi-Dirac distribution of the charge carrier density  $n$  and a non-negligible amount of traps and defects, the authors derive an overall mobility for disordered materials:

$$\mu = \frac{\sigma}{qn_c} = \frac{q \int_{-\infty}^{+\infty} N(E)D(E) \left[ -\frac{\partial f(E)}{\partial E} \right] dE}{\int_{-\infty}^{+\infty} N(E)f(E)dE} \quad (6)$$

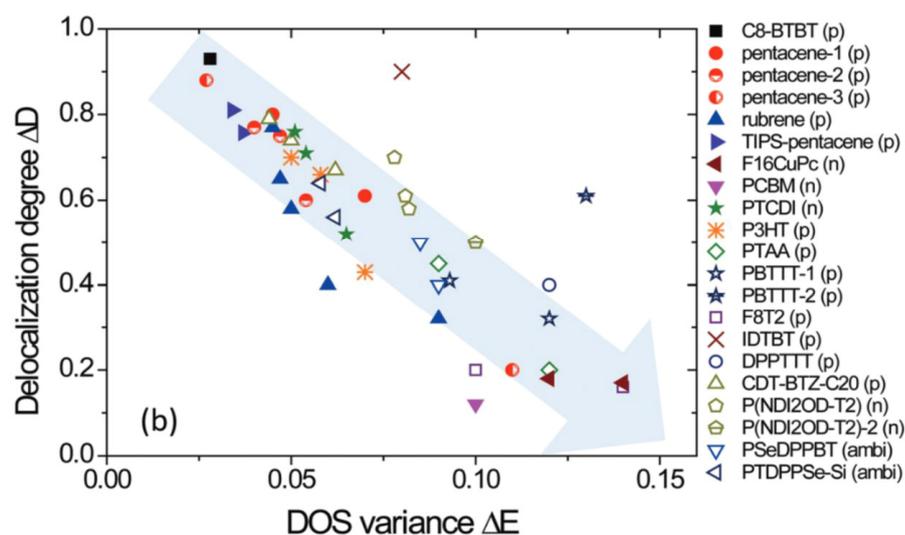
with  $n_c$  as the total carrier concentration,  $N(E)$  as the DOS,  $f(E)$  the Fermi function and  $D(E)$  the diffusivity for each energy. Here, the influence of localized states due to grain boundaries, polymeric twisting and chemical impurities in the tail states in the DOS on transport properties is also taken into account in a microscopic and energy dependent conductivity of electronic states  $\sigma'$ .

$$\sigma'(E) = \frac{\sigma_0}{\sqrt{2\pi(\Delta D \Delta E)}} \exp \left[ -\frac{(E-E_0)^2}{2(\Delta D \Delta E)^2} \right] \quad (7)$$

$\sigma_0 = \frac{N_c q \mu_0}{2}$  and  $\mu_0$  are the material-specific characteristic conductivity and mobility.

In conclusion the GER renders it possible to unify the aforementioned transport models and hence to compare the charge transport determined by  $\Delta E$  and  $\Delta D$  for different OSCs in Figure 3. Here the impact of energetic disorder and the delocalization degree on charge transport is illustrated by the grey arrow.

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**Figure 3. Comparison of the disorder in the charge transport for different semiconductors in a  $\Delta E - \Delta D$  map.** The arrow indicates the direction of increasing disorder in the charge transport. Figure reproduced with permission from ref. [55], Royal Society of Chemistry.

While general phenomenological models to describe charge transport in polymers are known, the complex microstructure of polymers has made it challenging to a-priori predict clear structure-property relationships with clear and universal ideas of charge transport. In the remainder of the manuscript, charge transport investigations at the nanoscale within homogeneous regions from fully amorphous to crystalline could be a versatile tool to gain a deeper understanding of the underlying physical reasons leading to the applicability of a specific charge transport model.

### Impact of molecular structure on charge transport

The field-effect mobility of an organic FET is critically dependent on the local intramolecular structure and the intermolecular packing between the molecules. The above mentioned charge transport models lead to the conclusion that an improved long-range crystallinity is the preferred path to an improvement in mobility. This led to the development of highly crystalline structures with a long-range order and a charge transport along the  $\pi$ -direction including poly-3-hexylthiophene (P3HT) ( $\mu \leq 0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ) [56,57], poly[2,5-bis(3-tetradecylthiophen-2-yl)thieno[3,2-b]thiophene] (PBTTT) ( $\mu \leq 1 \text{ cm}^2 \text{ V}^{-1}$

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s<sup>-1</sup>) [58,59] or diketopyrrolopyrrole (DPP) based conjugated polymers ( $\mu \leq 3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ) [60–62], to name a few. Besides highly crystalline polymers, promising results of high mobility D-A copolymers with limited or almost no long-range crystallinity showed that there is more than one way to obtain high mobilities [10,12,63]. Specifically, for indacenodithiophene-benzothiadiazole (IDT-BT) [10] the high mobility of  $2.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  is attributed to a low degree of energetic disorder confirmed by a small Urbach energy of 24 meV. The reason is, that a reduced chain folding and torsion leads to a highly planar and rigid backbone with close  $\pi$ - $\pi$  contacts and enables charge transport that approaches the material specific intrinsic limits (just like in the above mentioned example of the DPP polymer). Another reason for the torsion-free backbone of IDT-BT is its resilience to side-chain disorder.

Besides a superior charge transport caused by a planar and rigid backbone another critical path to improve the charge transport behaviour is to enhance intermolecular  $\pi$ - $\pi$  stacking by side chain engineering. More specifically, this means that the usually limiting intermolecular charge transfer can be improved by an increased  $\pi$ - $\pi$  overlap due to a reduced stacking distance of adjacent polymer chains [64,65]. We now give several examples how  $\pi$ - $\pi$  stacking of popular polymer backbones could be enhanced to also show that there is no general route for all backbones. For example, by varying the molar ratio of CO(NH<sub>2</sub>)<sub>2</sub> containing alkyl chains versus branching alkyl chains in (DPP)-quaterthiophene conjugated polymers an almost fourfold mobility increase could be demonstrated [66]. In a series of DPP-selenophene vinylene selenophene polymers with branched alkyl groups and linear spacers from two to nine C atoms it has been shown that the charge transport strongly depends not only on the length of the spacer but also on the question if the spacer number is even or odd [67]. Thus, the mobility exhibits a zigzag-like behaviour with a one order of magnitude higher mobility for even numbers of C. This dependency is confirmed by X-ray diffraction (XRD) and grazing incidence X-ray diffraction (GIXD) analysis with a denser molecular packing and hence stronger interdiffusion with a reduced intermolecular spacing in the out-of-plane direction for even C atom numbers. However this does not seem to be a general concept. Dou et al. [68] figured out for benzodi-furandione-based oligo(p-phenylenevinylene) (BDPPV) polymers with alkyl chains branched at different positions that a shorter  $\pi$ - $\pi$  stacking distance not automatically correlates with higher carrier mobilities. Indeed the interplay between backbone alignment, crystallinity, thin film disorder and  $\pi$ - $\pi$  stacking distance by maintaining good solubility properties and solution processabilities has to be balanced. As a side note, side-chain engineering not only affects intrinsic charge transport properties, but also can control the mode of operation in electrolyte gated transistors by changing the susceptibility to interdiffusion of ions into the film. Measurements with an aqueous NaCl gate on two polymers with the same bithiophene–thienothiophene (2T-TT) backbone unit but functionalized once with alkoxy side-chains (poly(2-(3,3'-bis(tetradecyloxy)-[2,2'-bithiophen]-5-yl)thieno[3,2-b]thiophene) p(a2T-TT)) and once with glycol side chains (poly(2-(3,3'-bis(2-(2-(2-methoxyethoxy)ethoxy)ethoxy)-[2,2'-bithiophen]-5-

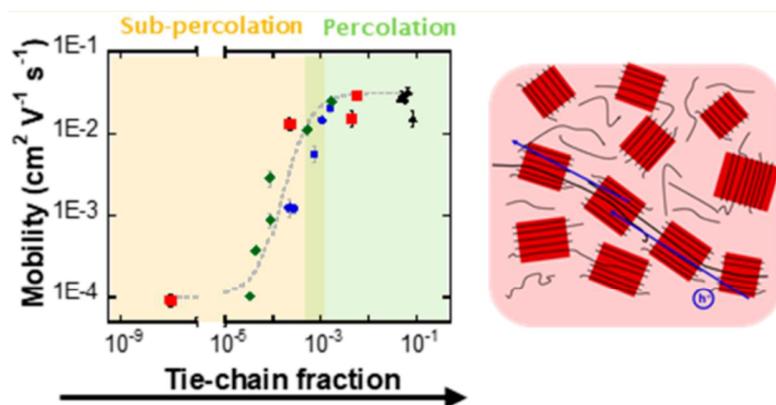
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yl)thieno[3,2-b]thiophene p(g2T-TT)) reveal a transformation from interfacial (p(a2t-TT) to bulk-doping p(g2T-TT) [69].

Not only a planar and rigid backbone as well as side chain engineering, but also the molecular weight (MW) has a strong impact on charge transport properties of polymeric semiconductors. Amongst others it was found, that for P3HT [70–72] and D-A copolymers as DPP- dithienylthieno[3,2-b]thiophene (DPP-DTT) [73] and poly[2,6-(4,4-bis-alkyl-4H-cyclopenta[2,1-b;3,4-b']-dithiophene)-alt-4,7-(2,1,3-benzothiadiazole)] (cyclopentadithiophene–benzothiadiazole) (CDT-BTZ) [74], that the MW correlates with charge carrier mobility. Although low MW polymers exhibit high degrees of crystallinity, charge transport is limited by hopping processes between crystalline domains. As the MW increases, more and more interconnection via long and planar tie chains facilitate charge transport between ordered regions. According to the model proposed by Noriega et al. [39] charge transport is improved by increased MWs and hence increased connectivity between adjacent crystallites until a saturation point. From this point the mobility is mainly limited by lattice disorder induced trapping within the crystallites. Recently Gu et al. [8] quantified the relation of tie chain fraction  $f_{TC}$  and mobility for P3HT blends with different MWs (see Figure 4). Red crystalline grains are interconnected via blue tie chains. Once  $f_{TC}$  exceeds  $\sim 10^{-4}$  the mobility increases until a plateau with sufficient intercrystallite connectivity ( $f_{TC} \sim 10^{-3}$ ) is reached. From that point the mobility is limited as aforementioned by intradomain disorder. Tseng et al. [75] utilized a slow drying process on nano-grooved substrates to fabricate well aligned poly[4-(4,4-dihexadecyl-4H-cyclopenta[1,2-b:5,4-b']dithiophen-2-yl)-alt-[1,2,5]thiadiazolo[3,4-c]pyridine] polymer (PCDTPT) fibers with a high density and a MW ranging from 30 to 300 kDa. For non-aligned films a similar dependency as explained above with increasing mobility for higher MWs and a maximum value of  $1.9 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  for 300 kDa could be observed. On the other hand aligned films revealed MW independent higher mobilities than the non-aligned films. AFM images both for non-aligned and aligned films indicate the fundamental morphology differences. Whereas in the non-aligned samples grain boundaries in the lower MW polymers limit the carrier mobility and these trapping sites are reduced for randomly arranged high MW polymers, charge transport in the aligned films occur along the conjugated backbone with occasional interchain  $\pi$ - $\pi$  hopping. The huge potential of suitable polymer fiber alignment for improved charge transport without the need of high MWs and the associated challenges of purification and solution processability will be explained in more detail in the next section.

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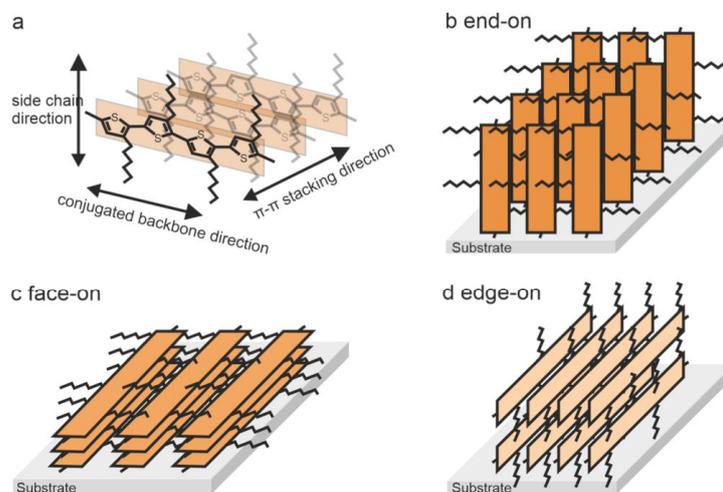


**Figure 4.** Field-effect mobility of transistors comprising P3HT blends as a function of the tie chain fraction ( $f_{TC}$ ). The schematic picture on the right illustrates single crystalline domains (red) interconnected via tie chains (blue) to form a percolating network. Figure reproduced with permission from ref.[8], American Chemical Society.

### Thin-film alignment effects

In the last couple of years a lot of effort was put in improving the device performance of polymeric OFETs by aligning the conjugated polymer films, with the goal to limit the number of interchain hopping events. A more detailed description of how the alignment of conjugated polymers correlates with the performance of OFETs can be found in several excellent reviews [76–79]. Interchain charge hopping is defined by the  $\pi$ - $\pi$  overlap of adjacent polymer chains, the latter of which in turn is mainly controlled by the microstructure of the polymer. In this regard a fundamental distinction has to be made regarding the polymer chain orientations with respect to the substrate surface, which can be seen exemplary for polythiophenes in Figure 5. The fastest transport processes occur along the conjugated backbone direction and the slower interchain charge transfer via overlapping  $\pi$ -orbitals along the  $\pi$ - $\pi$  stacking direction. The lowest conductivity and mobility is observed along the insulating alkyl side chain direction [80]. The end-on orientation with the polymer backbone direction normal to the substrate exhibits the highest out-of-plane transport behaviour and is therefore a suitable candidate for the field of organic photovoltaics [81] instead of TFTs. In the face-on orientation the conjugated backbone and the alkyl side chain axis are parallel to the substrate whereas the  $\pi$ - $\pi$  stacking direction lies out-of-plane to the substrate. In contrast, the  $\pi$ - $\pi$  stacking and the conjugated backbone axis lie parallel and the alkyl side chain axis perpendicular to the substrate in the edge-on orientation. With both the  $\pi$ - $\pi$  stacking and the backbone direction in plane the most promising configuration for

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**Figure 5. Schematic illustration of possible polymer orientations on a substrate exemplary shown for polythiophenes with a, charge transport along the  $\pi$ - $\pi$  direction or the conjugated backbone and the isolating side chain direction. b, end-on, c, face-on and d, edge-on orientation.**

high-performance OFETs was believed to be edge-on [4]. However edge-on orientation is not a prerequisite for high mobility polymers as has been shown e.g. for face-on P(NDI2OD-T2)[82,83] or DPP-based [84] devices. Also it was demonstrated that many high-performance D-A polymers exhibit a coexistence of edge-on and face-on packing structures [85–89]. There are even reports of high mobility D-A polymers with only local order and an almost amorphous microstructure [10–12]. This unpredictable good charge transport behaviour is related to the superior transport along the conjugated backbone and a high interconnectivity via side chains and  $\pi$ -overlaps between different grains with different orientations [90]. As already mentioned the ratio between intra- and interchain transport can be shifted by properly aligning polymer films resulting in an improved device performance with a reduction of interchain hopping events.

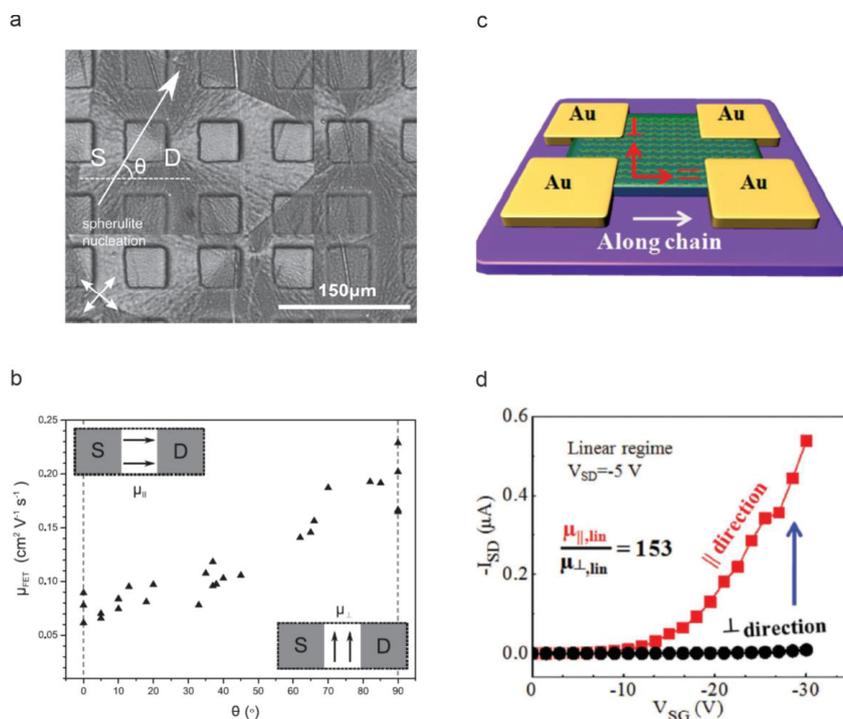
For unidirectional aligned polymer films various techniques have been developed including off-center spin coating [91,92], nanogrooved substrate assisted directional solvent evaporation [93,94], mechanical rubbing [95,96], dip-coating [97,98], wire-bar coating [99,100] and blade coating [62,101–105], to name just a view, whereby all of them showing a superior charge transport for aligned compared to non-aligned films. For unidirectional aligned PCDTPT and CDT-BTZ films on nanogrooved substrates a 13.6 and 17.6 fold enhancement of saturation hole mobilities between parallel and perpendicular measurements with respect to the backbone have been observed [106]. Similar

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enhancements with a factor  $>10$  were shown for poly[[2,5-bis(2-octadecyl)-2,3,5,6-tetrahydro-3,6-DPP[3,4-c]pyrrole-1,4-diyl]-alt-(2-octylnonyl)-2,1,3-benzotriazole] (DPP-BTZ) [84] and isoindigo-based conjugated polymer (PII-2T) [98] aligned films. By horizontally compressing a thin CDT-BTZ film lying on the ionic liquid [EMIM][TFSI], uniaxially aligned films reaching a 9 fold [44] and a 14 fold [107] mobility increase compared to drop casted films could be prepared. Remarkably these films exhibit band-like transport characteristics along the aligned backbone direction proven (1) by an increasing mobility with decreasing temperature and (2) Hall effect measurements indicating charge carrier delocalization. While these alignment techniques have helped to understand and improve  $\mu$  in polymers, an ideal scenario to investigate the charge anisotropy of aligned polymer chains would be the fabrication of single polymer crystals, which turns out to be very challenging due to the large degree of conformational freedom and hence inevitable morphological disorder. Nevertheless several groups have attempted to realize single crystals. Starting with spin coated P3HT films, controlled dissolution and recrystallization by an exact control of solvent swelling, results in a radial growth of spherulitic domains (see Figure 6 a) [108]. To make sure that transport is measured within single crystals proven by AFM images at the surface, the P3HT films were delaminated and inverted. Here a 2 to 4 fold increase of mobility was found in the direction perpendicular to the lamellar crystallites, i.e. along the aligned polymer chains (see Figure 6 b). In another approach proposed by Yao et al.[109], high quality poly-10,12-pentacosadiynoic acid (poly-PCDA) crystals were fabricated by surface-supported topological polymerization. The highest mobility-anisotropy ratio measured within a single crystal parallel ( $\parallel$ ) and perpendicular ( $\perp$ ) to the polymer backbone is 153 (see Figure 6 c,d). These results elucidate the superior intrachain charge transport along the polymer backbone with only occasional interchain  $\pi$ - $\pi$  hopping compared to almost exclusively interchain transport along the  $\pi$ - $\pi$  direction (perpendicular to the polymer backbone). By improving transport via uniaxial alignment of conjugated polymer films one can estimate the intrinsic charge transport properties on the microscale with macroscopic methods. A further improvement of device performance could be realized by reducing the channel length and hence the amount of interchain hopping events.

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**Figure 6. Single polymer crystals measured parallel and perpendicular to polymer backbone orientation.** **a**, Single P3HT spherulites and transistors within a single crystal domain ( $L = 20 \mu\text{m}$ ). **b**, Mobility  $\mu$  as a function of angles between source-drain transport and radial spherulite growth direction  $\theta$ . Figure reproduced with permission from ref. [103], WILEY-VCH. **c**, Schematic of poly-PCDA single crystal transistors. **d**, Linear transfer curve of a single poly-PCDA crystal device ( $W_{\parallel} = 1.6 \mu\text{m}$ ,  $L_{\parallel} = 3.3 \mu\text{m}$ ,  $W_{\perp} = 4.9 \mu\text{m}$  and  $L_{\perp} = 2.7 \mu\text{m}$ ). Figure reproduced with permission from ref. [104], WILEY-VCH.

### Nanogap state of the art

Macroscopic measurements are extremely valuable, but since structure-property related characterization is quite complex to address, there are only few reports for selected polymers at larger scales. Hence charge transport investigations at the nanoscale would be a profound approach to gain deeper insights into morphological limitations. Furthermore, electrical measurements compared to e.g. high frequency non-contact measurements, would be beneficial since the extracted numbers are also relevant for later devices. In an ideal scenario one would need to measure and compare single or

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a few polymer chains embedded between nanogap electrodes without noteworthy contact and short channel effects. Reducing the channel length to the nm regime would minimize interchain charge transfer and would lead to a strong reduction of structural defects. Due to the increasing challenge with downsizing device designs, there are however only few works relating reliable charge transport measurements to morphology at the nanoscale in OSCs yet. Not only the fabrication of nanogap devices is challenging and requires high resolution lithography techniques, but also, as already mentioned, short channel effects and contact resistances become the limiting factor. In general, nanogap electrodes allow the characterization independent from the macroscopic morphology of the polymer. However when measuring a large scale deposited polymer film, what has been successfully demonstrated for poly(9,9-dioctylfluorene-co-bithiophene) (F8BT) with channel lengths down to 30 nm [110] and P3HT with channel lengths down to 50 nm [111], numerous potential conduction pathways along amorphous and ordered regions (see Figure 1) over the whole width of the source and drain electrode make a clear mapping of morphology to conductivity challenging. Hence, research has primarily focused on measuring charge transport in highly crystalline regions.

For polymers, highly crystalline regions, which are marked as blue areas in the cartoon representation in Figure 1, are typically anisotropic and consequently called nanofibers. Here the hurdle of a precise deposition of single polymer fibers on prefabricated electrodes or the search for protection techniques for subsequent electrode patterning has to be taken. This could be realized by using orthogonal materials to the OSCs, e.g. the fluoropolymer Cytop, as sacrificial layers, which was already done to pattern OSC films [112,113].

On the road to locally measuring charge transport in individual polymer nanofibers, one can benefit from the previous developments made for single nanowires based on various inorganic semiconducting materials, including ZnO [114], GaN [115], Si [116], InAs [117],  $V_2O_5$  [118], GaAs [119] and core shell heterostructures [120–122] because of their outstanding physical properties and possible application in nanoscale electronic devices. For organic semiconductors the most prominent representatives are single walled carbon nanotube (SWCNT) transistors [123–125], but there are also reports about single polymer wire light emitting FETs [126] and single wire based sensors [127,128]. In addition also nanowire FETs down to lengths of one micron based on regioregular P3HT [130,131] and polypyrrole [132,133] were presented.

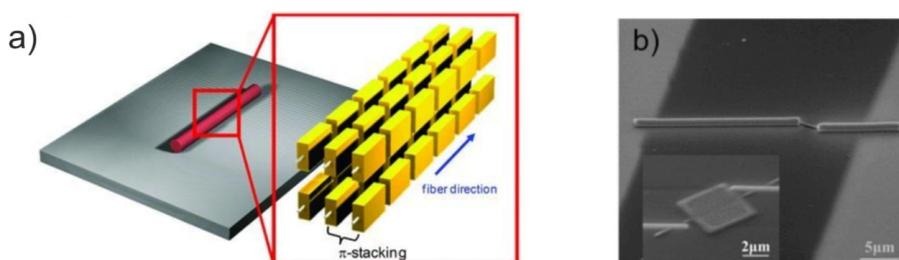
Despite these first results, to the best of our knowledge single or few polymer fiber transistors in the nm regime (i.e. at dimensions approaching e.g. the persistence length) have not been realized yet. However in the following we want to highlight some examples that could show improved electrical performance of single crystalline polymer nanowire transistors with channel lengths in the  $\mu\text{m}$  regime. All these publications show an increased mobility up to several orders of magnitude for high crystalline

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single wires with the  $\pi$ - $\pi$  stacking direction perpendicular to the nanowire growth axis compared to macroscale TFT devices employing the same polymer.

In 2012 Wang and coworkers[134] fabricated highly ordered single polymer fibers with widths between  $0.3\ \mu\text{m}$  and  $0.6\ \mu\text{m}$ , thicknesses between  $80\ \text{nm}$  and  $150\ \text{nm}$  and length of  $5\ \mu\text{m}$  to  $20\ \mu\text{m}$  based on the copolymer CDT-BTZ using solvent vapour enhanced drop casting (SVED) (see Figure 7 a).



**Figure 7. Single CDT-BTZ fiber transistor.** **a**, Schematic of the fiber composition with single CDT-BTZ molecules. **b**, Contacted single fiber with a  $\text{SiO}_2$  protection cover. Figure reproduced with permission from ref. [134], WILEY-VCH.

$\text{SiO}_2$  covered single fiber transistors with a channel length of  $3\ \mu\text{m}$  in Figure 7 b show remarkable saturation mobilities of  $5.5\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$  compared to  $0.67\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$  for low ordered and  $1.4\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$  for directional aligned films of the same polymer[135]. The authors attribute this superior device performance for single fibers mainly to the high crystallinity proven by selected area electron diffraction (SAED) and an improved charge transport in the aligned backbone along the fiber axis in combination with a reduction of structural defects due to the rather short channel lengths. In the field of D-A polymers, the high crystallinity and short  $\pi$ - $\pi$  stacking enabling good intra- and interchain charge transport makes DPP-based conjugated polymers a promising candidate for high performance organic FETs with good solubility properties due to proper side chain alignment[65,136,137]. The innately large mobility of DPP-based FETs can be exploited by fabricating highly crystalline nanowires and e.g. Kim et al.[138] reported a one magnitude increased maximum hole mobility of  $7\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$  for a single wire  $15.9\ \mu\text{m}$  channel length device. The group of Dong Hoon Choi further improved the saturation mobility of a  $10\ \mu\text{m}$  DPP-based nanowire FET about a factor of 15.7 compared to thin film devices of the same polymer [134]. The authors attribute the high mobility to fast intramolecular charge transport along the polymer backbone and less interchain hopping. Xiao et al. [139] fabricated nanowire transistors consisting of the same DPP-benzodithiophene (BDT) polymer which are linked via

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different aromatic heterocycles thiophene (T) and thiazole (TZ). Interestingly PDPP2TBDT nanowires exhibit an edge-on orientation whereas PDPP2TzBDT nanowires crystallised in a face-on orientation. Both orientations reveal hole mobilities up to  $7.42 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , which indicates that an aligned conjugated backbone might be more important than the molecular orientation. It is worth noting that the nanowire transistors show a 17-fold (39-fold) mobility increase compared to PDPP2TBDT (PDPP2TzBDT) thin film devices.

Recently, a sharp 60 times current increase by reducing the channel length from 200 nm to 80 nm was shown for poly-[2,5-bis(2-octyldodecyl)-3,6-di(thiophen-2-yl)pyrrolo[3,4-c]pyrrole-1,4(2H,5H)-dione]-alt-thieno[3,2-b]thiophene (DPPT-TT) films parallel to the alignment direction [140] which can be attributed to intra-domain charge transport in the 80 nm DPPT-TT aligned domains. This current boost is also verified by a 160 times larger current comparing 80 nm channel devices parallel and orthogonal to the aligned polymer. Although the experimental data suffers from an absence of saturation in the output characteristics as well as an absence of current modulation in the transfer characteristics without a visible off-state for the shortest devices, the results indicate the potential of intra domain charge transport.

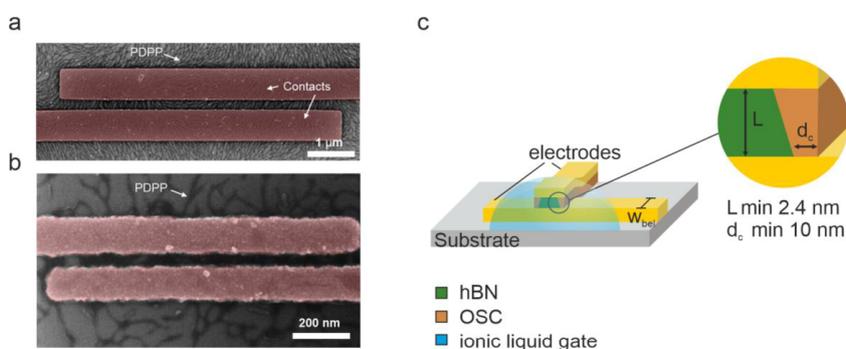
All these results elucidate a superior charge transport of crystalline polymer nanowires with a well-ordered molecular orientation. The improved mobility (while in some cases still to be validated against the established routines described in ref. [35]) is related to a much faster charge transport along the aligned polymer backbone along the fiber growth axis with less intermolecular charge transport across the  $\pi$ - $\pi$  stacking compared to conventional organic TFTs.

To stay within the gradual channel approximation and to avoid short channel effects for devices with channel lengths in the nm regime the gate coupling has also been increased. This could e.g. be realized as recently suggested by using thin high-permittivity gate dielectrics [141]. Another currently widely used method is the usage of liquid or polymer electrolytes as a gate. Thiburce and coworkers [111] measured almost ideal device characteristics with on/off ratios of up to  $10^8$  and channel widths normalized transconductances above  $10 \text{ S m}^{-1}$  for a P3HT transistor with a P14:TFSI (1-Butyl-1-methylpyrrolidinium bis(trifluoromethylsulfonyl)imide) – PEO ion gel gate for channel lengths down to only 50 nm. The large gate coupling of the electrolyte gate allows for an almost complete control of the charge carrier density in short channel devices [142]. Using ion gates one has to differentiate between electrostatic doping comparable to conventional MOSFETs and electrochemical doping, where the whole bulk of the OSC is gated [143,144]. In the first case, a nm thick electric double layer [145] is formed at the semiconductor interface and the former deviation with Equations (4) and (5) holds true. In the case of electrochemical doping ions penetrate the whole bulk of the OSC. This volume effect leads to a 3D capacity instead of a distinct double layer which makes the theoretical

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description more sophisticated [146,147]. Utilizing the large capacity of ionic gates could pave the way for realizing nanogap single polymer fiber transistors while maintaining ideal electrical characteristics. We believe that such devices, where electrochemical doping is unlikely to happen in a single crystalline fiber and the aforementioned mobility deviation is valid, could be a valuable tool for charge transport investigations at the nanoscale. In this context another huge advantage of ion gated OFETs is the reduction of contact resistances by several orders of magnitude [148,149] probably induced by electrochemical doping of the contacts. In our previous work we realized transistors with channel lengths down to 30 nm and a countable number of DPP-based single fibers utilizing the ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl) imide ([EMIM][TFSI]) as a gate [149] (see Figure 8 a)). The devices exhibit exceptionally low contact resistances of below  $3 \Omega\text{cm}$  and saturation output currents.

An easy and helpful way to manufacture ultra short channels is moving from a lateral to a vertical device design. Usually in this case the channel length is defined by the thickness of the OSC layer embedded between the two vertically aligned source drain electrodes. In that way channel lengths in the nm regime can easily be achieved. Recently we presented an approach utilizing an insulating hexagonal boron nitride (hBN) layer between the two electrodes (see Figure 8 b)), whereby the channel length  $L$  can be tuned with atomic precision by the thickness of the hBN layer [150]. In conjunction with the high capacity of the electrolyte gate, almost ideal electrical characteristics with fully saturation output currents have been demonstrated for channel lengths down to 2.4 nm.



**Figure 8. Electrolyte gated DPP-based transistors.** a,b Scanning electron microscopy images of nanoscale DPP-based transistors. Figure reproduced with permission from ref. [149], Springer Nature Ltd. c, Schematic illustration of a DPP-based vertical electrolyte gated transistor with hBN as insulating spacer. Figure reproduced with permission from ref. [150], Springer Nature Ltd.

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Although the theoretical description is more complicated and it seems more difficult to investigate the OSC morphology and to maybe improve charge transport properties by proper alignment, VOFETs could be a very meaningful tool for charge transport investigation at the nanoscale due to the facilitated nanogap fabrication possibilities.

### **Conclusion**

In this perspective we focused on charge transport properties of polymeric organic semiconductors at the nanoscale. Highly ordered phases in the mesoscale of a polymer are separated by amorphous regions and can be interconnected via tie chains. Hence in macroscopic devices different length scales has to be considered as charge transport needs to be regarded as a multiscale process. Therefore to gain a unified understanding of charge transport in polymers individual processes occurring at specific length scales need to be addressed and described separately until different length scales can be joined to a macroscopic picture. In fact, this becomes also clear by the comparably large variety of rather phenomenologically charge transport models, whereby different theories according to morphology and microstructure have been successfully applied to different experiments. Disregarding the very inefficient transport in amorphous regions due to a lack of  $\pi$ -stacking order, transport is limited by the less efficient interchain transport compared to intrachain transport, if a sufficient interconnectivity between ordered regions is provided. In general, different approaches from thin film alignment to the fabrication of highly crystalline nanowires arrived at the same conclusion: The device performance of polymeric systems can be drastically improved by (1) increasing the portion of fast intrachain transport along the polymer backbone with as few as possible interchain transport events and (2) by increasing the interchain charge transfer rate via overlapping  $\pi$ -orbitals by reducing the  $\pi$ - $\pi$  stacking distance. In academia research a facilitated theoretical understanding and better description of experimental results can usually be achieved by reducing the amount of outside interferences and overlaying effects, which leads to the possibility to find better models and in turn routes for new materials and devices. Hence we believe that for rather less ordered polymeric semiconductors with a large degree of conformational freedom of polymer chains a detailed understanding of individual of structure related properties of charge transport processes at the nanoscale within homogeneous regions from fully amorphous to highly crystalline is inevitable.

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## 2 Theoretical Foundations

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# 3 Device fabrication and characterization

*This chapter will give an overview of the main device fabrication and characterization techniques that have been carried out in the course of this thesis. First the wafer preparation and contact fabrication is presented. Second wet and dry etching techniques as well as the fabrication of high-quality 2D hBN and graphite is discussed. Finally different approaches of OSC deposition and electrical device characterization are given.*

*Part of the findings presented in this chapter have been published<sup>56,108</sup>. The articles can be found in appendix A.1 and A.3.*

## 3.1 Wafer preparation

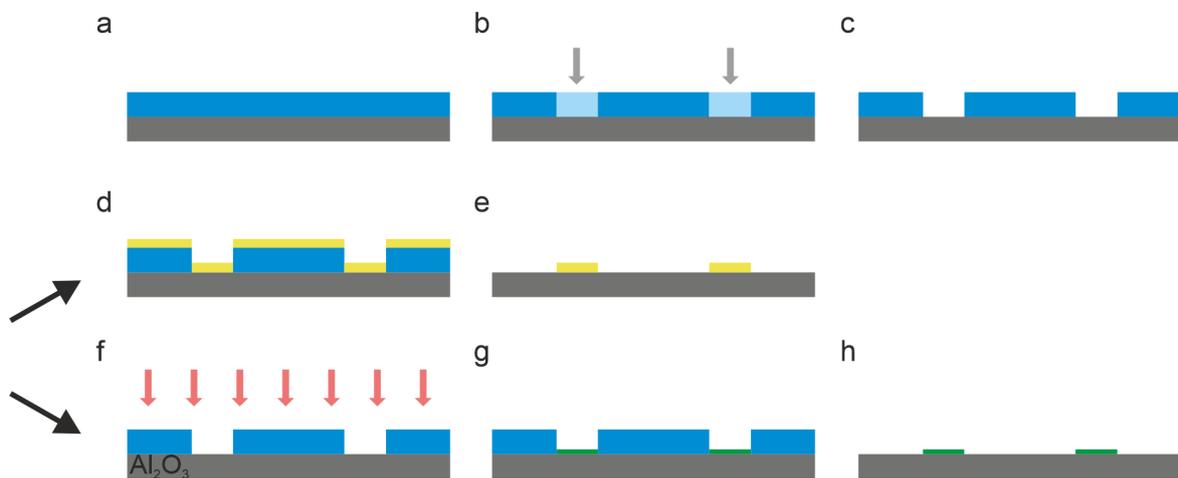
For the sake of simplicity all devices were fabricated on 300 nm SiO<sub>2</sub> slightly boron-doped silicon wafers. Since in all projects different gate arrangements as IL gating or local TDPA functionalized Al<sub>2</sub>O<sub>3</sub> respectively graphite/hBN gates were utilized the silicon wafers were solely used as a substrate. Prior to further processing steps the substrates were cleaned for 5 min each in an ultrasonic bath in acetone and isopropanol and blow-dried with nitrogen. The pre-cleaned substrates were directly used for electrode fabrication in the next step. Only substrates used for graphite and hBN exfoliation were further cleaned in an oxygen plasma for 5 min at 50 W and 10 sccm O<sub>2</sub> (PICO Plasma Cleaner, Diener) followed by a 20 min Piranha acid bath. To facilitate the later flake pick-up after exfoliation, the substrates were etched in 5 % hydrofluoric acid (HF) to remove ~10 nm SiO<sub>2</sub> resulting in a highly hydrophilic surface with less adhesion to the graphite or hBN flakes.

## 3.2 Electrode fabrication

In the semiconducting industry there are different techniques available for device structuring as e.g. the use of shadow masks, or photo, laser or electron beam lithography, whereby the particular use depends on the desired resolution, scalability or ease of processability. For this thesis almost exclusively electron beam lithography was used for contact patterning and Figure 3.1 schematically illustrates the individual lithography steps. At first the positive resist polymethylmethacrylat (PMMA, 4.5 wt.% 950 k in anisole, AR-P 672.045 Allresist) was spin coated onto the pre-cleaned substrates at 800 r.p.m. for 1s and 4000 r.p.m. for 30s. After a soft-bake at 150 °C for 3 min (120 °C for 5 min for

### 3 Device fabrication and characterization

top contacts) the resist was patterned with an electron energy of 10 kV and an electron beam dose of  $165 \mu\text{C cm}^{-2}$  for the  $60 \mu\text{m}$  aperture,  $140 \mu\text{C cm}^{-2}$  for the  $30 \mu\text{m}$  aperture,  $104 \mu\text{C cm}^{-2}$  for  $10 \mu\text{m}$  aperture and  $98 - 107 \mu\text{C cm}^{-2}$  for the  $7.5 \mu\text{m}$  aperture. The exposed structures were developed in a 1:3 solution of methylisobutylketon (MIBK):isopropanol for 1 min 45 sec. For structures smaller than 100 nm, a high-contrast developer with the addition of 2 % methylethylketone (MEK) was used<sup>109</sup>. In order to stop the development process the substrates were rinsed with isopropanol. If the desired structures exceed a height of 100 nm, the PMMA resist was spin-coated twice to ensure better lift off behavior with a soft-bake after each layer, resulting in a total PMMA thickness of  $\sim 500 \text{ nm}$  ( $\sim 250 \text{ nm}$  per layer). Here the development time increases to 3 min. The electrodes were formed via electron-beam physical vapor deposition of  $0.3 - 1 \text{ nm}$  chromium or titanium as adhesion layer (at  $0.1 - 0.3 \text{ \AA s}^{-1}$ ) and  $30 - 100 \text{ nm}$  gold (at  $0.9 - 1.2 \text{ \AA s}^{-1}$ ) at pressures  $< 5 \times 10^{-7} \text{ mbar}$  (see Figure 3.1 d)). Top contacts on OSCs are fabricated through thermal evaporation of  $0.3 \text{ nm}$  titanium (at  $0.1 \text{ \AA s}^{-1}$ ) and  $30 \text{ nm}$  gold (at  $1 \text{ \AA s}^{-1}$ ) at a pressure of  $\sim 5 \times 10^{-6} \text{ mbar}$ . To fabricate top contacts in vertically staggered electrodes prior to metal deposition, an additional insulating  $\text{SiO}_2$  layer of  $35 - 50 \text{ nm}$  can be sputtered with a RF power of  $50 \text{ W}$  and an argon pressure of  $p = 2 \times 10^{-2} \text{ mbar}$ . Lift off to dissolve the remaining PMMA was performed in three consecutive acetone baths at  $40 \text{ }^\circ\text{C}$ . For single polymer fiber transistors electron beam lithography was additionally used to locally apply a SAM on an  $8 - 10 \text{ nm}$  thick  $\text{Al}_2\text{O}_3$  layer sputtered with a RF power of  $40 \text{ W}$  and an argon pressure of  $2 \times 10^{-2} \text{ mbar}$  on pre-fabricated gold gate electrodes. To this end the  $\text{Al}_2\text{O}_3$  surface was locally activated via inductively coupled plasma reactive-ion etching (ICP-RIE, Plasmalab System 100, Oxford Instruments) for 1 min



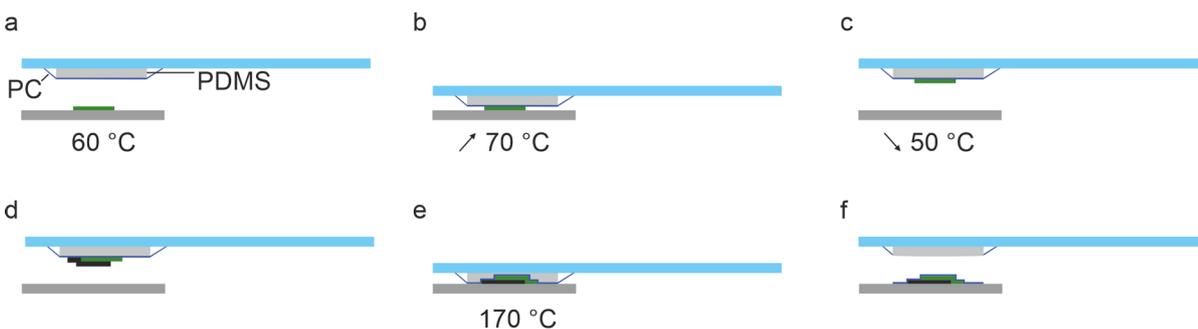
**Figure 3.1 Schematic electron beam lithography.** a) Spin coating of the PMMA resist (blue) on the substrate (grey). b) Electron beam exposure (indicated by grey arrows) according to the designed structure. c) Developing to remove solely exposed PMMA areas. d) Metal (yellow) or dielectric physical vapor deposition. e) Lift off via dissolving of remaining PMMA. f) Alternatively to step d), reactive ion etching (RIE) (indicated by red arrows) of developed regions and g) subsequent SAM (green) deposition. h) Lift off analogous to e).

### 3.3 Exfoliation and flake transfer

with a RF power of 200 W, IPC power of 70 W, a O<sub>2</sub> flow of 30 sccm and a pressure of 10 mTorr (see Figure 3.1 f)). Immediately after RIE the sample was immersed in a 1mM solution of 1-Tetradecylphosphonic acid (TDPA) in isopropanol. After 2 h, the sample is rinsed with isopropanol, blow-dried with nitrogen and baked for 5 min at 150 °C. After SAM deposition lift off was performed in the same way as explained above.

### 3.3 Exfoliation and flake transfer

Few-layer hBN and graphene were fabricated on pre-cleaned and HF etched substrates by mechanical exfoliation from the bulk material. The detailed procedure for few-layer hBN can be found in the methods section of publication A.3 in the appendix. Graphene exfoliation is completely analogous with the only difference of using directly the as-received natural graphite bulk instead of crushed small crystals. In order to fabricate nanometer thin insulating spacers for VOFETs and to fabricate graphite hBN gates a stamping method adopted from ref.<sup>110,111</sup> was used to transfer prior exfoliated hBN and graphite flakes. A detailed description of the stamp fabrication can be found in the methods section of publication A.3 in the appendix. Figure 3.2. schematically illustrates the process of transferring single hBN flakes or building graphite/hBN stacks. At first the stamp was slowly brought into contact with the substrate (heated to 60 °C). By increasing the temperature to 70 °C in the course of 5 min, the polydimethylsiloxane (PDMS)-polycarbonate (PC) block expands until the hBN flake is fully covered. After 2 min, the temperature was cooled down within 5 min to 50 °C whereby the PDMS-PC block shrinks and the hBN flake delaminates from the substrate. It turned out that a higher substrate temperature might improve the adhesion of hBN to PC relative to SiO<sub>2</sub> with a higher flake pick up yield<sup>110</sup>. For VOFET fabrication the hBN flake on the stamp was then brought into contact with



**Figure 3.2 Schematic flake transfer.** a) The substrate with the priorly exfoliated hBN flake (green) is heated to 60 °C. b) After bringing the stamp made from PDMS and PC into contact with the substrate, the temperature is ramped up to 70 °C until the flake is fully covered by PC. c) Ramping down the temperature to 50 °C retracts the stamp and delaminates the flake. d) This procedure (a – c) can be repeated to pick up a graphite flake (black). e) The stack is slowly brought into contact with the final substrate which is heated to 170 °C. f) The PC including the stack is melted down on the substrate and the stamp can be retracted.

### 3 Device fabrication and characterization

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the pre-fabricated bottom electrode (substrate temperature 70 °C). Now the substrate was heated to 170 °C above the glass transition temperature of PC ( $T_G \approx 150 \text{ °C}$  <sup>110,112</sup>) to melt down the PC. This sequence facilitates an exact positioning of the hBN flake on the bottom electrode. However, the subsequent heating procedure to 170 °C might lead to folds in the flake due to thermal expansion of the PDMS-PC block. To fabricate graphite/hBN stacks the process a) – c) in Figure 3.2 was repeated and the graphite electrode was picked up due to the strong van der Waals adhesion of hBN to graphite. Here the final substrate is directly heated to 170 °C and the stamp with the graphite / hBN stack is brought into contact. Once the stamp touched the hot substrate, the PC was melted again. After a waiting time of 30 min in order to improve the adhesion of PC to the SiO<sub>2</sub> substrate, the stamp was moved upwards whereby the PC detached from the PDMS. To remove the melted PC the cooled down substrate was immersed in chloroform for at least 30 min. Finally to remove bubbles between the flakes and to further clean the surface the substrates were annealed in a vacuum chamber at a pressure of less than  $1 \times 10^{-8}$  mbar for 12 h at 200 °C.

#### 3.4 Electrical characterization

Room temperature electrical measurements were performed in a probe station setup, whereby needle probes were used to contact the gate, drain and source pads, respectively. Two source-measure units (Keithley 2450) were used to apply the gate and drain voltages  $V_{GS}$  and  $V_{DS}$  and to simultaneously measure the corresponding gate and drain currents  $I_G$  and  $I_D$ . The grounded source contact was used as reference potential both for drain and gate potential. Electrical measurements on single polymer-fiber transistors and on IL gated SWCNT transistors were conducted in a Lakeshore CRX-VF probe station under vacuum. The temperature can be changed from 5 K to 450 K. Analogous to the room-temperature measurements, electrical contacting is realized via needle probes. In order to ensure sufficient thermal conductivity the substrates were glued with silver-conducting paint on the substrate holder of the probe station. The gate voltage  $V_{GS}$  was applied and the gate current  $I_G$  measured with a Keithley 2450. The drain voltage  $V_{DS}$  was applied with a Yokogawa 7651 DC source. To allow highly accurate current measurements down to the sub nA regime the drain current  $I_D$  was measured with a current preamplifier (1211 DL Instruments) and a HP 34401 A voltage meter.

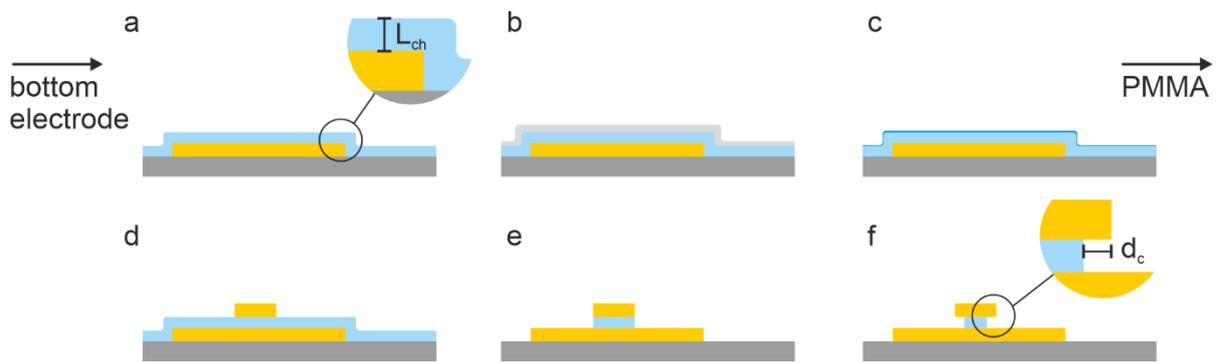
# 4 VOFETs

*When moving from a lateral to a vertical electrode alignment, one of the main advantages is the ease of fabricating short-channel lengths devices with all the associated benefits as explained in section 2.5. The main findings of electrolyte-gated VOFETs can be found in publication A1 and A3, both attached as full text in appendix A. Here, additional results regarding other insulating spacer materials and other OSCs as active materials are presented.*

## 4.1 CYTOP as insulating spacer

Apart from using SiO<sub>2</sub> in publication A1 and hBN in publication A3, additionally the amorphous fluoropolymer CYTOP (CTL 809-M, AGC Chemicals Europe, 9 wt.%) was investigated as insulating spacer between the vertically aligned source and drain electrodes. CYTOP was chosen because it is unaffected by all successive fabrication steps due to its orthogonal solubility to all solvents further used. CYTOP was diluted with perfluorotrialkylamine (CT-Solv 180, AGC Chemicals Europe) and stirred for at least 10 min at 500 r.p.m.. In a next step, the solution was spin coated on the substrate with pre-fabricated bottom electrodes for 10 sec at 500 r.p.m. followed by 30 sec at 1500 r.p.m.. Now the sample was first baked in a vacuum oven (Mettert VO 200) at 10 mbar for 15 min at 50 °C in order to remove remaining bubbles, followed by 45 min at 80 °C to remove remaining solvent and finally for 45 min at 200 °C to improve the adhesion to the substrate and to planarize the CYTOP film. In order to increase the wettability of CYTOP (contact angle ~ 110°<sup>113</sup>) and to ensure the adhesion to subsequent layers, a metallic surface treatment was applied (see Figure 3.3) prior to PMMA deposition for top-contact fabrication (see section 3.2). Evaporating a covering aluminum layer of at least 20 nm and subsequent wet etching of aluminum via a buffered NaOH solution (AZ 351B, Microchemicals) results in oriented end-groups towards the polymer surface with a reduced contact angle of 80°<sup>113</sup>. It has to be noted that this whole process is reversible and the hydrophobicity is restored by heating the CYTOP layer above 100 °C<sup>114</sup>. After top contact patterning, CYTOP was first removed anisotropically using RIE with a RF power of 50 W, IPC power of 70 W, a O<sub>2</sub> flow of 20 sccm and a pressure of 20 mTorr (see Figure 3.3 e)). The etching time was chosen according to the etching rate (0.3 nm s<sup>-1</sup> for the given setup and etching parameters) and the CYTOP thickness. The thickness defines the channel length  $L_{ch}$  and can be adjusted by varying the CYTOP concentration. To form the underetched top contact with the underetched distance  $d_c$  (see publication A1 and A3), CYTOP is

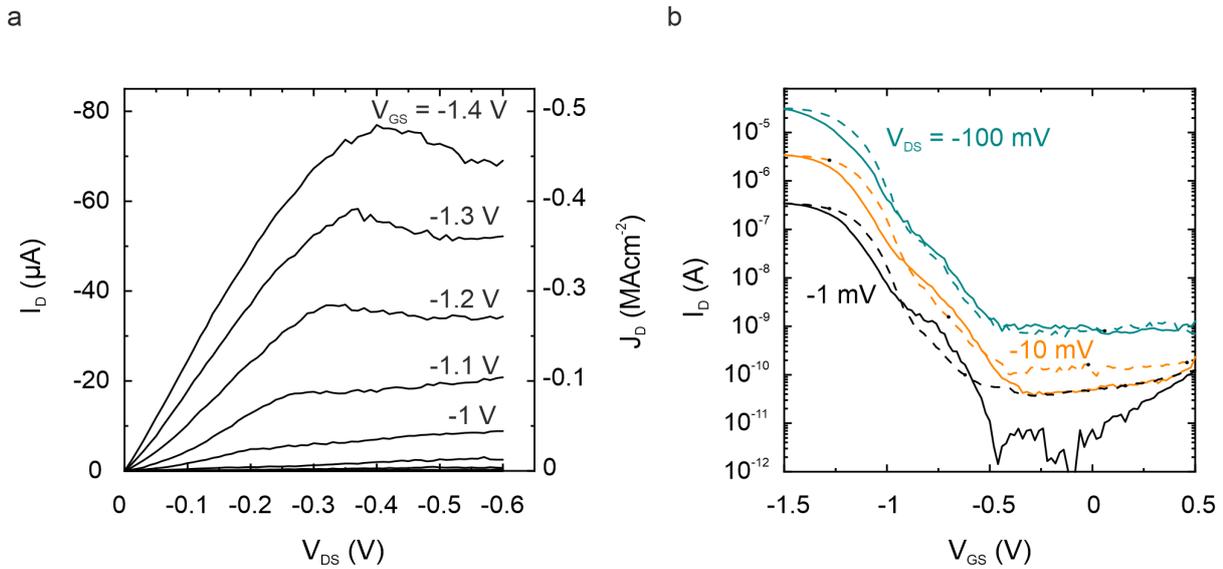
## 4 VOFETs



**Figure 3.3 Schematic VOFET fabrication process with CYTOP as insulator.** a) CYTOP (blue) is deposited on the substrate with pre-fabricated bottom electrodes. b) Evaporation of a thin Al layer (grey). c) Etching of aluminum with buffered NaOH solution resulting in a more hydrophilic surface due to oriented end-groups of the polymer (dark blue). Now the PMMA resist can be spin coated for the top electrode fabrication via electron beam lithography. After top contact patterning in d), CYTOP is e) first etched anisotropically via RIE and f) etched isotropically to form an underetched top contact.

etched isotropically using a plasma asher (Giga-Etch 100-E) with a power of 200 W and 1.2 torr O<sub>2</sub> (etching rate 2.17 nm min<sup>-1</sup>). From here the finalization of electrolyte-gated VOFETs is identical to publications A1 and A3, both attached as full text in appendix A. Although the current density of up to 450 kA cm<sup>-2</sup> is almost one order of magnitude lower, the electrical characteristics in Figure 3.5 exhibit comparable device performance as with SiO<sub>2</sub> or hBN as insulating spacer with fully saturating output currents. Here a concentration of 22.44 wt.% CTL 809-M in CT-Solv 180 resulted in a layer thickness of 60 nm measured via ellipsometry (Plasmos PC 2300). Analogous to hBN (publication A3), the smaller current density might be explained by an only partial OSC channel filling due to the high restored hydrophobicity (150 °C PMMA soft-bake for top contact patterning, see section 3.2) and hence poor wettability during OSC deposition. This issue could be solved by an additional aluminum treatment prior to OSC deposition or by choosing low surface-tension solvents with optimized wettability as e.g methanol or hexane. The negative differential resistance for high V<sub>GS</sub> in the output characteristics in Figure 3.5 a) has also been observed when using hBN as insulating spacer (publication A3). This can be attributed to a peak like behavior of the conductivity versus V<sub>GS</sub> when using electrolyte gates<sup>115,116</sup>. As for all electrolyte-gated VOFETs, DIBL as a short-channel effect was observed by a V<sub>DS</sub> dependent shift of V<sub>th</sub> in the transfer characteristics in Figure 3.5 b). When increasing V<sub>DS</sub>, also the off current increases (see V<sub>DS</sub> = -100 mV), which can be explained by an increasing electrical field and hence increasing leakage current through CYTOP.

## 4.2 MDMO-PPV as active material

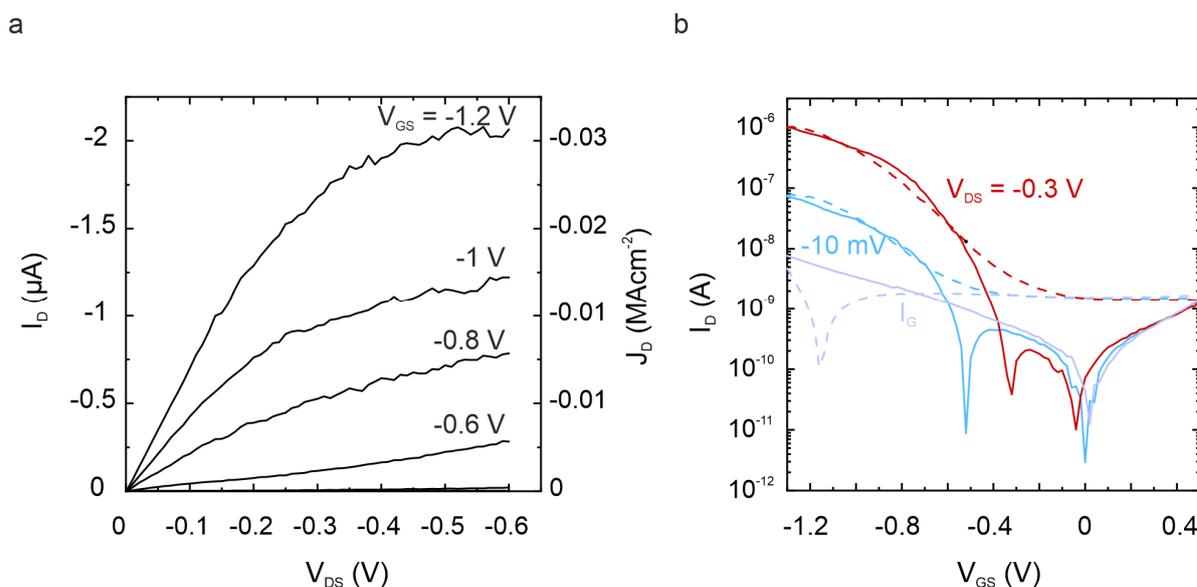


**Figure 3.5** Electrical characteristics of [EMIM][TFSI] gated PDPP VOFETs and CYTOP as insulator. a) Output ( $V_{DS}$  sweep rate  $20 \text{ mV s}^{-1}$ ) and b) transfer characteristics ( $V_{GS}$  sweep rate  $23 \text{ mV s}^{-1}$ ) with  $w_{bel} = 80 \text{ nm}$ ,  $d_c = 100 \text{ nm}$  and  $L_{ch} = 60 \text{ nm}$ . The solid lines represent the forward and the dashed lines the backwards sweep direction.

## 4.2 MDMO-PPV as active material

In publication A1 and A3, both attached as full text in appendix A, poly(diketopyrrolopyrrole-terthiophene) (PDPP) and poly(3-hexylthiophene) (P3HT) were used to fabricate electrolyte-gated VOFETs. Additionally the same device geometry was used with the polymer Poly-[5-(3',7'-dimethyloctyloxy)-2-methoxy-1,4-phenylvinylene] (MDMO-PPV, Sigma Aldrich). The fabrication was exactly the same except a  $5 \text{ mg ml}^{-1}$  MDMO-PPV in 1,3-meta-dichlorobenzene (MDCB) solution was spin coated for 40 sec at 800 r.p.m. and a ramp of 800 r.p.m.  $s^{-2}$ . The electrical characteristics in Figure 3.6 reveal saturating output curves with current densities of up to  $30 \text{ kA cm}^{-2}$  and on-off ratios of up to  $10^4$  at  $-0.3 \text{ V}$  bias operation. MDMO-PPV devices were not fabricated to investigate the upper current-density limit and should rather be seen as a proof of principle that the functionality of electrolyte-gated VOFETs is not limited to specific types of polymers. However, the lower device performance compared to [EMIM][TFSI]-gated PDPP and P3HT devices with mobilities of up to  $\mu_{PDPP} = 3 \text{ cm}^2 \text{ V}^{-1} \text{ S}^{-1}$  and  $\mu_{P3HT} = 1.1 \text{ cm}^2 \text{ V}^{-1} \text{ S}^{-1}$  is probably related to the lower intrinsic mobility of MDMO-PPV in the  $10^{-5} \text{ cm}^2 \text{ V}^{-1} \text{ S}^{-1}$  regime<sup>117</sup>. As for PDPP and P3HT, also for MDMO-PPV DIBL in the transfer characteristics (Figure 3.6 b)) could be observed.

## 4 VOFETs



**Figure 3.6 Electrical characteristics of electrolyte-gated MDMO-PPV VOFETs.** a) Output ( $V_{DS}$  sweep rate  $20 \text{ mV s}^{-1}$ ) and b) transfer characteristics ( $V_{GS}$  sweep rate  $41 \text{ mV s}^{-1}$ ) with  $w_{bel} = 110 \text{ nm}$ ,  $d_c = 35 \text{ nm}$  and  $L_{ch} = 40 \text{ nm}$ . The solid lines represent the forward and the dashed lines the backwards sweep direction.

To conclude, electrolyte-gated VOFETs have been fabricated in the course of this thesis using three different insulators SiO<sub>2</sub>, hBN and CYTOP as spacer between the vertical electrodes. Additionally three different OSCs PDPP, P3HT and MDMO-PPV have been used as active material. These results elucidate the flexible field of application of the developed geometry for nanoscale organic high-performance transistors. The presented device geometry is neither limited to the insulating spacer nor to a specific type of polymeric semiconductor.

# 5 Single polymer fiber transistors

*Reducing the dimensions of organic transistors could pave the way to investigate intrachain charge transport mechanisms along the polymer backbone. Charge transport at different length scales in polymeric OSCs as well as the huge potential of intrachain charge transport has been addressed in the manuscript M1. The full article can be found in section 2.7. Within this thesis, single polymer fiber transistors were realized using a local hybrid  $Al_2O_3$ /TDPA gate dielectric as well as an hBN gate. The detailed fabrication steps can be found in appendix C.1.*

## 5.1 Introduction

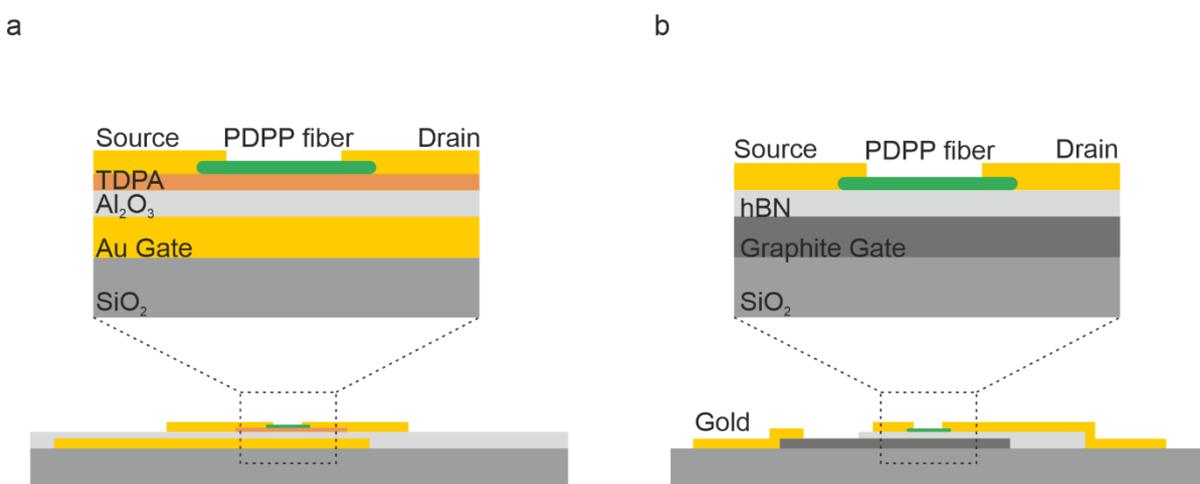
The deposition of a sub-monolayer thin film of the donor-acceptor polymer PDPP, provided by BASF SE, with distinguishable single fibers is demonstrated in publication A1. This approach built the basis for the fabrication of single PDPP fiber transistors. To realize transistors with channel lengths in the sub-100 nm regime, special care has to be taken to maintain a sufficient gate coupling and to stay within the gradual channel approximation (see section 2.2). This can be realized by decreasing the gate thickness and by using high-k gate oxides such as  $Al_2O_3$  ( $\epsilon = 9$ <sup>118</sup>) (see equation 2.1). However, reducing the dielectric thickness is automatically accompanied with increased leakage currents and small breakdown voltages, which can be prevented by the utilization of self-assembled monolayers (SAM) in hybrid oxide/SAM gate dielectrics. The chemical modification of the oxide surface results in a passivation of the gate-oxide due to the high packing density of the formed SAM. The improved electrical characteristics with a reduction of traps at the oxide OSC interface, reduced leakage currents and the tunability of  $V_{th}$  has been widely investigated<sup>119–122</sup>.

To investigate charge transport behavior at the nanoscale, single PDPP fiber transistors were fabricated according to section 3.4 with a local hybrid  $Al_2O_3$ /TDPA gate dielectric as depicted in Figure 5.1 a). For a sputtered  $Al_2O_3$  layer of 10 nm thickness with an experimentally measured dielectric constant of  $\sim 7$ <sup>123</sup>, a TDPA thickness of  $1.74$  nm<sup>124</sup> and a dielectric constant of  $\epsilon_{TDPA} = 2.5$ <sup>119</sup>, the total unit-area gate capacitance  $\hat{C}_{tot}$  can be calculated using equation 2.1 and

$$\frac{1}{\hat{C}_{tot}} = \frac{1}{\hat{C}_{Al_2O_3}} + \frac{1}{\hat{C}_{TDPA}}, \quad (5.1)$$

yielding  $\hat{C}_{tot} = 0.42 \mu F cm^{-2}$ .

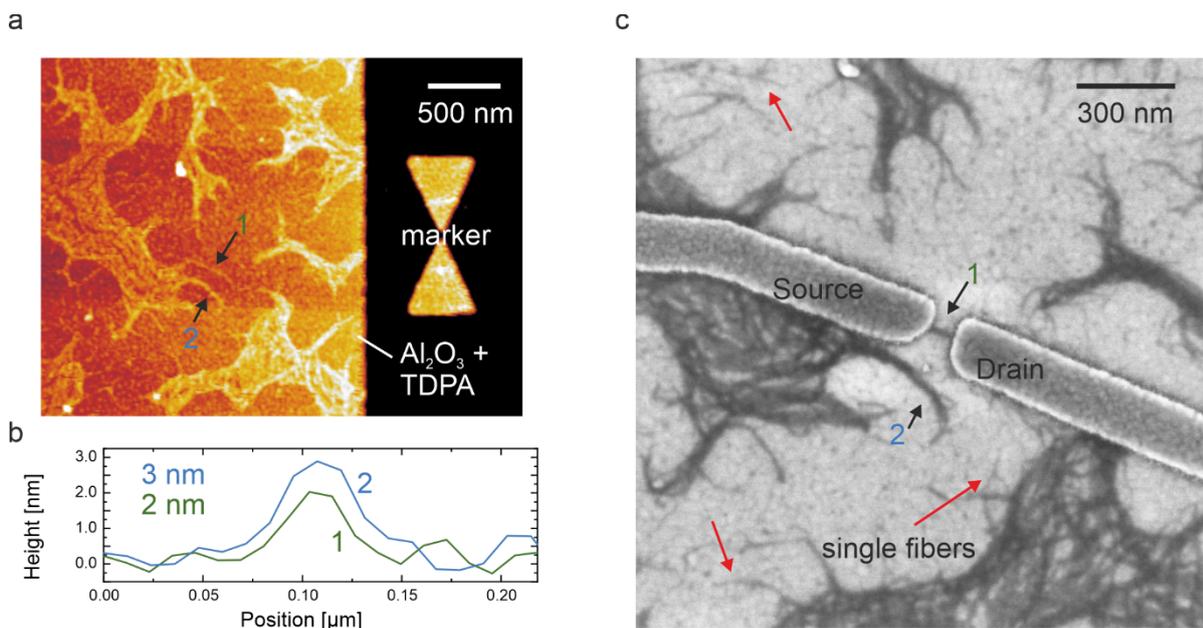
## 5 Single polymer fiber transistors



**Figure 5.1** Schematic illustration of the device geometry of single PDPP fiber transistors. *a, b*) Single PDPP fiber transistor with an  $\text{Al}_2\text{O}_3/\text{TDPA}$  gate (*a*) and a graphite/hBN gate configuration (*b*).

In the field of two-dimensional (2D) materials, using hBN both as a dielectric substrate or to completely encapsulate graphene has shown to drastically increase the electrical characteristics in terms of mobility and charge disorder<sup>125–127</sup>. hBN is an insulating 2D material with a band gap of  $\Delta = 5.97 \text{ eV}$ , high breakdown voltages ranging from  $0.8$ <sup>128</sup> to  $1.2 \text{ V nm}^{-1}$ <sup>129</sup> and a dielectric constant of  $\epsilon \approx 3 - 4$ <sup>125</sup>. The improved device performance is mainly related to a reduction of surface charge traps<sup>125</sup>. Additionally to the hybrid  $\text{Al}_2\text{O}_3/\text{TDPA}$  gate, single PDPP fiber transistors were also realized using hBN as a dielectric (depicted in Figure 5.1 b)). In order to maintain the atomically flatness of hBN, graphite consisting of several graphene layers was used instead of gold as gate electrode. The graphite was contacted with an additional gold electrode (see Figure 5.1 b)). The unit-area capacity for graphite/hBN samples is calculated according to equation 2.1 with the specific hBN thicknesses measured via atomic force microscopy (AFM).

An example of a single PDPP fiber transistor with an  $\text{Al}_2\text{O}_3/\text{TDPA}$  gate dielectric can be seen in Figure 5.2. The AFM image shows both single fibers as well as larger fiber networks. Line traces of two different fibers reveal heights of  $2 \text{ nm}$  and  $3 \text{ nm}$ , respectively, which already indicates that the term “single fiber” does not refer to single polymer molecules. This is also confirmed in the SEM image where even smaller fibers that are not resolvable using AFM become visible (highlighted by red arrows). Within this thesis the phrase “single fiber” refers to individual fibers consisting of several well aligned parallel polymer molecules. A finished device where a single fiber is contacted with electrodes can be seen in the SEM image in Figure 5.2 c). Although a comparison of the AFM image after fiber deposition and the SEM image after contact patterning indicates that PDPP is not affected by the electron beam lithography process (PMMA deposition,  $120 \text{ }^\circ\text{C}$  soft bake, lift-off in acetone and isopropanol) (see section 3.2), small damage or conformational changes cannot be fully excluded. It

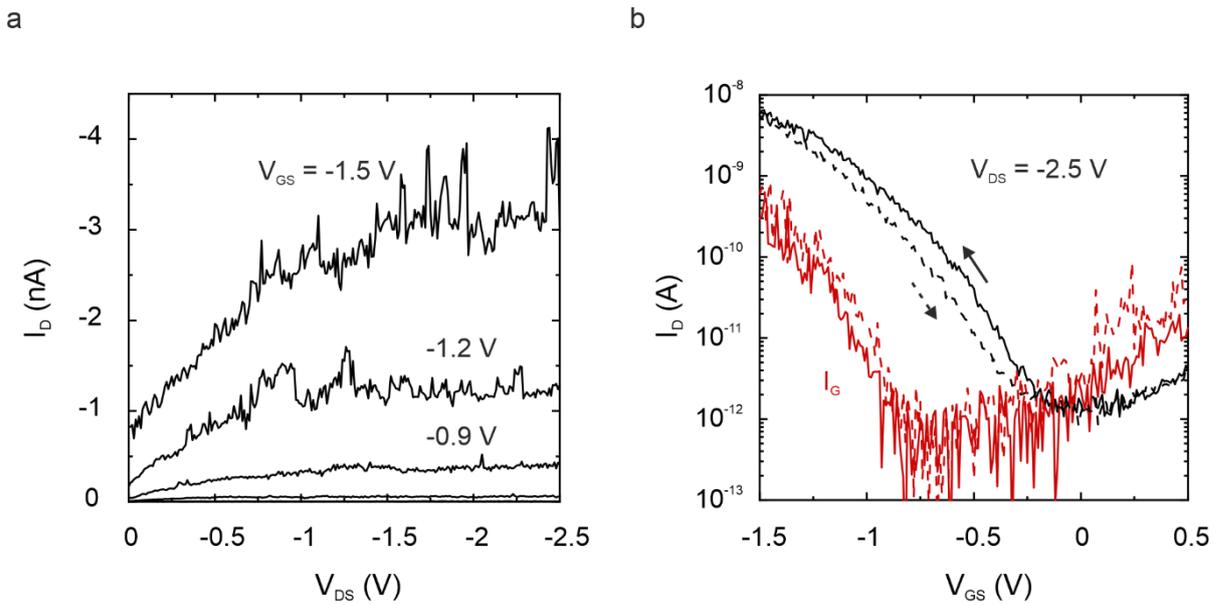


**Figure 5.2 Single PDPP fiber transistor with a local  $\text{Al}_2\text{O}_3/\text{TDPA}$  gate.** a) AFM image of PDPP fibers deposited on  $\text{Al}_2\text{O}_3/\text{TDPA}$ . b) Line traces across two different fibers reveal thicknesses of 2 nm and 3 nm. c) SEM image of the same region of an electrically contacted fiber exhibit fibers that are not resolvable with AFM (indicated by red arrows).

has to be noted that when measuring single polymer-fiber transistors, the device performance is not an average measure as in macroscopic devices. Small variations in the fiber composition in terms of the number, packing and alignment of single polymer molecules within the fiber as well as the electrical contacts lead to different results, which in turn makes a device comparison difficult. Additionally, a comparison between the two gate configurations is also questionable as different surface energies (defined by different contact angles of  $115^\circ$  for TDPA<sup>130</sup> and  $135^\circ$ <sup>131</sup> for hBN) might lead to different fiber compositions during the growing process.

The results of single PDPP fiber transistors with both presented gate configurations is organized as follows: At first room temperature measurements in vacuum are presented. The next section is focused on temperature dependent measurements and in the last part Coulomb-blockade oscillations at low temperatures are discussed. In total three hBN/graphite gate devices (sample H1-3) and two  $\text{Al}_2\text{O}_3/\text{TDPA}$  gate devices (sample A1, A2) have been investigated. Due to thermal coupling problems in the Lakeshore CRX-VF probe station between the chuck and the sample, the adjusted temperatures for H1, H3, and A1 are not expected to be actually reached exactly. At elevated temperatures above 100 K, when connecting the cool probe arms to the transistors electrodes resulted in an offset of up to -50 K. However, qualitative interpretations when cooling down from 300 K to base temperature ( $\sim 5$  K) are still valid. Sample H2 and A2 have been thermally coupled with

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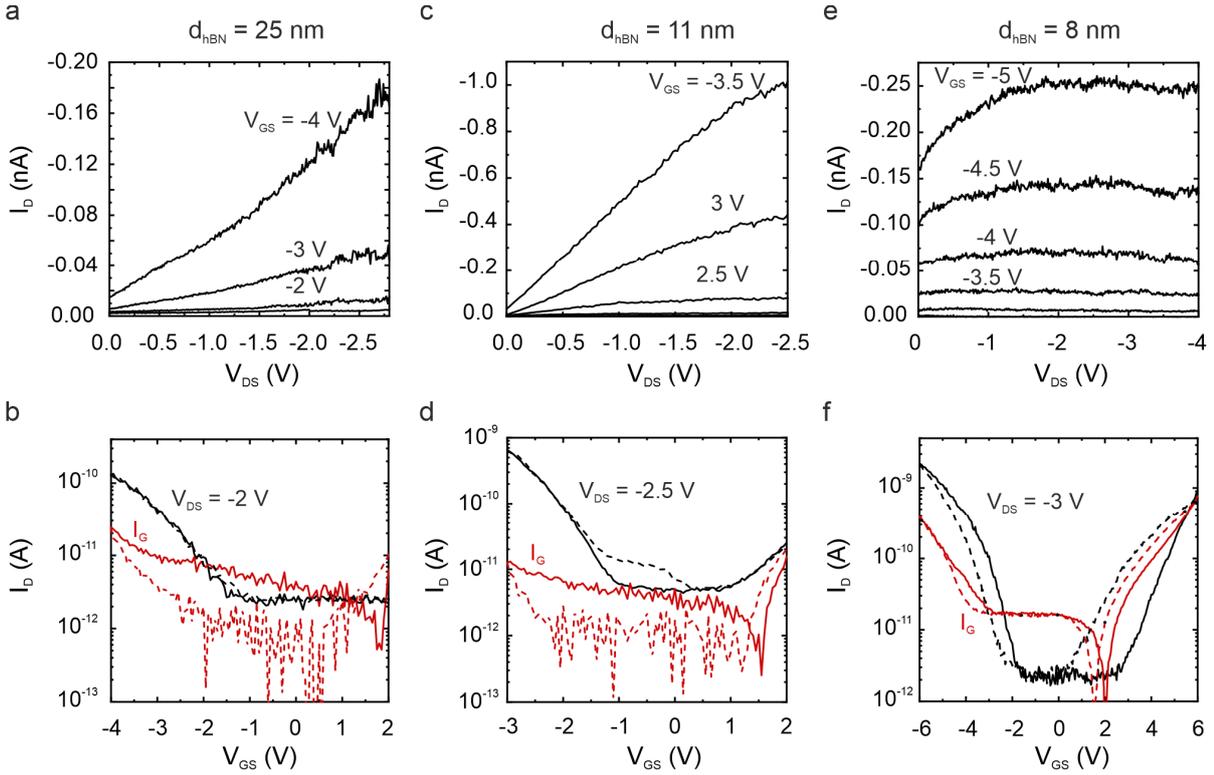
**Figure 5.3** Electrical characteristics of a single PDPP fiber transistor with an  $\text{Al}_2\text{O}_3/\text{TDPA}$  gate (sample A2) and a channel length of  $L_{ch} = 56$  nm ( $T = 300$  K,  $p = 1.6 \times 10^{-7}$  mbar). a) Output and b) transfer characteristics in the saturation regime (black) with corresponding gate current  $I_G$  (red). The solid lines represent the forward and the dashed lines the backwards sweep direction.

silver conducting paste, resulting in a maximum temperature offset of 2K.

### 5.2 Room temperature electrical characteristics

The electrical characteristics of a single PDPP fiber transistor with a local  $\text{Al}_2\text{O}_3/\text{TDPA}$  gate (sample A2) measured at 300 K are shown in Figure 5.3. Despite a channel length of only 56 nm, the output curves exhibit fully saturating currents. The increasing offset in the output characteristics for  $V_{DS} = 0$  V are related to an increasing gate-leakage current for higher  $V_{GS}$ . The saturation transfer characteristics reveal an on-off ratio of 6000 and a subthreshold swing of  $250$  mV  $\text{dec}^{-1}$  with a threshold voltage of  $V_{th} = -0.89$  V. The  $V_{GS}$  and hence carrier-density-independent mobility according to equation 2.8 of  $\mu_{sat} = 6.88 \times 10^{-1}$   $\text{cm}^2$   $\text{V}^{-1}$   $\text{s}^{-1}$  for an assumed channel width of  $W = 3$  nm is still a factor of 5 lower compared to a macroscopic device with a channel length of 200  $\mu\text{m}$ <sup>132</sup>. It has to be noted that for some devices the influence of the gate current at room temperature is dominating the source drain current. Also some devices do not show a saturation behavior in the output characteristics. This demonstrates the individuality of single fibers, whereby small deviations in the fiber composition or the gate coupling strongly influences the electrical characteristics. Figure 5.4 shows the electrical performance of single PDPP fiber transistors with varying hBN thicknesses, where a-d) refer to sample H2 and e,d) to sample H3. For the  $d_{hBN} = 25$  nm transistor with  $L_{ch} = 40$  nm, the

## 5.2 Room temperature electrical characteristics



**Figure 5.4 Electrical characteristics of single PDPP fiber transistors with a hBN/graphite gate and varying hBN thicknesses.** a,b) Output and transfer characteristics (black) with corresponding gate current  $I_G$  (red) measured at  $T = 296$  K and  $p = 1.7 \times 10^{-7}$  mbar on region 1 ( $d_{hBN} = 25$  nm) and c,d) on region 2 ( $d_{hBN} = 11$  nm) of sample H2 (see appendix C.1). e,f) Electrical characteristics of sample H3 with a gate thickness of  $d_{hBN} = 8$  nm measured at  $p = 4.5 \times 10^{-5}$ . The real sample temperature due to poor thermal coupling is  $T_{real} \approx 250$  K. The solid lines represent the forward and the dashed lines the backwards sweep direction.

output current exhibits no saturation behavior above the pinch-off point. This is a known effect for short-channel length devices and can be attributed to an insufficient transversal electric field compared to the longitudinal drain-source field<sup>33</sup> (see section 2.3). For another transistor on the same sample but different hBN region with  $d_{hBN} = 11$  nm the output curves start to saturate despite a shorter channel length of  $L_{ch} = 25$  nm, which indicates the transition to a sufficient gate coupling and the applicability of the gradual channel approximation. The different regions 1 and 2 of sample H2 can be seen in Figure C.3 in appendix C.1. Decreasing the gate thickness further to  $d_{hBN} = 8$  nm in sample H3 ( $L_{ch} = 67$  nm) results in fully saturating output currents. As the mobility exhibits no carrier-density-independent region, no meaningful values can be calculated for sample H2<sup>30</sup>. The mobility calculated with the transfer curve in Figure 5.4 f) is  $\mu_{sat} = 3.72 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ .

In summary, these results indicate that the realization of single polymer fiber transistors with nanoscopic device dimensions is possible. However, the device performance by reducing the channel length and potentially reaching the intrachain charge transport regime does not surpass the

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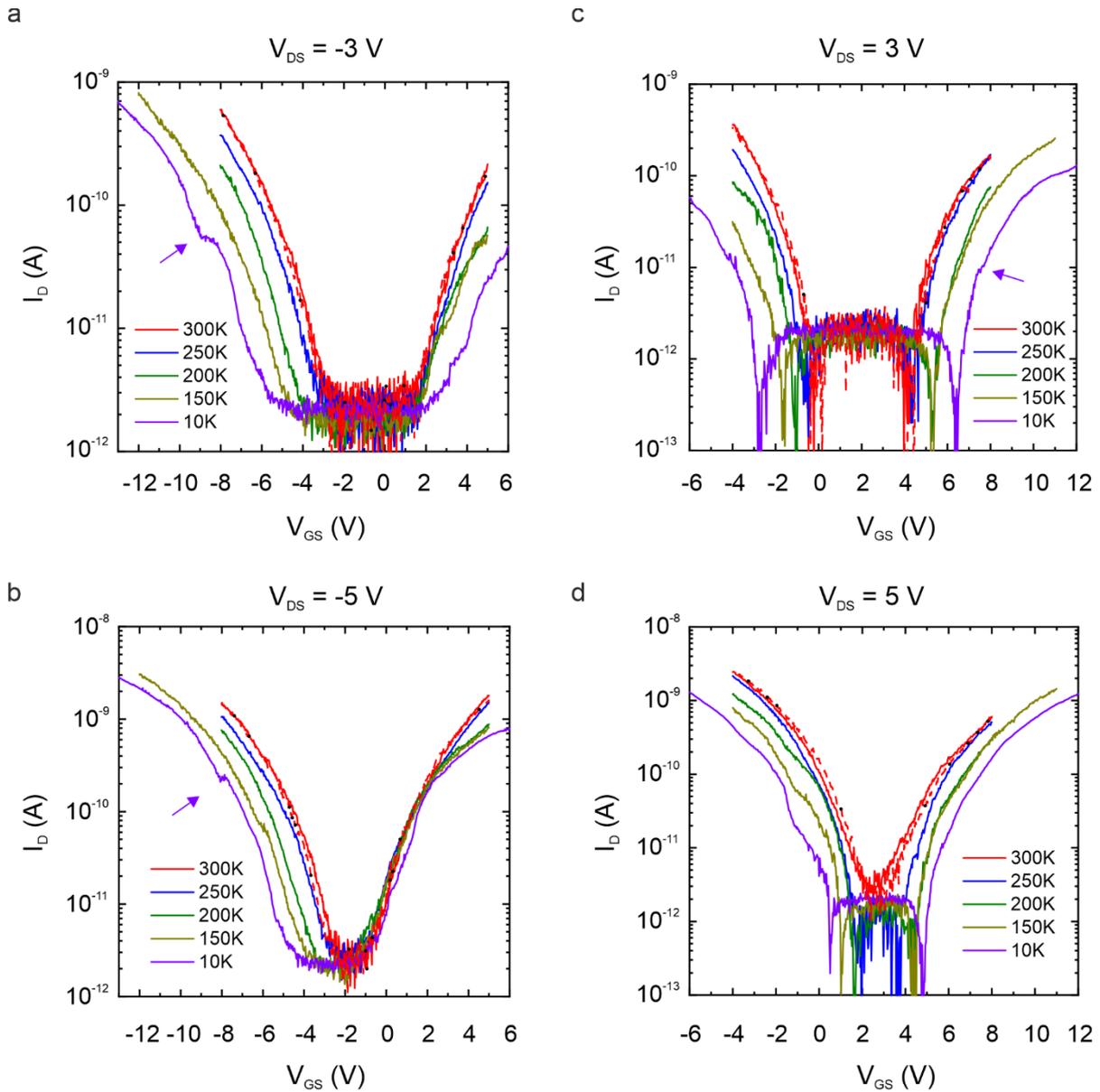
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performance of macroscopic devices yet. As can be seen even for channel lengths down to  $L_{ch} = 25 \text{ nm}$ , comparably large  $V_{DS}$  values need to be applied to reach the saturation regime. This might indicate that these devices suffer from large contact resistances. However, so far no meaningful method to reliably evaluate contact resistances of single polymer fibers could be found. As the PDPP fibers exhibit maximum lengths of  $\sim 300 \text{ nm}$ , the gated four-point probe method to evaluate contact resistances, which would require two additional electrodes small enough to not influence the potential in the channel<sup>31</sup>, is not realizable. The transfer-line method could in principle be applied for different fibers. However, it turned out that the varying performance of individual fibers dominated the necessary linear relation of the total channel width-normalized resistance to the channel length. Another reason for the poorer performance compared to macroscopic devices could be the last lithography process including the contact of the polymer fibers with several organic solvents (see the fabrication steps in appendix C.1). The potential influence of different solvents on PDPP might be investigated in future experiments by comparing X-ray diffraction measurements in addition to electrical measurements prior and after solvent exposure of a macroscopic monolayer film.

### 5.3 Temperature dependent electrical characteristics

A commonly used method to differentiate between charge transport mechanisms in OSCs is to measure the temperature dependence of the mobility (see manuscript M1 for more details). Figure 5.5 shows the transfer characteristics of a single PDPP fiber transistor with an hBN/graphite (sample H1) as a function of temperature. As already explained above, the poor thermal coupling results in a decreasing offset of  $\Delta T \approx -50 \text{ K}$  for a set point temperature of  $T_{set} = 300 \text{ K}$  to an offset of  $\Delta T \approx 5 \text{ K}$  for  $T_{set} = 10 \text{ K}$ . However the qualitative temperature-dependent results in Figure 5.5 are still valid. With decreasing temperature the threshold voltage  $V_{th}$  shifts to more negative values for  $V_{GS} < 0$  and to more positive values for  $V_{GS} > 0$ , which can be explained by the filling of shallow and deep trap states<sup>133,134</sup>. With decreasing temperature, the thermal energy of charge carriers decreases and larger  $|V_{DS}|$  values are required to remobilize trapped charges. A decreasing gate current  $I_G$  for decreasing temperatures renders it possible to increase the  $V_{GS}$  sweep range for lower temperatures. Interestingly, when using hBN as a gate dielectric, ambipolar charge transport could be observed. One of the major requirements that has to be ensured to realize ambipolar charge transport in OFETs is a trap-free gate dielectric<sup>24,135</sup>. The observation of ambipolar transport elucidates the high potential of using hBN as a gate dielectric not only in the field of 2D materials<sup>125</sup> but also for OFETs. This becomes even clearer as the same behavior was not observed for  $\text{Al}_2\text{O}_3/\text{TDPA}$  gate dielectrics. Although it is well established that the electron trap density of  $\text{Al}_2\text{O}_3$  is much higher compared to e.g.  $\text{SiO}_2$ <sup>136</sup>, the passivation with phosphonic acid SAMs leads to a reduction of traps at the oxide surface<sup>119</sup> with improved electron conduction<sup>137</sup>. However the threshold voltage to achieve electron conduction for  $\text{Al}_2\text{O}_3/\text{TDPA}$  gates could not be reached due to the priorly occurring dielectric

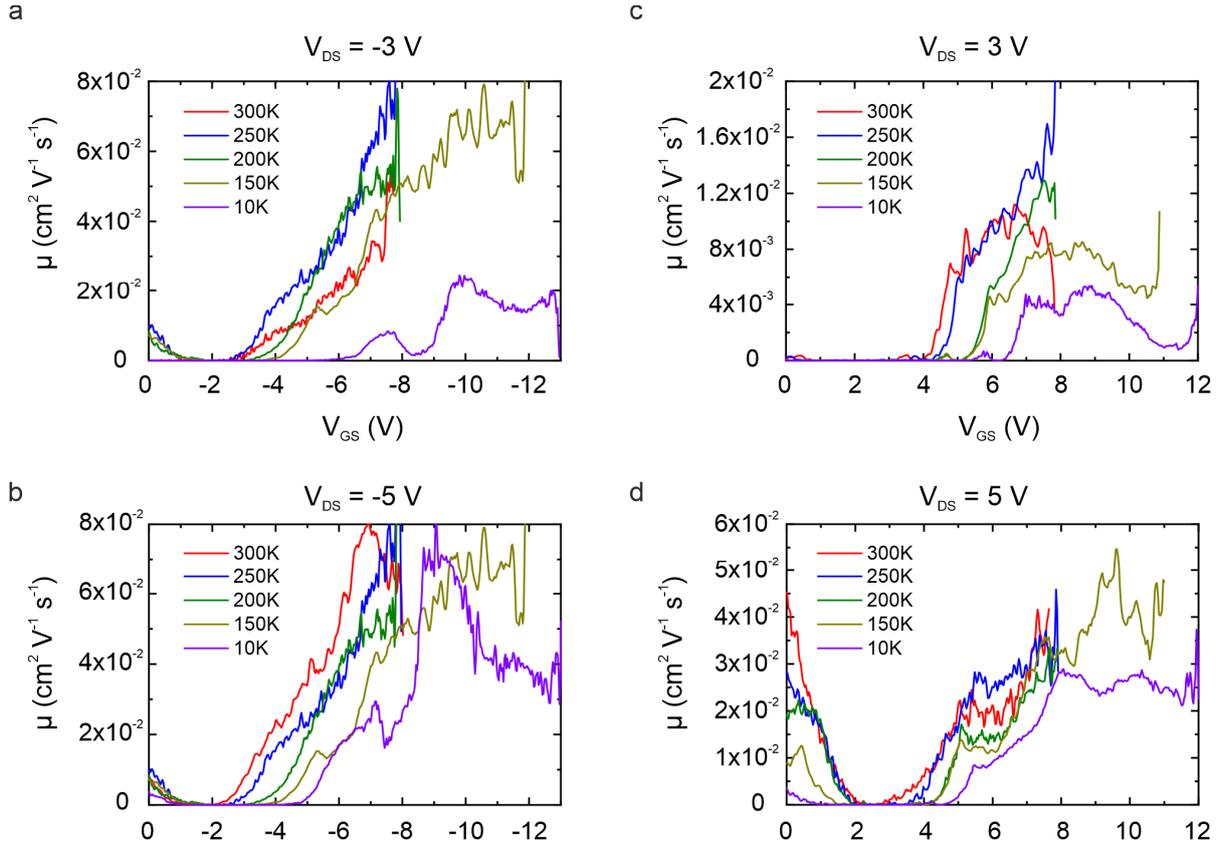
## 5.3 Temperature dependent electrical characteristics



**Figure 5.5** Transfer characteristics of a single PDPP fiber transistor with a hBN/graphite (sample H1,  $d_{\text{hBN}} = 25 \text{ nm}$ ) for varying temperatures ( $p = 1.6 \times 10^{-7} \text{ mbar}$ ). a, b) p-type transfer characteristics for  $V_{\text{DS}} = -3 \text{ V}$  and  $V_{\text{DS}} = -5 \text{ V}$  and c,d) n-type transfer characteristics for  $V_{\text{DS}} = 3 \text{ V}$  and  $V_{\text{DS}} = 5 \text{ V}$ . Due to poor thermal coupling the given temperatures are not the real sample temperatures. The qualitative temperature behavior is still valid. For the curves at  $T_{\text{set}} = 300 \text{ K}$ , the backwards sweep is plotted with red dashed lines.

breakdown. Another evidence for the high quality of both hBN and  $\text{Al}_2\text{O}_3/\text{TDPA}$  gate dielectrics is the absence of a noteworthy hysteresis between forward and backwards  $V_{\text{GS}}$  sweeps. Although some devices exhibit a small hysteresis at room temperature (see Figures 5.3 and 5.4), it almost fully disappears for lower temperatures. In Figure 5.5, this absence of hysteresis is indicated for a realistic

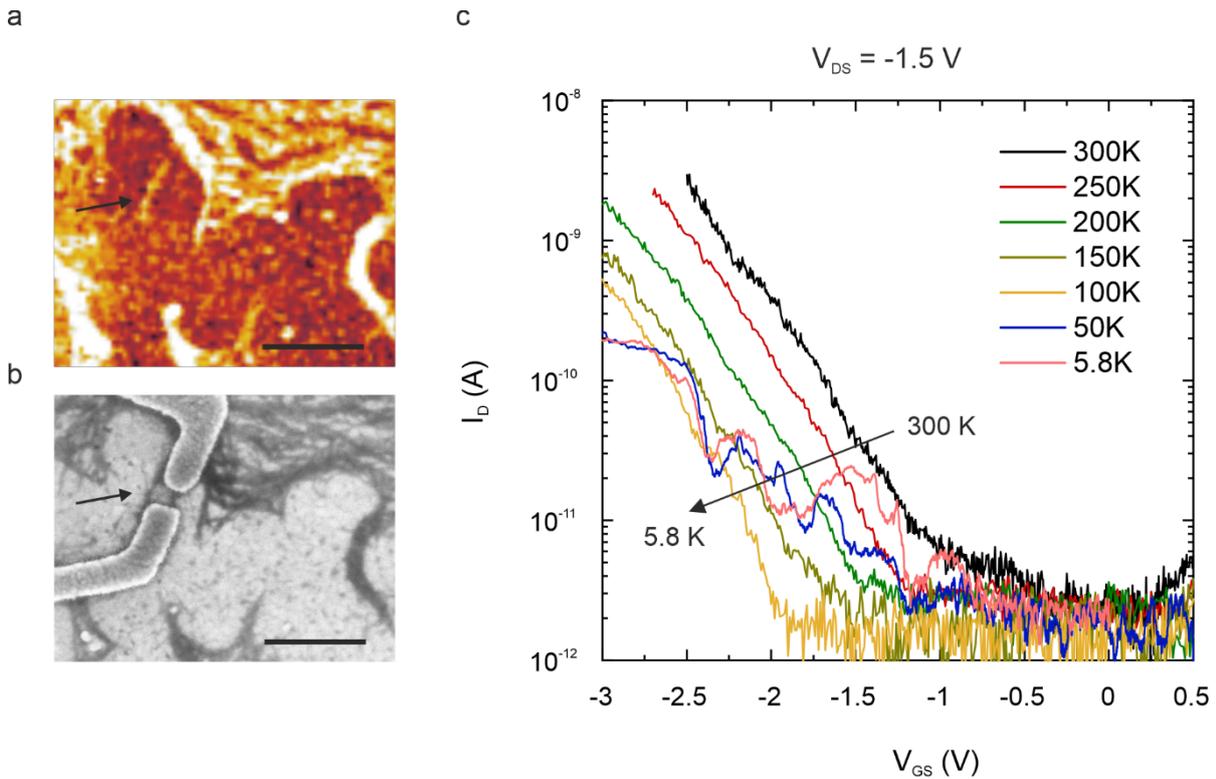
## 5 Single polymer fiber transistors



**Figure 5.6 Temperature dependent mobility with respect to  $V_{GS}$  of the graphs in Figure 5.5 (sample H1).** a, b) p-type for  $V_{DS} = -3$  V and  $V_{DS} = -5$  V and c, d) n-type for  $V_{DS} = 3$  V and  $V_{DS} = 5$  V. Due to poor thermal coupling the given temperatures are not the real sample temperatures. The qualitative temperature behavior is still valid.

temperature of  $T_{real} = 250$  K ( $T_{set} = 300$  K, red curve). When cooling down, the transfer characteristics starts to deviate from the behavior at elevated temperature with the formation of plateaus (see  $T_{set} = 10$  K, highlighted by violet arrows in Figure 5.5), which will be explained in more detail at later parts. Unfortunately, the device of Figure 5.5 was destroyed due to electrostatic discharge in the final stages of the measurements and the exact channel lengths could not be measured. To estimate the mobility, the width of the specific fiber transistor was extracted from a previously measured AFM image ( $W = 1.8$  nm) and a channel length of  $L_{ch} = 80$  nm from the electron beam lithography design was used. According to equation 2.8 with  $d_{hBN} = 25$  nm, the temperature dependent mobility extracted from the data in Figure 5.5 is shown in Figure 5.6. Except for  $V_{DS} = -3$  V at elevated temperatures, all curves in the p-type ( $V_{GS}$  and  $V_{DS} < 0$ ) and in the n-type mode ( $V_{GS}$  and  $V_{DS} > 0$ ) exhibit a charge-carrier density-independent mobility region. Although the mobility for  $V_{DS} = \pm 3$  V is decreasing with decreasing temperature, it remains almost constant for higher  $V_{DS} = \pm 5$  V. These results without the indication of a thermally activated transport for high  $V_{DS}$  can be regarded as a first hint towards band-like

## 5.3 Temperature dependent electrical characteristics



**Figure 5.7** Transfer characteristics of a single PDPP fiber transistor with an  $\text{Al}_2\text{O}_3/\text{TDPA}$  gate and  $L_{ch} = 48$  nm (sample A1) for varying temperatures ( $p = 1.9 \times 10^{-7}$  mbar). a) AFM image prior and b) SEM image after contacting a single fiber indicated by the black arrow. The scale bar is 300 nm. c) Transfer characteristics for  $V_{DS} = -1.5$  V for different temperatures with evolving oscillations below  $T_{set} = 100$  K. Due to poor thermal coupling the given temperatures are not the real sample temperatures. The qualitative temperature behavior is still valid.

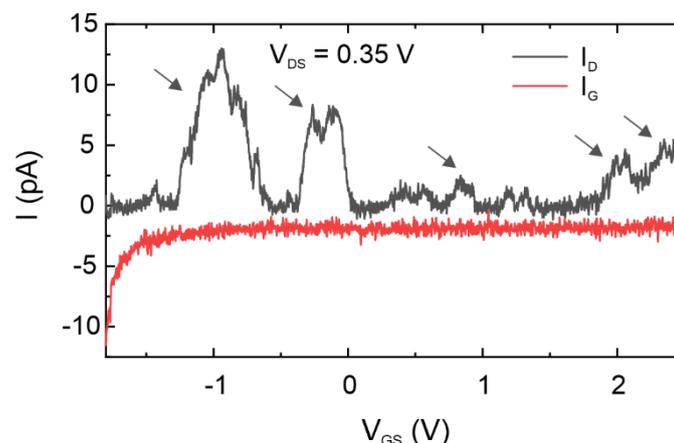
transport along the highly oriented polymer backbone. This temperature independent mobility regime has not been observed for all devices, while some devices showed thermally activated transport with a transport freeze-out at lower temperatures (see Figure C.4 in the appendix. In most scenarios the evolving oscillations at  $T \leq 100$  K, which are also indicated by the plateaus in Figure 5.5 at  $T_{set} = 10$  K, makes temperature dependent mobility investigations very challenging. A much more pronounced emergence of these oscillations can be seen in Figure 5.7. Originally it was aimed to contact the fiber highlighted by the black arrow in the AFM and SEM images. However, in the SEM image a second fiber between the source and drain electrode seems to be present. As this fiber is not observable in the AFM image it cannot be reasonably estimated if this transistor covers two single fibers or if the emerging fiber is either an SEM artefact or dirt residues from the last lithography step. Nevertheless, when cooling down from  $T_{set} = 300$  K to the base temperature of the system  $T_{set} = 5.8$  K, the transport is first forming plateaus starting at  $T_{set} = 100$  K, and then clearly starting to oscillate when decreasing the temperature further. The  $(V_{GS}, V_{DS})$ -current map measured

## 5 Single polymer fiber transistors

at  $T_{set} = 5.8\text{ K}$ , shown in Figure C.5 in the appendix, already indicates the formation of Coulomb blockade with indicated Coulomb Diamonds (see section 2.6).

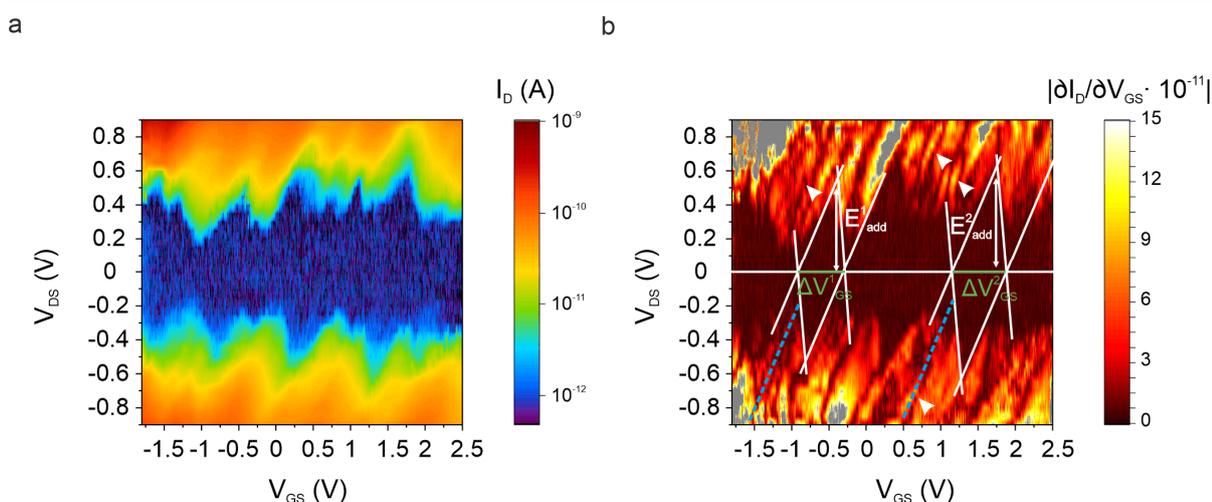
### 5.4 Coulomb blockade oscillations at cryogenic temperatures

In this section, Coulomb blockade oscillations with clearly observable Coulomb blockade diamonds are presented for the first time for single polymer fiber transistors and two different gate configurations. As explained in section 2.6 Coulomb and size-quantization effects can be best investigated at low temperatures. The results presented here have been measured at temperatures between  $5.5\text{ K}$  and  $10\text{ K}$ . The absolute currents within the pA regime are very low. To make sure that the observed results are not influenced or dominated by gate leakage currents, an exemplary measurement at  $V_{DS} = 0.35\text{ V}$  with both the drain (black) and gate (red) current is given in Figure 5.8 for an  $\text{Al}_2\text{O}_3/\text{TDPA}$ -gated single fiber (sample A2). First of all, it can clearly be derived that the gate current noise has no influence on the measured oscillations. In the drain current, several irregularly spaced current peaks with varying amplitudes, highlighted with black arrows, are observable. According to section 2.6, this indicates that either the formed quantum dots are small enough that the splitting energy  $\Delta$  cannot be neglected, or as will be discussed later, the fiber is composed of different sized quantum dots in series. Also a superposition of both effects is possible. Figure 5.9 shows the corresponding current and differential-conductance map as a function of  $V_{GS}$  and  $V_{DS}$ . The current is blocked in the dark blue region (Figure 5.9 a)) in a range of  $|V_{DS}| \lesssim 0.6\text{ V}$ . The clearly visible Coulomb diamonds are irregular and exhibit different sizes and shapes. The differential conductance map shows a superposition of different sized Coulomb diamonds with addition energies ranging from  $E_{add} = 0.56\text{ eV} - 0.63\text{ eV}$ . These values are slightly increased to what has been reported for single



**Figure 5.8 Exemplary transfer characteristic with drain current  $I_D$  (black) and gate current  $I_G$  (red) of a single PDPP fiber transistor on sample A2 measured at  $T = 5.5\text{ K}$  ( $p = 1.7 \times 10^{-7}\text{ mbar}$ ).**

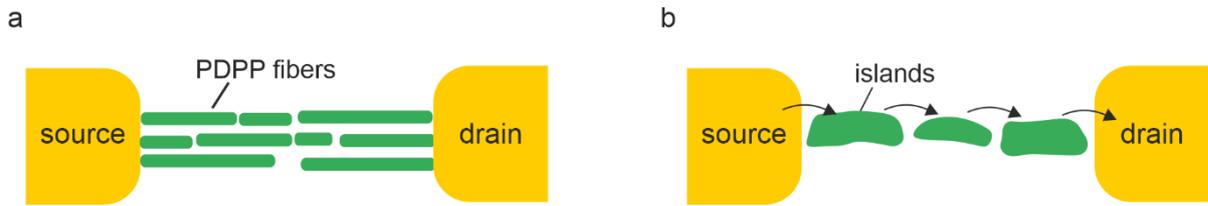
## 5.4 Coulomb blockade oscillations at cryogenic temperatures



**Figure 5.9 Coulomb blockade diamonds of a single PDPP fiber transistor on sample A2 measured at  $T = 5.5 \text{ K}$  ( $p = 1.7 \times 10^{-7} \text{ mbar}$ ).** (a)  $(V_{GS}, V_{DS})$ -current map and (b) differential conductance  $\partial I_D / \partial V_{GS}$  as a function of  $V_{GS}$  and  $V_{DS}$ . Two Coulomb diamonds of different size are indicated by white lines. Excited states are highlighted by white arrows and blue dashed lines.

organic molecule transistors with maximum values of  $0.21 \text{ eV}$ <sup>95</sup> and  $0.39 \text{ eV}$ <sup>96</sup>, which might be explained according to equation 2.9 with a smaller capacitance  $C_x$  of the quantum dot. Using equation 2.9 and 2.10, with  $\Delta V_{GS}^1 = 0.62 \text{ V}$  and  $\Delta V_{GS}^2 = 0.74 \text{ V}$  (extracted from Figure 5.9), the gate coupling factor  $\alpha_{\text{Al}_2\text{O}_3/\text{TDPA}}$  is varying from 0.9 to 0.85 for the different sized Coulomb diamonds. In the differential-conductance map in Figure 5.9 b), various excited states are visible as lines running parallel to the Coulomb diamond edge (see also Figure 2.8 in section 2.6), some of them highlighted by white arrows and blue dashed lines. According to section 2.6, excitation energies varying from  $E_{ex} = 0.17 \text{ eV} - 0.28 \text{ eV}$  can be extracted. For this specific polymer no Raman/IR data could be found in literature. For similar polymers Barszcz et al.<sup>138</sup> identified the CC stretching vibration of thiophene rings at  $\approx 0.173 \text{ eV}$  and the in-phase C=C stretching of the DPP core at  $\approx 0.2 \text{ eV}$ . Similar results has been presented by Adil et al.<sup>139</sup> and Francis et al.<sup>140</sup>. These results compare very well with the electrically measured results in this thesis which proves that excited states can be investigated also for OSCs via charge transport measurements. This could be used to determine excitations that are not detectable with Raman/IR spectroscopy, as has been demonstrated for oligophenylenevinylene-based single molecule junctions<sup>95</sup>. It has to be noted that the excited states are only visible on one side of the Coulomb diamond for positive slopes what is related to asymmetric coupling and hence different tunnel barriers for the source and drain electrode<sup>100,102</sup>. The asymmetric coupling is also verified by the sheared diamonds (see also Figure 2.7 in section 2.6). The different tunnel barriers are schematically shown in Figure C.6 in the appendix. Upon exchanging the source and drain electrodes in two consecutive measurements, the size, shape and position of the Coulomb oscillations changes.

## 5 Single polymer fiber transistors



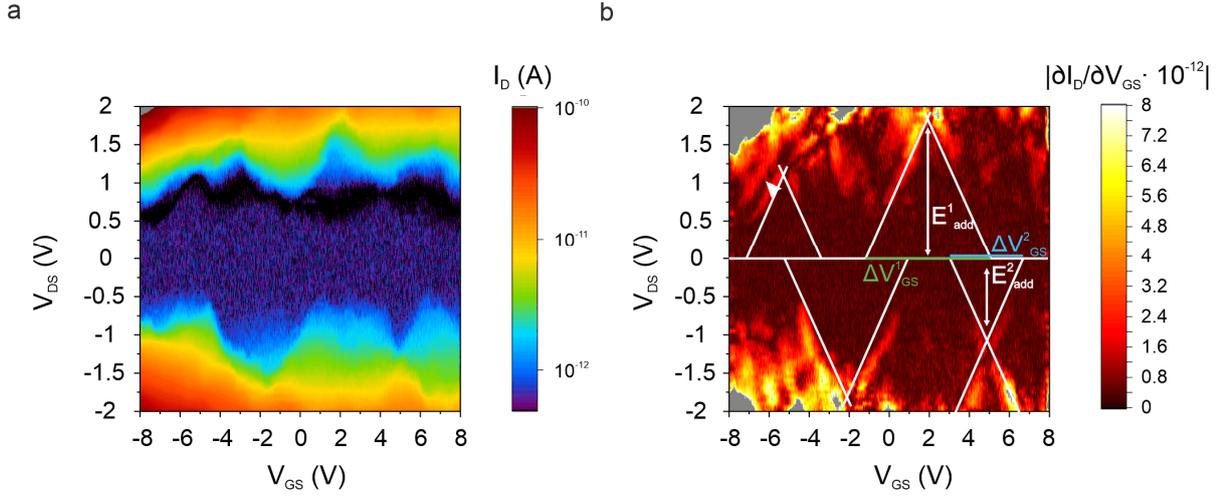
**Figure 5.10 Schematic illustration of single PDPP fiber composition.** a) Possible configuration of single PDPP molecules within a single fiber. b) Schematic representation in the picture of single isolated islands.

Similar results for another measured single PDPP fiber on the same sample can be found in Figure C.7 in the appendix.

In all measurements the Coulomb diamonds are not closed near  $V_{DS} = 0$  V. The occurring gap in addition with different sizes and shapes of the diamonds has been widely investigated<sup>141–145</sup> and is based on an array of single quantum dots with multiple tunnel junctions. Figure 5.10 illustrates a schematic representation with the formation of several quantum dots in a single PDPP fiber. Within a single fiber, composed of several PDPP molecules, several different conduction paths between different molecules are available. In a schematic representation, one path of highest conductance is formed between several islands. These different islands with different capacitances are connected via tunnel barriers. Here, the charge transport is dominated by the junction with the largest barrier within this path of highest conductance. Since individual diamonds are distinguishable in Figure 5.9, the number of conduction paths as well as the number of islands in the channel is very small. Otherwise individual diamonds would be lost due to peak superimposition<sup>145</sup>. A theoretical description of a multigrain system connected via different tunnel barriers can be found in ref.<sup>146</sup>.

In analogy to the  $\text{Al}_2\text{O}_3/\text{TDPA}$  gate, Coulomb and size-quantization effects were investigated for an hBN/graphite gate. The current and differential conductance map as a function auf  $V_{GS}$  and  $V_{DS}$  measured at a temperature of 7 K can be seen in Figure 5.11 for sample H2. Here, the current is blocked in a range of  $|V_{DS}| \lesssim 1$  V in the dark blue region (Figure 5.11 a)). In principle the same behavior as for the  $\text{Al}_2\text{O}_3/\text{TDPA}$  gate in Figure 5.9 with a superposition of different sized and irregular Coulomb diamonds is observable. However, no meaningful explanation why the Coulomb diamonds are less regular and hence only partially visible in the differential conductance map in Figure 5.11 b) could be found yet. The addition energies are varying from  $E_{add} = 1.1$  eV – 1.8 eV and are hence increased compared to what has been observed for the single fiber in Figure 5.9. One possible explanation could be that the different surface energies of hBN and TDPA (defined by different contact angles of  $115^\circ$  for TDPA<sup>130</sup> and  $135^\circ$ <sup>131</sup> for hBN) might lead to different fiber compositions with different sized quantum dots (The larger  $E_{add}$ , the smaller the size of the quantum dot). In order to get more statistics, however, more measurements would be beneficial. With  $\epsilon = 4$  (see section

## 5.4 Coulomb blockade oscillations at cryogenic temperatures



**Figure 5.11 Coulomb blockade diamonds of a single PDPP fiber transistor on sample H2 measured at  $T = 7\text{ K}$  ( $p = 1.6 \times 10^{-7}\text{ mbar}$ ).** ( $V_{GS}, V_{DS}$ )-current map and b) differential conductance  $\partial I_D / \partial V_{GS}$  as a function of  $V_{GS}$  and  $V_{DS}$ . Two different sized Coulomb diamonds are indicated by white dashed lines. Excited states are highlighted by white arrows.

5.1), the capacitance for sample H2 with an hBN thickness of  $25\text{ nm}$  is, according to equation 2.1,  $\hat{C}_{hBN} = 0.14\ \mu\text{F cm}^{-2}$ , which is  $\approx 33\%$  of the capacitance of the  $\text{Al}_2\text{O}_3/\text{TDPA}$  gate ( $\hat{C}_{tot} = 0.42\ \mu\text{F cm}^{-2}$ , see equation 5.1). The gate-coupling factor  $\alpha_{hBN}$  calculates with  $\Delta V^1_{GS} = 6.2\text{ V}$  and  $\Delta V^2_{GS} = 3.6\text{ V}$  to  $0.29$  and  $0.3$ , respectively. Hence, the experimental results for the two different gate configurations with  $\alpha_{hBN} \approx 0.33\ \alpha_{\text{Al}_2\text{O}_3/\text{TDPA}}$  are in very good agreement with the theoretically derived capacity scaling ( $\hat{C}_{hBN} \approx 0.33\ \hat{C}_{tot}$ ). The energy  $E_{ex}$  for the observed excited state in Figure 5.11 b), highlighted by the white arrow, cannot be calculated as the lines running parallel to the Coulomb diamonds doesn't hit the diamond edges. Similar results for another measured single PDPP fiber on the same sample can be found in Figure C.8 in the appendix.

The transfer characteristics at room temperatures in Figures 5.3 and 5.4 exhibit a clear off-state in the region around  $V_{GS} = 0\text{ V}$ , which is related to the band gap of  $E_{gap} \approx 1.8\text{ eV}$  of PDPP. Usually one would expect a zero-current gap in the ( $V_{GS}, V_{DS}$ )-current maps with  $N = 0$  charge carriers in the quantum dot, reflecting the semiconducting gap corresponding to the off-current  $V_{GS}$  region of the transfer curves. This has been successfully demonstrated for carbon nanotube quantum dots<sup>147,148</sup>. The tendency of a full depletion with an emptied quantum dot can be seen to some extent in Figure C.5 in the appendix in the form of increasing Coulomb blockade regions close to  $V_{GS} = 0\text{ V}$ . In all other devices however this behavior was not observable. One possible explanation is that at elevated temperatures, different thermally activated preferred paths of high conductance form which freeze out when cooling down and that conduction paths over an array of quantum dots only form at cryogenic temperatures. The formation of different sized quantum dots (see Figure 5.10) at low temperatures, where smaller dots results in larger band gaps, makes a comparison with the transfer

## 5 Single polymer fiber transistors

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curves at elevated temperatures questionable. Presumably for most devices, a complete emptied fiber cannot be achieved due to the priorly dielectric breakdown when increasing  $V_{GS}$ . In order to investigate this discrepancy, however, further measurements would be beneficial.

In summary, Coulomb blockade oscillations with clearly observable Coulomb blockade diamonds have been presented for the first time for single polymer fiber transistors and two different gate configurations. These observations probe the formation of quantum dots within single fibers at cryogenic temperatures. The irregularly shaped and sized diamonds in conjunction with the gap at zero bias match very well the results for an array of multiple quantum dots. Additionally, also excited states are detectable. To verify the energy scale of these excited states, optical measurements as e.g. Raman/IR measurements have to be done. To prevent the superposition of different conduction paths and to reduce the influence of different quantum dots, for further investigations the number of quantum dots in the channel has to be decreased. This can be e.g. achieved by contacting thinner fibers (see Figure 5.2) or by further reducing the channel length.

# 6 Conclusion and Outlook

In this work, charge transport dynamics at the nanoscale have been investigated. To this end, three different types of polymers, namely PDPP, P3HT and MDMO-PPV, as well as SWCNTs were studied with the aid of FETs with nanoscopic device dimensions.

In the first part, the three polymers have been characterized in a newly developed vertical transistor geometry using the IL [EMIM][TFSI] as a gate. The semiconducting channel was formed by underetching the insulator separating the source and drain electrodes. Depending on the insulator material, the underetching was realized by wet or dry etching. During the device fabrication, all parameters can be precisely controlled. The channel length is given by the thickness of the insulating spacer and the channel cross section by the width of the bottom electrode and the distance of the underetched top electrode. These so called electrolyte-gated VOFETs exhibit excellent device performance metrics. In particular, when using PDPP as active material and SiO<sub>2</sub> as electrode spacer with channel lengths down to 40 nanometers, the transistors were able to drive stable current densities in the MA cm<sup>-2</sup> regime, which outperforms previously reported VOTs about a factor of 1000 and compares well to inorganic vertical devices. Furthermore, the devices exhibit record transconductances of up to 5000 S m<sup>-1</sup>, on-off ratios of up to 10<sup>8</sup> and can be operated at bias voltages down to 10 μV. Additionally also P3HT and MDMO-PPV were successfully studied for the same device architecture, while the lower device performance is related to the lower intrinsic mobility of these materials compared to PDPP. When using CYTOP as insulating spacer and PDPP as OSC, the unteretched channel can be formed with an O<sub>2</sub> plasma. The smaller on-current density might be explained by an only partial OSC channel filling due to the high hydrophobicity of CYTOP. To boost the electrical characteristics in future experiments, an improved wettability of the channel could be realized by an additional aluminium treatment prior to OSC deposition resulting in a reduced CYTOP hydrophobicity. Alternatively, further improvements can be made by choosing low surface-tension solvents with optimized wettability as e.g methanol or hexane. In general the channel length scaling is limited by the dielectric strength of the used insulator. Utilizing the high breakdown voltages of up to 1.2 V nm<sup>-1</sup> of hBN as spacer enabled the fabrication of devices with channel lengths down to only 2.4 nanometers with atomically precise thickness control. Here a subthreshold swing of 65 mV dec<sup>-1</sup> close to the room temperature limit of 60 mV dec<sup>-1</sup> could be achieved. From an application point of view, downscaling of the transistor dimensions is a promising pathway to compensate the slow switching behavior and comparably low output currents for the given limited mobilities of currently

## 6 Conclusion and Outlook

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available materials. For all investigated electrolyte-gated VOFETs, the high capacity of the IL resulted in almost ideal electrical device characteristics with saturating output currents despite such short-channel lengths and DIBL as the only observed short-channel effect. In summary this newly developed device geometry offers huge potential for the use in low power electronics and due to the small device dimensions in highly integrated applications. On the other hand, channel lengths down to 2.4 nanometers could pave the way for intrachain charge transport investigations within single polymer chains.

However, one drawback when using electrolyte gates is the limited switching frequency of up to 10 kHz<sup>51</sup> with a predicted limit of 10 MHz<sup>43</sup> due to the limited ion diffusion velocity. This currently excludes their possible application in fast switching devices in digital circuits or active matrices. Hence for future experiments one major goal is to replace the IL of the presented VOFETs by solid dielectrics, a sufficient gate coupling to stay within the gradual channel approximation provided. This could be e.g. realized by stamping hBN on top of finished VOFETs, utilizing the large dielectric strengths down to atomically thin layers of this material. Another approach could be the deposition of high-k Al<sub>2</sub>O<sub>3</sub> by low temperature atomic layer deposition<sup>149</sup> to prevent the OSC from thermal damage. Finite element simulations for the largest observed on-current density of 3 MA cm<sup>-1</sup> have revealed an upper temperature of 70 °C during constant current flow caused by Joule heating. These findings in conjunction with a continuous and stable operation for at least 50 min at MA cm<sup>-2</sup> current densities without significant degradation proves the potential of these devices for future realization of organic electrically driven laser diodes. Here the hurdle of implementing two different electrode materials to inject both electrons and holes has to be taken. Transparent indium tin oxide (ITO) with a work function of 4.7 eV could serve as the anode for hole injection and aluminum with a work function of 4.3 eV as the cathode for electron injection. HF, necessary to form the underetched contact when using SiO<sub>2</sub> as a spacer, would exclude this configuration, as also ITO and aluminum would be simultaneously etched. To also prevent aluminum from oxidation, one approach could be using CYTOP or hBN as spacer in an oxygen free atmosphere. Another possibility could be to pattern a narrow aluminum top contact by e.g. top lithography or stencil masks, without the need of an insulating spacer.

Further, the developed electrolyte-gated VOFET architecture with PDPP as OSC and SiO<sub>2</sub> as insulator was reused together with an additional poly(3,4-ethylenedioxythiophene) polystyrene sulfonate gate electrode in contact with the IL to investigate its application as neuromorphic devices. Applying consecutive V<sub>GS</sub> pulses, the transistor is already in a higher conductive state before another V<sub>GS</sub> pulse is applied, pushing more and more ions in the channel. Here a reversibly switching of the channel conductivity over five orders of magnitude (3.8 nS to 392 μS) has been shown. To prove synaptic plasticity, basic synaptic functions as pair pulse facilitation and post tetanic potentiation has been demonstrated. Given the high switching range, depending on the desired application, different conductance ranges from the nS to the hundreds of μS regime are accessible. Another huge

## 6 Conclusion and Outlook

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advantage of this approach is the low energy consumption as the devices can be operated at voltages down to 1 mV, which is inevitable in terms of up-scaling neuromorphic devices in hardware-based artificial neural networks. Indeed, with a first prototypes we showed the operation of up to three interconnected transistors. However for future possible application in large scale artificial neural networks, the device-to-device variability has to be reduced and the retention time for long-term operation increased<sup>10</sup>. Therefore, the IL should be replaced by solid gels, where the IL is embedded in a polymer matrix. Second, a new measurement setup has to be developed to simultaneously address more than three different devices in vacuum, to guarantee a sufficient long-term stability and constant water content within the electrolyte gate. Finally, an increased retention time could be achieved by further increasing the underetching, resulting in longer distances the ions have to travel out of the channel when no gate bias is applied.

The potential of using electrolyte gates to investigate charge transport at the nanoscale was further demonstrated by measuring almost ideal electrical transistor characteristics of SWCNTs with channel lengths down to 10 nanometers. Here, by comparing measurements in vacuum right after loading the samples to measurements after a vacuum storage of more than two weeks, it was demonstrated that the hysteresis of IL gated devices not only depends on polarization dynamics and the  $V_{GS}$  sweep rate, but also on charge traps in the vicinity of the SC IL interface, which might act as trap states for the IL ions. The experimental results were theoretically qualitatively described by the Landauer-Büttiker formalism.

In the last part, single PDPP fiber transistors with channel lengths below 50 nanometers and two different gate configurations, a hybrid  $Al_2O_3$ /TDPA gate and a graphite/hBN gate, were fabricated. Temperature dependent measurements of some devices are giving first hints for band-like transport at high  $V_{DS}$ , as the mobility at least remains constant from room temperature to a temperature of 10 K. In most scenarios with decreasing temperature the electrical characteristics exhibit non-linear behavior with clearly distinguishable Coulomb oscillations. At low temperatures between 5 K and 10 K Coulomb blockade diamonds in the stability diagram were demonstrated. The irregularly shaped diamonds indicate the formation of an array of single quantum dots within a single PDPP fiber. These results demonstrate that for small and highly crystalline organic systems, when size quantization as well as Coulomb interactions have to be considered, charges can only be transported over discrete energy levels. Additionally excited states in the form of lines running parallel to the Coulomb diamond edge were verified. By further reducing the channel lengths and contacting thinner fibers, the number of quantum dots could be reduced. Additionally to avoid potential thermal damage of the PDPP fibers during vacuum metal evaporation of the contacts<sup>150-152</sup>, one approach would be the deposition of single fibers on pre-fabricated bottom contacts. An alternative possibility to fabricate nanoscopic top contacts without directly evaporating metal on the OSC is by pre-fabricating metal contacts embedded in hBN and subsequently transfer the flakes including the contacts onto single fibers, as has been already demonstrated for 2D materials<sup>153,154</sup>. However in both approaches the control to

## 6 Conclusion and Outlook

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contact prior selected fibers via AFM would be lost and single fibers could only be contacted by chance.

# A PUBLICATIONS

Peer-reviewed first author publications that are part of this cumulative thesis:

**J. Lenz**, F. del Giudice, F. R. Geisenhof, F. Winterer, and R. T. Weitz, "Vertical, electrolyte-gated organic transistors show continuous operation in the MA cm<sup>-2</sup> regime and artificial synaptic behavior", *Nat. Nanotechnol.*, **14**, 579–585 (2019)

**J. Lenz**<sup>1</sup>, A. Janissek<sup>1</sup>, F. del Giudice, M. Gaulke, F. Pyatkov, Si. Dehm, F. Hennrich, L. Wei, Y. Chen, A. Fediai, M. Kappes, W. Wenzel, R. Krupke and R. T. Weitz, "Ionic liquid gating of single walled carbon nanotube devices with ultra-short channel length down to 10 nm". *Appl. Phys. Lett.*, **118**, 063101 (2021)

**J. Lenz**, A. M. Seiler, F.R. Geisenhof, F. Winterer, K. Watanabe, T. Taniguchi and R. T. Weitz, "High-Performance Vertical Organic Transistors of Sub-5 nm Channel Length", *Nano Lett.*, **21**, 4430-4436 (2021)

**J. Lenz** and R. T. Weitz, "Charge transport at the nanoscale in semiconducting polymers",  
*In preparation*

C. Eckel<sup>1</sup>, **J. Lenz**<sup>1</sup>, A. Melianas, A. Salleo and R. T. Weitz, "A.4 Nanoscopic electrolyte-gated vertical organic transistors with low power operation and five orders of magnitude switching range for neuromorphic systems", *Submitted to Adv. Mater.*

Other peer-reviewed publications

L.S. Schaffroth, **J. Lenz**, V. Geigold, M. Kögl, A. Hartschuh, and R.T. Weitz, "Freely suspended, van-der-Waals bound organic nm-thin functional films: mechanical and electronic characterization", *Adv. Mater.* **31**, 1808309 (2019)

## A PUBLICATIONS

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F. R. Geisenhof, F. Winterer, S. Walkolbinger, T. D. Gokus, Y. C. Durmaz, D. Priesack, **J. Lenz**, F. Keilmann, K. Watanabe, T. Taniguchi, R. Guerrero-Aviles, M. Pelc, A. Ayuela and R. T. Weitz, “Anisotropic strain induced soliton movement changes stacking order and bandstructure of graphene multilayers”, *ACS Appl. Nano Mater.* **2**, 6067–6075 (2019)

F. Winterer, L.S. Walter, **J. Lenz**, S. Seebauer, Y. Tong, L. Polavarapu, J. Feldmann and R. T. Weitz, “Charge Traps in All-Inorganic CsPbBr<sub>3</sub> Perovskite Nanowire Field Effect Phototransistors”, *Adv. Electron, Mater.*, **7**, 2100105 (2021)

F. R. Geisenhof, F. Winterer, A. M. Seiler, **J. Lenz**, T. Xu, F. Zhang and R. T. Weitz, Tunable quantum anomalous Hall octet driven by orbital magnetism in bilayer graphene, *Nature accepted*

<sup>1</sup> These authors contributed equally.

## A.1 Vertical, electrolyte-gated organic transistors show continuous operation in the MA/cm<sup>2</sup> regime and artificial synaptic behavior

Jakob Lenz, Fabio del Giudice, Fabian R. Geisenhof, Felix Winterer, and R. Thomas Weitz

*Nat. Nanotechnol.*, **14**, 579–585 (2019)

DOI: 10.1038/s41565-019-0407-0

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### **Abstract**

Until now, organic semiconductors have failed to achieve high performance in highly integrated, sub-100 nm transistors. Consequently, single-crystalline materials such as single-walled carbon nanotubes, MoS<sub>2</sub> or inorganic semiconductors are the materials of choice at the nanoscale. Here we show, using a vertical field-effect transistor design with a channel length of only 40 nm and a footprint of  $2 \times 80 \times 80 \text{ nm}^2$ , that high electrical performance with organic polymers can be realized when using electrolyte gating. Our organic transistors combine high on-state current densities of above  $3 \text{ MA cm}^{-2}$ , on/off current modulation ratios of up to  $10^8$  and large transconductances of up to  $5,000 \text{ S m}^{-1}$ . Given the high on-state currents at such large on/off ratios, our novel structures also show promise for use in artificial neural networks, where they could operate as memristive devices with sub-100 fJ energy usage.

### **Contribution**

I performed all sample preparations, experiments and data analysis for the vertical devices and the data analysis for the lateral devices. Fabio del Giudice performed the sample preparations and experiments for the lateral devices. The first draft of the manuscript was written entirely by me and I produced the final version. All figures were designed by me.

# Vertical, electrolyte-gated organic transistors show continuous operation in the $\text{MA cm}^{-2}$ regime and artificial synaptic behaviour

Jakob Lenz<sup>1</sup>, Fabio del Giudice<sup>1,4</sup>, Fabian R. Geisenhof<sup>1</sup>, Felix Winterer<sup>1</sup> and R. Thomas Weitz<sup>1,2,3\*</sup>

**Until now, organic semiconductors have failed to achieve high performance in highly integrated, sub-100 nm transistors. Consequently, single-crystalline materials such as single-walled carbon nanotubes, MoS<sub>2</sub>, or inorganic semiconductors are the materials of choice at the nanoscale. Here we show, using a vertical field-effect transistor design with a channel length of only 40 nm and a footprint of  $2 \times 80 \times 80 \text{ nm}^2$ , that high electrical performance with organic polymers can be realized when using electrolyte gating. Our organic transistors combine high on-state current densities of above  $3 \text{ MA cm}^{-2}$ , on/off current modulation ratios of up to  $10^5$  and large transconductances of up to  $5,000 \text{ S m}^{-1}$ . Given the high on-state currents at such large on/off ratios, our novel structures also show promise for use in artificial neural networks, where they could operate as memristive devices with sub-100 fJ energy usage.**

Organic semiconductors are promising components for novel flexible electronics such as displays and sensors. Large-scale processability via printing and the inherent flexibility of organic materials are two key advantages in this context. Attributes that do not usually come to mind when discussing organic materials are high current densities in the  $\text{MA cm}^{-2}$  range, large transconductances in the  $10\text{--}100 \text{ S m}^{-1}$  regime, low-power operation or low supply voltages in the sub-volt regime, as are common in highly integrated nanoscale transistors<sup>1</sup>. More specifically, while, for example, state-of-the-art single-walled carbon nanotube (SWCNT) or MoS<sub>2</sub> field-effect transistors (FETs) are able to sustain current densities in the range of  $\text{MA cm}^{-2}$  (refs. <sup>1–3</sup>), organic transistors are currently only able to operate at tens of  $\text{kA cm}^{-2}$  (refs. <sup>4,5</sup>). Although such high current densities in the  $\text{MA cm}^{-2}$  range are crucial for realizing highly integrated, high-performance electronics<sup>1</sup>, low-power operation is critical for operation in handheld devices or in neuronal networks. In the latter, the energy per switching event is required to be in the sub-pJ regime, implying the need for high on-state conductance, large current modulation ratios and low voltage operation.

Here, we discuss a nanoscopic device design based on a vertical transistor structure that enables electrolyte-gated organic semiconductors to drive  $\text{MA cm}^{-2}$  currents combined with on/off ratios of  $10^5$ . The small channel length of less than 50 nm and nanoscopic device footprint of  $2 \times 80 \times 80 \text{ nm}^2$  in principle allows the use of such devices in highly integrated circuits. Additionally, we show that our device design makes organic semiconductors prime candidates for use in low-power neuromorphic computing.

The established approach to the realization of nanoscopic channels is a planar transistor geometry, which we also used in our initial investigations (Fig. 1a). We used a diketopyrrolopyrrole–terthiophene donor–acceptor polymer (PDPP, Fig. 1a inset) as the prototype semiconductor for our device structures<sup>6</sup>. A PDPP solution was deposited via doctor blading, yielding a sub-monolayer thin film. After deposition of the ionic liquid 1-ethyl-3-methylimid-

azolium bis(trifluoromethylsulfonyl)imide ([EMIM][TFSI])<sup>7</sup> the transistors were electrically characterized in vacuum or ambient atmosphere. Electrolyte gating has been established in the past as a reliable method to enable large gate coupling<sup>8–11</sup>. Consequently, the short channel effects in laterally sub-micrometre devices have been drastically reduced<sup>12</sup>. Typical transfer curves of transistors with 220 nm and 40 nm channel lengths as well as corresponding scanning electron microscopy (SEM) images are shown in Fig. 1a–d. As is common for electrolyte-gated transistors, due to the large capacitance of the electrolyte<sup>7</sup> the transistors can be operated at a gate–source voltage  $V_{\text{GS}}$  below 2 V. The respective output characteristics are provided in Supplementary Fig. 1. We note that the maximum on-state currents of the transistors shown in Fig. 1a,b are different because the threshold voltages of the transistors differ. Transistors with similar threshold voltage exhibit an increased on-state current for shorter channel lengths (Supplementary Fig. 2). An important figure of merit of short-channel transistors is the contact resistance<sup>13</sup>. Our transistors show exceptionally low contact resistances of below  $3 \Omega \text{ cm}$  (estimated from transmission line measurements; Supplementary Fig. 3), which are similar to values previously observed in electrolyte-gated transistors and can be explained by electrochemical doping of the contacts<sup>14</sup>, and which are a prerequisite to the operation of transistors at high frequencies. Furthermore, high on/off current ratios of  $10^5$  are observed, and our devices show large transconductances of up to  $6 \text{ S m}^{-1}$ . Even though these values are lower than what has been shown before, for example in P3HT transistors<sup>15</sup>, the electrical characteristics are encouraging, especially given the fact that the semiconducting film is only 2 nm thick (Fig. 1d). Finally, our on-state resistance of  $\rho_{\text{on,PDPP}} = 5.4 \times 10^{-4} \Omega \text{ m}$  compares favourably to P(NDI2OD-T2) transistors ( $\rho_{\text{on,P(NDI2OD-T2)}} = 0.12 \Omega \text{ m}$ )<sup>16</sup>, the only other monolayer polymer transistors of which we are aware.

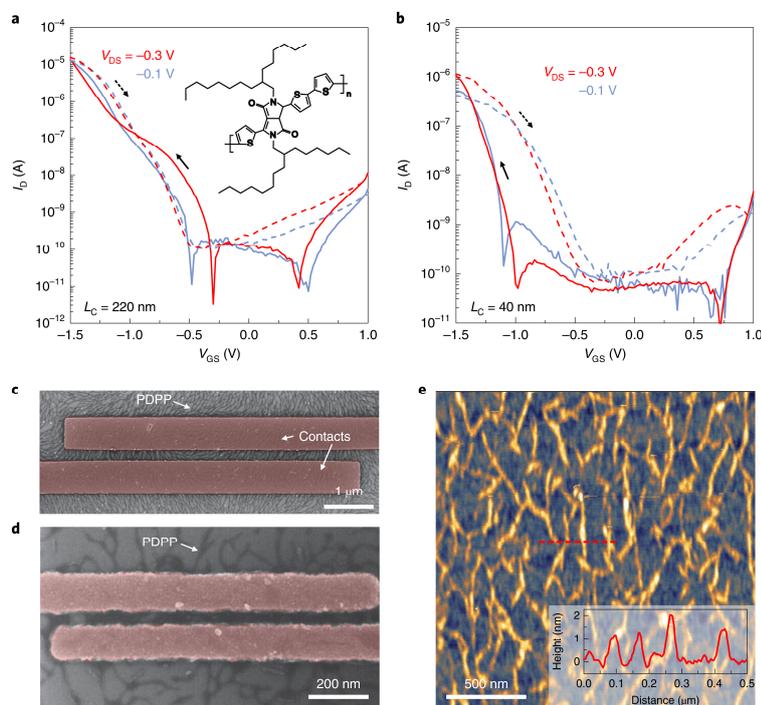
Although the electrical characteristics of these lateral transistors are very encouraging, for highly integrated applications a smaller-footprint channel is needed. We thus realized transistors with

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## A.1 Vertical, electrolyte-gated OFETs show operation in the MA/cm<sup>2</sup> regime

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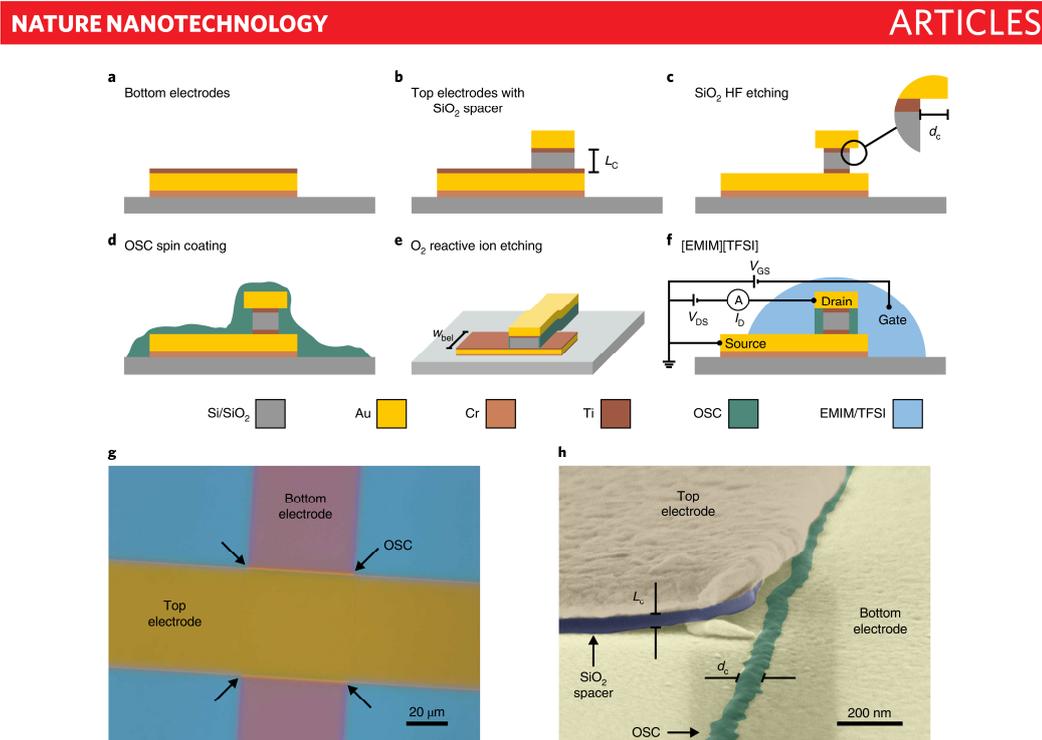


**Fig. 1 | Planar, electrolyte-gated nanoscopic PDPP OFETs.** **a–d**, Transfer characteristics of two transistors with  $L_c$  of 220 nm (**a**) (inset, molecular structure of the PDPP used) and 40 nm (**b**), and corresponding SEM images (**c,d**) (measured at  $32 \text{ mV s}^{-1}$  under vacuum). **e**, Atomic force microscopy topography image of a  $\text{SiO}_2$  substrate with sub-monolayer PDPP coverage, allowing the height of individual polymer nanofibres to be measured (inset). In **a** and **b**, the solid lines represent the trace and the dashed lines the re-trace.

vertical contact separation that can be gated with an electrolyte. Vertical organic field-effect transistors (VOFETs) have been established as a promising approach to achieve nanoscopic source–drain contact separation without the need for high-resolution patterning<sup>17,18</sup>. Several groups have previously reported the high device performance of VOFETs<sup>19–23</sup>. We now introduce electrolyte gating to VOFETs and find surprisingly improved performance compared to the above lateral device design as well as existing VOFETs. The device fabrication is shown in Fig. 2a–f. Two gold electrodes serving as source and drain were patterned for convenience by electron-beam lithography. The channel length  $L_c$  of the transistors was controlled by the thickness of the insulating  $\text{SiO}_2$ . The  $\text{SiO}_2$  and titanium layers were subsequently removed across a width  $d_c$  with 1% HF acid, resulting in an under-etched top contact. The magnitude of  $d_c$  was controlled by the etching time, with smaller  $d_c$  enabling better control of the channel with the electrolyte, because the ions have to diffuse a smaller length to control the entire channel. The channel area  $A_{ch}$  (its footprint) is given by  $A_{ch} = 2 \times w_{bel} \times d_c$ , where  $w_{bel}$  is the width of the bottom electrode. Subsequent semiconductor deposition and reactive ion etching (RIE) completed the transistors. The directional etching process allowed us to remove the semiconductor everywhere except below the top electrode, because the latter served as an etching mask for the semiconductor (Fig. 2g)<sup>24</sup>. A cross-sectional SEM image of a device broken through the transistor channel is presented in Fig. 2h. In all devices inspected via SEM, the vertical gap was observed to be completely

filled with organic semiconductor (Supplementary Fig. 4). For electrical measurements we again utilized [EMIM][TFSI]<sup>27</sup> to control the charge carrier density in the semiconducting channel. In this configuration, the ions diffuse sideways directly into the vertical bulk channel. Typical  $I$ – $V$  characteristics of an electrolyte-gated VOFET with a channel area of  $A_{ch} = 1.6 \times 10^{-11} \text{ m}^2$  are shown in Fig. 3a,b. As can be seen in the output characteristics in Fig. 3a, the transistor exhibits good saturation behaviour, which is indispensable for active-matrix organic light-emitting diode (AMOLED) displays, for example, and all other applications where transistors are used as a current source<sup>25,26</sup>. Also, this provides good proof that even though the channels are only 40 nm short, the high gate coupling via the ionic liquid fully controls the charge carrier density in the channel. The corresponding transfer curves are shown in Fig. 3b, where one can clearly see the large on/off ratio of up to  $10^8$ . The drain–source voltage ( $V_{DS}$ ) dependent shift of the threshold voltage stems from voltage-induced drain barrier lowering<sup>27</sup> and is the only short-channel effect we observed. The current density in Fig. 3b is  $J_{-0.3V} = 32.9 \text{ kA cm}^{-2}$  at  $V_{DS} = -0.3 \text{ V}$  and  $J_{-10mV} = 11.3 \text{ kA cm}^{-2}$  at  $V_{DS} = -10 \text{ mV}$  with a transconductance of up to  $g_m = 58.5 \text{ S m}^{-1}$  (Supplementary Fig. 5a). The sub-threshold swing for the transistor in Fig. 3b is  $139 \text{ mV dec}^{-1}$  at  $V_{DS} = 10 \text{ mV}$  (Supplementary Fig. 6a). For a transistor with a reduced  $d_c$  of 40 nm the sub-threshold swing improves to  $90.5 \text{ mV dec}^{-1}$  (Supplementary Fig. 6b), which is close to the minimum observed sub-threshold swing previously observed for ionic-liquid-gated transistors of about  $70 \text{ mV dec}^{-1}$

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**Fig. 2 | Device fabrication process of electrolyte gated VOFETs.** **a, b.** Patterning of the bottom (**a**) and top (**b**) electrodes by electron-beam lithography. **c.** HF under-etching of the top electrode. **d, e.** Spin-coating of the organic semiconductor solution (OSC) (**d**) and subsequent directional oxygen RIE (**e**). **f.** Fully finished transistor. **g.** Polarization microscopy image of a finished VOFET without electrolyte gate. The PDPP appears bright between the electrodes (labelled OSC). **h.** Coloured cross-sectional SEM image of a VOFET with two gold electrodes (yellow), SiO<sub>2</sub> spacer (blue) and PDPP (green). The top electrode has bent upwards during breaking of the device. The breaking is needed to take the cross-sectional image; in the working devices the electrodes sit immediately above and below the semiconductor.

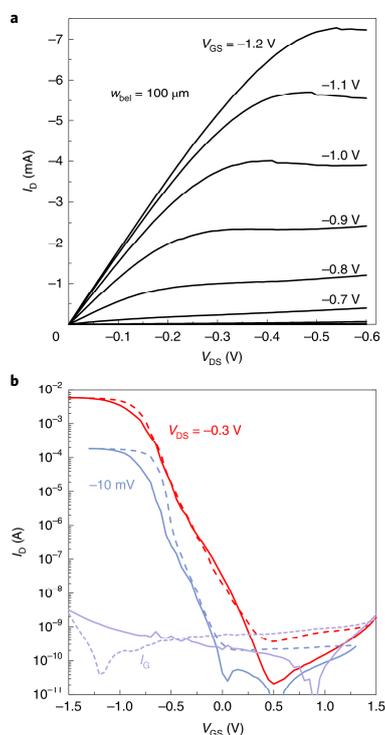
(ref. 28). The trend towards lower sub-threshold swing for thinner semiconductor thickness has been observed previously in lateral electrochemical transistors where it has been attributed to the shorter distance the ions diffuse into the channel<sup>28</sup>, which is also probably the case in our work. Currently, we can only speculate about the microscopic reason for the significantly improved electrical characteristics of the vertical compared to lateral device designs. We anticipate that it is related to a favourable morphology of the semiconductor and better charge injection (that is, a lower contact resistance).

The geometry developed here can not only be used with PDPP polymers, but provides a general platform for nanoscale organic high-current transistors. For example, the  $I$ - $V$  characteristics for a P3HT transistor ( $A_{\text{ch}} = 1 \times 10^{-12} \text{ m}^2$ ), fabricated in the same manner as described in Fig. 2 with a comparable current density ( $J_{-0.3\text{V}} = 129 \text{ kA cm}^{-2}$ ) and on/off ratio ( $10^6$ ), are shown in Supplementary Fig. 7.

The combination of short channels with electrolyte gating is of interest for a number of potential applications where low voltages, high on-state current densities or large transconductances are required. Examples include the driving of OLEDs<sup>17</sup>, sensors<sup>13</sup> or memristors<sup>29–33</sup>. We first focus on explaining, in detail, charge transport at high current densities, before demonstrating the use of the electrolyte-gated VOFETs in the field of low-power memristive devices.

**Operation of organic transistors in the  $\text{MA cm}^{-2}$  regime.** In the transistor discussed in Fig. 3a,b, the total resistance  $R_{\text{on}}$  in the on state, with a maximum on current of  $I_{\text{on}} = 5.6 \text{ mA}$  at  $V_{\text{DS}} = -0.3 \text{ V}$ , is  $R_{\text{on}} = 54 \Omega$ . Control experiments revealed similar total resistances for just the measurement set-up including contact resistances. The channel resistance seems to be almost negligible in this specific device geometry, and  $I_{\text{on}}$  is predominantly limited by the contact and lead resistances. To find an upper limit for  $I_{\text{on}}$ , we increased the relative resistance of the channel by reducing the channel area  $A_{\text{ch}}$  to a nanoscopic  $2 \times 80 \times 80 \text{ nm}^2$  (the resistance of the current leads stays the same as in the previously described devices). The maximum current density for these nanoscopic transistors is  $J_{-0.3\text{V}} = 2.7 \text{ MA cm}^{-2}$  (on/off ratio of  $10^7$ ) and  $J_{-10\text{mV}} = 89.9 \text{ kA cm}^{-2}$ , at  $V_{\text{DS}} = -0.3 \text{ V}$  and  $-10 \text{ mV}$ , respectively (Fig. 4a,b). Although the calculation of mobility in electrolyte-gated transistors is challenging, we provide a rough estimate in the Supplementary Information.

Because the current densities are exceptionally large for organic transistors (see below for a detailed comparison to other state-of-the-art transistors), we carried out a series of test experiments to make sure that the current is really flowing through the organic semiconductor and is not caused by shorts in the device. First, we found that a transistor structure before semiconductor deposition only showed insulating behaviour and no response to ionic liquid gating (Supplementary Fig. 8a). Second, after removing the ionic liquid and depositing the semiconductor, the same transistor showed



**Fig. 3 | Electrical characteristics of electrolyte-gated PDPP VOFET measured in ambient atmosphere.** **a**, Output characteristics measured at  $16 \text{ mV s}^{-1}$ . **b**, Transfer characteristics with corresponding gate current  $I_g$  measured at  $80 \text{ mV s}^{-1}$ . At  $V_{DS} = -0.3 \text{ V}$ , a high on/off ratio of  $10^8$  and an on-state current density of  $34.9 \text{ kA cm}^{-2}$  are achieved. Dimensions of the device:  $w_{\text{ch}} = 100 \mu\text{m}$ ,  $d = 80 \text{ nm}$ ,  $L_g = 40 \text{ nm}$ . The solid lines represent the trace and the dashed lines the re-trace.

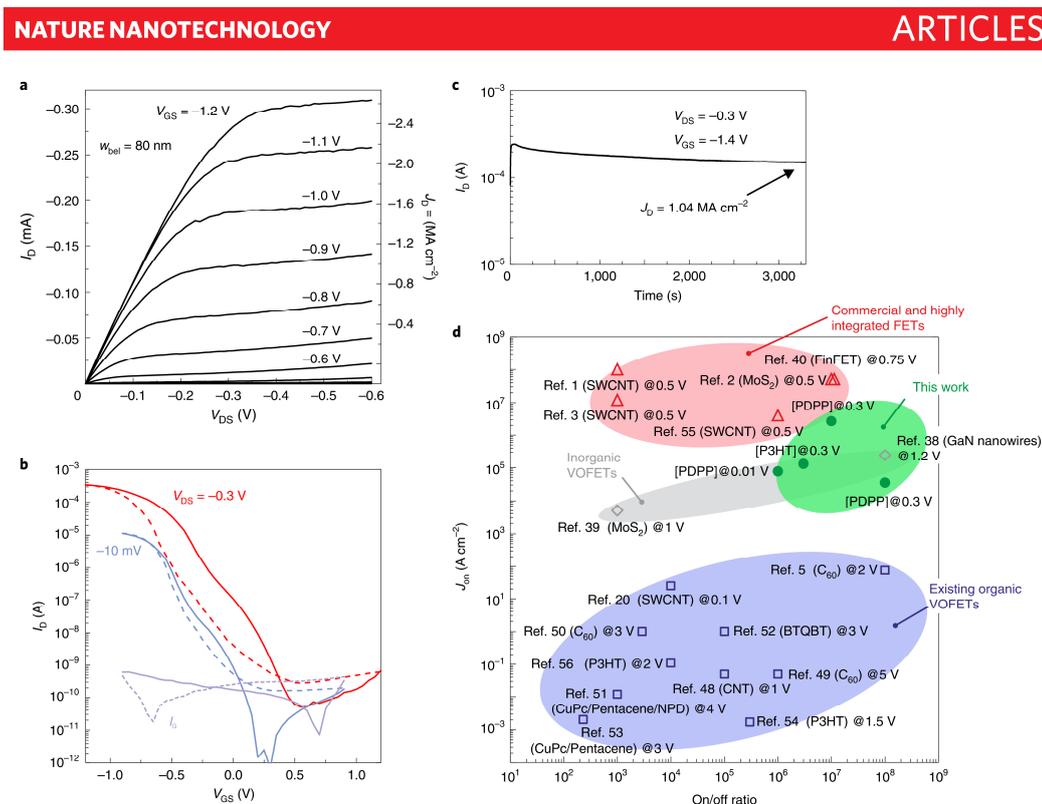
a clear response to the ionic liquid gate with a maximum current density of about  $3 \text{ MA cm}^{-2}$  (Supplementary Fig. 8b). Finally, we purposely removed the organic semiconductor of the previously working VOFET by 10 min sonication in a xylene bath followed by treatment with anisotropic  $\text{O}_2$  plasma, and again observed insulating behaviour (Supplementary Fig. 8c). Furthermore, SEM images of once working VOFETs after electrical measurements revealed no damage to the gold electrodes. In fact, the failure current density of gold nanowires exceeds the maximum observed current density in our electrolyte-gated VOFETs by at least a factor of 100 (ref. 34). We also tested whether we could intentionally destroy our device by applying a higher drain-source voltage. Indeed, at  $V_{DS} = -1.8 \text{ V}$ , the current decreases slowly down to the noise level (Supplementary Fig. 9b). Because this voltage is close to the electrochemical window reported for [EMIM]/[TFSI] at room temperature<sup>35</sup>, the failure mechanism might be attributed to an electrochemical reaction of the organic semiconductor with the electrolyte. The combined experimental evidence is clear proof that the current is carried exclusively by the organic semiconductor. We also assessed the cycling stability of the VOFETs, and measurements of 20  $I_D$ - $V_{GS}$  cycles showed no obvious drift in the threshold voltage or decrease

in  $I_D$  (Supplementary Fig. 10). Finally, we measured the same transistor after three months of storage in a desiccator; this showed the same on current and only a small shift in  $V_{th}$  (Supplementary Fig. 11).

For applications it is also important to test how long the devices can sustain  $\sim 1 \text{ MA cm}^{-2}$  currents. This question is especially critical because previous VOFETs showed significant degradation due to Joule heating if operated for more than a few milliseconds at current densities above  $1 \text{ kA cm}^{-2}$ , and are therefore only operated in pulsed mode<sup>7</sup>. In contrast, as shown in Fig. 4c, our transistors can be operated continuously for at least 50 min at  $\text{MA cm}^{-2}$  current densities without significant degradation (Supplementary Fig. 12). We assume that the stability at these high current densities stems from the favourable device geometry, because the small channel width and length provide intimate contact of the semiconductor with the source and drain contacts as well as the  $\text{SiO}_2$  and the ionic liquid, which all act as a heat sink to allow for rapid dissipation of the developing heat. To estimate the upper temperature caused by Joule heating, we performed finite element simulations (see Joule heating section and Supplementary Figs. 13 and 14 in the Supplementary Information). The calculations revealed that the organic semiconductor in the most realistic scenario simulated heats only up to below  $70^\circ\text{C}$  during constant current flow. We believe that this is also the reason why neither a self-heating-induced N-shaped negative differential resistance, as reported for inorganic transistors<sup>36</sup>, nor an S-shaped negative differential resistance, as recently presented for organic permeable-base transistors<sup>37</sup>, was found in our devices.

The observed current densities are uniquely high for organic transistors and Fig. 4d summarizes and compares the device performances of several state-of-the-art VOFETs and lateral FETs with respect to their on-state current densities and on/off ratios. The performance of our electrolyte-gated VOFETs exceeds the best vertical organic transistors and is in fact comparable to inorganic vertical transistors based on GaAs, for example<sup>38,39</sup>. This is particularly surprising, because our VOFETs were operated only at  $V_{DS}$  values of  $-0.3 \text{ V}$  and  $-10 \text{ mV}$ , respectively, which is at least a factor of 4 smaller than the operation voltage of inorganic vertical FETs. Furthermore, our VOFETs also perform well compared to SWCNT,  $\text{MoS}_2$  and FIN-FET<sup>40</sup> devices. Additionally, the favourable properties are not limited to PDPP and are comparable for different polymers, such as P3HT, which demonstrates that this device architecture can be expected to be suitable for a wide range of semiconductors. Finally, our transistors show large transconductances of above  $5,000 \text{ S m}^{-1}$  (Supplementary Fig. 5b), larger than SWCNT network FETs<sup>9</sup> or PEDOT:PSS FETs<sup>15,41</sup>. A more detailed comparison of transconductances is provided in Supplementary Table 3.

**VOFET-based low-power memristive devices.** The large on-state conductances, high on/off ratios and low operational voltages of our device design also make it suitable for ultralow-power electronics. For example, we can operate our devices at a  $V_{DS}$  of only  $10 \mu\text{V}$  and still obtain on/off ratios of  $10^2$  (Supplementary Fig. 15). Such low-power operation is especially relevant for applications in artificial neural networks as memristive devices. More specifically, our VOFETs combine the ability for low-voltage operation with a small footprint, large on/off ratio, high switching speed, long-term stability of the electrical performance and the use of electrolyte gating<sup>29</sup>. To prove the general usability of our devices in this field, we show artificial synaptic behaviour with short- and long-term plasticity (STP and LTP). As previously reported for electrolyte-gated OFETs, the contact to the liquid electrolyte can be seen as the presynaptic terminal and the source electrode as the postsynaptic terminal<sup>41,42</sup>. On application of a voltage pulse at the gate electrode (corresponding to a presynaptic potential spike), the increase in  $I_D$  can be viewed as the excitatory post-synaptic current (EPSC), which represents the synaptic strength. Before a presynaptic spike, the anions and cations



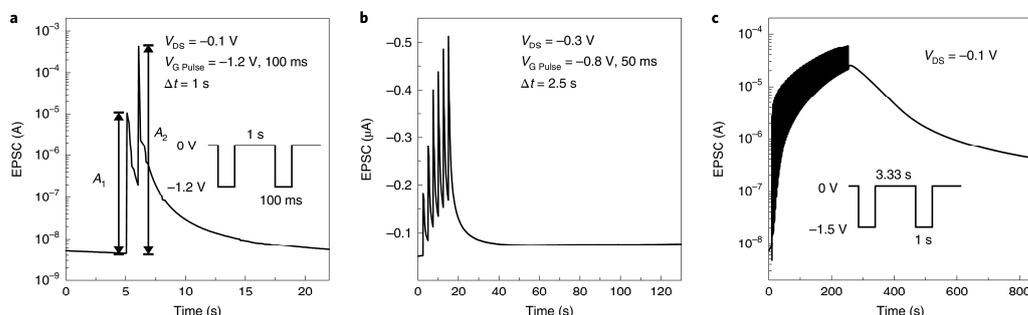
**Fig. 4 | Nanoscopic electrolyte-gated PDPP VOFET measured in ambient atmosphere and comparison to state-of-the-art transistors. a, b,** Output characteristics measured at  $16 \text{ mV s}^{-1}$  (**a**) and transfer characteristics measured at  $50 \text{ mV s}^{-1}$  (**b**) of a nanoscopic VOFET with a current density of  $2.7 \text{ MA cm}^{-2}$ . Device dimensions:  $d_c = 80 \text{ nm}$ ,  $w_{\text{bel}} = 80 \text{ nm}$ ,  $L_c = 40 \text{ nm}$ . **c,** Continuous operation for 55 min above  $1 \text{ MA cm}^{-2}$  ( $w_{\text{bel}} = 90 \text{ nm}$ ,  $d_c = 80 \text{ nm}$ ,  $L_c = 40 \text{ nm}$ ). **d,** Comparison of on-state current densities and on/off ratios for different vertical and planar transistors<sup>1-3,5,20,38-40,48-56</sup>. The respective operation voltages  $V_{\text{DS}}$  are also indicated.

are randomly distributed in the liquid electrolyte. A short negative voltage pulse causes anions to penetrate into the bulk of the semiconductor, leading to an accumulation of free holes in the semiconducting channel. These charge carriers contribute to the EPSC on application of a source-drain voltage. After the presynaptic spike there is no driving force for the ions to remain in the semiconductor, so they slowly return to a random distribution and the EPSC decays. The EPSC change over time is regarded as synaptic plasticity that can be distinguished in STP and LTP. Although STP is more important for the application of memristive elements in computational applications, LTP is more important in learning<sup>20</sup>. As we show in the following, with our device geometry we can tune the relative strengths of STP and LTP via the device design, thus making the layout suitable for a wide range of potential applications. Paired-pulse facilitation is a possible means to simulate STP<sup>12</sup>. Figure 5a shows the EPSC where the amplitude of the second postsynaptic response ( $A_2 = 608 \mu\text{A}$ ) is amplified compared to the first one ( $A_1 = 10.5 \mu\text{A}$ ) by a factor of 58. Because before the second presynaptic spike the ions have not returned to a completely random distribution, these residual ions contribute to the second presynaptic spike, resulting in an increased EPSC.

For long-term memory formation it is necessary to transform STP to LTP. LTP in our electrolyte-gated VOFETs is shown in

Fig. 5b. After six pulses ( $-0.8 \text{ V}$ , 50 ms) with an inter-spike interval of 2.5 s, an increase of the EPSC after each pulse and an obvious non-volatile channel current is measured, which constitutes memory formation. Another method to realize LTP is by increasing the magnitude of the gate pulse (Supplementary Fig. 16). The magnitude of the EPSC and consequently LTP can easily be increased in our devices by enlarging the  $d_c$  of the semiconducting film, which in turn is determined by the amount of underetching of the top electrode in Fig. 2c. An extreme case is shown in Fig. 5c where only PDPP is sandwiched between the electrodes (for fabrication details see Supplementary Fig. 17). In these devices the EPSC is increased by a factor of almost 3,000 after the last spike and is still increased by a factor of 50 after 10 min. The larger channel area and therefore the larger volume for potential bulk gating results in an increased memory formation compared to smaller channel areas and thus enhanced LTP compared to devices with shorter  $d_c$ .

Besides synaptic plasticity, the minimum energy required for a switching operation is also a critical factor for possible integration of memristors into complex neuronal networks. Given the large on-state current densities, high on/off ratios and low operation voltages of our devices, we can tune the currents and also switching energies across a wide range depending on the choice of applied voltages. The minimal switching energies we have



**Fig. 5 | Short- and long-term synaptic plasticity of electrolyte-gated PDDP VOFETs measured in ambient atmosphere. a**, EPSC triggered by two pre-synaptic spikes ( $-1.2$  V,  $100$  ms) with an inter-spike interval of  $1$  s ( $d_c = 100$  nm,  $w_{\text{gate}} = 500$   $\mu\text{m}$ ,  $L_c = 40$  nm). **b**, EPSC versus time simulated by six gate pulses ( $-0.8$  V,  $50$  ms) with an interval of  $2.5$  s. **c**, EPSC triggered by 73 pulses ( $-1.5$  V,  $1$  s) with an inter-spike interval of  $3.33$  s for an electrolyte-gated VOFET without  $\text{SiO}_2$  spacer and only PDDP between the two electrodes (Supplementary Fig. 11).

achieved so far are in the  $10^{-13}$  to  $10^{-14}$  J range (Supplementary Fig. 18), where  $V_{\text{DS}} = 100$   $\mu\text{V}$  and  $V_{\text{GS}} = -0.4$  to  $-1.2$  V were used. Such low switching energies are already below what is currently used in CMOS neuromorphic devices, and only one magnitude larger than the  $10$  fJ per event used in the brain<sup>29</sup>. Furthermore, the switching energies obtained here are only a factor of  $100$  larger than the best reported switching energies that have been obtained in core-sheath nanowires<sup>43</sup>.

### Conclusions

In summary, we have reported the fabrication process and electrical characterization of a nanoscopic vertical transistor (VOFET) architecture with an electrode separation of  $40$  nm and a minimal footprint of  $2 \times 80 \times 80$  nm<sup>2</sup> (neglecting the gate contact). Utilizing the high capacitances of liquid electrolytes, our VOFETs can continuously sustain current densities above  $2$  MA cm<sup>-2</sup> at  $-0.3$  V bias with on/off ratios up to  $10^8$  and ultra-high transconductances of up to  $5$  kS m<sup>-1</sup>. Furthermore, we have shown that the electrolyte-gated VOFETs can also be operated at low driving voltages down to  $10$   $\mu\text{V}$  and can be utilized as versatile memristive elements; depending on the operation voltage and exact transistor layout, the relative susceptibility of the memristive element to STP and LTP can be tuned. Additionally, switching events that require only  $10$ – $100$  fJ per event have been realized. We expect the VOFET structure also to be interesting for other fields of research, such as assessing the vertical mobility of semiconductors for use in solar cells or—given the high current densities in the MA cm<sup>-2</sup> regime—possibly also for electrically driven lasing<sup>44,45</sup>. A further step is to increase the switching speed of our (in this respect) unoptimized devices from  $1$  kHz (Supplementary Fig. 19) to the  $10$  MHz already demonstrated in other electrolyte-gated transistors<sup>46</sup>. Finally, although the work presented here shows the general suitability of organic materials to support MA cm<sup>-2</sup> current densities in nanoscopic devices, future work will need to address, for example, the structuring of the electrolytic gate or parasitic capacitances between the electrolyte and the source-drain contacts. This could be realized, for example, by utilizing solid ionic gel dielectrics<sup>9</sup>, which have been shown in the past to allow the realization of organic transistors with patterned gate contacts<sup>47</sup>.

### Online content

Any methods, additional references, Nature Research reporting summaries, source data, statements of data availability and associated accession codes are available at <https://doi.org/10.1038/s41565-019-0407-0>.

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#### Author contributions

J.L. and R.T.W. conceived the project. J.L. prepared the VOFET samples and conducted the measurements and data analysis. Ed.G prepared the lateral transistor samples and conducted the measurements and data analysis. All authors discussed the data. J.L. and R.T.W. wrote the manuscript with input from all authors. R.T.W. supervised the project.

#### Competing interests

J.L. and R.T.W. have submitted a patent application to the German patent office (no. 10 2018 221 361.5) covering the structure of the VOFET and the applications discussed in this manuscript.

#### Additional information

Supplementary information is available for this paper at <https://doi.org/10.1038/s41565-019-0407-0>.

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#### Methods

**Electrode fabrication.** Before further treatment, all substrates were cleaned for 10 min each in an ultrasonic bath in acetone and isopropyl alcohol and blow-dried with nitrogen. The electrodes were patterned by electron-beam lithography (e-line system, Raith). For the bottom electrodes a 250-nm-thick layer of PMMA 950K (Allresist) was spin-coated followed by a 150 °C soft bake of 3 min. After electron beam exposure, the resist was developed for 100 s in a 1:3 methylisobutylketone:isopropyl alcohol mixture and 1–3 nm chromium (evaporated at 0.3 Å s<sup>-1</sup>), 30 nm gold (evaporated at 1 Å s<sup>-1</sup>) and 0.5–1 nm titanium (evaporated at 0.1 Å s<sup>-1</sup>) were evaporated in an electron-beam evaporator. For the lateral device structures, we used gold-palladium to realize contacts with a separation between 30 nm and 500 nm, and in these devices we have not capped the electrodes with an additional titanium layer. For the vertical transistors, chromium or titanium were used for better adhesion between the gold and SiO<sub>2</sub>; chromium was only evaporated below the bottom electrode because it is resistant to HF acid. Liftoff was performed in acetone with low-power sonication. The width of the bottom electrode  $w_{\text{bot}}$  was varied between 80 nm and 500 μm. For the top electrodes a 500 nm layer of PMMA 950K (Allresist) was spin-coated and patterned by electron-beam lithography as described above. After development, 35–50 nm of SiO<sub>2</sub> was sputtered with a power of 50 W and an argon pressure of  $p = 2 \times 10^{-2}$  mbar. Titanium (1 nm) and 90 nm gold were evaporated in the same manner as for the bottom electrode. Titanium was used between the electrodes and could be etched with HF. The sputtered SiO<sub>2</sub> was etched with 1% HF acid ( $d_t = 40$ –120 nm).

**Organic semiconductor and gate preparation.** PDPP (P3HT) was dissolved in 1,3-dichlorobenzene (Sigma-Aldrich) (15 mg ml<sup>-1</sup>) at 80 °C (70 °C for P3HT) and stirred for at least 12 h (4 h for P3HT). For planar devices a diluted semiconductor

solution was doctor-bladed (Zehntner ZAA 2300, ZUA 2000, ACC225). For the vertical devices the semiconductor solution was spin-coated on the substrate for 40 s (1,000 r.p.m.), followed by a bake of 2 min at 80 °C. By directional RIE (Oxford Plasmalab 100 ICP RIE) with oxygen plasma the semiconductor was removed everywhere except below the top contacts, which served as etching masks (20 s.c.c.m., 20 mbar, 10 W, 180–210 s). The liquid electrolyte [EMIM][TFSI] was dropped with a syringe such that the crossing point of the bottom and top electrodes was covered. Before electrical measurements the samples were stored in a vacuum oven (50 °C, 10 mbar, >12 h) to bake out moisture residues from the electrolyte.

**Electrical characterization.** Measurements were performed, unless noted otherwise, under ambient conditions with a conventional point probe station and two source meters (Keithley 2450) as source-drain and gate bias, respectively. To connect the gate, the needle was immersed in the liquid electrolyte. Although we did not measure the capacitance of the electrolyte in our specific geometry one can assume an average value of 11 μF cm<sup>-2</sup> as the lower bound, as has been determined in previous measurements of the same electrolyte<sup>7</sup>. Synaptic plasticity measurements were performed with a Keysight 33500B waveform generator and for switching response measurements a PeakTech 1325 USB oscilloscope was also used. Vacuum measurements were performed with a Lakeshore CRX-VF probe station.

#### Data availability

The raw data that support the plots within this paper and other findings of this study are provided in the Supplementary Information and are available from the authors upon reasonable request.



## A.2 Ionic liquid gating of single walled carbon nanotube devices with ultra-short channel length down to 10 nm

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### **Abstract**

Ionic liquids enable efficient gating of materials with nanoscale morphology due to the formation of a nanoscale double-layer that can also follow strongly vaulted surfaces. On carbon nanotubes this can lead to the formation of a cylindrical gate layer, allowing an ideal control of the drain current even at small gate voltages. In this work we apply ionic liquid gating to chirality sorted (9, 8) carbon nanotubes bridging metallic electrodes with 20 nm and 10 nm gap size. The devices exhibit diameter-normalized current densities of up to 2.57 mA/ $\mu\text{m}$ , on-off ratios up to  $10^4$  and a subthreshold swing of down to 100 mV/dec. Measurements after long vacuum storage indicate that the hysteresis of ionic liquid gated devices not only depends on the  $V_{\text{GS}}$  sweep rate and the polarization dynamics but also on charge traps in the vicinity of the carbon nanotube, which in turn might act as trap states for the ionic liquid ions. The ambipolar transfer characteristics are compared to calculations based on the Landauer-Büttiker formalism. Qualitative agreement is demonstrated, and the possible reasons for quantitative deviations and possible improvements to the model are discussed. Besides being of fundamental interest, the results have potential relevance for biosensing applications employing high density device arrays.

### **Contribution**

I performed all electrical measurements and major parts of the data analysis. Alexander Janissek prepared the samples and Artem Fediai developed the theoretical model. I wrote the major part of the manuscript and produced the final version.

# Ionic liquid gating of single-walled carbon nanotube devices with ultra-short channel length down to 10 nm

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## ABSTRACT

Ionic liquids enable efficient gating of materials with nanoscale morphology due to the formation of a nanoscale double layer that can also follow strongly vaulted surfaces. On carbon nanotubes, this can lead to the formation of a cylindrical gate layer, allowing an ideal control of the drain current even at small gate voltages. In this work, we apply ionic liquid gating to chirality-sorted (9, 8) carbon nanotubes bridging metallic electrodes with gap sizes of 20 nm and 10 nm. The single-tube devices exhibit diameter-normalized current densities of up to 2.57 mA/ $\mu\text{m}$ , on-off ratios up to  $10^4$ , and a subthreshold swing down to 100 mV/dec. Measurements after long vacuum storage indicate that the hysteresis of ionic liquid gated devices depends not only on the gate voltage sweep rate and the polarization dynamics but also on charge traps in the vicinity of the carbon nanotube, which, in turn, might act as trap states for the ionic liquid ions. The ambipolar transfer characteristics are compared with calculations based on the Landauer-Büttiker formalism. Qualitative agreement is demonstrated, and the possible reasons for quantitative deviations and possible improvements to the model are discussed. Besides being of fundamental interest, the results have potential relevance for biosensing applications employing high-density device arrays.

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Single-walled carbon nanotubes have been a subject of study for nearly three decades, and over 20 years have passed since the first carbon nanotube transistor had been reported by Tans *et al.*<sup>1</sup> Since then, research in the field of carbon nanotube electronics has explored the potential of both high-performance and thin-film transistors,<sup>2</sup> and with the recent realization of the first carbon nanotube-based microprocessor,<sup>3</sup> the vision of carbon nanotubes replacing silicon seems to be within reach. As in classical silicon electronics, reducing the channel length of a carbon nanotube transistor enhances the device performance, and sub-10 nm channel lengths have been

demonstrated in solid-state devices.<sup>4,5</sup> One of the challenges in making ultra-short channel devices is the fabrication of the gate dielectric and electrode in closest proximity.

A rather simple, low-cost approach is employing liquid gating, where the double layer that forms on any surface is subjected to an electrolyte that functions as an insulating layer appropriate for electric field gating.<sup>6-8</sup> A disadvantage of liquid gating is the inherently low ion mobility in electrolytes, which makes liquid gated devices not suitable for high-frequency transistors. Consequently, the cutoff frequency of electrolyte gated organic transistors is currently limited to the kHz

## A.2 Ionic liquid gating of SWCNT devices with ultra-short channel lengths

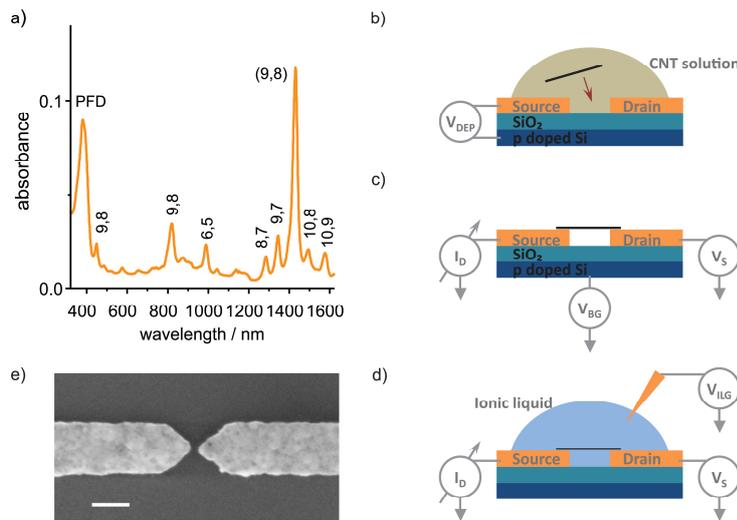
regime<sup>8,9</sup> and even the predicted 10 MHz<sup>10</sup> is far below the 100 GHz<sup>11,12</sup> operation shown for solid gated CNT transistors. However, for ultra-low power operation devices<sup>13</sup> and for biological and chemical sensing applications, where the response time is less demanding, liquid gating—in particular, in water-based electrolytes—is of great interest.<sup>14</sup> Also, the usage of a hydrogen-doped poly(ethylene glycol) monomethyl ether gated CNT transistor as an artificial synapse was already realized.<sup>15</sup> Several groups have demonstrated liquid gating as an effective way of gating carbon nanotubes using a range of different electrolytes, such as NaCl,<sup>16,17</sup> KCl,<sup>18</sup> PEO/LiClO<sub>4</sub> polymer,<sup>19</sup> and phosphate buffer.<sup>20–23</sup> More recently, ion gels consisting of the ionic liquid [EMIM][FAP] and a fluorinated polymer were also used.<sup>24</sup> Ionic liquids and gels have the great advantage that their vapor pressure is negligible, and as molten salts, their screening length is expected to be on the scale of the ionic radii and, hence, sub-nanometer.

While these existing works took advantage of the large capacitance and nanoscopic dimension of the ionic double layer, a reduction in the source/drain dimensions—i.e., the other critical parameter for transistor miniaturization—has not been tested extensively. In this work, we consequently investigate ionic liquid gated ultra-short channel transistor devices with source-drain separations down to 10 nm, which—as we show—exhibit superior electrical characteristics. Since the experiments were performed with mono-chiral (9, 8) carbon nanotubes, and due to the short channel length of the devices, a direct comparison with a rather simple model calculation based on the

Landauer–Büttiker formalism for a ballistic carbon nanotube is possible; this lays the basis for future in-silico optimization of device parameters.

Our nanotubes were produced by a selective catalytic CVD method,<sup>25,26</sup> dispersed in toluene by wrapping in poly(9,9-di-n-dodecylfluorenyl-2,7-diyl) (PFD), and purified and length sorted by gel filtration. For details, we refer to Refs. 27 and 28. The absorption spectrum in Fig. 1(a) gives evidence for a high content of (9,8) nanotubes and the presence of (8,7), (9,7), (10,8), and (10,9) species in minor concentrations in the dispersion. To comply with the nominal charge transfer length for side-contacted nanotubes,<sup>29</sup> fractions of length-sorted (9,8) nanotubes were selected for depositions such that nanotubes were at least 200 nm longer than the distance between the source-drain electrodes. Mono-chiral (9, 8) nanotube transistors with Pd source-drain electrodes were fabricated on 300 nm SiO<sub>2</sub>/p-doped Si substrates by electron-beam lithography, metallization, and simultaneous electric field site-selective-assisted deposition of single nanotubes (dielectrophoresis),<sup>27</sup> as illustrated schematically in Figs. 1(b) and 1(c). A representative contact with a gap size of 20 nm before nanotube deposition is shown in Fig. 1(e). Since scanning electron imaging before measurements is not advisable and after the application of the ionic liquid not possible, we refer for images with nanotubes to comparable devices shown in Ref. 27.

The electrochemical window given by the anodic and cathodic limits is defined as the difference between the reduction and oxidation potential of anions and cations, respectively. Here, an increasing water



**FIG. 1.** (a) Absorption spectrum of length-fractionated, PFD-polymer wrapped carbon nanotubes dispersed in toluene containing mainly the (9, 8) chirality. (b) Deposition of CNTs from the dispersion by dielectrophoresis at bias voltage  $V_{DEP}$  onto Pd electrodes/300 nm-SiO<sub>2</sub>/p-Si. After CNT deposition, the sample was rinsed with toluene. (c) and (d) Measurement of drain current ( $I_D$ ) vs source bias ( $V_S$ ) and ionic liquid gate voltage ( $V_{ILG}$ ). (e) Scanning electron micrograph of a device before nanotube deposition. The gap size between Pd electrodes is 20 nm. The scalebar is 100 nm.

content results in narrowing of the electrochemical window at both the cathodic and anodic limits, which is most likely caused by water electrolysis.<sup>30</sup> Depending on the water content, different anodic and cathodic limits for [EMIM][TFSI] can be found in the literature. For 24 h 333 K vacuum dried samples ( $\text{H}_2\text{O}$  content 105 ppm), O'Mahony *et al.*<sup>31</sup> measured  $-2.2\text{ V}$  ( $-2.4\text{ V}$ ) as the cathodic limit and  $2\text{ V}$  ( $2.2\text{ V}$ ) as the anodic limit vs an  $\text{Fc}/\text{Fc}^+$  reference electrode at a current density of  $1\text{ mA}/\text{cm}^2$  ( $5\text{ mA}/\text{cm}^2$ ). For an  $\text{H}_2\text{O}$  content of 3385 ppm in an ambient atmosphere, the cathodic limit reduces to  $-1.2\text{ V}$  ( $-2\text{ V}$ ) and the anodic limit to  $1.6\text{ V}$  ( $1.7\text{ V}$ ). In a different approach where the ionic liquid is dried with sparging  $\text{N}_2$  (no water content given), the cathodic and anodic limit vs an  $\text{Ag}/\text{AgCl}$  reference electrode is  $-2.07\text{ V}$  and  $2.2\text{ V}$ .<sup>32</sup> For the liquid gating in our experiments, a small drop of the ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide [EMIM][TFSI] was placed on top of the sample. To reduce the water content, our samples were stored for 12 h at  $50^\circ\text{C}$  and 5 mbar in a vacuum oven prior to further investigations. In our measurements, we have used probe needles made from beryllium copper, whereby the electrode material could have some influence on the electrochemical window due to irreversible electrode reactions at the reductive and oxidative limits. However, for all our measurements, we never exceeded  $|V_{\text{GS}}| \leq 1.9\text{ V}$  (typically  $\leq 1.5\text{ V}$ ) to stay within the electrochemical window as lower bound. Moreover, the overall device behavior did not change when sweeping up to  $1.9\text{ V}$  compared to the  $1.5\text{ V}$  sweeps, indicating that no irreversible electrochemical reactions take place. Transfer and output curves were measured at room temperature in a high vacuum using the wiring scheme in Fig. 1(d) using a Lakeshore CRX-VF probe station. A Yokogawa 7651 DC source was used to apply  $V_{\text{DS}}$  to the drain electrode. To allow for highly accurate current determination, the drain current  $I_{\text{D}}$  was measured using a current preamplifier (1211 DL Instruments) and an HP 34401 A voltage meter. For the gate voltage  $V_{\text{GS}}$  and gate current  $I_{\text{G}}$ , a Keithley 2450 was used. The charge transport calculations are based on the Landauer-Büttiker formalism,<sup>33</sup> and consider assumptions for the band alignment, doping, temperature, and gate control imperfection due to quantum capacitance. The code has been implemented in python, and the main code, as well as the input functions and parameters, is available online.<sup>34</sup> The simulation model allows simple and quick calculations by considering a perfect ballistic nanotube, where losses occur only at the CNT/electrode contacts.

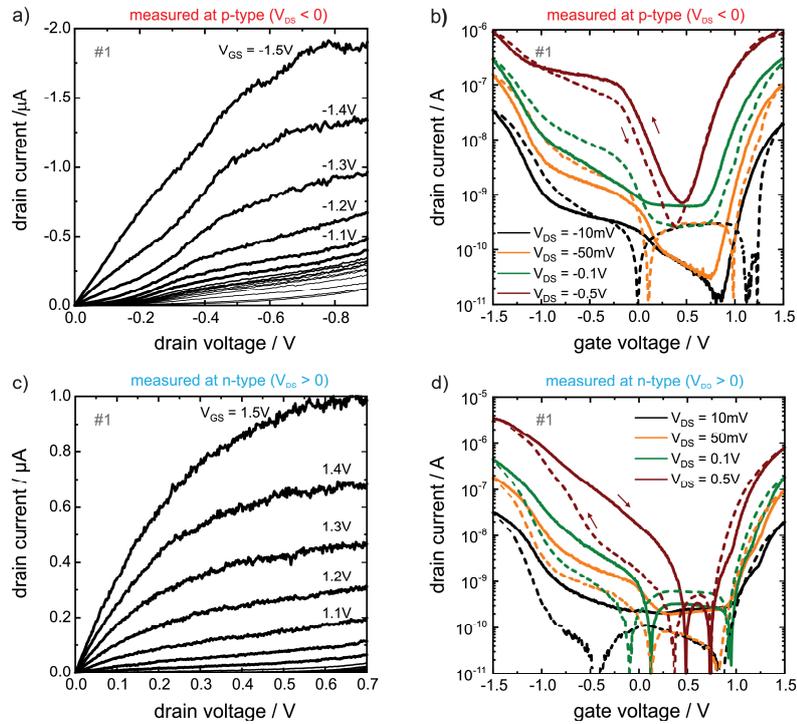
The electrolyte gated CNT transistors typically show on-off ratios up to  $10^4$ , a subthreshold swing down to  $100\text{ mV}/\text{dec}$ , and a maximum diameter-normalized current density of  $2.57\text{ mA}/\mu\text{m}$ . The latter value slightly outperforms  $2.41\text{ mA}/\mu\text{m}^4$  of a solid gated CNT transistor with similar device dimensions at the same source-drain voltage of  $-0.5\text{ V}$ , which demonstrates the high quality of our devices. We have measured various devices that are labeled with #1–3 for a channel length of  $20\text{ nm}$  and #4–5 for a channel length of  $10\text{ nm}$ . Output and transfer characteristics of a  $20\text{ nm}$  channel length CNT transistor (device #1) are given in Fig. 2 for negative  $V_{\text{DS}}$  (a) and (b) and positive  $V_{\text{DS}}$  (c) and (d). The transfer curves for all devices exhibit ambipolar transport for electrons and holes. Despite the short channel length of  $20\text{ nm}$ , only small short channel effects were observable: For one, at small  $V_{\text{GS}}$ , the output curves exhibit a non-ideal saturation of the drain current  $I_{\text{D}}$ . Second, in the transfer characteristics, a slight  $V_{\text{DS}}$ -dependent shift of the threshold voltage  $V_{\text{th}}$ , which is related to drain-induced barrier lowering,<sup>35</sup> could be measured. The current

plateaus in Fig. 2(b) for  $V_{\text{GS}} < 0$  can be associated with contributions of the second band, as will be explained in the theory section. Even devices with a channel length of only  $10\text{ nm}$  show almost ideal electrical device characteristics with a complete saturation in the output current, well defined off and on regime in the transfer curves with a steep subthreshold slope (see the supplementary material, Fig. 1, device #5). The absence of noteworthy short channel effects can be explained by the high capacity and, hence, large gate coupling of the ionic liquid that allows for an almost complete control of the charge carrier density throughout the CNT.<sup>36</sup> The best measured subthreshold swing for a  $10\text{ nm}$  channel length transistor (see the supplementary material, Fig. 2 device #4) was  $100\text{ mV}/\text{dec}$ , which compares well with  $94\text{ mV}/\text{dec}$  of solid-state gated short-channel FETs ( $L_{\text{ch}} = 9\text{ nm}$ )<sup>1</sup> and again underlies the excellent electrical parameters of our devices. A more detailed comparison between this work and literature can be found in the supplementary material, Table 1.

It is noticeable in all our transistors that the transfer curves are shifted to positive gate values, which indicates p-doping of our transistors. We consequently have analyzed the threshold voltage in greater detail to find the cause of the p-doping. Since the extraction of  $V_{\text{th}}$  for small  $V_{\text{DS}}$  in the p-branch for negative  $V_{\text{GS}}$  of the transfer characteristics is delicate due to different slopes with intermediate plateaus [see Figs. 2(b) and 2(d)], we focus on  $V_{\text{DS}} = -0.5\text{ V}$ . The  $V_{\text{th}}$  values in our measurements are  $0.2\text{ V}$  [device #1, Fig. 2(b)],  $0.22\text{ V}$  [device #2, Fig. 3(a)], and  $0.28\text{ V}$  [device #3, supplementary Fig. S3(d)]. An overview of all  $V_{\text{th}}$  values can be found in the supplementary material, Table 2. In the literature, two main physical reasons for p-type doping are discussed. For one, metal-induced p-doping at the SWCNT/Pd electrode interface<sup>37,38</sup> has been observed for short channel lengths down to  $9\text{ nm}$ .<sup>39</sup> However, the p-doping due to the Pd electrode is not expected as large in our FETs as in traditional CNT-FETs, where the tube is usually embedded into metal electrodes. In contrast, in our devices, the tubes lie on top of the contacts<sup>40</sup> and are potentially additionally protected from contact metal-induced doping by the polymer wrapping around the CNTs. While we cannot exclude contact-induced doping altogether, we anticipate that a second scenario dominates in these particular measurements, the p-doping, namely, residual oxygen dissolved in the CNT's surrounding ionic liquid. The physical reasons for p-doping of oxygen can be a modification of the barrier height at the semiconductor metal interface<sup>41</sup> or that oxygen adsorbates act as electron trap states (thus leading to hole doping) since the LUMO of oxygen lies in between the CNT's bandgap.<sup>42</sup> Also, a combination of both effects has been shown to be possible.<sup>43</sup>

To investigate the influence of residual oxygen and water on the electrical device characteristics in further detail, we performed additional measurements while keeping the samples in vacuum (see the supplementary material, Fig. 3). The initial measurements (which were discussed until now) were conducted in the first two days after loading the samples into the chamber at a pressure of  $6.2 - 2.5 \times 10^{-5}$  mbar. After storing the samples in vacuum for more than two weeks, the pressure had dropped to  $1 \times 10^{-5}$  mbar and we performed a second measurement. In this second measurement (again measured at  $V_{\text{DS}} = -0.5\text{ V}$ ),  $V_{\text{th}}$  decreases for all three devices both in the p-branch for negative  $V_{\text{GS}}$  and in the n-branch for positive  $V_{\text{GS}}$  (see the supplementary material, Table 2). This effect becomes particularly obvious by applying positive  $V_{\text{DS}}$  in device #1, whereby  $V_{\text{th}}$  decreases about  $0.15\text{ V}$ – $0.18\text{ V}$  for different  $V_{\text{DS}}$  values (see the supplementary material

## A.2 Ionic liquid gating of SWCNT devices with ultra-short channel lengths



**FIG. 2.** Electrical transport measurements of the (9, 8) carbon nanotube device (#1) with a channel length of 20 nm under ionic liquid gating measured within two days after loading the sample in the vacuum setup at a pressure of  $6.2 - 2.5 \times 10^{-5}$  mbar. (a-b) P-type and (c) and (d) n-type transfer and output characteristics measured at a  $V_{GS}$  sweep rate of  $26 \text{ mV s}^{-1}$  (solid lines: forward sweep; dashed lines: backward sweep). Gate voltages ( $V_{GS}$ ) and Source-drain voltages ( $V_{DS}$ ) are indicated. For the measurements in (b) (d), we started the gate sweep at  $V_{GS} = +1.5 \text{ V}$  ( $V_{GS} = -1.5 \text{ V}$ ).

Fig. 4 and supplementary material Table 3). These results indicate oxygen to be the main reason for the initial strong p-doping (as previously reported<sup>41–43</sup>) instead of metal-induced p-doping since in this case, the threshold voltage should not be affected by different pressures. It has to be mentioned that water molecules cannot fully excluded to be the reason for the initial p-doping. However, we could not find conclusive evidence in the literature for this argument.

A further non-ideality of our devices is the hysteresis between forward and backward sweep in the transfer characteristics. Hysteretic behavior in nanoscale transistors is well-known,<sup>44,45</sup> and the higher back sweep current hysteresis [see Fig. 2(b)] can be explained by a slow polarization change in the ionic liquid caused by the diffusion of mobile ions in the liquid electrolyte.<sup>10,46,47</sup> Note that the measurements conducted in Fig. 2(b) were performed as p-type, i.e., starting at  $+1.5 \text{ V } V_{GS}$  and it follows that, e.g., for  $V_{DS} = -10 \text{ mV}$ , for both hole and electron conduction, the current is larger upon tuning the Fermi

level toward the bandgap (i.e., on both p- and n-sides, the current is larger upon tuning that particular conduction channel off). We also find for measurements in the p-mode [also compare Fig. S1(b)] that for high  $V_{DS}$ , the direction of the hysteresis for hole conduction reverses. We anticipate that the reason is that for increasing  $V_{DS}$ , the total current increases, and hence, more charge carriers can be trapped. Charge trapping (potentially by residual water<sup>44</sup> or oxygen molecules around the nanotube<sup>42,43</sup>) dominates the slow polarization effect of the ionic liquid, which results in a lower back sweep current hysteresis for  $V_{DS} = -0.5 \text{ V}$  [see Figs. 2(b), 3(a), and supplementary material Figs. S1(b) and S3(d)]. In the second measurement performed after the devices had been stored in vacuum for more than two weeks, the counterclockwise hysteresis is reduced consistent with a reduction in the water and oxygen concentration, as also put forward in the literature previously<sup>44,45</sup> [see the supplementary material, Fig. S3(d) again for high  $V_{DS}$ ]. The remaining small hysteresis might be due to residual

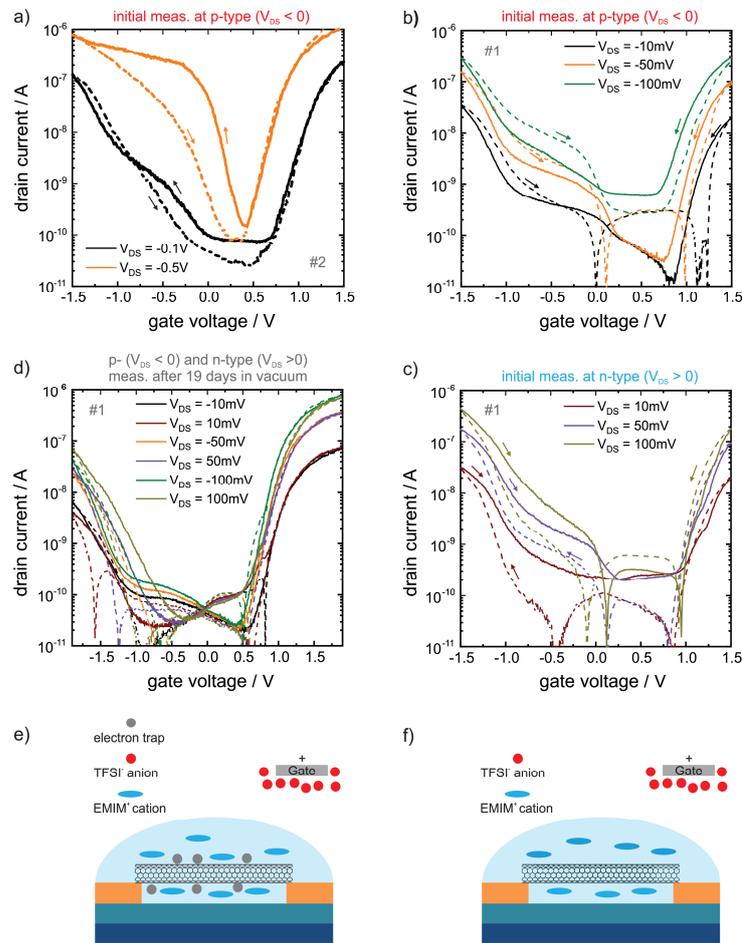
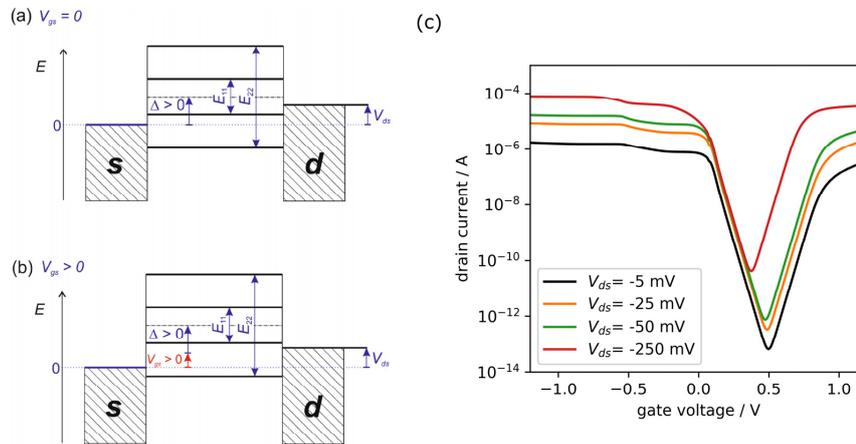


FIG. 3. P-type transfer characteristic of (a) device #2 ( $p = 5.4 \times 10^{-5}$  mbar, measured within two days after loading the sample in the vacuum setup) with  $L_{ch} = 20$  nm. (b) and (c) first measured ( $p = 2.5 \times 10^{-5}$  mbar and  $V_{GS}$  sweep rate,  $26 \text{ mV s}^{-1}$ ) p- and n-type transfer characteristics of device #1. (d) P- and n-type transfer characteristics of the same device after storing the sample in vacuum ( $p = 1 \times 10^{-5}$  mbar and  $V_{GS}$  sweep rate  $10 \text{ mV s}^{-1}$ ). (e) Schematic illustration of the higher pressure first measurement with electron traps (oxygen and water) in the vicinity of the nanotube, which attracts the EMIM<sup>+</sup> cation of the ionic liquid. (f) Analog scenario with reduced traps after storing the sample in vacuum for the lower pressure second measurement. With less trapped electrons and, hence, less attracted cations, the hysteresis decreases.

water still present in high vacuum, as recently shown by Kettner *et al.*,<sup>49</sup> and due to the still existing slow polarization effect. We have found a further interesting point upon measuring the devices for small  $V_{DS}$  ( $|V_{DS}| = 10, 50, \text{ and } 100 \text{ mV}$ ), which had a smaller water and oxygen content [for most devices, this was the case after storage for

two weeks in vacuum [Fig. 3(d)], and others apparently were cleaner and showed this effect immediately [e.g., Fig. 3(a)]. The effect can be seen clearer in the devices presented in Figs. 3(b)–3(d) for the electron branch (positive gate-source voltages). While after directly loading back the devices [Figs. 3(b) and 3(c)] on the electron side, a higher current back

## A.2 Ionic liquid gating of SWCNT devices with ultra-short channel lengths



**FIG. 4.** Simulations (a) and (b) band alignment of the carbon nanotube with respect to the source (s) and drain (d) contact, with the energy difference  $E_{11}$  and  $E_{22}$  of the first and second pair of bands, the doping parameter  $\Delta$ , source-drain voltage  $V_{DS}$ , and gate voltage  $V_{GS}$ . (c) Calculated transfer characteristic for a (9,8) carbon nanotube using the Landauer–Büttiker formalism with parameters  $E_{11} = 0.879$  eV,  $E_{22} = 1.533$  eV,  $\Delta = 0.5$  eV,  $T = 300$  K, screening length  $l = 1.7$  nm, and dielectric permittivity of the ionic liquid  $\epsilon = 12$ .

gate hysteresis could be seen (consistent with the slow polarization dynamics of the ionic liquid), after two weeks in vacuum, all hysteresis for  $V_{GS} > 0$  has vanished [see Fig. 3(d)]. This is surprising at first sight since *a priori* one might anticipate that the polarization dynamics of the ionic liquid is not dependent on the residual water content and should affect both  $V_{GS} < 0$  and  $V_{GS} > 0$  branches similarly. One can explain the effect, however, as schematically shown in Fig. 3(e), by anticipating that oxygen and water in the vicinity of the tube trap electrons, which, in turn, then attract cations from the ionic liquid. These trapped cations remain longer in the vicinity of the tube, thus leading to the higher current back sweep hysteresis for  $V_{GS} > 0$ . While it is well established that oxygen molecules can act as electron trap states,<sup>42,43</sup> it has been shown that water molecules can trap both electrons<sup>49</sup> and holes.<sup>50</sup> We can only speculate why for ionic liquid gated CNT transistors, water tends to trap predominantly electrons. If the number of trap states is reduced, the cations become more mobile, and hence, the hysteresis reduces. We, thus, believe that this is a hysteresis mechanism for ionic liquid gating, which is relevant at the slow sweeping frequencies that we have used and complements the usually found hysteresis mechanism of ionic liquids at higher frequencies. As a consequence, for the same sweep rate of  $10$  mV  $s^{-1}$ , forward and backward sweeps for positive  $V_{GS}$  are almost identical in Fig. 3(d), whereas the hysteresis remains observable for negative  $V_{GS}$ .

The influence of oxygen and water is further underlined by comparing the electron and hole conduction branches between the first and second measurements. Supplementary material Figs. S3 and 3(b)–3(d) show that in the second measurement (i.e., after devices had been stored in vacuum for more than two weeks),  $I_{on}$  in the p-branch decreases, while  $I_{on}$  in the n-branch increases. This effect has been widely

discussed<sup>41–43</sup> and can be explained by a reduction in the oxygen concentration in vacuum with a subsequent reduction in the injection barrier for electrons at the contacts. The superior electron conduction in the second measurement in Fig. 3(d) in the absence of hysteresis and almost identical curves for positive and negative  $V_{DS}$  for  $V_{GS} > 0$  indicates nearly ideal electron transport characteristics without external influences.

After discussing the non-idealities in the electrical characteristics, we now try to obtain possible experimental knowledge for device improvement by performing the charge transport calculation based on the model developed on the basis of Landauer–Büttiker (LB) formalism for a ballistic carbon nanotube as described in the supplementary material, Sec. S1. The effect of the quantum capacitance has been taken into account, as described in the supplementary material, Sec. S2. The main code, input functions, and all parameters are available in a repository.<sup>54</sup>

Having computed both quantum and electrostatic capacitances, we have found that for a given ionic liquid (dielectric permittivity  $\epsilon = 12$  and<sup>51</sup> screening length  $l = 1.7$  nm<sup>52</sup>) the quantum capacitance has the same order of magnitude as the electrostatic gate capacity and, thus, cannot be neglected. Figures 4(a) and 4(b) illustrate the CNT's band alignment for zero  $V_{GS}$  and  $V_{GS} > 0$ . In the proposed model, the shift of the Fermi level due to p doping is taken to be 0.5 eV, so that the Fermi level slightly penetrates the first valence energy band. This is consistent with Ref. 40, which shows that even for the on-top contact, the Fermi level lies slightly below the valence band edge. The p-type simulated data for varying  $V_{DS}$  values [see Fig. 4(c)] show V-shaped transfer characteristics and a threshold voltage shift to lower  $V_{GS}$  for increasing negative  $V_{DS}$ . Concerning the shape and structure of the curves in Figs. 2(b) and 3(a), the experiment and model are in qualitatively good agreement. The slight asymmetry in

the on-state current of the experimental data might be attributed to different Schottky barriers for electrons and holes, whereby the LB model assumes symmetric Ohmic contacts. At  $V_{GS} \approx -0.25 \dots -0.5$  V in Fig. 4(c), the current increases again after a first saddle point due to the contribution of the second band. The increase in the current occurs steadily, because of the quantum capacitance (see the [supplementary material](#), Fig. S8). A saddle point with a subsequent increase in the current can also be seen in the experimental data in Fig. 2(b).

Both experimental and simulation data feature ambipolar transfer characteristics, which is explained by a strong gate control due to a liquid gate. As shown in Fig. S8 of the [supplementary material](#), the effect of the quantum capacitance does not affect the magnitude of the subthreshold swing. An experimentally observed SS value of 100 mV/dec (vs theoretical 60 mV/dec) has to be, thus, related to the residual polymer (PFD), short-channel effects, and other factors.

Except for the high drain-source voltage, the experimental data demonstrate a diverse shape of the transfer curve, while the model always predicts V-shaped characteristics. This cannot be explained by internal nanotube properties and is not captured by a proposed model. We may speculate that it may be caused by shallow charge traps, where de-trapping requires higher drain-source voltages.

Another important discrepancy between the model and the experiment is the difference in the on-current, which reaches two orders of magnitudes. As far as the tube contacts are p-type doped, we expect no Ohmic barriers at least for the p-branch. The current reduction can, thus, be primarily related to the effect of the polymer wrapping, which may increase an effective distance between the tube and the metallic electrode; this may be critical in on-top geometry where orbitals of the metal only overlap with a few bottom C atoms of the tube. As a result of these two effects, despite a considerable overlap ( $\sim 100$  nm contact length), the tube may still be unable to accept all the current from the metal. In Ref. 40, it has been shown that the necessary contact length quickly increases as the coverage of the tube by the metal decreases. The expected increase in the tube-metal separation due to the residual polymer would facilitate this effect greatly, as the orbital overlap drops exponentially with the interatomic distance.

In summary, we have shown high-performance nanoscopic SWCNT transistors in which the use of an electrolyte gate allows efficient control of the electrostatics in the nanoscopic channel even though the channel is made as short as 10 nm. Our transistors show a small subthreshold swing down to 100 mV/dec and diameter-normalized current densities as high as 2.6 mA/ $\mu$ m, which is comparable to all-solid-state short-channel SWCNT transistors.<sup>7</sup> Whereas a higher current back sweep hysteresis in ionic liquids usually is attributed to the ion dynamics in the ionic liquid itself, we have identified that electron trapping can also lead to the same type of hysteresis. The favorable device characteristics allow good comparison with the developed model based on Landauer-Büttiker formalism, including the effect of the quantum capacitance. Based on this model, the theoretically reachable performance of fabricated devices has been estimated, and the experimental data have been validated. From the simulations, we can deduce that a reduction of traps influencing the subthreshold slope and the better contact between the SWCNTs and the metal will improve the device characteristics even further.

See the [supplementary material](#) for additional electrical measurements and details on the simulation.

The experiments were conceived and designed by R.K., T.W., F.P., and A.F. The nanotube raw material was provided by L.W. and Y.C. and was purified and length fractionated by F.H. and M.M.K. Devices were fabricated by A.J., M.G., and S.D. The ionic liquid gating was performed by J.L., F.G., A.J., and M.G. The software was written by A.F. Simulations were performed by A.J. and A.F. This manuscript was written by R.K., J. L., T.W., and A.F. with input from all coauthors.

A.J. and J.L. contributed equally to this work.

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#### DATA AVAILABILITY

The data that support the findings of this study are either available from the corresponding author upon reasonable request or available in GitHub repository, Ref. 34.

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## A.2 Ionic liquid gating of SWCNT devices with ultra-short channel lengths

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## A.3 High-Performance Vertical Organic Transistors of Sub-5 nm Channel Length

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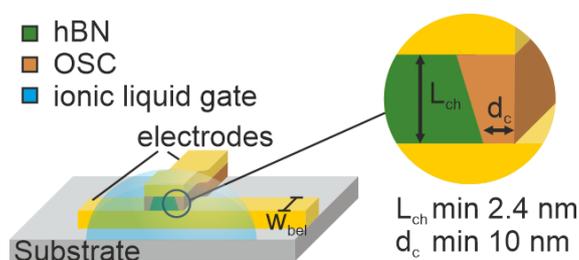
### Abstract

Miniaturization of electronic circuits increases their overall performance. Electronics based on organic semiconductors have up to now not played an important role in the miniaturization race. Here, we show the fabrication of liquid electrolyte gated vertical organic field effect transistors with channel lengths down to 2.4 nanometers. These ultra-short channel lengths are enabled by the atomically precise thickness and flatness of an insulating hexagonal boron nitride spacer separating the vertically aligned source and drain electrodes. The transistors reveal promising electrical characteristics with output current densities up to  $2.95 \text{ MA cm}^{-2}$  at  $-0.4 \text{ V}$  bias, on-off ratios of  $10^6$ , a steep subthreshold swing of  $65 \text{ mV/dec}$  and a transconductance of  $714 \text{ S m}^{-1}$ . Realizing channel lengths in the sub-5 nanometer regime and operation voltages down to  $100 \mu\text{V}$  proves the potential of organic semiconductors for future highly integrated or low power electronics.

### Contribution

I performed all sample preparations, experiments and data analysis. The first draft of the manuscript was written entirely by me and I produced the final version. All figures were designed by me.

### Table of Contents Graphic



## High-Performance Vertical Organic Transistors of Sub-5 nm Channel Length

Jakob Lenz, Anna Monika Seiler, Fabian Rudolf Geisenhof, Felix Winterer, Kenji Watanabe, Takashi Taniguchi, and Ralf Thomas Weitz\*

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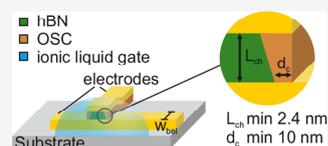
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**ABSTRACT:** Miniaturization of electronic circuits increases their overall performance. So far, electronics based on organic semiconductors has not played an important role in the miniaturization race. Here, we show the fabrication of liquid electrolyte gated vertical organic field effect transistors with channel lengths down to 2.4 nm. These ultrashort channel lengths are enabled by using insulating hexagonal boron nitride with atomically precise thickness and flatness as a spacer separating the vertically aligned source and drain electrodes. The transistors reveal promising electrical characteristics with output current densities of up to  $2.95 \text{ MA cm}^{-2}$  at  $-0.4 \text{ V}$  bias, on–off ratios of up to  $10^6$ , a steep subthreshold swing of down to  $65 \text{ mV dec}^{-1}$  and a transconductance of up to  $714 \text{ S m}^{-1}$ . Realizing channel lengths in the sub-5 nm regime and operation voltages down to  $100 \mu\text{V}$  proves the potential of organic semiconductors for future highly integrated or low power electronics.

**KEYWORDS:** vertical organic transistor, electrolyte gate, organic electronics, nanogap electrodes, molecular electronics



### INTRODUCTION

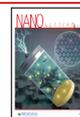
Organic field effect transistors (OFETs) are a critical ingredient for flexible and low cost electronics.<sup>1–5</sup> Despite the spectacular increase in mobilities of up to  $10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-16-8}$  in the past years, it still requires improvement to meet the prerequisites of integrated logic. Downscaling of the organic transistor dimension is a promising pathway to compensate the slow switching behavior and comparably low output currents at usually high (i.e.,  $>10 \text{ V}$ ) operation voltages.<sup>9</sup> This strategy is also used in commercial silicon transistors where in 2020 the production of 5 nm node chips has started.<sup>10</sup> However, there are only few reports of organic transistors with nanoscopic device dimensions<sup>11–15</sup> and it remains unclear whether the device functionality can be preserved at such short length scales. Additionally, fabricating nanometer contact separation compatible with organic semiconductors (OSCs) is nontrivial; to reach nanometer source–drain distances, typically techniques such as mechanical breakjunctions, electromigration, or electrochemical deposition are used<sup>16,17</sup> with the aim of implementing single molecule transistors.<sup>18,19</sup> In such geometries, the realization of an effective gate electrode is very challenging, and even for high capacitance ionic liquid gated devices the output current is limited to the nanoampere regime.<sup>20,21</sup> Moreover, in such nanoscopic device dimensions organic transistors suffer from short channel effects<sup>22</sup> and most prominently contact resistance limitations.<sup>9</sup> One successful strategy to allow for easier device scaling has been to implement vertical organic field effect transistors (VOFET) in which submicrometer channel lengths can be realized with simple processing

steps.<sup>23–26</sup> Additionally, VOFETs can show performance superior to lateral transistors. For example, in our previous work we introduced VOFETs with a liquid electrolyte gate that can drive on-state current densities of above  $3 \text{ MA cm}^{-2}$ , have an on/off current modulation of up to  $10^8$  and transconductances of up to  $5000 \text{ S m}^{-1}$ .<sup>26</sup> The insulating spacer between the top and bottom electrode was made of  $\text{SiO}_2$  and channel lengths down to 40 nm could be realized. The minimal thickness was mainly limited by the breakdown voltage of the  $\text{SiO}_2$  layer. This implies, that in our previous work, the minimal possible channel length was not limited by the organic semiconductor. However, it is *per se* unclear if organic materials can show good performance in FETs at a few nanometers length scale. To test out the limits in device scaling, we consequently needed to look for alternative dielectrics that are easy to manufacture and preserve good isolation properties also at the few nanometers scale. Thus, we have developed an approach using hexagonal boron nitride (hBN)<sup>27</sup> as an insulator, whereby channel lengths in the sub-5 nm regime could be consistently realized. To our surprise, even at these small channel lengths the encouraging device performance of our previous work<sup>26</sup> could be preserved.

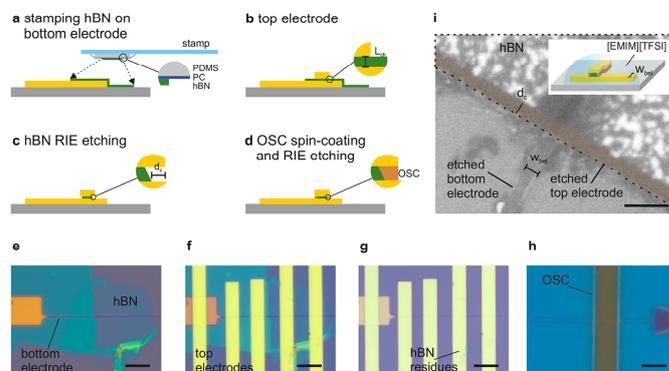
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## A.3 High-Performance Vertical Organic Transistors of Sub-5 nm Channel Length



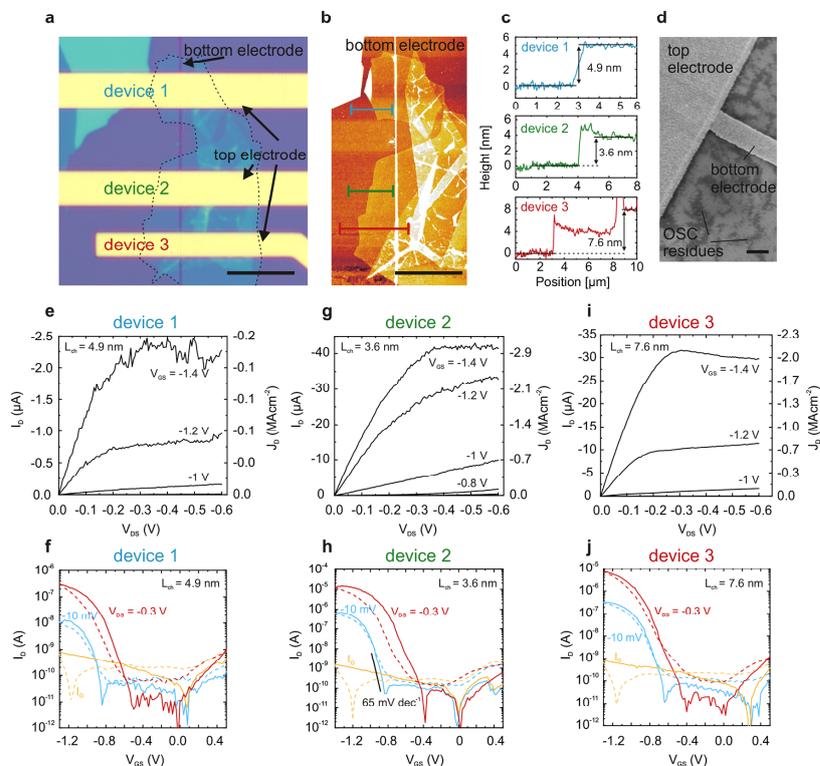
**Figure 1.** Device fabrication process. (a) Stamping of few-layer hBN flakes on bottom electrodes fabricated by e-beam lithography. (b) Patterning of the top electrode by e-beam lithography. (c) The devices were etched isotropically via RIE to fabricate under-etched top electrodes. (d) Spin-coating of the OSC solution and subsequent  $O_2$  RIE. (e) Optical microscopy image of a stamped hBN flake on top of the bottom electrode (f) after top electrode fabrication and (g) after hBN etching. (h) Polarization microscopy image after OSC etching with bright appearing OSC below the top electrode. (i) SEM image after removing [EMIM][TFSI] and after etching the gold contacts with a  $KI/I_2$  solution. The under-etched region ( $d_c$ ) is colored. The black scale bar is 200 nm. Inset: Finished device with [EMIM][TFSI] droplet as gate electrode.

### RESULTS AND DISCUSSION

hBN is an insulating two-dimensional material with a monolayer thickness of 0.33<sup>28</sup> nm and high breakdown voltages ranging from 0.8<sup>29</sup> to 1.2 V nm<sup>-1</sup>.<sup>30</sup> The device fabrication is illustrated in Figure 1 and described in more detail in the Experimental Section. The two gold electrodes for source and drain contacts were patterned by electron-beam lithography. hBN was first exfoliated on a clean  $SiO_2$  substrate and then transferred on top of the bottom electrode (Figure 1a,e) with a stamp made from a polydimethylsiloxane (PDMS) block and a polycarbonate (PC) film.<sup>31,32</sup> After top contact patterning (Figure 1b,f), the sandwiched hBN layer was isotropically removed via reactive ion etching (RIE) to form an underetched region of width  $d_c$  between the top and bottom electrode (Figure 1c,g). Using  $SF_6$  as the process gas increases the etch isotropy and hence lateral etching rate in the normally vertical directed RIE due to a high density of  $SF_6^*$  and  $F^*$  radicals, which in turn are responsible for bulk etching.<sup>33–36</sup> The process steps, including spin-coating of the donor-acceptor polymer poly(diketopyrrolopyrrole-terthiophene) (PDPP),<sup>26</sup> removal of PDPP via directional RIE, and deposition of the ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide ([EMIM][TFSI]) as the gate electrode, complete the devices.<sup>26</sup> Using ionic liquids as gate care should be taken to not exceed the electrochemical window which is defined by the difference between the oxidation and reduction potential of cations and anions. For the used ionic liquid [EMIM][TFSI], depending on the water content, different anodic (1.7 to 2 V) and cathodic (−2 to −2.4 V) limits can be found in the literature.<sup>37,38</sup> In our experiments, we never exceeded  $|V_{GS}| \leq 1.5$  V. PDPP is removed during the RIE everywhere except below the top electrode (i.e., in the channel) which served as etching mask (Figure 1d,h). The channel length  $L_{ch}$  is defined by the thickness of the used hBN layer. The channel area  $A_{ch}$  (i.e., the transistor footprint) is given by  $A_{ch} = 2w_{bel} \times d_c$  with  $w_{bel}$  being the width of the bottom electrode. While  $w_{bel}$  is defined by the lithography process, the under-etched distance (i.e.,  $d_c$ ) and

hence lateral hBN etching rate was measured with scanning electron microscopy (SEM) after the electrical characterization by prior removal of the gold contacts of a finished sample with potassium iodide ( $KI/I_2$ ) solution (see Figure 1i). The darker former electrodes can be well distinguished from the bright appearing hBN flake (previously covered by the top electrode). The dark grains on top of the hBN flake are the adhesion layers Ti/Cr (that have oxidized to oxygen exposure after gold etching).

Figure 2a shows an optical image of three different transistors on the same hBN flake prior to RIE of hBN. The thickness of the hBN flakes was determined using atomic force microscopy (AFM). An AFM image obtained before deposition of the top electrodes with line traces in the region of the subsequently deposited top electrodes (see Figure 2b,c) reveals hBN thicknesses and hence channel lengths of 4.9 nm for device #1, 3.6 nm for device #2, and 7.6 nm for device #3. An exemplary SEM image after OSC RIE (Figure 2d) illustrates that the OSC is fully removed with some residues remaining on the substrate. Special care was taken during the OSC RIE to avoid any undesired parasitic conduction paths aside from the vertical channel (see Supporting Information (SI) Figure 1). The gate contact was realized by two different configurations (see Experimental Section and SI Figure 2). An overview of all measured devices with corresponding parameters and performance can be found in SI Table 1. The output and transfer characteristics for device #1–3 (measured with gate configuration 2) are displayed in Figure 2e–j. The gate current  $I_G$  is  $V_{DS}$  independent and only shown exemplary (see also SI Figure 3). It has to be noted that the conductivity versus gate voltage of electrolyte-gated devices can exhibit a peaklike behavior<sup>39,40</sup> which results in a negative differential resistance at high  $V_{GS}$ . This effect can be seen in Figure 2h,i and in SI Figure 4 and we usually try to avoid exceeding that peak. The devices exhibit almost ideal electrical device characteristics with fully saturating output currents for high  $V_{GS}$ , on/off ratios of up to  $10^6$  (device #3), a maximum channel width normalized transconductance of 264 S m<sup>-1</sup>

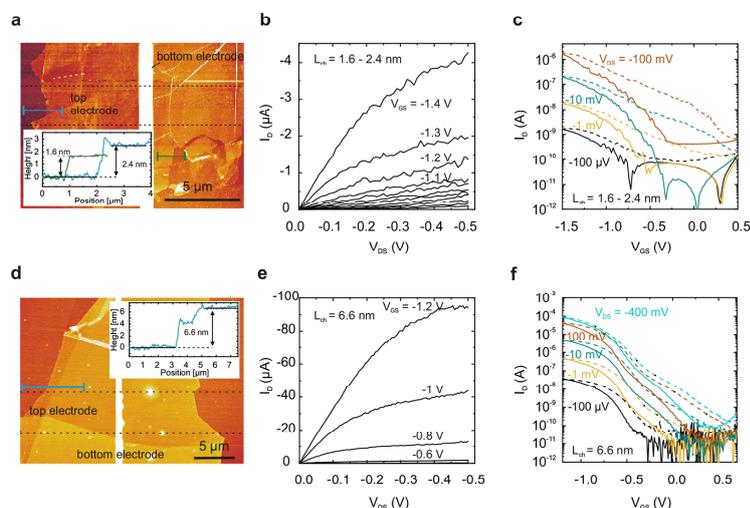


**Figure 2.** Electrical characteristics of ultrashort-channel electrolyte-gated vertical PDPP transistors with  $w_{\text{gate}} = 70$  nm and  $d_c = 10$  nm ( $A_c = 1400$  nm<sup>2</sup>). (a) Optical microscopy image of VOFETs with three top electrodes on the same bottom electrode and same hBN flake before hBN RIE. (b) AFM image of the same hBN flake before top electrode patterning. The black scale bar in (a,b) is 10  $\mu$ m. (c) The line traces represented by different colors are measured at the position of the corresponding top electrodes, indicated in (b). (d) SEM image after OSC RIE. The black scale bar is 500 nm. (e,f) Output and transfer characteristics with corresponding gate current  $I_G$  for device #1, (g,h) for device #2, and (i,j) for device #3. The subthreshold swing is schematically indicated in (h). Output curves were measured at a  $V_{\text{DS}}$  sweep rate of 10 mV s<sup>-1</sup> and transfer curves at a  $V_{\text{GS}}$  sweep rate of 40 mV s<sup>-1</sup>. All data were measured with gate configuration 2. The solid lines represent the forward sweep direction, and the dashed lines represent the backward sweep direction.

(device #2), and a very steep subthreshold swing of down to 65 mV dec<sup>-1</sup> (device #2) (more details below). This may seem surprising at first for channel lengths of only a few nanometers. However, electrolyte gating has been proven to facilitate very high gate coupling<sup>41–44</sup> that enables full control of the charge carrier density via ions diffusing sidewise into the semi-conducting channel. In this way, short channel effects are drastically decreased.<sup>45,26</sup> Because contact resistances<sup>9,26,15</sup> also can be substantially reduced, this technology opens the way to fabricate nanoscopic organic transistor devices.<sup>46</sup> The lowest subthreshold swing of 65 mV dec<sup>-1</sup> (device #2,  $V_{\text{DS}} = -10$  mV), which was extracted by fitting an exponential function to the transfer data below  $V_{\text{th}}$ , almost reaches the theoretical thermionic limit at room temperature of 60 mV dec<sup>-1</sup>, whereas for  $V_{\text{DS}} = -0.3$  V a subthreshold swing of 107 mV dec<sup>-1</sup> was calculated. It is well established for MOSFETs that in the sub-100 nm regime the subthreshold swing increases for decreasing channel lengths.<sup>47,48</sup> On the other hand the effective channel

length reduces with increasing  $V_{\text{DS}}$  due to a shift of the pinch-off point from the drain to the source electrode.<sup>49</sup> Hence we believe that the increasing subthreshold swing for higher  $V_{\text{DS}}$  can be explained by a reduction of the effective channel length due to the pinch-off. It has to be mentioned that when using ionic liquids as a gate the device performance is sensitively dependent on the ratio between the area of the gate electrode (surface of immersed needle and surface of covered Au gate pad) and the active channel. Here, higher ratios result in higher on-currents caused by more surface charges at the electrode/ionic liquid interface with increased capacities.<sup>50,51</sup> This effect can be seen by applying both gate configurations 1 and 2 on the same devices in S1 Figure 5. The best measured subthreshold swing of 65 mV dec<sup>-1</sup> (device #2) measured for gate configuration 2, for example, reduces to 233 mV dec<sup>-1</sup> for gate configuration 1, whereby the best transconductance of 714 S m<sup>-1</sup> was measured for gate configuration 1 compared to 171 S m<sup>-1</sup> for gate configuration 2 (device #3). The maximum

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**Figure 3.** Limits of device scaling of electrolyte gated vertical PDPP transistors. (a) AFM image before top electrode patterning of the shortest measured device. Inset: Two line traces revealing a channel length between 1.6 and 2.4 nm. The subsequently fabricated top electrode is indicated with dashed lines. The black scale bar is 5  $\mu\text{m}$ . (b) Corresponding output and (c) transfer characteristics ( $w_{\text{bel}} = 1 \mu\text{m}$ ,  $d_c = 45 \text{ nm}$ ), both measured with gate configuration 2. (d) AFM image before top electrode patterning of the device with the highest on-current  $I_{\text{on}}$ . Inset: Line trace showing a channel length of 6.6 nm. The subsequently fabricated top electrode is indicated. The black scale bar is 5  $\mu\text{m}$ . (e,f) Corresponding output and transfer characteristics ( $w_{\text{bel}} = 500 \text{ nm}$ ,  $d_c = 80 \text{ nm}$ ), both measured with gate configuration 1. Output characteristics are measured at a  $V_{\text{DS}}$  sweep rate of 10  $\text{mV s}^{-1}$  and transfer characteristics at a  $V_{\text{GS}}$  sweep rate 20  $\text{mV s}^{-1}$ . The solid lines represent the forward and the dashed lines the backward sweep direction.

current density of 2.95  $\text{MA cm}^{-2}$  for  $V_{\text{DS}} = -0.4 \text{ V}$  and a channel length of 3.6 nm (see Figure 2g, device #2) compares well to the 3.1  $\text{MA cm}^{-2}$  of our previous work.<sup>26</sup> Interestingly, despite the same device dimensions ( $w_{\text{bel}} = 70 \text{ nm}$ ,  $d_c = 10 \text{ nm}$ ) and the fact that all three devices are on the same hBN flake, devices #2 and #3 exhibit similar on-currents and hence on-state current densities in the  $\text{MA cm}^{-2}$  regime, whereas the on-current density of device #1 is 1 order of magnitude lower in the 100  $\text{kA cm}^{-2}$  regime. The on-current densities (measured at  $V_{\text{DS}} = -0.4 \text{ V}$ ) of all devices vary from 8.89  $\text{kA cm}^{-2}$  to 2.9  $\text{MA cm}^{-2}$  (see Table 1 in the Supporting Information). The huge variance can be explained by an only partial OSC coverage of the underetched channel. We think that the short distance of only a few nanometers between the electrodes might impede the wettability and hence hinder the OSC solution to fully penetrate the underetched region. The yield for high on-state current density devices could be improved by choosing proper solvents with optimized wettability. For example, this could be realized by adding fractions of low surface tension solvents, that is, methanol or hexane, to the OSC solution. Finally, even for channel lengths in the nanometer regime only small short channel effects could be measured. First, for small  $V_{\text{GS}}$  the output curves exhibit small deviations of the ideal saturation behavior. Second, in the transfer curves a small  $V_{\text{DS}}$  dependent shift of the threshold voltage  $V_{\text{th}}$  caused by drain-induced barrier lowering,<sup>53</sup> can be observed.

Encouraged by these results, we tested the extrema both in device scaling of channel length and also how large we could increase the absolute current value. The shortest realized

channel length device is shown in Figure 3a–c (device #16). As can be seen in the AFM image, the transferred hBN flake exhibited wrinkles and folds with a different number of layers. Hence, we measured the thickness at different positions, which was found to vary between 1.6 to 2.4 nm (see line trace in Figure 3a). Even for such extremely short channel lengths the transistor characteristics stay intact and on/off ratios  $> 10^3$  as well as saturating transfer curves can be seen (see Figure 3b). With increasing  $V_{\text{DS}}$ , also the off current increases (see  $V_{\text{DS}} = -100 \text{ mV}$  in Figure 3c), which is related to the large electric field and hence increasing leakage current flowing either through PDPP or hBN. Nevertheless, it is highly encouraging that lithographically defined organic transistors of channel length with less than 2.5 nm can be obtained. Finally, we also wanted to test the highest obtainable absolute currents without increasing the dimensions of the electrodes. This can be done by increasing the underetched distance  $d_c$  in our case to 80 nm. In this device, the maximum on-current was  $\sim 100 \mu\text{A}$  (Figure 3d–f, device #5). Assuming full filling of the underetched region, this calculates to a current density of 125  $\text{kA cm}^{-2}$  close to what has been obtained in previous experiments. These results indicate that by increasing the filling fraction of the channel equivalent on-currents as in our previous work<sup>26</sup> of up to several milliamperes should be achievable. Given the high on-state conductivities, on/off ratios of more than  $10^3$  were within reach even at low power operation with  $V_{\text{DS}}$  of only 100  $\mu\text{V}$  (see Figure 3f). Finally, we observed the expected higher back sweep current hysteresis due to the polarization dynamics of the ionic liquid and the limited diffusion velocity of mobile ions<sup>53,54</sup> for almost all our devices (see Figure 3c,f and also SI

Figure 5 for a comparison of the hysteresis for the different gating configurations). Remarkably, for the devices in Figure 2 we measured a lower back sweep current hysteresis which might be explained by the comparably small distance  $d_c$  of 10 nm. If the ions only have to penetrate such short distances, the polarization response is faster and the hysteresis is dominated by trap states resulting in a lower back sweep current hysteresis.<sup>3,9</sup>

### CONCLUSION

In summary, we have fabricated high-performance nanoscopic vertical organic field effect transistors with channel lengths of down to 2.4 nm with subnanometer precision. The liquid electrolyte gate enables current densities up to 2.95 MA cm<sup>-2</sup> and a subthreshold swing of down to 65 mV dec<sup>-1</sup>. Utilizing such short channel lengths could pave the way for nanoscopic charge transport investigations within single polymer chains by reducing the lateral device dimensions further. The small device dimensions make these transistors an ideal candidate for highly integrated devices. However, the major hurdle of the slow switching speed of ionic liquid gating by implementing solid gates maintaining the electrical characteristics has to be taken. Finally, although we tested only PDPP as an active material we anticipate that this approach, similar to our previous work, provides a blueprint for developing transistors with ultrashort channel lengths and can be generalized to a broad range of OSC materials.

### EXPERIMENTAL SECTION

**Electrode Fabrication.** As first step, all substrates were cleaned for 5 min in an ultrasonic bath in acetone and then isopropyl alcohol and blow-dried with nitrogen. The electrodes were patterned by electron beam lithography (e-line system, Raith). First, a 4.5 wt % solution of the positive-resist polymethyl methacrylate (PMMA) 950 k dissolved in anisole (AR-P 672.045, Allresist) was spin coated onto the substrates at 800 rpm for 1 s and 4000 rpm for 30 s followed by a 3 min 150 °C softbake. After electron beam patterning (10 kV, 108  $\mu\text{C cm}^{-2}$  for 10  $\mu\text{m}$ , 145  $\mu\text{C cm}^{-2}$  for 30  $\mu\text{m}$  and 165  $\mu\text{C cm}^{-2}$  for 60  $\mu\text{m}$  aperture), the resist was developed for 110 s in a 1:3 methylisobutylketone/ isopropyl alcohol mixture. For bottom electrodes, 1 nm Cr (@ 0.3 Å/s) or 1 nm Ti (@ 0.1 Å/s) and 30 nm Au (@ 1 Å/s) and for top electrodes, 0.3 nm Cr or Ti and 100 nm Au were evaporated in an electron beam physical vapor deposition at  $\sim 10^{-7}$  mbar. Cr and Ti are used as adhesion layers between gold and SiO<sub>2</sub>. For the lift-off, the substrates were immersed in acetone at room temperature.

**Insulating hBN Spacer Preparation.** Few-layer hBN flakes were exfoliated on precleaned 300 nm SiO<sub>2</sub> substrates (3 min acetone and isopropanol each). The substrates were etched for 10 s in hydrofluoric acid (5%) to facilitate the later flake pick-up. The as-received hBN crystals<sup>27</sup> were crushed into smaller grains and exfoliated after repeated peeling with scotch tape onto preheated substrates (100–120 °C) by pressing the scotch tape (with thinned down to few layer hBN) for 10–30 s on the substrates. The desired hBN flakes were located using optical microscopy and transferred on the bottom electrode with a stamp made of a PDMS block and a film of PC. PDMS (Sylgard 184, Dowsil) films with a thickness of approximately 2 mm were prepared with a mass ratio of 10.5:1. PC films with a thickness of approximately 10–20  $\mu\text{m}$  were prepared from a solution of PC in chloroform (8 wt %

using a film application machine (ZAA 2300, Zehntner). To fabricate the stamps, a double-sided adhesive tape with a cutout square (approximately 0.5 cm<sup>2</sup>) was placed on a precleaned glass slide. A PDMS block slightly smaller than the tape window was cut out and placed inside the window of the adhesive tape. The PC film was placed on the PDMS block with another tape (again with a cut out square of approximately 1 cm<sup>2</sup>). To pick up a hBN flake, the stamp was brought into contact with the substrate (at 60 °C). The temperature was increased to 70 °C over 5 min. The PDMS–PC block expands and the hBN flake is fully covered. Cooling down the stage to 50 °C over 5 min slowly retracts the stamp and delaminates the hBN from the substrate. Next, the stamp was brought into contact with the hBN flake on top of the bottom electrode (substrate temperature 70 °C). By heating the substrate to 180 °C, the PC melts down and sticks to the SiO<sub>2</sub> substrate. After 30 min, the stamp was moved upward whereby the PC detached from the PDMS. By immersing the substrate in chloroform for 30 min, the melted down PC can be dissolved. Finally, to clean the hBN flakes the substrates were annealed in a vacuum chamber at a pressure of less than  $1 \times 10^{-8}$  mbar for 12 h at 180 °C. After the top electrode fabrication, the sandwiched hBN flakes were etched via reactive ion etching (Oxford Plasmalab 100 ICP RIE) with a SF<sub>6</sub> and Ar plasma (10 sccm SF<sub>6</sub>, 5 sccm Ar, 10 mbar, 50 W). The vertical and lateral hBN etching rate were 1 nm s<sup>-1</sup> and 0.35 nm s<sup>-1</sup>, respectively.

**Organic Semiconductor and Gate Preparation.** PDPP was dissolved in 1,3-dichlorobenzene (Sigma-Aldrich) (15 mg mL<sup>-1</sup>) and stirred for at least 12 h at 80 °C. The semiconductor solution was spin-coated onto the substrates at 1000 rpm for 40 s followed by a bake at 80 °C for 2 min. PDPP was removed everywhere except between the electrodes via RIE with an oxygen plasma (20 sccm, 20 mbar, 10 W), as the top electrode serves as an etching mask. Subsequently, a droplet of the liquid electrolyte gate [EMIM][TFSI] was applied over the conducting channel. To reduce the water content and hence the influence of water electrolysis in the all ionic liquid sample were stored in a vacuum oven (50 °C, 10 mbar, >12 h) prior to electrical measurements. All steps including PDPP preparation and electrical characterization were performed in an ozone-free atmosphere and otherwise ambient conditions.

**Electrical Characterization.** Measurements were performed at ambient condition with a home-built point probe station and two Source Meters (Keithley 2450) as source–drain and gate bias, respectively. The gate contact was realized by contacting an additionally patterned gate gold electrode (gate configuration 1) or by immersing the gate needle directly in the liquid electrolyte (gate configuration 2) (see SI Figure 1).

### ASSOCIATED CONTENT

#### Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acs.nanolett.1c01144>.

Tabular overview of device parameters and performance of all devices; scanning electron microscopy (SEM) imaging after OSC reactive ion etching (RIE); schematic illustration of different gate configurations; gate currents  $I_G$  for varying source–drain bias  $V_{DS}$ ; linear transfer

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characteristics; comparison of transfer characteristics for different gate configurations (PDF)

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#### Author Contributions

The experiments were conceived and designed by J.L. and R.T.W. J.L. prepared the samples, conducted the measurements, and data analysis. A.M.S., F.R.G., and F.W. helped with the sample preparation. J.L. and R.T.W. wrote the manuscript with the input of all authors. R.T.W. supervised the project. K.W. and T.T. synthesized the hBN crystals.

#### Notes

The authors declare no competing financial interest.

### ■ ACKNOWLEDGMENTS

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## A.4 Nanoscopic electrolyte-gated vertical organic transistors with low power operation and five orders of magnitude switching range for neuromorphic systems

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### **Abstract**

Electrolyte-gated organic transistors are promising candidates as a new class of neuromorphic devices in hardware-based artificial neural networks which can outperform their CMOS counterparts regarding time and energy consumption. Here, we utilize vertical electrolyte-gated transistors with a donor-acceptor diketopyrrolopyrrole-terthiophene polymer as active material to reversibly switch the channel conductivity over five orders of magnitude (3.8 nS to 392  $\mu$ S). In addition to fundamental synaptic functions, we also demonstrate operation voltages down to 1 mV to minimize the energy consumption per switching event, which is a prerequisite in terms of upscaling hardware-based artificial neural networks. To investigate the potential of these transistors in future neuromorphic networks, we show the operation of up to 3 interconnected transistors. The high switching range, low operation voltage and basic interconnection highlights the promise of electrolyte-gated organic transistors for future integration into hardware-based neural networks.

### **Contribution**

I invented the device structure and did preliminary experiments using electrolyte gated VOFETs as artificial synapses. Christian Eckel and myself fabricated all the samples and wrote the main manuscript.

### Nanoscopic electrolyte-gated vertical organic transistors with low power operation and five orders of magnitude switching range for neuromorphic systems

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Keywords: electrolyte gated, organic transistor, vertical structure, synaptic plasticity, conductance switching, synaptic plasticity

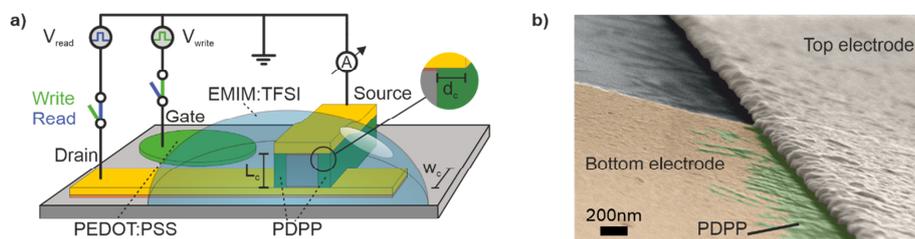
#### **Abstract**

Electrolyte-gated organic transistors are promising candidates as a new class of neuromorphic devices in hardware-based artificial neural networks which can outperform their CMOS counterparts regarding processing speed and energy consumption. Here, we utilize nanoscopic vertical electrolyte-gated transistors with a donor-acceptor diketopyrrolopyrrole-terthiophene polymer as active material to reversibly switch the channel conductivity over five orders of magnitude (3.8 nS to 392  $\mu$ S). In addition to fundamental synaptic functions, we also demonstrate operation voltages down to 1 mV to minimize the energy consumption per switching event, which is a prerequisite in terms of upscaling hardware-based artificial neural networks. To investigate the potential of these transistors in future neuromorphic networks, we show the operation of up to 3 interconnected transistors. The high switching range, low operation voltage and basic interconnection highlights the promise of electrolyte-gated organic transistors for future integration into hardware-based neural networks.

### 1. Introduction

Since the development of the first classical computer by K. Zuse in 1941<sup>[1]</sup>, the complexity of computational tasks rapidly increased from simple algebra problems to nowadays high complex simulations and calculations. However, where classical computing reaches its limits in tasks without a well-defined input and output, as e.g., language processing and picture recognition<sup>[2,3]</sup>, the superiority of humans becomes clear. Inspired by the human brain capabilities, a new field of computing arose based on so-called artificial neural networks (**ANNs**). Such networks emulate the learning process in brains and thus allow to solve not completely deterministic problems. However, existing **ANNs** still exhibit two major disadvantages compared to the biological system. First, the energy consumption is higher compared to the human brain with only ~10 W<sup>[2]</sup>. Second, the sequential processing in conventional computers, due to the von Neumann architecture<sup>[4]</sup>, hinders a more time efficient computing<sup>[3]</sup>. A parallel processing approach as found in the brain would be beneficial. To overcome these disadvantages, purely software based **ANNs** are embodied in hardware directly on a chip<sup>[5]</sup>. For an enhanced hardware realization, the demand for new materials and devices with tuneable and history dependent conductivities, also called neuromorphic devices, is growing, as CMOS reaches its limits<sup>[6]</sup>. Neuromorphic devices have been already implemented via filament forming<sup>[7]</sup>, charge trapping<sup>[8]</sup>, phase change<sup>[9]</sup>, and other conductivity switching mechanisms<sup>[10]</sup>. A further approach uses electrolyte gated organic transistors (**EGOT**) and the electrochemical doping of the polymer by ion diffusion<sup>[11–15]</sup>.

Here, we present the use of an **EGOT** as a synaptic memory with the organic semiconducting diketopyrrolopyrrole-terthiophene donor–acceptor polymer (**PDPP**) which has a low conductivity when not doped. In a previous work we investigated the transistor properties of the vertical **EGOT** design that showed an On/Off current modulation of up to  $10^8$ , low Off-currents and sufficiently intact transistor characteristics down to an operation voltage of only 10  $\mu\text{V}$ <sup>[14,15]</sup>. These features, combined with the small footprint down to  $2 \times 80 \times 80 \text{ nm}^2$ , outperform comparable neuromorphic devices based on other polymers such as poly(3,4-ethylendioxythiophene) (**PEDOT**)<sup>[16]</sup> and poly(3-hexylthiophen-2,5-diyl) (**P3HT**)<sup>[12]</sup> with respect to their electrical properties. All together this would make our design a promising candidate for usage in **ANNs**. Here, we demonstrate conductive switching over five orders of

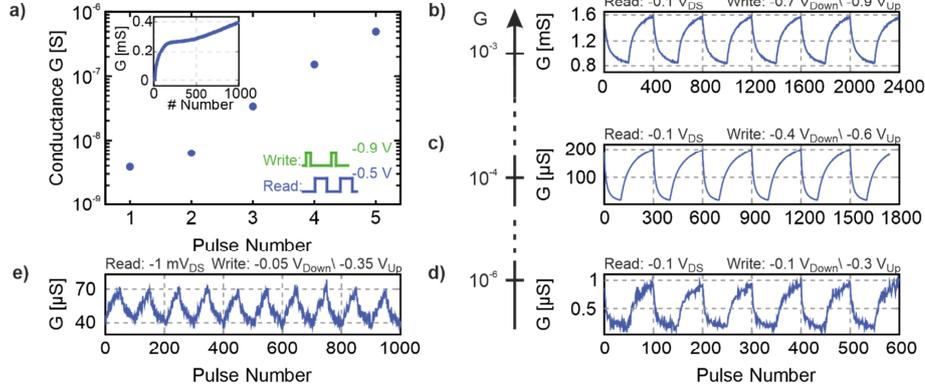


**Figure 1 EGOt design:** **a)** Device structure and used measurement circuit. Pulses with  $V_{\text{Write}}$  change the amount of ions in the PDPP channel. Hence, the conductivity changes, followed by a read-out pulse  $V_{\text{read}}$ . Switches at the drain and gate separate the read- and write-operations. **b)** SEM picture of the channel (green) with top and bottom contacts. For original picture see figure S2

magnitude and reduced drain-source bias operation down to only 1 mV that meet the low power requirements of hardware ANNs. Furthermore, the emulation of basic biological synaptic plasticity functions is shown using an interconnected system based on 3 EGOts.

## 2. Device design

The device design is based on our previous work <sup>[15]</sup> using a vertical organic field-effect transistor (VOFET) structure. The small footprint down to  $0.0128 \mu\text{m}^2$  (not counting the electrolyte area) fulfils the required single device size of  $< 0.04 \mu\text{m}^2$  for on-chip solutions of ANNs according to Gokem et al. <sup>[17]</sup>. Using an ion gel instead of the liquid electrolyte possibly allow patterning and subsequently decrease the area of the electrolyte for scalability purposes <sup>[18]</sup>. As the active channel material of the transistor, PDPP <sup>[19]</sup> is used and combined with the liquid electrolyte 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (EMIM:TFSI) as the gate. A droplet of poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) serves as gate electrode (see **Figure 1a**). For a detailed description of the individual fabrication steps we refer to the methods section in the supplementary material and our previous work <sup>[15]</sup>. In brief, the source and drain gold contacts are patterned via photolithography and e-beam evaporation. The silicon oxide spacer between the contacts is sputtered. With hydrofluoric acid (HF), the top contact gets underetched to make space for the PDPP channel material, which is then deposited via spin coating. The excess PDPP is removed everywhere except between the two electrodes with reactive ion etching (see supplementary **Figure S1**). The SEM picture (see **Figure 1b**, original supplementary **Figure S2**) shows the remaining PDPP channel between top and bottom electrode. Finally, the PEDOT:PSS gate-electrode and the EMIM:TFSI electrolyte are dropcasted. An optical image of a finished device can be found in supplementary **Figure S3**. A typical transfer curve of a device is shown in



**Figure 2 Switching of EGOT:** **a)** Conductance change over several orders of magnitude. A section of the pulse train is depicted in the bottom right. Write operations consisted of a  $-0.9$  V pulse with  $10\ \mu\text{s}$  duration. For the read-out a  $-0.5$  V pulse is applied at the drain for  $0.1$  s. The time gap between read and write is  $1$  ms. The inset shows the current after up to  $1000$  pulses. **b-d)** Cyclic switching in different working regions while using other write voltages. All measurements are done with a read-out voltage of  $-0.1$  V. Both read and write duration are  $0.1$  s. Read and write operations are  $100\ \mu\text{s}$  apart. **e)** Cyclic switching at a low read-out voltage of only  $-1$  mV. The read-out and write time were  $50$  ms and  $200\ \mu\text{s}$ , respectively. The time gap between pulses was  $100\ \mu\text{s}$ . For up (down)-writing a voltage of  $-0.35$  V ( $-0.05$  V) is used. The conductance is calculated by dividing the average current by the applied read voltage.

**Figure S4** showing two important electrical characteristics, namely the large current modulation ratio of  $10^8$  on the one side and the hysteresis in the drain current due to the time-lag of ion diffusion during gating on the other <sup>[20]</sup>. In the remainder of the manuscript we describe the suitability of our devices for two potential implementations, namely memory devices and synaptic devices.

### 3. Memory device

For use of our **EGOTs** as a memory device, once the write operation is complete, any subsequent time-dependent change of the channel conductance due to ion drift must be reduced as far as possible to ensure high non-volatility. Additionally, to ensure that the write and read operations do not affect each other, these operations should be completely decoupled. For this purpose, we have used a specifically designed circuit around our **EGOTs**. A schematic illustration of the contacted device is shown in **Figure 1a**. The switching circuit for write and read operations can be found in supplementary section 3. The main idea of using the circuit is the decoupling of the conductance readout and the updating process of the channel conductance combined with the prolonged retention time of the memory state <sup>[16]</sup>. The readout process is used to probe the channel conductance. This is done by applying only short read-pulses at the

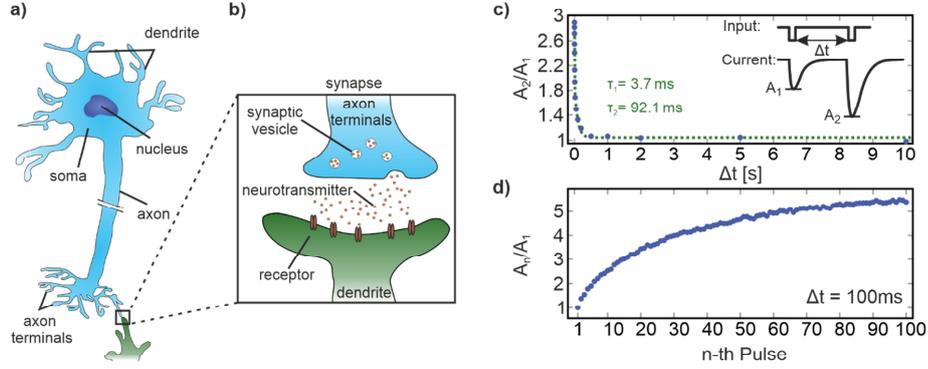
drain of the **EGOT**, whereas the updating writing process is done by short voltage pulses at the gate. During a writing operation, the external transistors attached to the gate and source electrodes are switched into a conductive state thereby allowing ions to penetrate from the electrolyte into the active channel. Hence, the conductivity is changed by charging the organic semiconductor in the channel <sup>[21]</sup>. This process is called electrochemical doping and changes the **EGOT**'s conductive state. Conversely, ions can also be reversibly extracted from the channel. Consequently, the doping of the polymer decreases, and a lower conductivity state is adjusted. For potential integration in hardware based deep neural networks (**DNNs**) where the conductance of the device emulates the synaptic weight (see supplementary **Figure S5b** and section 4 of the SI), devices ideally exhibit a time stable and tuneable conductance <sup>[5,16]</sup>, whereby the conductance should be programmable into as many distinguishable conductive states as possible<sup>[22]</sup>. This means that a high ON/OFF ratio is desirable. The size of the bandgap of the organic polymer used in the channel determines the achievable current modulation rate. Typically organic polymers such as **PEDOT** have On-Off ratios of  $10^5$  which is consequently the maximum limit for conductance switching using write pulses <sup>[23]</sup>.

Transfer and output characteristics of an **EGOT** as used in our work exhibit high On-Off ratios of up to  $10^8$  at -0.3 V bias (see supplementary **Figure S6**). **Figure 2a** shows as an example a switching measurement over five orders of magnitude which exceeds the full On-Off ratio in transfer curve measurements of comparable devices based on other polymer materials as **PEDOT:PSS** <sup>[23]</sup> and **P3HT** <sup>[24]</sup>. The first five pulses upon which the conductance changes by two orders of magnitude is shown in the main figure, the final conductance of 392  $\mu\text{S}$  after 1000 pulses is shown in the inset of **Figure 2a**. Due to resolution limitations of the used oscilloscope, the whole conductance region was measured in two different runs (see supplementary **Figure S7**). According to van de Burgt et al. <sup>[5]</sup> at least 100 distinct conductive states for synaptic devices are required to work adequate as a synaptic weight in a **DNN**. Hence, having more than 100 distinct conductive states would not significantly improve the performance of future **DNNs**. An exemplary measurement of distinct states including their measurement noise shows, that our devices will allow to distinguish more than 300 distinct conductive states (see supplementary section 6), and decreasing the measurement noise would allow to increase the number of addressable states even further.

The large switching range of our **EGOTs** allows to operate the device over a selected suitable conductance range and regime of maximum linearity (note that the conductance is not linear across the entire measurement range of  $10^5$  shown in **Figure 2a**, but is more linear over a

smaller range such as shown in **Figure 2e**). As an example that writing can be performed in different conductivity regions, and to show that the synaptic weights can be updated in both directions (a further requirement for **DNNs** <sup>[25]</sup>), the down writing process (i.e. a controlled decrease of the conductance) has also been realized for various conductance regions (**Figure 2b-d**). Here, all measurement parameters as write time, read time, Off-time and read voltage were kept constant and only the write voltage for up and down writing is varied. **Figure 2b-d** each shows 6 cycles out of a continuous measurement done in a highly conductive area with gate voltages of -0.9 V (-0.7 V), an intermediate conductive area with gate voltages of -0.6 V (-0.4 V) and low conductive area with gate voltages of -0.3 V (-0.1 V) for up (down)-writing. This illustrates the flexible use of our devices over a large conductance range corresponding to the high On-Off ratios whereby the conductance is switched from 1  $\mu$ S to 1.6 mS, respectively. The slope of the conductance change in the up- and down-writing process can be tuned by the duration or magnitude of the voltage pulses (see supplementary section 7). Pulses with a longer writing time (see supplementary **Figure S9a**) or a higher write voltage (see supplementary **Figure S9b/S10**) lead to a steeper conductance change allowing to adopt the synaptic weight to a specific memory design. Varying the pulse parameters has an effect on the linearity of the conductance modulation and hence, the linearity of our devices can be increased by adjusting the pulse shape. For example, the traces in **Figure 2e** show a more linear trace compared to **Figure 2b**.

Low energy consumption is a further critical aspect for hardware based neural networks <sup>[5]</sup>. Therefore, we reduced the energy consumption during read-out pulses by lowering the voltage at the drain down to -1 mV (see **Figure 2c**). Despite such a low bias and increased noise, a clear tuneable conduction is still observable in the tens of  $\mu$ S regime. Such low conductance operation is highly desirable to reduce the overall ANN currents and power consumption. Blending the **OSC** to reduce the conduction even further would be an additional approach to realize scalability in regard to the energy consumption.



**Figure 3 Synaptic plasticity:** **a)** Schematic biological neuron **b)** Biological synapse **c)** PPF measurement with two equal gate pulses ( $-0.6$  V,  $10$  ms) separated by  $\Delta t$  are applied at the **EGOT** while a constant drain voltage of  $-0.1$  V is present. The ratio of the maximum current responses  $A_2/A_1$  between the first and second pulse is plotted over the time separation. A double exponential decay with the given time constants is fitted to the data. **d)** PTP measurement: The gate and the drain contacts are connected and a train of  $100$  input pulses with a bias of  $-0.7$  V and  $100$  ms duration is applied. Between each pulse, a  $100$  ms pause with  $0$  V at the input is present. An increasing response with higher pulse number was measured because of the ion accumulation in the channel.

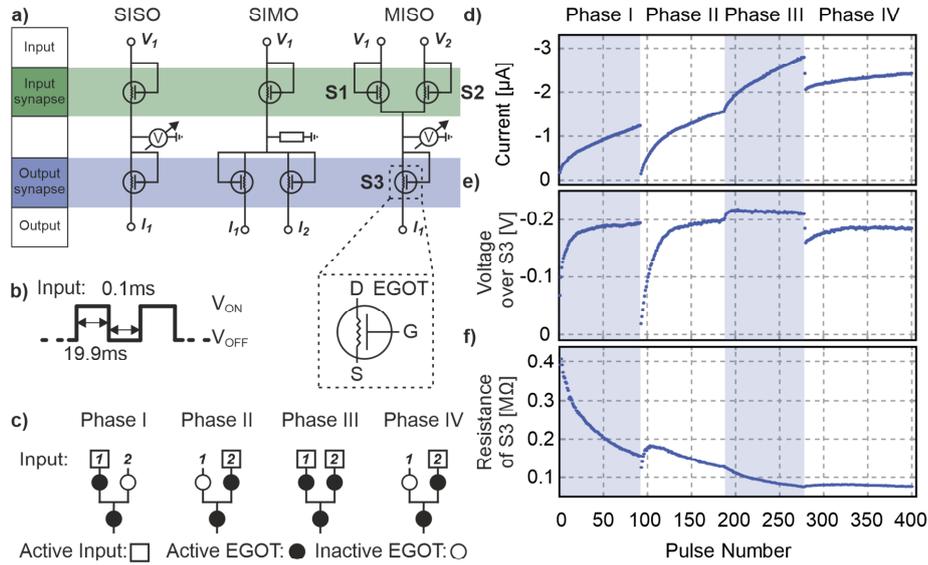
#### 4. Synaptic application

Besides demonstrating the use of our **EGOTs** as low-energy memory devices in DNNs, we have also investigated their ability to mimic brain functionality. The biological network in the brain works fundamentally different than a **DNN**. Its main contrast is the time and frequency dependent change of the synaptic weights often referred to as transient plasticity functions [3]. The combination with its massive ramified system existing of  $\sim 10^{11}$  neuron cells (see **Figure 3a**) interconnected via  $\sim 10^{15}$  synapses (see **Figure 3b**) [26] makes equivalent brain performance unreachable for **ANNs** up to now. Information in the brain is carried via electrical impulses from the dendrites of a neuron through the axon to the terminals and is finally transported over synapses to the following neurons. The transport with the neurotransmitter, a chemical signal, allows a time and frequency dependent change in the synaptic connection which is the key for the brain efficiency and is often referred to as synaptic plasticity functions. Different plasticity functions, such as paired pulse facilitation (**PPF**) [16,27–30], short-term potentiation (**STP**) [27,30,31], long-term potentiation (**LTP**) [31], and spike-timing-dependant plasticity (**STDP**) [7,32], model this behaviour and are already realized with neuromorphic devices. Specifically, **PPF** describes the conductivity increase after two consecutive pulses separated by varying times  $\Delta t$ .

After a first pulse, neurotransmitters are still present in the synaptic cleft before the second pulse arrives. Hence, a higher accumulation of neurotransmitters is present at the end of the second pulse leading to a stronger synaptic strength<sup>[33]</sup>.

**PPF** can also be mimicked with our **EGOTs** (see **Figure 3c**). Here, the devices were measured without the external transistor circuit used for the **DNNs** to allow the time-dependent change of the channel resistivity due to the time-dependent out-diffusion of ions from the channel back to the electrolyte with concomitant time-dependent conductance change of the channel. The double exponential decay fit results in comparable timescales (ms) as in biological synapses<sup>[33,34]</sup>. Here, the physical reason for the **PPF** effect is the varying amount of ions which are stored in the **PDPP** channel. For small  $\Delta t$ , ions forced by both pulses into the channel accumulate there, resulting in a large conductive change. With longer time gaps between the pulses, the ions diffuse back into the electrolyte in the time  $\Delta t$ . Alternatively, a sequence of input pulses can increase the accumulation of ions in the channel. This process is referred to as post tetanic potentiation (**PTP**)<sup>[34,35]</sup> and can be mimicked by our devices as well (see **Figure 3d**). A more detailed description of **PPF** and **PTP** can be found in supplementary section 8. As final proof of the synaptic functionality of our devices, we successfully built an electrical version of Pavlov's classical conditioning experiment<sup>[16,36]</sup> (see supplementary section 9).

While the above described functions only included use of one **EGOT**, we also investigated the information transfer over multiple **EGOT** devices (as is also done in the human brain). In this test, each **EGOT** emulates one synapse. For that purpose, the gate and drain contacts of each **EGOT** are connected to realise the **PPF** effect. Every input pulse leads to a current response at the source and simultaneously changes the conductivity state of the **EGOT** channel due to penetrating ions into the channels. We realized three different circuit configurations (see **Figure 4a**) to analyse the potential of interconnected systems with multiple inputs and outputs. By investigating these three cases we can demonstrate a history dependent information transfer over multiple synapses with more than one input and output which is reminiscent of the biological neuron. While the comparably Single-Input Single Output (**SISO**) and Single-Input



**Figure 4 Interconnected EGOT devices:** **a)** Tested circuit configurations. Only the MISO measurement is shown here with **b)** the input signal parameters  $V_{OFF} = 0$  V and  $V_{ON} = -0.6$  V/ $-0.7$  V (1. Input/2. Input). **c)** The MISO measurement is split into four phases, where either only one of the inputs is active or both together (the activation of the inputs during the phases is depicted). **d)** the current output **e)** the voltage drop over the output **EGOT** **f)** the resistance of the output **EGOT** are shown.

Multiple Output (**SIMO**) cases are described in supplementary sections 10 and 11, the more complex case of a multiple-input single-output (**MISO**) setup with two input and one output synapses is shown in **Figure 4b-f**. The purpose of this configuration is the realization of information accumulation from independent inputs and the corresponding plasticity effects at the output side reminiscent of neuron cells. Thereto, we have performed the measurement in four phases to clarify the interconnectedness of the **EGOTS** mimicking three synapses S1-S3 (see **Figure 4c**): Phase I: The input signal is only applied at S1. Phase II: Subsequently, the input signal is applied only to S2. Phase III: Both input **EGOTs** S1 and S2 are active at the same time. Phase IV: Only the **EGOT** of the second phase receives a signal. Between phase I and phase II, the magnitude of the current drops abruptly (see **Figure 4d**) due to the high resistance of S2 which is still in the non-conducting state. This is also the reason for the decrease in voltage drop over S3 (see **Figure 4e**). The resistance of S3 on the other hand remains relatively constant due to the memory effect of the devices (see **Figure 4f**), since ions from the pulses in phase I are still present. The output current and conductance in phase III increases further which is a summation effect of the inputs comparable to those of biological neurons. In

the transition between phase III and phase IV, a memory effect can be observed again for the resistance of S3. This is shown by the difference in resistance change of S3 during this phase compared to the change in phase II. The resistance is smooth during the transition. The current and voltage drop exhibit an expected jump to lower values at the transition to phase IV caused by switching off one input path. Together, these measurements show that information can be passed over synapses. While these measurements only encompass the use of three **EGOTs** they nevertheless show the basic interconnectivity of **EGOTs** as required for more complex circuits.

### Conclusion

In summary, we have demonstrated that electrolyte-gated vertical organic transistors can be used as artificial synapses with an outstanding resistance switching range of up to five orders of magnitude. This implies that depending on the desired application, the device can be operated over different conductance ranges from the nS to the hundreds of  $\mu$ S. Aside from fundamental synaptic plasticity functions as **PPF** and **PTP**, we have realized interconnected devices mimicking a biological neuron. Here, the information transport over several devices exhibits a learning behaviour depending on the input history. Furthermore, the applicability for ultra-low energy consumption with a switching behaviour down to 1 mV bias operation has been shown.

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# B Supplementary material for the publications

## B.1 Vertical, electrolyte-gated organic transistors show continuous operation in the MA/cm<sup>2</sup> regime and artificial synaptic behavior

Jakob Lenz, Fabio del Giudice, Fabian R. Geisenhof, Felix Winterer, and R. Thomas Weitz

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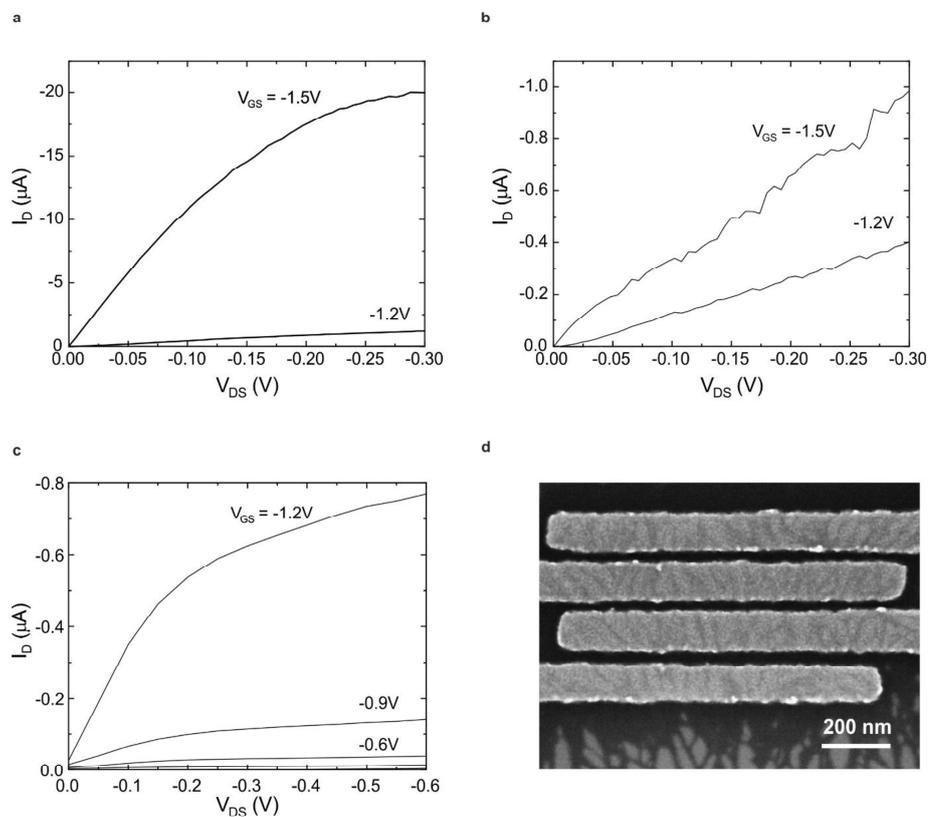
In the format provided by the authors and unedited.

## Vertical, electrolyte-gated organic transistors show continuous operation in the $\text{MA cm}^{-2}$ regime and artificial synaptic behaviour

Jakob Lenz<sup>1</sup>, Fabio del Giudice<sup>1,4</sup>, Fabian R. Geisenhof<sup>1</sup>, Felix Winterer<sup>1</sup> and R. Thomas Weitz<sup>1,2,3\*</sup>

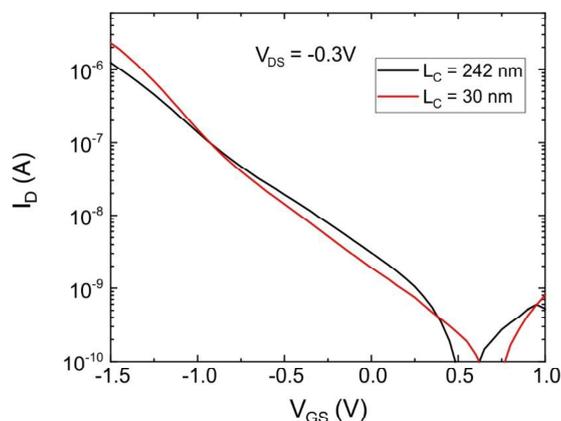
<sup>1</sup>Physics of Nanosystems, Department of Physics, Ludwig-Maximilians-Universität München, Munich, Germany. <sup>2</sup>Nanosystems Initiative Munich (NIM), Munich, Germany. <sup>3</sup>Center for NanoScience (CeNS), Ludwig-Maximilians-Universität München, Munich, Germany. <sup>4</sup>Present address: Walter-Schottky Institute, Technical University Munich, Garching, Germany. \*e-mail: [thomas.weitz@lmu.de](mailto:thomas.weitz@lmu.de)

## B.1 Vertical, electrolyte-gated OFETs show operation in the MA/cm<sup>2</sup> regime



**Supplementary Fig. S1.** Output characteristics of planar PDPP OFETs with a) 220 nm and b) 40 nm channel length measured at 9.5 mV/s under vacuum. c) 30 nm channel length measured at 132 mV/s under ambient conditions. The respective transfer curves of FETs in a) and b) are shown in the main manuscript in Fig. 1. d) SEM image of the transistor shown in (C).

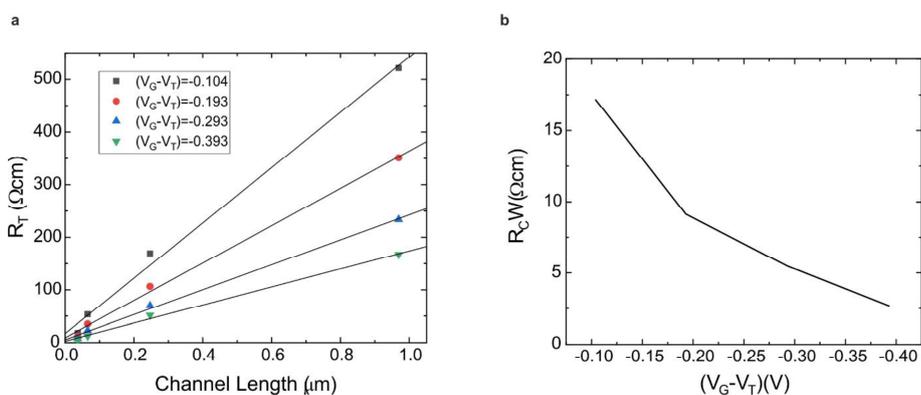
## B Supplementary material for the publications



**Supplementary Fig. S2.** Transfer characteristics of two lateral electrolyte-gated PDPP transistors measured under ambient conditions which have similar threshold voltages. Device parameters see Table 1.

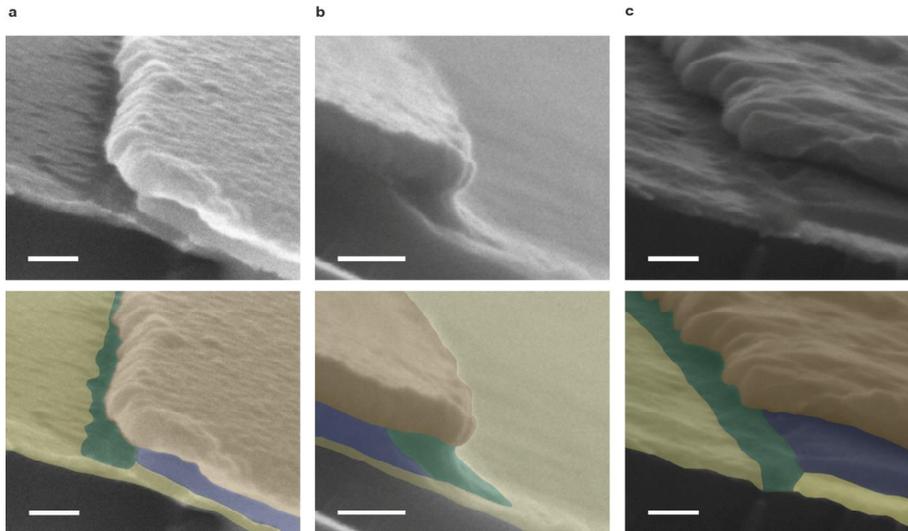
**Supplementary Table T1.** Device parameters for transistors in Supplementary Fig. S3 with channel length  $L_C$ , channel width  $W_C$ , maximum drain current  $I_{max}$  and maximum conductivity  $\sigma_{max}$  both at  $V_{GS} = -1.5V$ . For the conductivity calculations, a film thickness of 2 nm was assumed.

$L_C$	$W_C$	$I_{max}$	$\sigma_{max}$
242 nm	6.024 $\mu m$	1.24 $\mu A$	0.83 S/cm
30 nm	1.013 $\mu m$	2.3 $\mu A$	1.135 S/cm

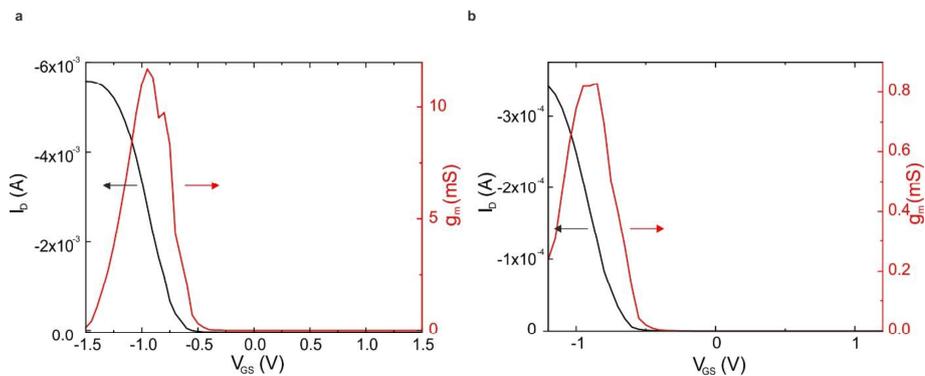


**Supplementary Fig. S3.** Channel width normalized total ( $R_T$ ) and contact ( $R_C$ ) resistance for lateral electrolyte-gated PDPP transistors ( $V_{DS} = 100mV$ ). **a)** Channel width normalized total resistance versus varying channel length for different  $V_{GS}$ . **b)** Contact resistance extracted with the transfer line method<sup>1</sup> and  $R_C W_{min} = 2.69 \Omega cm$ .

## B.1 Vertical, electrolyte-gated OFETs show operation in the MA/cm<sup>2</sup> regime

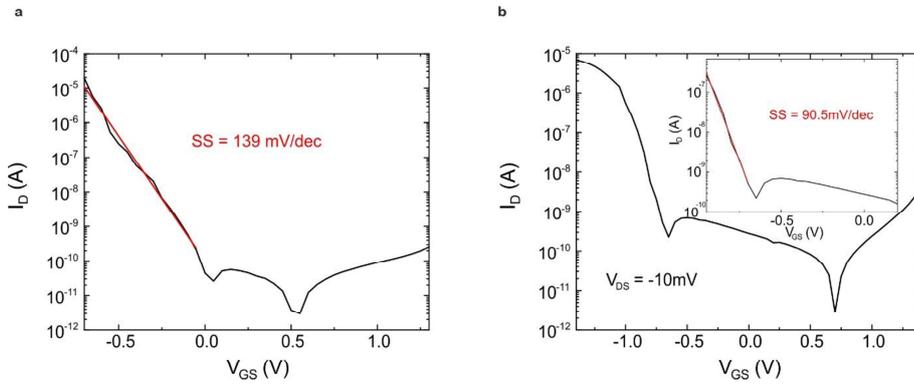


**Supplementary Fig. S4.** SEM images of different samples demonstrating that the vertical gap between source and drain contact is fully filled along the underetched distance  $d_c$  with the organic semiconductor. The bottom row show the same images but artificially coloured to visualize the organic semiconductor (green) even clearer (same colour coding used as Figure 2 of the main manuscript: yellow/brown: top and bottom metal electrode, blue: SiO<sub>2</sub> spacer, green: organic semiconductor). The scale bar is 100 nm in all images.

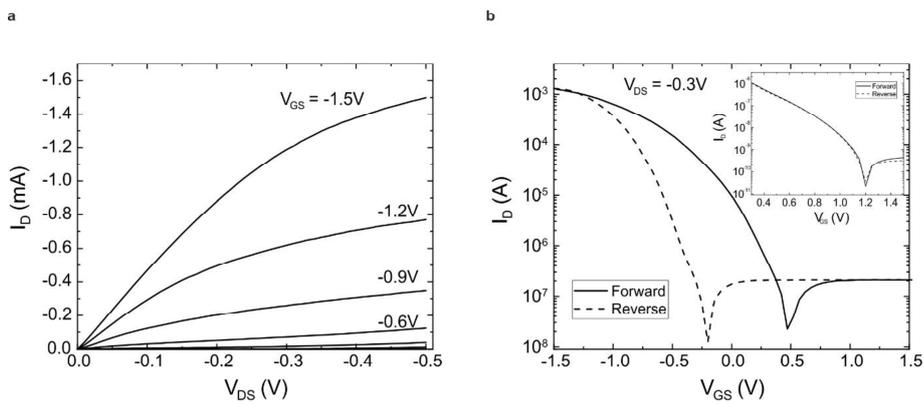


**Supplementary Fig. S5.** Transfer characteristic for  $V_{DS} = -0.3V$  and transconductance for the transistors shown a) in the main manuscript in Fig. 3 and b) in the main manuscript in Fig. 4.

## B Supplementary material for the publications



**Supplementary Fig. S6.** Subthreshold swing  $SS$  of electrolyte-gated PDPP VOFETs. **a)**  $SS$  of the transistor shown in the main manuscript in Fig. 3 for  $V_{DS} = 10$  mV. **b)** Transfer characteristics of a transistor with  $w_{bel} = 100$  nm,  $d_c = 40$  nm and  $A_{ch} = 8 \times 10^{-15}$  m<sup>2</sup>. Inset: Enlarged subthreshold region showing the  $SS$  of the device.



**Supplementary Fig. S7.** Electrical characteristics of an electrolyte-gated P3HT VOFET ( $w_{bel} = 100$   $\mu$ m,  $d_c = 100$  nm,  $A_{ch} = 10^{-12}$  m<sup>2</sup>,  $L_c = 40$  nm). **a)** Output characteristics. **b)** Transfer characteristics. For  $V_{DS} = -0.3$  V an on-off ratio of  $10^6$  and an on-state current density of  $129$  kA/cm<sup>2</sup> was measured. This measurements were performed with a different setup. To this end a Femto current-to-voltage converter was used and the on- and off state had to be measured with a different amplification. The inset shows the off-region.

## B.1 Vertical, electrolyte-gated OFETs show operation in the MA/cm<sup>2</sup> regime

### Charge carrier mobility estimation of lateral and vertical transistors

Since the charge carriers in the electrolyte gated transistors flow in the bulk of the semiconductor, we have not used the conventional approach to calculate the field-effect mobility. The charge carrier mobility  $\mu$  can be calculated using the following equation:

$$\mu = \frac{\sigma}{en}$$

With the elementary charge  $e$ , the yet unknown charge carrier density  $n$  and the device parameters given in Table T1 the mobility for lateral transistors can be calculated as:

$$\mu_{Lateral,242nm} = 5.2 \cdot 10^{18} \frac{1}{V_{scm}} * \frac{1}{n}$$

$$\mu_{Lateral,30nm} = 7.1 \cdot 10^{18} \frac{1}{V_{scm}} * \frac{1}{n}$$

For the electrolyte-gated PDPP VOFET in Fig. 4b in the main manuscript with  $L_c = 40$  nm,  $A_{ch} = 1.28 \times 10^{-14}$  m<sup>2</sup> and  $I_{max} = 3.4 \times 10^{-4}$  A, the mobility can be calculated to

$$\mu_{VOFET} = 2.2 \cdot 10^{20} \frac{1}{V_{scm}} * \frac{1}{n}$$

Assuming the same charge carrier density  $n$  for lateral and vertical devices, the mobility of the electrolyte-gated VOFET is larger by a factor of 31 and a factor of 43 compared with the lateral 30 nm and 242 nm device, respectively.

The absolute charge carrier mobility is hard to determine unambiguously. The reason is, that while we know the general capacitance of the electrolyte in the case it forms a purely electrostatic double layer without penetrating the semiconductor, we do not know in detail the amount as to how much the electrolyte penetrates the bulk of our organic semiconductor and therefore can only give an estimate to the gate capacitance. For a presumed charge carrier density  $n$  of  $10^{20}$  cm<sup>-3</sup> at  $V_{GS} = -1.5$  V [Ref 2] one can calculate the following tentative mobilities:

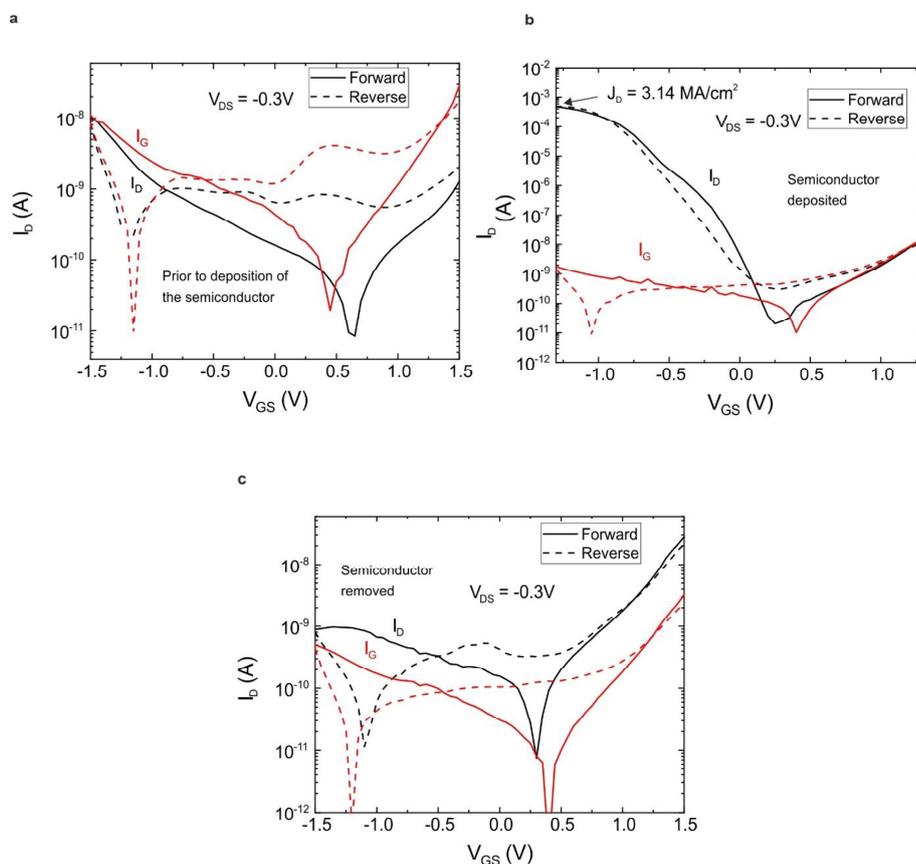
$$\mu_{Lateral,242nm} = 0.052 \frac{cm^2}{V_S}$$

$$\mu_{Lateral,30nm} = 0.071 \frac{cm^2}{V_S}$$

$$\mu_{VOFET} = 2.2 \frac{cm^2}{V_S}$$

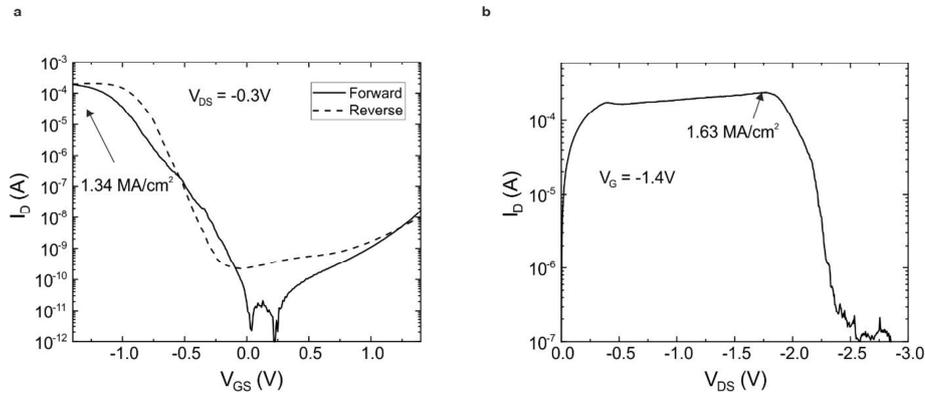
As the small contact and lead resistances (see also Figure S2) are neglected and we have taken a lower limit for the induced charge carrier density, the mobilities calculated above can be regarded as a lower limit.<sup>3</sup>

## B Supplementary material for the publications

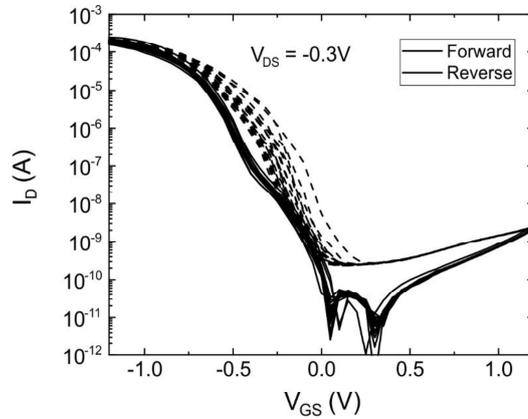


**Supplementary Fig. S8. Transfer characteristics of an electrolyte-gated vertical transistor structure measured in ambient atmosphere with an EMIM-TFSI electrolyte gate ( $w_{bel} = 96 \text{ nm}$ ,  $d_c = 80 \text{ nm}$ ,  $A_{ch} = 1.53 \times 10^{-14} \text{ m}^2$ ). a) Before PDPP deposition measured at  $90 \text{ mV/s}$ .  $I_D$  and  $I_G$  show very similar behavior. b) After PDPP deposition measured at  $56 \text{ mV/s}$ . c) Measured at  $90 \text{ mV/s}$  after removing PDPP with 10 minutes sonication in a xylene bath followed by 45 min  $O_2$  plasma (70 W). Again  $I_D$  and  $I_G$  show almost identical behavior.**

## B.1 Vertical, electrolyte-gated OFETs show operation in the MA/cm<sup>2</sup> regime

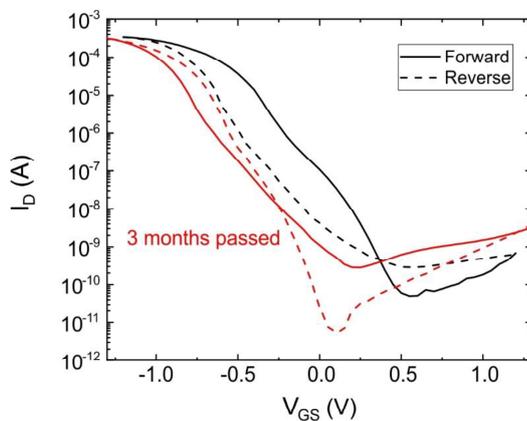


**Supplementary Fig. S9.**  $V_{DS}$  breakdown measurements of an electrolyte gated PDPP VOFET in ambient atmosphere ( $w_{bel} = 90 \text{ nm}$ ,  $d_c = 80 \text{ nm}$ ,  $A_{ch} = 1.44 \times 10^{-14} \text{ m}^2$ ). **a)** Transfer characteristics measured at  $18 \text{ mV/s}$ . **b)**  $I_D$ - $V_{DS}$  characteristics forcing the breakdown of the transistor. The breakdown voltage was measured for  $V_{DS} = -1.8 \text{ V}$ .

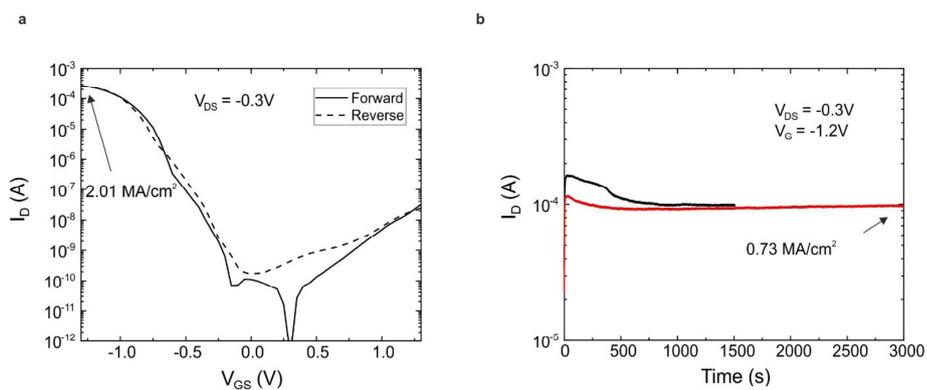


**Supplementary Fig. S10.** 20  $I_D$ - $V_{GS}$  cycles of an electrolyte gated PDPP VOFET ( $w_{bel} = 110 \text{ nm}$ ,  $d_c = 80 \text{ nm}$ ,  $A_{ch} = 1.76 \times 10^{-14} \text{ m}^2$ ) measured at  $85 \text{ mV/s}$  in ambient atmosphere. The maximum on current density was  $1.4 \text{ MA/cm}^2$ .

## B Supplementary material for the publications



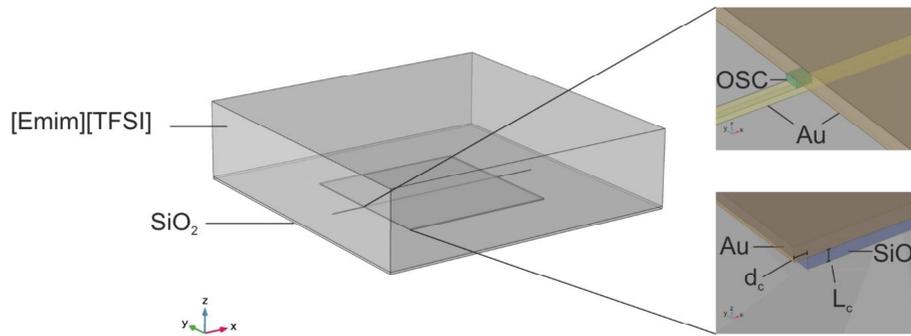
Supplementary Fig. S11. Comparison of  $I_D$ - $V_{GS}$  characteristic of the transistor in Fig. 4 in the main manuscript measured right after fabrication and after three months stored in a desiccator.



Supplementary Fig. S12. Long-term stability measurement of an electrolyte-gated PDPP VOFET in ambient atmosphere ( $w_{bel} = 83$  nm,  $d_c = 80$  nm,  $A_{ch} = 1.328 \times 10^{-14}$  m<sup>2</sup>). a) Transfer characteristics measured at 45 mV/s. b) Two temporal measurements of the maximum on current. The red curve was taken directly after the black one on the same transistor.

## B.1 Vertical, electrolyte-gated OFETs show operation in the MA/cm<sup>2</sup> regime

### Finite element analysis of the heating in the semiconductor in the vertical transistors during constant device operation



Supplementary Fig. S13. Geometrical model used for Joule heating simulations.

Stationary Joule heating was calculated by finite element simulation with Comsol Multiphysics under the following conditions and assumptions:

- 1) For the geometrical model (see Fig. S13) we used a 40 x 40  $\mu\text{m}$   $\text{SiO}_2$  substrate with a thickness of 300 nm. The dimensions were build corresponding to the transistor with maximal current density in Fig. 4b in the main manuscript.
  - bottom electrode:  $w_{\text{bel}} = 80$  nm, thickness 30 nm
  - $\text{SiO}_2$  spacer:  $w = 19.84$   $\mu\text{m}$  (symmetric  $d_c = 80$  nm), thickness 40 nm
  - top electrode:  $w = 20$   $\mu\text{m}$ , thickness 90 nm
  - [EMIM][TFSI]: 40 x 40  $\mu\text{m}$ , thickness 10  $\mu\text{m}$
- 2) Since chromium and titanium adhesive layers are only 1 nm thick (and titanium is etched away anyway), they are neglected in the simulation.
- 3) The current in the bottom electrode was calculated via the maximum observed experimental current of 342.78  $\mu\text{A}$  at  $V_{\text{DS}} = -0.3$  V (Fig 4b in the main manuscript). The top electrode was set to ground. [EMIM][TFSI] was considered not to contribute to charge transport.
- 4) Heat transfer occurs through all materials, their initial temperature was set to 293.15 K. The temperature of the edge surface of the whole model (far away from the semiconductor) was kept at 293.15 K.
- 5) Densities  $\rho$ , thermal conductivities  $\lambda$ , heat capacities  $C$  and electrical conductivities  $\sigma$  of all materials are summarized in Table T2. The values for  $\text{SiO}_2$  were taken from the Comsol database for fused quartz. Due to a lack of data for the PDPP organic semiconductor, we used literature values for P3HT instead for the density  $\rho$  and heat capacity  $C$ . The electrical conductivity  $\sigma$  was calculated according to

$$\sigma = \frac{1}{\rho} = \frac{L_c}{RA_{ch}}$$

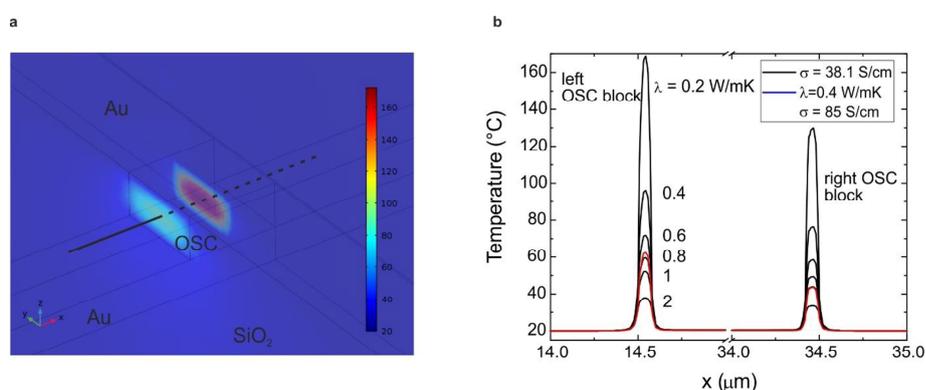
with the maximum observed experimental current of 342.78  $\mu\text{A}$  at  $V_{\text{DS}} = -0.3$  V (Fig 4b in the main manuscript),  $L_c = 40$  nm and  $A_{ch} = 1.28 \times 10^{-14}$  m<sup>2</sup> as  $\sigma = 38.1$  S/cm. The corresponding resistance  $R = 875.2$   $\Omega$  was corrected by the measurement setup resistance of approximately 55  $\Omega$  to

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$R_{\text{corr}} = 820.2 \Omega$ . As there are various values for the thermal conductivity of P3HT reported in literature in the range between  $\lambda = 0.2 - 2.2 \text{ W/mK}$  [Ref 4–7] we performed several simulations with varying thermal conductivity.

*Supplementary Table T2. Summary of the thermal and electrical parameters used for the finite element simulations.*

Material	$\rho$ (g/cm <sup>3</sup> )	$\lambda$ (W/mK)	C (J/gK)	$\sigma$ (S/cm)
Au	19.3 <sup>8</sup>	318 (bulk)	1.29 <sup>9</sup>	$35.7 \times 10^4$ <sup>10</sup>
[EMIM][TFSI]	1.52 <sup>11</sup>	1.2 <sup>12</sup>	1.242 <sup>13</sup>	/
OSC	1.33 <sup>14</sup>	0.2-1	1.32 <sup>15</sup>	38.11



*Supplementary Fig. S14. Joule heating simulations using Comsol Multiphysics. a) Temperature profile in the middle and the edge of the organic semiconductor (OSC) block for  $\lambda = 0.2 \text{ W/mK}$  and  $\sigma = 38.1 \text{ S/cm}$ . b) Temperature profile extracted from a line cut along the  $x$  axis through the middle of the OSC block (see black line in a)) for  $\lambda = 0.2 - 2 \text{ W/mK}$  and  $\sigma = 38.1 \text{ S/cm}$  in black and for  $\lambda = 0.4$  and  $\sigma = 85 \text{ S/cm}$  in red.*

In the simulation, the current has been applied at the left edge of the bottom gold electrode. Hence, the temperature of the right OSC block is decreased compared to the left block due to a voltage drop across the first gold electrode between the OSC blocks.

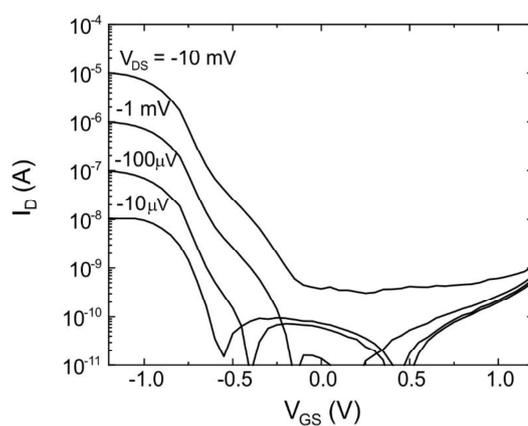
The calculated Joule heating can be seen as an upper limit since we included the resistance of the metallic leads into the resistance of the semiconductor. Hence, the real conductivity of the organic semiconductor should be larger resulting in smaller resistive heating. As an example, the Joule heating was also calculated for an estimated conductivity of  $\sigma = 85 \text{ S/cm}$  taken from [Ref 2] for comparison and the thermal conductivity  $\lambda = 0.4 \text{ W/mK}$  (as an average conductivity for P3HT).

## B.1 Vertical, electrolyte-gated OFETs show operation in the MA/cm<sup>2</sup> regime

Our simulations show, that the temperature in the middle of the semiconducting slab increases in the absolute worst case up to 160 °C, in a more realistic scenario with medium thermal conductivities of the organic semiconductor only to 50 – 70 °C – a temperature at which organic semiconductors are well known to be stable at.

*Supplementary Table T3. Comparison of the transconductance for the transistors in this work with the record values taken from literature (compare Ref. 16 and references therein).*

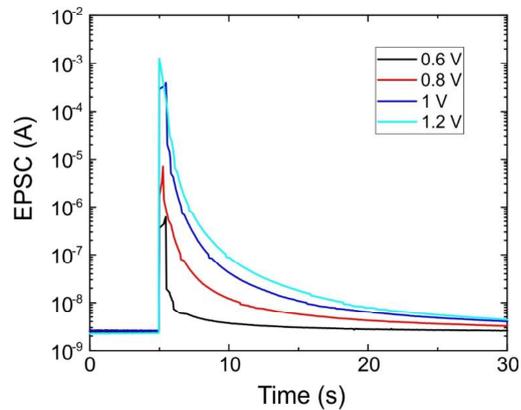
Active material	W (μm)	L (μm)	V <sub>GS</sub>   (V)	V <sub>DS</sub>   (V)	g <sub>m</sub> (mS)	g <sub>m</sub> /W (S/m)	g <sub>m</sub> / V <sub>DS</sub>   (mS/V)	I <sub>on/off</sub>
PDPP (Fig. 2)	100	0.04	0.95	-0.3	11.7	58.5	39	10 <sup>8</sup>
PDPP (Fig. 3)	0.08	0.04	0.9	-0.3	0.836	5225	2.787	10 <sup>5</sup>
P3HT (Fig. S10)	100	0.04	1.13	-0.3	1.47	7.35	4.9	10 <sup>4</sup>
PEDOT:PSS <sup>16</sup>	10	10	0.2	-0.6	4.02	402	6.7	2
PEDOT:PSS Vertical <sup>17</sup>	70		0.2	0.6	57	814	950	5
Graphene <sup>16</sup>	2.7	0.31	~1.2	2	1.863	690	0.932	4
P3HT <sup>16</sup>	100	20	~4	1	0.05	0.5	0.05	10 <sup>6</sup>
InAs NW	0.05	2	0.56	1	0.0975	1950	0.098	
SWCNT networks <sup>18</sup>	0.1	0.12	3	-0.5	4	40	8	<10 <sup>3</sup>



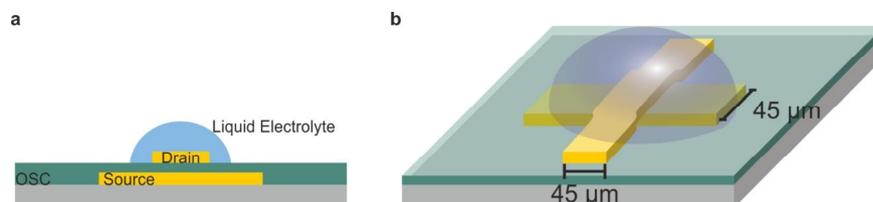
*Supplementary Fig. S15. Ultralow-voltage operation of VOFETs. Transfer characteristics of an electrolyte-gated PDPP VOFET measured in ambient atmosphere ( $W_{\text{bel}} = 90 \text{ nm}$ ,  $d_c = 80 \text{ nm}$ ,  $A_{\text{ch}} = 1.44 \times 10^{-14} \text{ m}^2$ ) for several  $V_{\text{DS}}$ .*

## B Supplementary material for the publications

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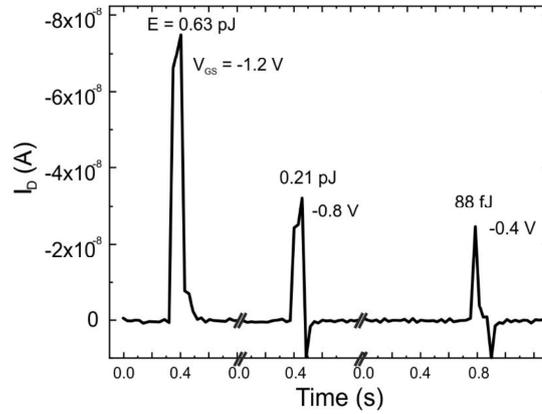


Supplementary Fig. S16. EPSC curves triggered by gate pulses with the same width of 500 ms and different gate amplitudes (same transistor as in the main manuscript Fig. 5a). For  $V_G = -0.8$  V,  $V_G = -1$  V and  $V_G = -1.2$  V a nonvolatile channel current could be observed (i.e. long term plasticity (LTP)).

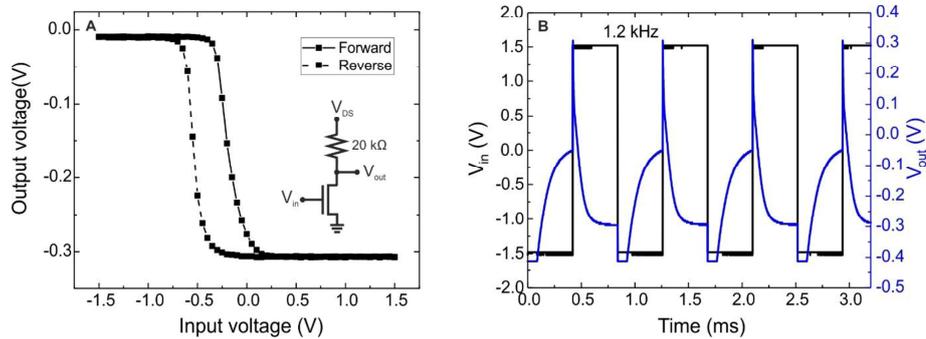


Supplementary Fig. S17. Electrolyte-gated vertical VOFET without  $\text{SiO}_2$  spacer and only PDPP sandwiched between the source and drain electrode. In this case the device was used without RIE etch of the semiconductor. Electrical characteristics of this device is shown in Fig. 5b (inset) of the main manuscript.

## B.1 Vertical, electrolyte-gated OFETs show operation in the MA/cm<sup>2</sup> regime



**Supplementary Fig. S18.** Switching energies for an electrolyte-gated PDPP VOFET ( $W_{\text{bel}} = 90 \text{ nm}$ ,  $d_c = 80 \text{ nm}$ ,  $A_{\text{ch}} = 1.44 \times 10^{-14} \text{ m}^2$ ).  $V_{\text{DS}}$  was  $100 \mu\text{V}$  and the width of the gate pulses  $100 \text{ ms}$ . The switching energy was calculated as  $E = V_{\text{DS}} * I_D * \Delta t$  (45) where  $\Delta t$  is the width of the resulting pulse and  $\Delta t * I_D$  was integrated.



**Supplementary Fig. S19.** Investigation of the switching speed of our VOFETs in a  $20 \text{ k}\Omega$  resistor loaded inverter. *a)* Input-output voltage characteristic of a resistor loaded electrolyte-gated VOFET inverter (see inset) at  $V_{\text{DS}} = -0.3 \text{ V}$ . The static response shows good inverter action. Sweeping the input voltage  $V_{\text{in}}$  between  $1.5 \text{ V}$  and  $-1.5 \text{ V}$  (sweep rate  $185 \text{ mV/s}$ ) the output voltage  $V_{\text{out}}$  was switched between the applied source-drain voltage  $V_{\text{DS}} = -0.3 \text{ V}$  and  $0 \text{ V}$ . *b)* Corresponding output-voltage response with the gate voltage pulsed at  $1.2 \text{ kHz}$ . The inverter shows a clear switching response to a  $1.2 \text{ kHz}$  square-wave input voltage signal. Since the device layout has not been optimized for the switching speed,  $1.2 \text{ kHz}$  can be seen as a lower limit.

## B Supplementary material for the publications

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## B.2 Ionic liquid gating of single walled carbon nanotube devices with ultra-short channel length down to 10 nm

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### **Ionic liquid gating of single-walled carbon nanotube devices**

#### **with ultra-short channel length down to 10 nm**

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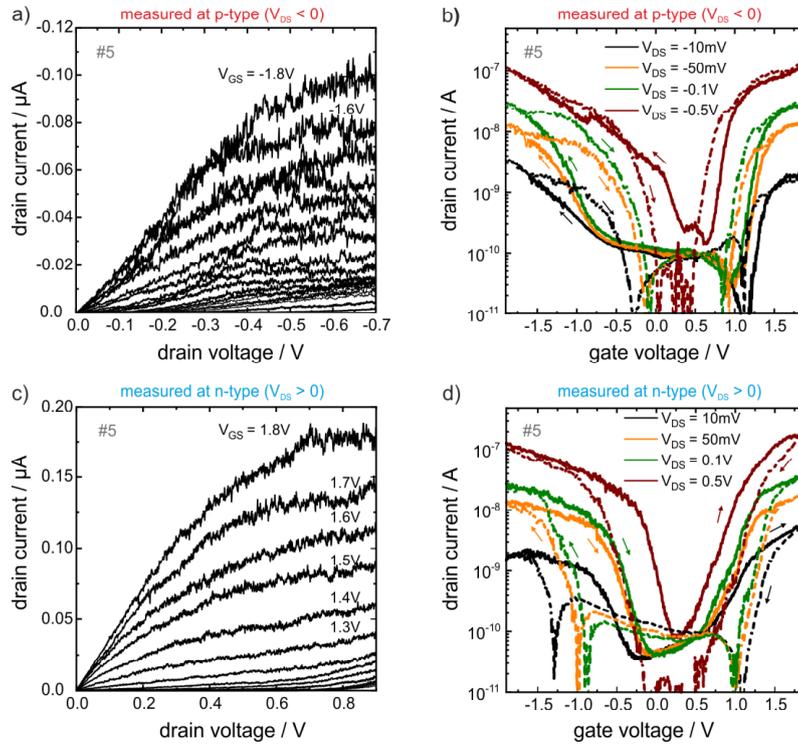
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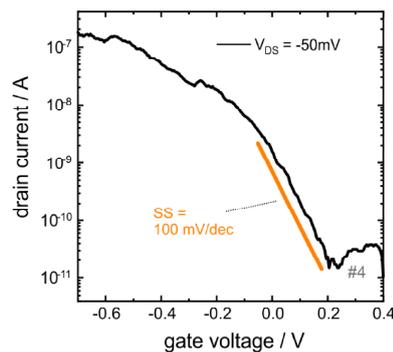
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## B.2 Ionic liquid gating of SWCNT devices with ultra-short channel lengths



**Figure S1:** Electrical transport measurements of (9, 8) carbon nanotube device (#1) with 10 nm channel length under ionic liquid gating ( $p = 8 \cdot 10^{-5}$  mbar). (a-b) P-type and (c-d) n-type transfer and output characteristics measured at  $10 \text{ mV s}^{-1}$  (solid lines: forward sweep; dashed lines: backwards sweep). Gate voltages ( $V_{GS}$ ) and Source-drain voltages ( $V_{DS}$ ) are indicated.



**Figure S2:** P-type transfer characteristics of device #4 (ambient conditions) with  $L_{ch} = 10 \text{ nm}$  measured at  $V_{GS}$  sweep rate of  $10 \text{ mV s}^{-1}$ . The SS-factor is schematically indicated.

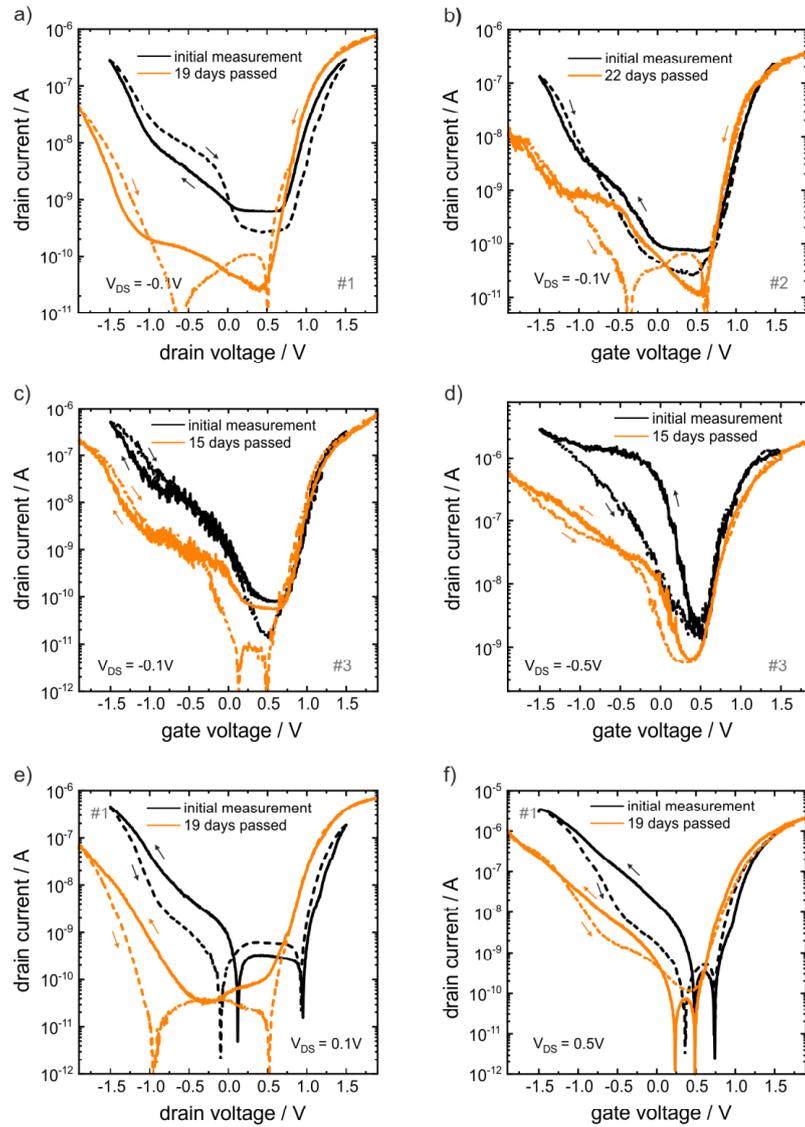
## B Supplementary material for the publications

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**Supplementary Table T1**

Literature	$L_{ch}$ (nm)	Gate dielectric	CNT $\phi$ (nm)	VDS  (mV)	SS (mV/dec)
Present work	10	EMIM-TFSI	1.2	50	100
Männik et al.[1]	60	Phosphate Buffer	2	No information	75
Franklin et al.[2]	9	3 nm HfO <sub>2</sub>	1.3	400	94
Weitz et al.[3]	100	3.6 nm Al <sub>2</sub> O <sub>3</sub> + n-octadecylphosphonic acid SAM	No information	100	68
Qiu et al.[4]	5	3.5 nm HfO <sub>2</sub>	1.3	100	75

## B.2 Ionic liquid gating of SWCNT devices with ultra-short channel lengths

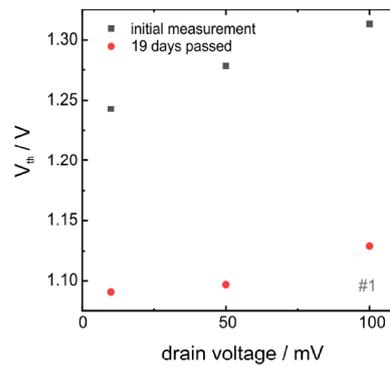


**Figure S3:** (a-d) P-type transfer characteristics and (e-f) n-type transfer characteristics (solid lines: forward sweep; dashed lines: backwards sweep;  $L_{ch} = 20$  nm). The initial measurements were performed in the first two days after the sample was loaded in the vacuum chamber at a pressure of  $6.2 - 2.5 \cdot 10^{-5}$  mbar and a sweep rate of  $26$  mV  $s^{-1}$ . The sample was stored in vacuum until another measurement was conducted at a pressure of  $1 \cdot 10^{-5}$  mbar and a sweep rate of  $10$  mV  $s^{-1}$ . Even though the sweeping speed is slower (here the hysteresis is caused by traps), the hysteresis is reduced.

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**Supplementary Table T2.  $V_{th}$  for different devices and  $V_{DS} = -0.5$  V.** In the p-branch,  $V_{th}$  is extracted for negative  $V_{GS}$  and in the n-branch for positive  $V_{GS}$ . White shaded cells refer to the first measurements recorded directly after loading the sample into the vacuum and blue shaded cells to the second measurements after storing the samples in vacuum for longer than two weeks. The threshold voltage was read for the n-branch as well even though we measured with negative  $V_{DS}$  for comparing the values before and after vacuum storage. Note that for device #1 and #3 no meaningful  $V_{th}$  extraction is possible due to different slopes with intermediate plateaus.

	device #1		device #2		device #3	
<b>p-branch</b>	0.2 V		0.22 V	0.21	0.28 V	
<b>n-branch</b>	0.66 V	0.506	0.66 V	0.61	0.66 V	0.63



**Figure S4:** Change of  $V_{th}$  of device #1 ( $L_{ch} = 20$  nm) between the initial measurement in the first two days after loading the sample in the vacuum setup at a pressure of  $2.5 \cdot 10^{-5}$  mbar and a second measurement at a pressure of  $1 \cdot 10^{-5}$  mbar for  $V_{DS} = 10$  mV, 50 mV and 100 mV.

**Supplementary Table T3.  $V_{th}$  values for device #1 used for Supplementary Figure 3.**

	$V_{DS} = 10$ mV	$V_{DS} = 50$ mV	$V_{DS} = 100$ mV
<b>1<sup>st</sup> measurement</b>	1.24 V	1.28 V	1.31 V
<b>2<sup>nd</sup> measurement</b>	1.09 V	1.1 V	1.13 V

## B.2 Ionic liquid gating of SWCNT devices with ultra-short channel lengths

### Supplementary Section S1. Drain source current from Landauer formula

Drain-source current  $I_{ds}$  can be computed using the Landauer formula[5]:

$$I_{ds}(\phi_{ds}, \phi_{CNT}) = 2 \frac{e^2}{2\pi\hbar} \int T(E, \phi_{ds}, \phi_{CNT}) (f_d(E) - f_s(E)) dE \quad (1)$$

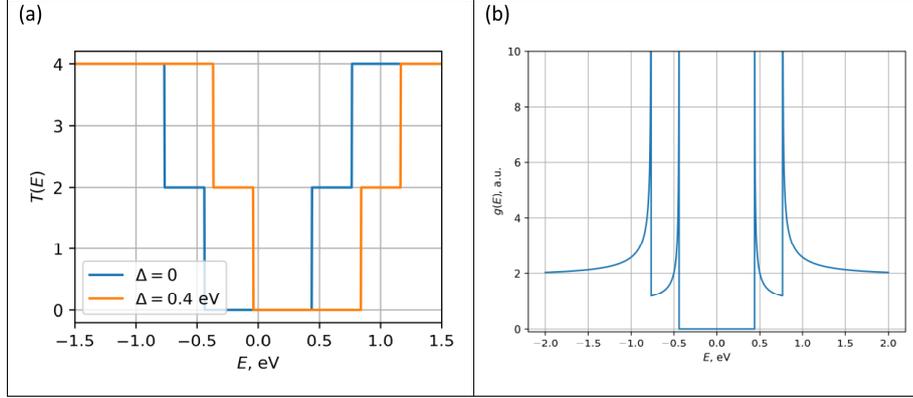
with  $T(E, \phi_{ds}, \phi_{CNT})$  as the transmission coefficient from left to right contact through the tube.  $E$  is the energy of an electron,  $\phi_{ds}$  and  $\phi_{CNT}$  are potential energy of electrons at the source electrode with respect to the source and potential energy on the carbon nanotube, respectively. These are related to  $V_{ds}$  and  $V_{gs}$ , drain-source and gate-source voltage:  $\phi_{ds}(V_{ds}) = -eV_{ds}$  (here  $e$  is the elementary charge);  $\phi_{CNT}(V_{gs})$ .  $f_d(E)$  and  $f_s(E)$  are the Fermi functions of the drain and source electrodes;  $f_d(E) = f_s(E - \phi_{ds})$ .

To estimate the current using Landauer formula, the following assumptions are made.

At zero voltage,  $T_0(E) \equiv T(E, V_{ds} = 0, V_{gs} = 0)$  is given by the following expression:

$$T_0(E) = 2 \times \begin{cases} 0, & |E - \Delta| < \frac{E_{11}}{2} \\ 1, & \frac{E_{11}}{2} < |E - \Delta| < \frac{E_{22}}{2} \\ 2, & |E - \Delta| > \frac{E_{22}}{2} \end{cases}$$

$E_{11}$  and  $E_{22}$  is the band-gap and the distance between the second conduction/valence band edges (See Figure 4a). These are known for the tube employed in this work:  $E_{11} = 0.879$  eV;  $E_{22} = 1.533$  eV.  $\Delta$  is the metal-induced doping, defined as the difference between the position of the center of the band gap  $E_0$  with respect to the chemical potential  $\mu$ :  $\Delta = E_0 - \mu$ .  $\Delta$  is positive for p-doping. The factor 2 accounts for the spin degeneracy. **Figure S5a** shows  $T_0(E)$  plotted for  $\Delta = 0.4$ .



**Figure S5.** (a) Transmission coefficient through the undoped ( $\Delta = 0$ ) and p-doped ( $\Delta = 0.4$  eV) (9,8) tube. (b) Density of states in undoped (9,8) carbon nanotubes due to the first two bands taken into account.

It is assumed that  $T(E, \phi_{ds}, \phi_{CNT})$  does not depend on the drain-source voltage and the dependence on the  $\phi_{CNT}$  is set by the shift of the electron energy by  $\phi_{CNT}$ , so that:

$$T(E, \phi_{CNT}) \equiv T_0(E - \phi_{CNT}).$$

In the case of the perfect gate control,  $\phi_{CNT} = -eV_{gs}$ . However, if the tube has a considerable density of states at a Fermi level, one generally cannot ignore the so-called quantum capacitance, defined as [6]:

$$C_q = e^2 \int g(E - \phi_{CNT} - \Delta) F_{th}(E, \mu) dE$$

**(Fehler!  
Verweisquelle  
konnte nicht  
gefunden  
werden.)**

where  $F_{th}(E, \mu)$  is the thermal broadening function defined as the derivative of the Fermi function with respect to the chemical potential:  $F_{th}(E, \mu) = \frac{\partial f(E, \mu)}{\partial \mu} = \frac{1}{4k_B T} \operatorname{sech}^2\left(\frac{E - \mu}{2k_B T}\right)$ . The argument  $(E - \phi_{CNT} - \Delta)$  accounts for the shift of the bands due to doping ( $\Delta$ ) and the effect of the gate electrode ( $\phi_{CNT}$ ).

## B.2 Ionic liquid gating of SWCNT devices with ultra-short channel lengths

This quantum capacitance  $C_q$  and the electrostatic gate capacitance  $C_g$  can be considered as two capacitors in series. The gate potential  $V_{gs}$  and the potential on the tube interface  $V_{CNT}$  is now connected according to ( $V_{CNT} = -\phi_{CNT}/e$ ):

$$V_{CNT} = \alpha(V_{CNT})V_{gs} \quad (2)$$

with

$$\alpha(V_{CNT}) = \frac{C_i}{C_i + C_q(V_{CNT})}.$$

Supplementary **Section S2** describes how to determine  $C_q(V_{CNT})$  and  $C_i$ , and, respectively,  $\alpha(V_{CNT})$ . As soon as this is done, we can relate gate-source voltage  $V_{gs}$  that is actually applied in the experiment to the potential energy of the electron in the tube  $\phi_{CNT}$ , which enters the Landauer equation:

$$\phi_{CNT} = -e\alpha(\phi_{CNT})V_{gs}.$$

The Landauer formula (1) thus can be rewritten as a function of  $V_{ds}$  and  $V_{gs}$ :

$$I_{ds}(V_{ds}, V_{gs}) \approx 2 \frac{e^2}{2\pi\hbar} \int T_0(E - \phi_{CNT}(V_{gs})) (f_s(E + eV_{ds}) - f_s(E - \phi_{ds})) dE.$$

### Supplementary Section S2. Quantum and electrostatic capacitance

Quantum conductance is computed using formula (**Fehler! Verweisquelle konnte nicht gefunden werden.**). The density of states is approximated with formula [7]:

$$g(E) \approx \sum_i g_{m,i}(E) \quad (3)$$

where

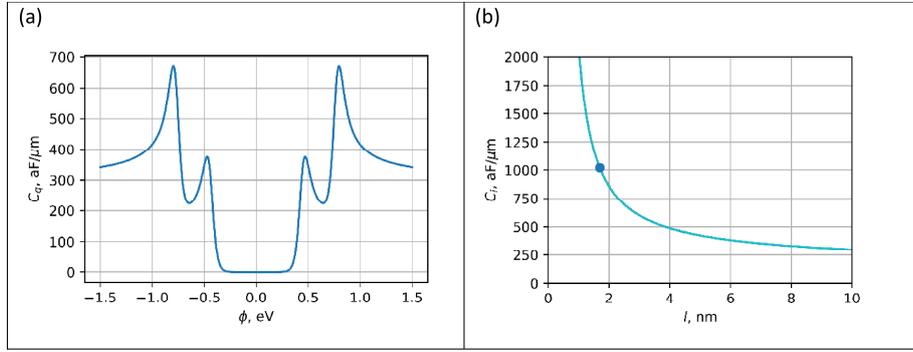
$$g_{m,i}(E) = \frac{g_0}{2} \frac{|E|}{\sqrt{E^2 - E_{ii}^2}}$$

is the density of states for mode  $i$ . We take only two modes, the same as for the transmission coefficient, so that  $i = \{1,2\}$  in (3). Here,  $g_0 = \frac{8}{\sqrt{3}a\pi\gamma}$ ,  $a = 2.46 \text{ \AA}$  (graphene Bravais lattice constant),  $\gamma = 3.1 \text{ eV}$  (overlap integral between two  $\pi$  orbitals of the nearest carbon atoms in a tube).

## B Supplementary material for the publications

The density of states approximated this way is plotted in **Figure S5b**.

Quantum capacitance computed using formula (Fehler! Verweisquelle konnte nicht gefunden werden.) with the density of states according to formula (3) as a function of  $\phi_{CNT}$  is plotted in **Figure S6a**. The tube is assumed to be undoped ( $\Delta = 0$ ). It is important to note that the quantum capacitance depends on the density of states in the vicinity of the Fermi level, and the latter can be altered by the doping and the effect of the gate electrode ( $\phi_{CNT}(V_{gs})$ ). Thus, for the undoped tube, this capacitance is close to zero for small  $\phi_{CNT}$  (as the Fermi level is in the centre of the bandgap), while it is maximized as the potential at the tube reaches the van Hove singularities, where the density of states tends to infinity.



**Figure S6.** Quantum  $C_q$  and electrostatic  $C_i$  capacitances. (a) Dependence of the quantum capacitance on the potential Fehler! Verweisquelle konnte nicht gefunden werden.at the tube,  $\phi_{CNT}$ . Peaks occurs at  $\phi_{CNT}$  that align the Fermi level with van Hove singularities:  $\phi_{CNT} = \pm \frac{E_{11}}{2}$  and  $\phi_{CNT} = \pm \frac{E_{22}}{2}$ . (b) Dependence of the electrostatic capacitance on the screening length  $l$  for the typical range of screening lengths of ionic liquids. The blue point corresponds to the screening length and dielectric permittivity of the actual ionic liquid, [EMIM][TFSI]:  $l = 1.7$  nm;  $\epsilon = 12$ .

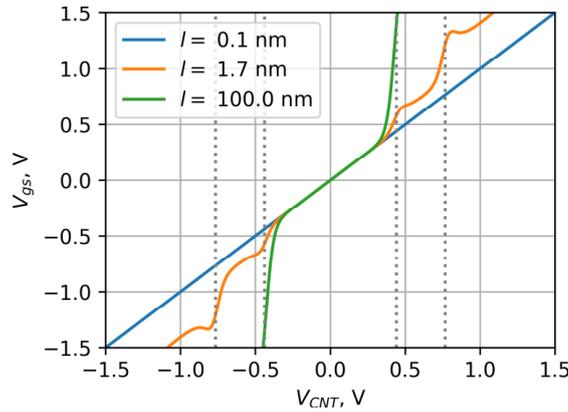
To estimate the electrostatics capacitance per unit length for a cylindrical “electrode” in the ionic liquid, we use the formula [6]:

$$C_i = \frac{2\pi\epsilon\epsilon_0}{K_0\left(\frac{R}{l}\right)}$$

## B.2 Ionic liquid gating of SWCNT devices with ultra-short channel lengths

where  $l$  is the screening length of the ionic liquid; for [EMIM][TFSI],  $l = 1.6$  nm. [8]  $\epsilon$  is the static dielectric permittivity;  $\epsilon = 12$  for [EMIM][TFSI]. [9] Finally,  $R$  is the radius of the carbon nanotube (9,8), which is 1.2 nm and  $K_0$  is the modified Bessel function of zeros order and second class. Computed value of  $C_i = 1000$  aF/ $\mu\text{m}$ , which is the same order of magnitude as that for  $C_q$  between the first two van Hove singularities. This means that the coefficient of  $\alpha$  in equation (3) will be appreciatively smaller than 1.0 in the region where the Fermi level is beyond or in the vicinity of the first van Hove singularities. Note that unlike the quantum capacitance, the electrostatic capacitance  $C_i$  does not depend on the gate voltage applied.

The dependence of the applied gate-source voltage on the actual potential felt by a carbon nanotube is shown in **Figure S7** for the screening length of the actual set-up ( $l = 1.7$  nm) and for two values corresponding to quasi-asymptotic cases.



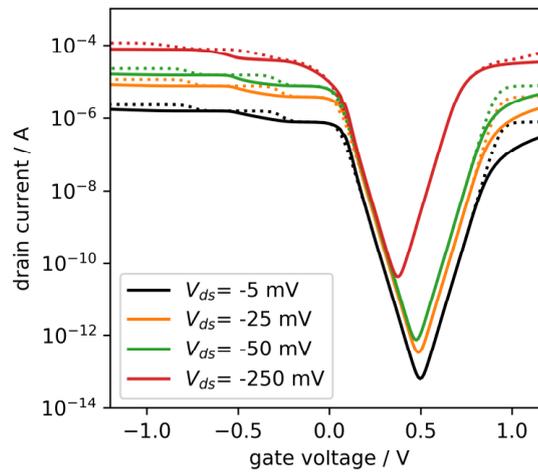
**Figure S7.** Relation between the potential applied to the gate ( $V_{gs}$ ) and the potential on the tube surface ( $V_{CNT}$ ). Actual screening lengths  $l = 1.7$  nm. Very large (100 nm) and very small (0.1 nm) screening lengths would lead to a weak gate control (once the gate voltage shift cause Fermi level to rich the first van Hove singularity) and a perfect control, respectively. In a given experiment, dielectric permittivity and the screening length provide an intermediate control as compared to those asymptotic cases.

Using the correspondence between  $V_{gs}$  and  $V_{CNT}$ , the transfer characteristic is computed and plotted in **Figure S8**. The effect of the quantum capacitance is appreciable once the transport window (region of the energy between the source and the drain chemical potentials) is outside the band gap. In our

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model, due to simple assumptions, in the on-state, the current does only increase if the next band is 'turned on', while in the experiment, the current may also increase due to contact barrier reduction, etc.



**Figure S8.** Transfer current-voltage characteristics of the liquid-gate transistor. Solid lines accounts for the effect of the quantum capacitance. Dotted lines demonstrate the current-voltage characteristics with the effect of the quantum capacitance neglected.

## B.2 Ionic liquid gating of SWCNT devices with ultra-short channel lengths

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## B.3 High-Performance Vertical Organic Transistors of Sub-5 nm Channel Length

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**Supplementary Information**

**for**

**High performance vertical organic transistors of sub 5 nm channel length**

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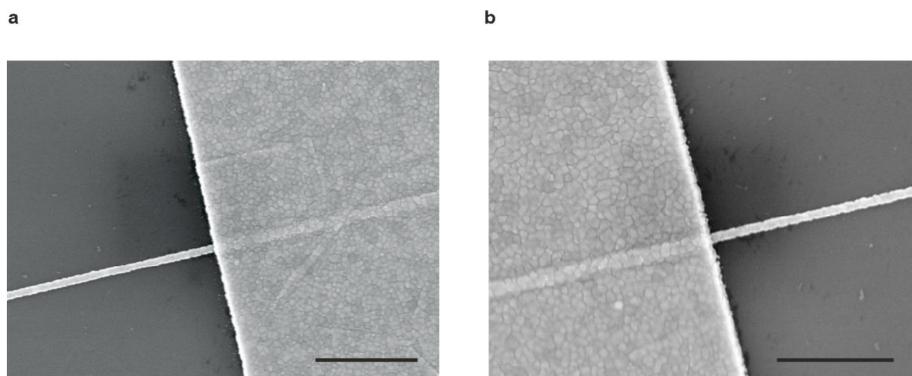
## B.3 High-Performance Vertical Organic Transistors of Sub-5 nm Channel Length

**Supplementary Table T1. Overview of device parameters and performance of all measured devices.** Blue shaded cells correspond to gate configuration 2, where the gate probe needle is directly immersed in the ionic liquid, and the white shaded cells correspond to gate configuration 1, where an additional gold gate pad is used (see supplementary Figure 1).

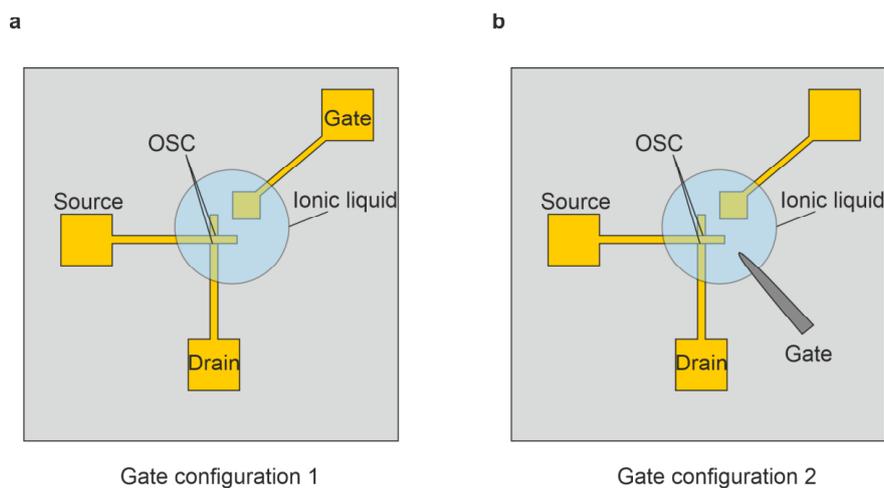
device	$L_{ch}$ (nm)	$J$ (MA cm <sup>-2</sup> ) @ -0.4 V	$V_{th}$ (V) @ -0.01V	$V_{th}$ (V) @ -0.3V	SS (mV dec <sup>-1</sup> ) @ -0.01V	SS (mV dec <sup>-1</sup> ) @ -0.3V	Transcond. (S m <sup>-1</sup> ) @ -0.3V	On/off @ -0.3 V
1	4.9	0.164	-0.95	-0.72	66	101	5.1	$3 \times 10^4$
2	3.6	2.95	-1.02	-0.72	65	107	264	$10^5$
3	7.6	2.14	-0.89	-0.77	83	100	171	$10^6$
4	6.6	$9.5 \times 10^{-3}$	-0.87	-0.67 <sup>1</sup>	115	152 <sup>1</sup>	$10^1$	$3.7 \times 10^{5.1}$
16	2.4	$8.88 \times 10^{-3}$	-1.02	X	135	X	X	X
2	3.6	2.95	-1.14	-0.55	233	285	X	$10^5$
3	7.6	2.14	-1.16	-1.03	400	370	714	$10^6$
4	6.6	$9.5 \times 10^{-3}$	-0.56	-0.38 <sup>1</sup>	162	207 <sup>1</sup>	8 <sup>1</sup>	$3 \times 10^{5.1}$
5	6.6	0.125	-0.73	-0.48 <sup>2</sup>	192	225 <sup>2</sup>	246 <sup>2</sup>	$10^{6.2}$
6	3	0.139	-0.78	-0.42	200	240	76	$10^4$
7	5	0.143	-0.9	-0.38	205	312	X	$10^5$
8	5	0.101	-0.94	-0.39	215	294	X	$10^4$
9	5	0.167	-0.77	-0.35	220	245	71.5	$10^5$
10	13.9	0.02	-1	-0.43	222	245	25	$10^6$
11	13.9	0.115	-1.08	-0.5	251	333	125	$10^5$
12	5.9	0.015	-0.92	-0.42	205	217	23	$10^4$
13	16	0.074	-1.02	-0.91	303	312	X	$10^5$
14	5	0.708	-0.85	-0.23 <sup>2</sup>	203	121 <sup>2</sup>	156 <sup>2</sup>	$5 \times 10^{5.2}$
15	10	0.041	-0.94	-0.44 <sup>2</sup>	204	217 <sup>2</sup>		$3 \times 10^{5.2}$

<sup>1</sup> measured at  $V_{DS} = -0.5V$

<sup>2</sup> measured at  $V_{DS} = -0.4V$

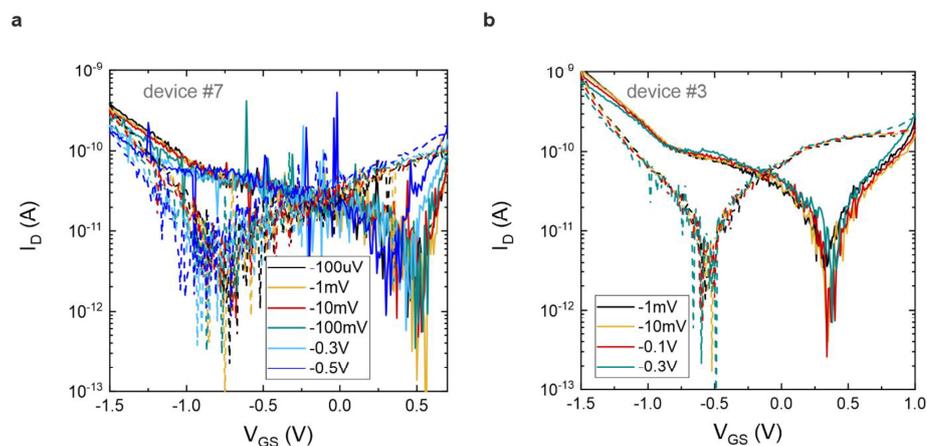


**Supplementary Figure S1.** SEM images of two exemplary FETs after OSC RIE where no OSC residues can be seen at the crossing point of the two electrodes. Scale bar a) 1 μm and b) 800 nm.

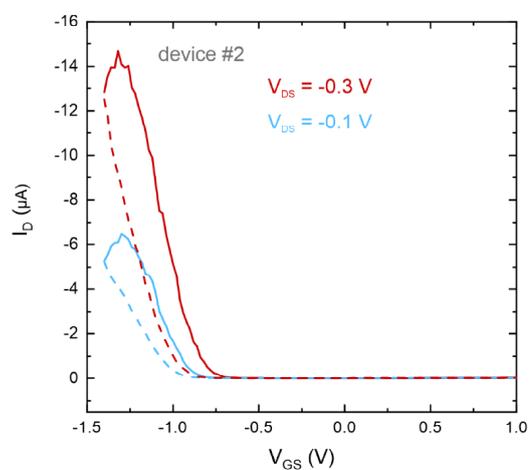


**Supplementary Figure S2.** Schematic illustration of different gate configurations. a) Gate configuration 1, where the gate needle is contacted with a gold gate pad, which is in contact with the ionic liquid. b) Gate configuration 2, where the gate needle is directly immersed in the ionic liquid.

## B.3 High-Performance Vertical Organic Transistors of Sub-5 nm Channel Length

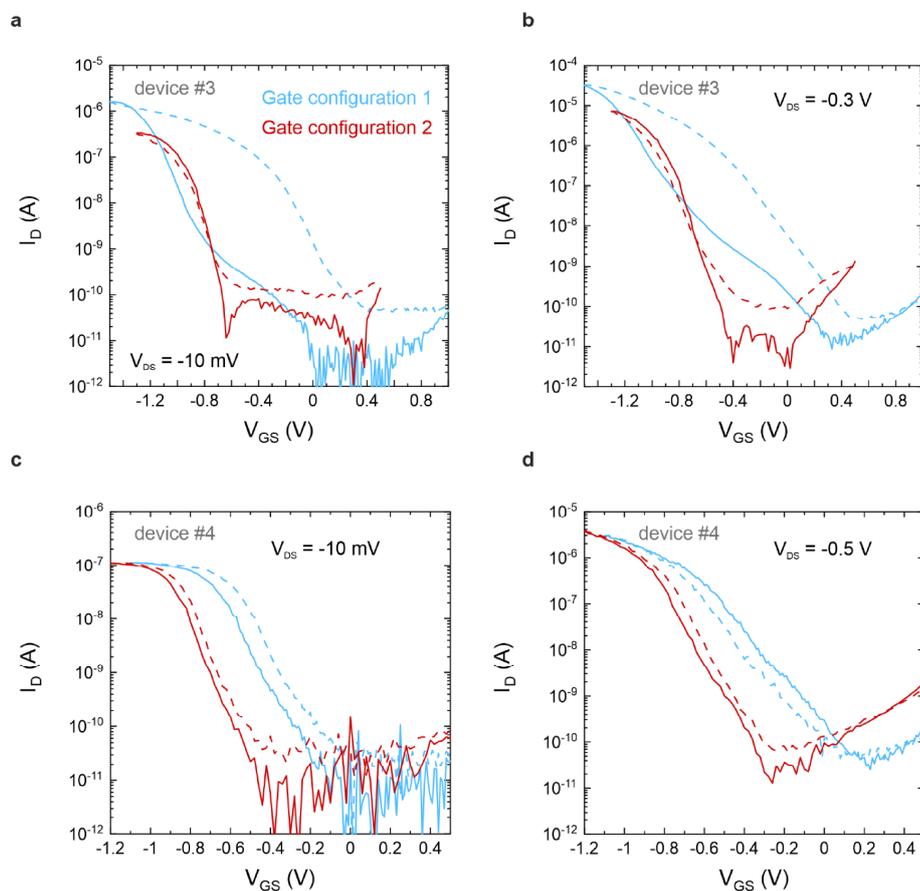


**Supplementary Figure S3.** Gate currents  $I_G$  for varying  $V_{DS}$  measured for gate configuration 1 (see supplementary Figure 2). a) Device #7 measured at a  $V_{GS}$  sweep rate of  $17 \text{ mV s}^{-1}$ . b) Device #3 measured at a  $V_{GS}$  sweep rate of  $20 \text{ mV s}^{-1}$ . Solid lines: forward sweep; dashed lines: backwards sweep.



**Supplementary Figure S4.** Linear transfer characteristics of device #2 measured for gate configuration 2 (see supplementary Figure 2) for the transistor shown in the main manuscript in Figure 2h). Solid lines: forward sweep; dashed lines: backwards sweep.

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**Supplementary Figure S5. Comparison of different gate configurations 1 and 2 (see supplementary Figure 2) measured at a  $V_{GS}$  sweep rate of  $20 \text{ mV s}^{-1}$ . Transfer characteristics of device #3 for a)  $V_{DS} = -10 \text{ mV}$  and b)  $V_{DS} = -0.3 \text{ V}$ . Transfer characteristics of device #4 for c)  $V_{DS} = -10 \text{ mV}$  and d)  $V_{DS} = -0.5 \text{ V}$ . The blue curves refer to gate configuration 1 and the red curves to gate configuration 2. Solid lines: forward sweep; dashed lines: backwards sweep.**

## B.4 Nanoscopic electrolyte-gated vertical organic transistors with low power operation and five orders of magnitude switching range for neuromorphic systems

Christian Eckel<sup>1</sup>, Jakob Lenz<sup>1</sup>, Armantas Melianas, Alberto Salleo and R. Thomas Weitz

*Submitted to Adv. Mater.*

<sup>1</sup> These authors contributed equally

## Supplementary Information

for

Nanoscopic electrolyte-gated vertical organic transistors with low power operation and five orders of magnitude switching range for neuromorphic systems

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### Materials and Methods

#### EGOT fabrication:

P-type silicon substrates with 300 nm SiO<sub>2</sub> layer are cleaned with isopropanol and acetone in an ultrasonic bath. The bottom contacts are patterned with photolithography as described below in the photolithography section. The width of the bottom contacts defines the channel width  $w_c$  (see **Fig. 1a** in the main manuscript and **Fig. S1**). 1 nm chromium (**Cr**), 30 nm Gold (**Au**) and 1 nm titanium (**Ti**) are deposited in an UHV-evaporation chamber (Bestec,  $p = 10^{-6} - 10^{-7}$  mbar), whereby Cr and Ti are used as adhesion layers. After lift-off in acetone the top contacts are patterned in the same manner. The thickness of the sputtered (Ardenne LS320) SiO<sub>2</sub> spacer defines the channel length  $L_c$  ( $P = 50$  W, argon pressure  $p = 2 \times 10^{-2}$  mbar, see Figure 1a in the main manuscript). The top contacts with 1 nm **Ti** and 90 nm **Au** are done again via evaporation. In the next step, SiO<sub>2</sub> between the top and bottom contacts is etched for 80 s with a 1 % **HF**-solution resulting in an under-etched channel distance  $d_c$  of around 80 nm (see Figure 1a in the main manuscript). The under etched region is filled with our **PDPP OSC** via spin-coating. The **PDPP** is dissolved in **MDCB** with a ratio of 15 mg/ml and is stirred overnight at 80 °C. Settings for the spin-coating: 40 s at 1000/min and a ramp of 1000 followed by a softbake for 2 min at

## B.4 Nanoscopic electrolyte-gated VOFETs for neuromorphic systems

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80 °C. The **OSC** is directional etched away with an **RIE** machine (Oxford PlasmaLab 100 ICP65) with an oxygen plasma (20 sccm, 20 mbar, 50 W), until the remaining **OSC** is solely under the top contact. A **PEDOT:PSS** droplet as gate electrode is placed next to the channel with a syringe and annealed for 10 min at 80 °C. Finally the **EMIM:TFSI** electrolyte is deposited over the channel with a syringe, building a connection to the **PEDOT:PSS**. An overnight bake in a vacuum oven at 10 mbar and 50 °C reduces moisture residues. An ozone clean atmosphere is ensured during all processing steps. The device dimensions for the used EGOTs are listed in Table S1. Top view microscope pictures of the devices can be found in **Fig. S1-S3**.

Photolithography:

As a photoresist we used AZ701 MIR combined with the adhesion coating Ti-Prime. For deposition, spin-coating is used with following settings. For Ti-Prime 10 s, 500 /min, 200 ramp followed by 30 s, 5000 /min, 1000 ramp with a 120 s, 90 °C softbake. The AZ701 MIR is spin-coated with 3 s, 800 /min 800 ramp followed by 30 s 6000 /min 4000 ramp with a 60 s, 90 °C softbake. A Maskaligner (KarlSuss MJB3) with a He-lamp as the source imprints the structure through a Cr mask with an exposure time of 90s. The development of the structure is done by immersing the sample for 30 s into AZ726 MIF followed by a DI-Water bath. The lift-off procedure after metal and SiO<sub>2</sub> deposition uses 3 x acetone and 1 x isopropanol in an ultrasonic bath with low power, each step taking 4 – 5 min.

Electrical measurement:

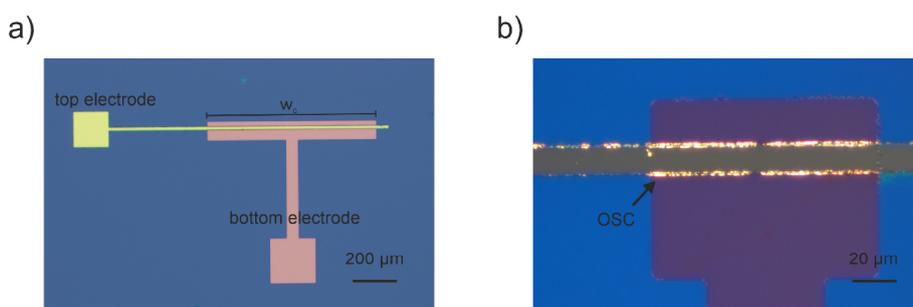
The electrical characterization measurements (transfer and output curve) are performed via two source-meter units (Keithley 2450). Except for Fig. S3, all synaptic measurements were performed in a vacuum chamber at pressures below 10<sup>-4</sup> mbar. Source, drain and gate electrodes are contacted with Au bonding wires. For pulse generation, Keysight 3350B units were used. The currents are translated into voltages with transimpedance amplifiers DLPCA-200 and monitored with an RTB2004 oscilloscope. For synchronisation of the units and measurement evaluation, a customized software is used.

## B Supplementary material for the publications

Nr.	Used in Figure	Channel dimension
1	Fig. 1b	$L_c = 35\text{nm}$ , $w_c = 12\mu\text{m}$ , $d_c = 80\text{nm}$
2	Fig. 1c	$L_c = 35\text{nm}$ , $w_c = 50\mu\text{m}$ , $d_c = 80\text{nm}$
3	Fig. 1d, Fig 3, Fig. 4, Fig. 5, Fig. S4b, Fig. S6, Fig. S8	$L_c = 35\text{nm}$ , $w_c = 50\mu\text{m}$ , $d_c = 80\text{nm}$
4	Fig. 3, Fig. 4, Fig. 5, Fig. S4a	$L_c = 35\text{nm}$ , $w_c = 12\mu\text{m}$ , $d_c = 80\text{nm}$
5	Fig. 4, Fig. 5	$L_c = 35\text{nm}$ , $w_c = 50\mu\text{m}$ , $d_c = 80\text{nm}$
6	Fig. S3	$L_c = 35\text{nm}$ , $w_c = 50\mu\text{m}$ , $d_c = 80\text{nm}$
7	Fig. S5, Fig. S7	$L_c = 35\text{nm}$ , $w_c = 4\mu\text{m}$ , $d_c = 80\text{nm}$

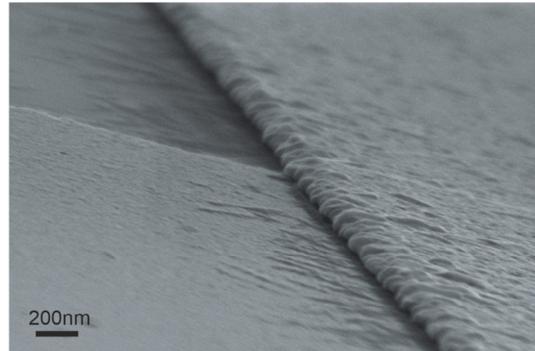
Table S1: EGOTs used in the figures of this article and their channel dimension.

### 1. Device pictures

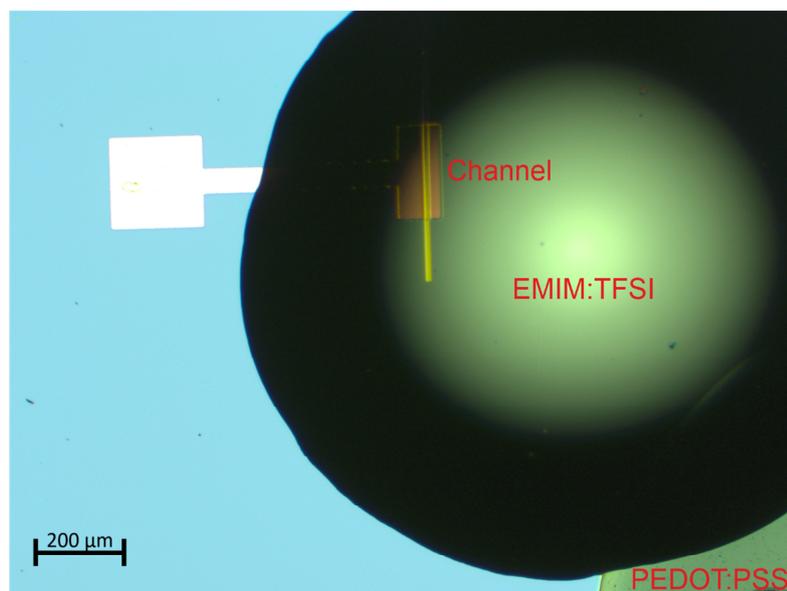


**Supplementary Figure S1: EGOT top view after RIE etching step.** a) Optical microscope picture of top and bottom contact. b) Polarised microscope picture of the channel. OSC remains can be seen only in the underetched region below the top gold contact.

## B.4 Nanoscopic electrolyte-gated VOFETs for neuromorphic systems



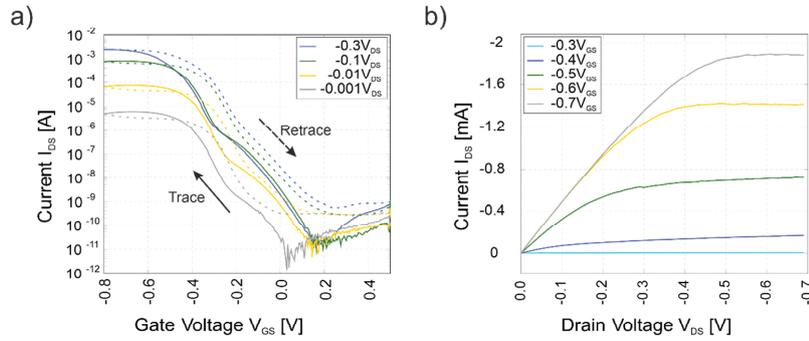
Supplementary Figure S2: SEM Picture. Original SEM Picture of Fig. 1b main manuscript. Side view of channel after RIE etching.



Supplementary Figure S3: Top view of gated transistor. In the bottom right is the PEDOT:PSS gate. The electrolyte droplet covers the channel of the transistor and connects it to the gate.

## B Supplementary material for the publications

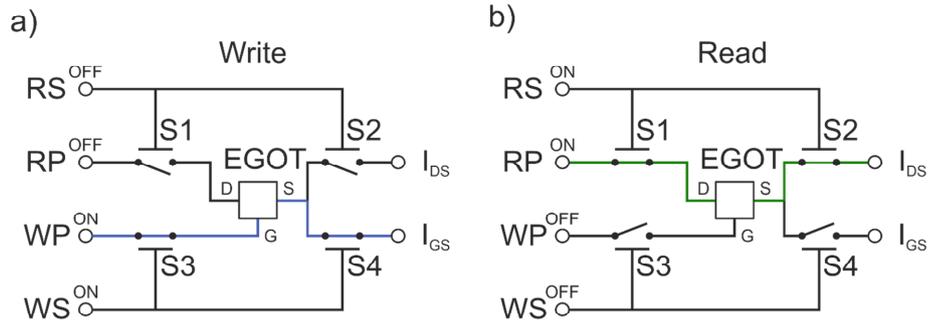
### 2. Electrical characteristic



**Supplementary Figure S4: Exemplary electrical measurement of an EGOT:** Measurements are taken in ambient atmosphere.

a) Transfer characteristics with sweep velocity 0.01V/s b) Output characteristics.

### 3. Switching Circuit



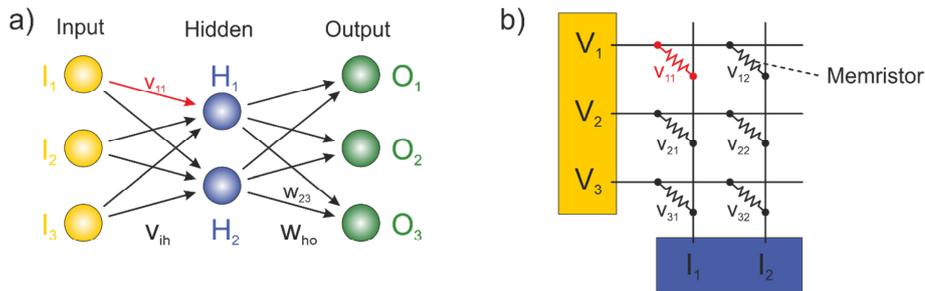
**Supplementary Figure S5: Switching circuit for the EGOT during a write and read-operation.** Switches S1-S4 are controlled by signals from the read-select (RS) and write-select (WS) inputs. a) During a write-pulse (WP), S3+4 are closed and the voltage is applied at the gate whereas the drain is floating. The gate-source-current  $I_{GS}$  flows over the blue path. b) During a read-pulse (RP), S1+2 are closed and the voltage is applied at the drain whereas the gate is floating. The drain-source-current  $I_{DS}$  flows over the green path.

The measurements for the conductance switching are performed using the electrical circuit of **Supplementary Fig5** (adapted from [1]). The main idea of the circuit is the decoupling of conductance change operation (write, **Fig. S5a**) and measuring the channel conductance (read, **Fig S5b**). For that purpose, four commercial transistors S1-S4 are placed around the EGOT. A write operation applies a write pulse (WP) at the gate while at the same time a synchronized signal at WS closes the switches S3 and S4. Hence, ions can penetrate into the channel and update the conductivity. The amount of

## B.4 Nanoscopic electrolyte-gated VOFETs for neuromorphic systems

penetrating ions is monitored by the gate-source-current  $I_{GS}$ . During a write-operation, the switches S1 and S2 are open to prevent any undesired currents. To extract the conductivity state, a read-pulse (RP) is applied at the drain of the EGOT together with a synchronized pulse at the RS to close the switches S1 and S2. With the measured drain-source-current  $I_{DS}$  it is possible to calculate the conductivity with Ohm's law and the drain voltage. Switches S3 and S4 are open, thereby hindering the discharging of the ions from the channel back into the electrolyte. The conductance state stays stable. In phases where no read or write pulse is applied, the EGOT is in a floating state due to the open switches S1-S4. The pulses are generated by two Keysight 3350B wavegenerators. For monitoring the currents, an RTB2004 oscilloscope is used combined with a transimpedance amplifier DLPCA-200. For the switches we used an IC-EPP394 with 1 M $\Omega$  Off-resistance. One can assume that the 1 M $\Omega$  resistance sufficiently prevents the discharging process.

### 4. Deep Neural Network

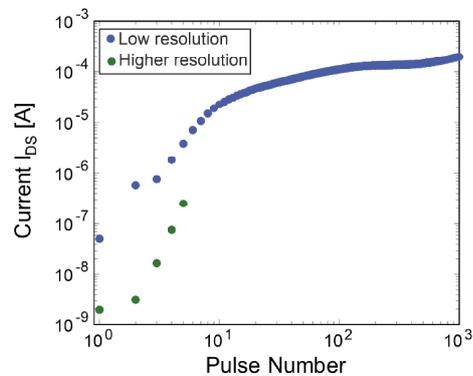


**Supplementary Figure S6: Artificial neural network.** a) A three layer feedforward network architecture. Each neuron, marked as circles, is connected with all neurons from the previous and the following layer with different connection strengths  $v_{ih}$  or  $w_{ho}$ . Information is traveling from the left to the right side. By applying a learning algorithm like the backpropagation algorithm, the network can be trained to optimize the output results. b) A crossbar array to realize a hardware based neural network. It shows the connection between the input and the hidden layer of a). The connection strengths are realized by memristors which have a tuneable conductance. Therefore, the current responses  $I_{1/2}$  depend on the input voltages  $V_{1-3}$  and the conductances  $v_{ih}$ . The connection  $v_{11}$  and the corresponding memristor in the array are both marked in red.

Multiple architecture types for artificial neural networks (ANN) have been developed. One network commonly used is the deep neural network (DNN), which is based on a feedforward-inference architecture in combination with a backpropagation algorithm [2, 3]. Fig. S6a shows an example of a neural network. It consists of an input layer with three input neurons (yellow), two neurons in the hidden layer (blue) and three output neurons (green). Every neuron is connected with all neurons of

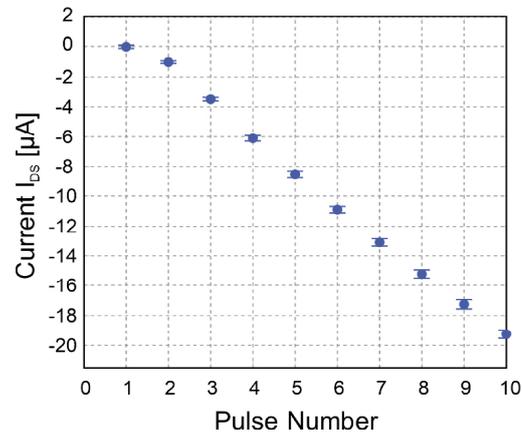
the previous and the following layer. No interconnection within one layer is allowed. Information only passes from the left to the right and is encoded in the activation of the single neurons. The connection weight, similar to the synaptic strength, is given by  $v_{ih}$  and  $w_{ho}$ . The number of layers and the amount of neurons in one layer are free to choose. Classical computers are build with a von Neumann architecture which entails processing problems in high data transfer tasks such as ANN [4]. To overcome this problem for computation in software-based networks, also referred to von Neumann bottleneck, a hardware realization with memristive devices can be used. It allows a highly parallel computing with the use of vector-matrix multiplication [5]. For that purpose, the devices are ordered in a crossbar array as shown in Fig. S6b. The activation of a neuron in such an array is represented by different voltage inputs, whereas the conductance of the memristive device emulates the corresponding synaptic weight. The sum of the currents over the memristive devices for each output path are translated into a voltage and serves as the input for the next layer.

### 5. High range switching Log-Log Plot



**Supplementary Figure S7: High switching measurement.** The plot shows the same data as in Fig. 2a of the main manuscript in a Log-Log diagram. Due to vertical resolution limitations of the used oscilloscope, the measurement is split into a high resolution (green) and low resolution (blue) part. Combining the two measurement runs results in a total switching range over 5 orders of magnitude. Settings:  $t_{write} = 10 \mu s$ ,  $V_{write} = -0.9 V$ ,  $t_{read} = 100 ms$ ,  $V_{read} = -0.5 V$ ,  $t_{pause} = 100 \mu s$ .

### 6. Explicit test of the accessible number of states

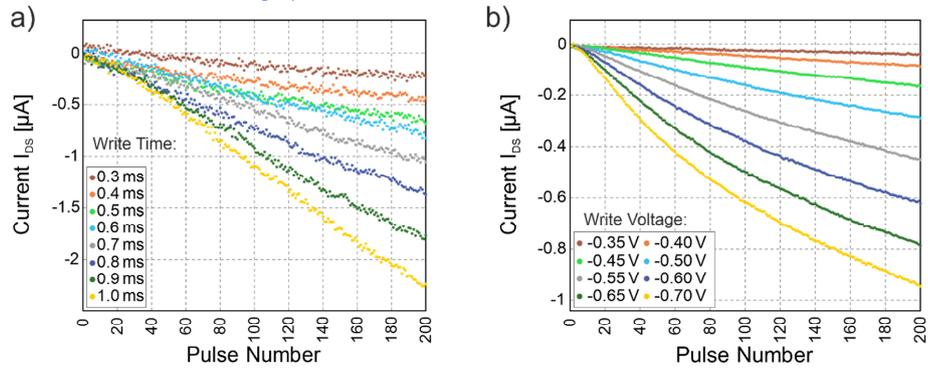


**Supplementary Figure S8: Distinct conductance states.** Increase of conductance over 10 pulses with error bars. Maximum standard deviation during a read pulse was 0.31  $\mu\text{A}$ . Settings:  $t_{\text{write}} = 0.1$  s,  $V_{\text{write}} = -0.7$  V,  $t_{\text{read}} = 0.1$  s,  $V_{\text{read}} = -0.1$  V,  $t_{\text{pause}} = 0.1$  s. The measurement error stems from noise and discharging during read out pulses.

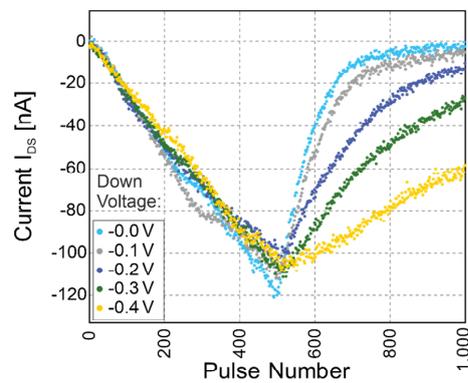
According to van de Burgt et al. [5] at least 100 distinct conductive states for synaptic devices are required to work adequate as a synaptic weight in a **DNN**. Additionally, Yu et al. simulated that the accuracy of their **DNN** starts to saturate at a state number of 128[6]. For a qualitative estimation of the possible states, we assume that a separation of the conductance level by two times the maximum measured standard deviation is sufficient for distinguishability. **Fig. S8** shows a measurement of 10 pulses together with the standard deviation. The maximum standard deviation was 0.31  $\mu\text{A}$ . As can be calculated from **Fig. 2a** in the main manuscript, the maximum current realized by switching was 0.2 mA (Conductance/Voltage = 392  $\mu\text{S}/0.5\text{V}$ ). Hence, the estimated number of distinguishable conductance states calculates to 322 (Calculation:  $0.2 \text{ mA}/(2 \times 0.31 \mu\text{A})$ ). Further studies in decreasing noise and reducing pulse times can increase this number.

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### 7. Conductive change parameters

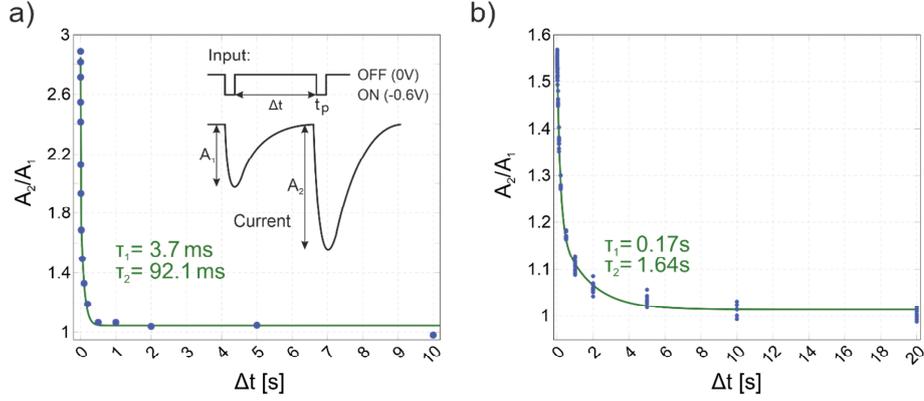


**Supplementary Figure S9: Write time/voltage sweep measurements:** Circuit as in Fig. S4. All measurements were performed with different devices. a) Changing the write pulse duration while keeping the other parameters constant at  $V_{write} = -0.8$  V,  $t_{read} = 5$  ms,  $V_{read} = -0.1$  V,  $t_{pause} = 100$   $\mu s$ . b) Changing the write voltage while keeping the other parameters constant at  $t_{write} = 100$   $\mu s$ ,  $t_{read} = 5$  ms,  $V_{read} = -1$  mV,  $t_{pause} = 100$   $\mu s$ .



**Supplementary Figure S10: Down writing sweep:** Changing the voltage of writing after pulse 500. Other parameters remain constant. Settings:  $t_{write} = 5$  ms,  $V_{write, up} = -1.2$  V,  $t_{read} = 10$  ms,  $V_{read} = -0.1$  V,  $t_{pause} = 100$   $\mu s$ .

### 8. PPF/PTP Measurement



**Supplementary Figure S11: Paired-Pulse facilitation measurement.** Two equal gate pulses with  $-0.6V_{GS}$  separated by  $\Delta t$  are applied at the EGOT while a constant drain voltage of  $-0.1V_{DS}$  is present. The ratio of the maximum current responses  $A_2/A_1$  between the first and second pulse is plotted over the time separation. A double exponential decay is fitted to the data. a) Pulse width  $t_p$  of 10 ms and b) pulse width  $t_p$  of 100 ms. Each measurement is acquired ten times.

Paired pulse facilitation (**PPF**) is a short-term plasticity effect in biological synapses and lasts between milliseconds to few minutes [7]. Two pre-synaptic action potentials separated by  $\Delta t$  in time lead to membrane potential changes at the post-synaptic side with corresponding amplitudes  $A_1$  &  $A_2$  due to ion penetration into the membrane. An increase of  $A_2$  with respect to  $A_1$  is called **PPF**. The opposite process, where  $A_2$  decreases, is called paired-pulse depression. By increasing the time delay  $\Delta t$  of the second pulse, the correlation between these two pulses becomes weaker. In some synapses the function of  $A_2/A_1(\Delta t)$  follows a double exponential decay according to

$$\frac{A_2}{A_1} = C_1 e^{-\Delta t/\tau_1} + C_2 e^{-\Delta t/\tau_2} + 1. \quad (1)$$

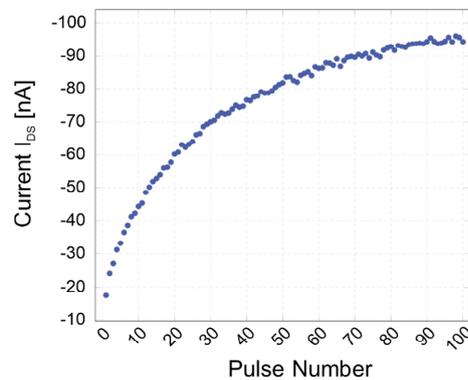
Often, a distinction of the two decays is not possible and a single exponential fit is sufficient. The decays originate from the ion diffusion out of the post-synapse back into the synaptic cleft and a relaxation of the neurotransmitter density in the cleft, if no action potential is present at the pre-synaptic side[7]. Similar holds for the **EGOT** devices. For shorter time delays, more ions accumulate in the channel. Hence, a higher current response for the second pulse is observed. Increasing the time gap allows the ions to diffuse back into the electrolyte and de-dope the channel [8]. We were able to measure similar decay behaviour as in human synapses. For the 10 ms pulse duration, (see **Supplementary Figure S11a**)) comparable timescales to the biological synapses are achieved with  $\tau_1 = 3.7$  ms and  $\tau_2 = 92.1$  ms

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[7, 9]. The time constants themselves depend on the pulse durations. For instance, **Fig. S11b** represents a measurement with a 100ms pulse duration and increased time constants  $\tau_1 = 0.17\text{s}$  and  $\tau_2 = 1.64\text{s}$ .

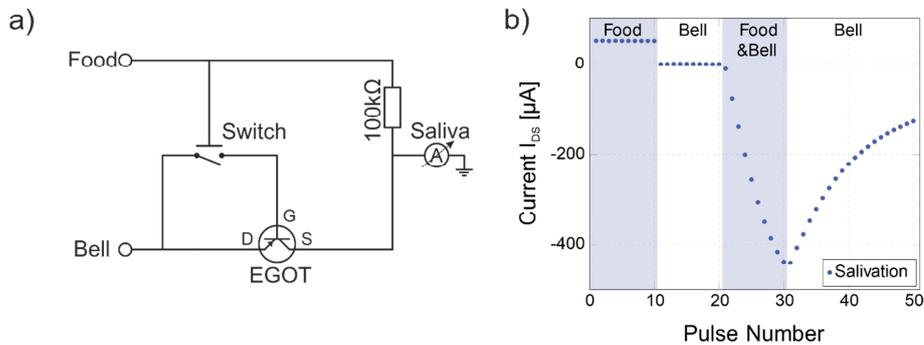
A train of pulses can facilitate the information transport over a synapse even further. This synaptic plasticity effect is called post tetanic potentiation (**PTP**) [9] and was already observed in a memristive device reported by Liu et al. [10]. Connecting the drain and gate electrodes during a pulse train of 100 pulses with a pulse length of 100 ms and a bias of -0.7 V lead to an overall increased current response (see **Fig. S12**). The time between the pulses (100 ms) is not sufficient for the ions to fully relax back into the electrolyte. Hence, an accumulation of the ions in the channel occurs.



**Supplementary Figure S12: Post-tetanic-potentiation measurement.** The gate and the drain contacts are connected and a train of 100 input pulses with a bias of -0.7 V and 100 ms duration is applied. Between each pulse, a 100 ms pause with 0 V at the input is present. An increasing current response with higher pulse number was measured because of the ion accumulation in the channel.

## B.4 Nanoscopic electrolyte-gated VOFETs for neuromorphic systems

### 9. Pavlov's experiment



**Supplementary Figure S13: Electrical version of Pavlov's dog.** a) The measurement is subdivided into four phases similar to the classical conditioning experiment. In the first phase only the food input is applied with a non-zero response of the salivation current, followed by merely bell input signals with no significant response. During the third phase, both inputs are activated simultaneously and an increasing response can be observed corresponding to learning. In the last phase, the bell signal is now sufficient to create a non-zero response. The current decrease is referred to unlearning mechanism. b) Electrical circuit of the experiment. Pulse duration and pause time each are 1 s. Food signal 5 V. Bell signal -0.6 V.

The well-known classical conditioning experiment performed by Pavlov was one of the first concepts of learning behaviour. The experiment had the following sequence.

Food is offered to a dog, which is used as an unconditioned stimulus (**UCS**). The natural response to food is salivation, an unconditioned response (**UCR**). Ringing a bell does not have any effect on the dog in the beginning and serves as a neutral stimulus (**NS**). Pavlov trained his dog by presenting food (**UCS**) together with ringing the bell (**NS**). After a while, the dog associates the ringing bell with getting food, thereby the **NS** is becoming a conditioned stimulus (**CS**). The salivation is now a conditioned response (**CR**) to the **CS**. If the dog only hears the bell (**CS**) without receiving food (**UCS**) for a while, the association will disappear and the bell is turning back into a **NS** [11].

We were able to realize this learning experiment with an electrical circuit including our **EGOT** device (see **Fig. S13a**). It contains two inputs as representatives of the bell and food from the original experiment. The measured current response mimics the salivation of the dog. Applying a food signal (**UCS**) leads to a current flow over the resistor (**UCR**) and simultaneously closes the switch. A bell signal (**NS**) produces a drain source current over the **EGOT** channel depending on the conductance state. Changing this state is only possible if a food signal is present and if consequently the switch is closed. Then the bell signal can force ions from the electrolyte to penetrate the channel and increase its conductance. This phase corresponds to the association process where the bell becomes a **CS**. The measurement run is depicted in **Fig. S13b**. It shows a current response in the case of solely food signals. During the first bell signals (**NS**), no current response was monitored. Synchronous food and bell signals

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show a steady increase of the current, which is corresponding to the learning phase, followed by a decreasing response when solely a bell signal is applied. The association becomes weaker over time and the food signal goes back to a **NS**.

### 10. Single-Input Single-Output (SISO)

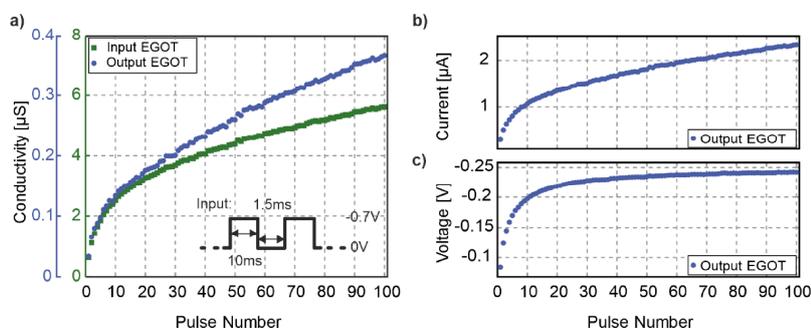
The single-input single-output (**SISO**) configuration (see **Fig. 4a**) shows the feasibility to send information over a chain of **EGOTs**. This setup reflects an information transfer through a neuron cell over the input and output synapses.

**Supplementary Figure S14:** shows the response during an input signal sequence (see inset

**Supplementary Figure S14:4a**). Both synapses exhibit an increase in their conductance (see

**Supplementary Figure S14:a**) due to ion accumulation in their channels. Additionally, higher output responses are measurable whilst keeping the input train present (see

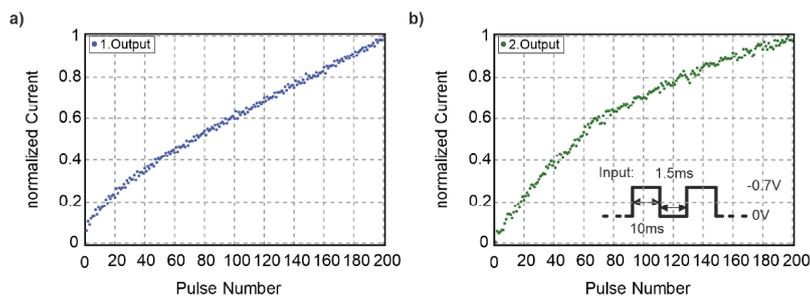
**Supplementary Figure S14:b**). This behaviour can be understood as a realization of learning reminiscent to biological synapses. The information transfer over our electrical neuron is facilitated during the usage. The voltage drop over the second **EGOT** is increasing (see **Fig. 14c**) caused by a reduced resistance ratio between the first **EGOT** and the parallel input resistance of the oscilloscope together with the second **EGOT**.



**Supplementary Figure S14: Single-Input Single-Output measurement.** Two EGOTs in series with their gate and drain contacts connected (see Fig. 4a). a) Output current, b) voltage drop over the second EGOT and c) resistance of the EGOTs over 100 applied pulses. The pulse sequence is represented in the inset of c). Input settings:  $t_{ON} = 10$  ms;  $t_{OFF} = 1.5$  ms;  $V_{ON} = -0.7$  V;  $V_{OFF} = 0$  V.

### 11. Single-Input Multiple-Output

On the other hand, the single-input multiple-output (**SIMO**) configuration allows verifying the possibility of an interconnection at the output side similar to the neuron cells at the axon terminals, which can transmit their electrical impulse to multiple post-neurons. The **SIMO** system consists of one input synapse and two output synapses (see **Fig. 4a**). The results of the output currents are plotted depending on the number of input pulses (see Fehler! Verweisquelle konnte nicht gefunden werden.). Our measurements show that input signals can be distributed over multiple **EGOTs** while both outputs exhibit the synaptic strength increase due to the ion accumulation. Since our devices are not industrially fabricated, the output current responses differ with respect to the absolute value. Whereas the relative current change is similar for both outputs. Enlarging the number of outputs would be the next step to achieve a comparison to the biological neurons.



**Supplementary Figure S15: Single-Input Multiple-Output measurement:** One input EGOT in series with two parallel output EGOTs. Each EGOT has its gate and drain contacts connected (See Fig. 2c). a,b) Normalized current response on 1. Output (a) and 2. Output (b) over 200 applied pulses. The pulse sequence is represented in the inset of c). Input settings:  $t_{ON} = 10\text{ms}$ ;  $t_{OFF} = 1.5\text{ms}$ ;  $V_{ON} = -0.6\text{V}$ ;  $V_{OFF} = 0\text{V}$ .

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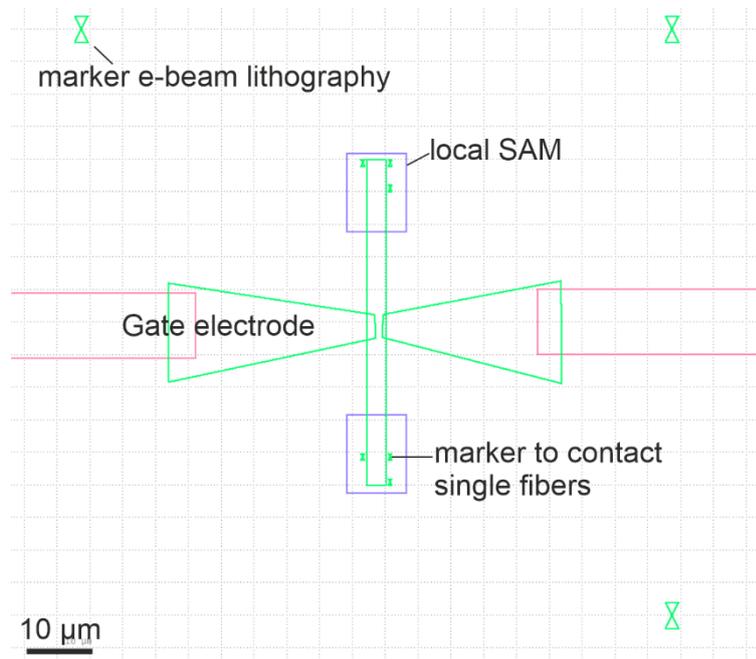
# C Supporting information: Single polymer fiber transistor

Lab book sample assignment: D21 → H1; D37 → H2; D8 → H3; D29 → A1; D36 → A2

## C.1 Fabrication of single fiber transistors

To avoid degradation of the PDPP polymer all fabrication steps involving exposure to ambient conditions were performed in an ozone cleaned atmosphere.

### Single polymer fiber transistors with a hybrid $\text{Al}_2\text{O}_3/\text{SAM}$ gate

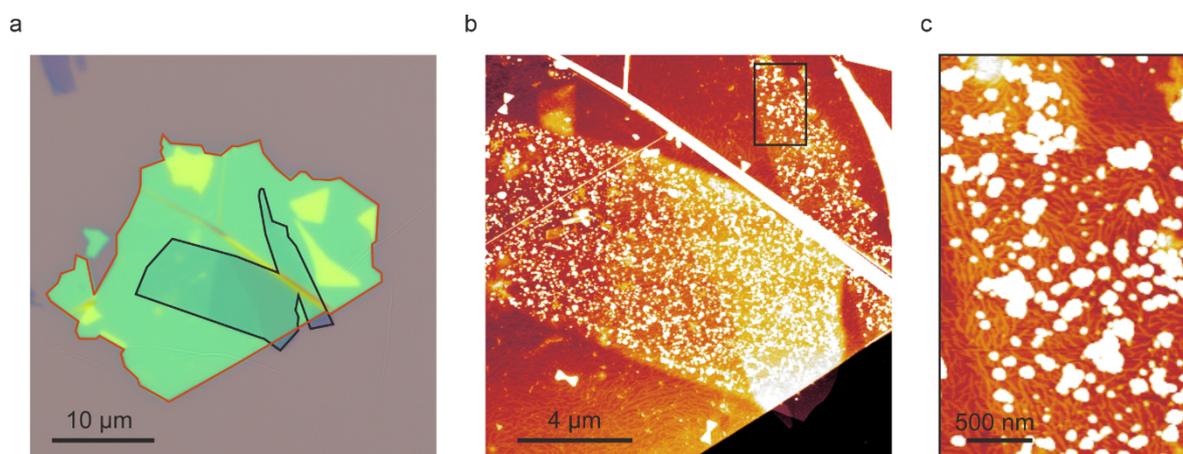


**Figure C.1** E-beam lithography layout for single polymer fibers on a local  $\text{Al}_2\text{O}_3/\text{SAM}$  gate.

## C Supporting information: Single polymer fiber transistor

The device fabrication for single polymer fiber transistors with a local hybrid  $\text{Al}_2\text{O}_3$ /SAM gate dielectric, which included three different lithography steps, was performed according to the klayout (version 0.24.4 by Matthias Köfferlein) design in Figure C.1. First the local gate electrodes and markers were patterned, whereby a  $1000\ \mu\text{m}$  writefield was used for the red gate leads and a  $100\ \mu\text{m}$  for the green local gate electrode and markers. The larger outer markers were used to align the layout for the second and third lithography step and the small markers next to the gate electrode to locate single polymer fibers using AFM (Dimension 3100). After  $\text{Al}_2\text{O}_3$  deposition on the whole surface the local SAM regions (violet) were patterned in a second lithography step (see section 3.2). While the rest of the substrate is covered with PMMA to maintain the hydrophilicity of  $\text{SiO}_2$ , the TDPA SAM was formed locally on the gate electrodes due to the large hydrophobicity of phosphonic acid SAMs<sup>156</sup> which would in case of a whole coverage prevent the wettability of PMMA in the last lithography step. Single polymer fibers on local  $\text{Al}_2\text{O}_3$ /SAM gate were deposited by immersing the sample overnight in a 0.02 wt.% solution of PDPP in MDCB at room temperature. The solution was previously stirred at least for 6 hours at  $80\ ^\circ\text{C}$ . The sample was blow-dried with nitrogen and baked for 5 min at  $80\ ^\circ\text{C}$ . After OSC deposition, a third lithography step was performed to contact the single polymer fibers (not shown in Figure C.1). Here, instead of a 3 min  $150\ ^\circ\text{C}$  softbake, the PMMA was baked for 5 min at  $120\ ^\circ\text{C}$  to prevent thermal damage of the OSC. In this last lithography step PDPP was contacted with PMMA and anisole, heated to  $120\ ^\circ\text{C}$  and immersed in acetone and isopropanol for lift-off.

### Single polymer fiber transistors with a graphite/hBN gate

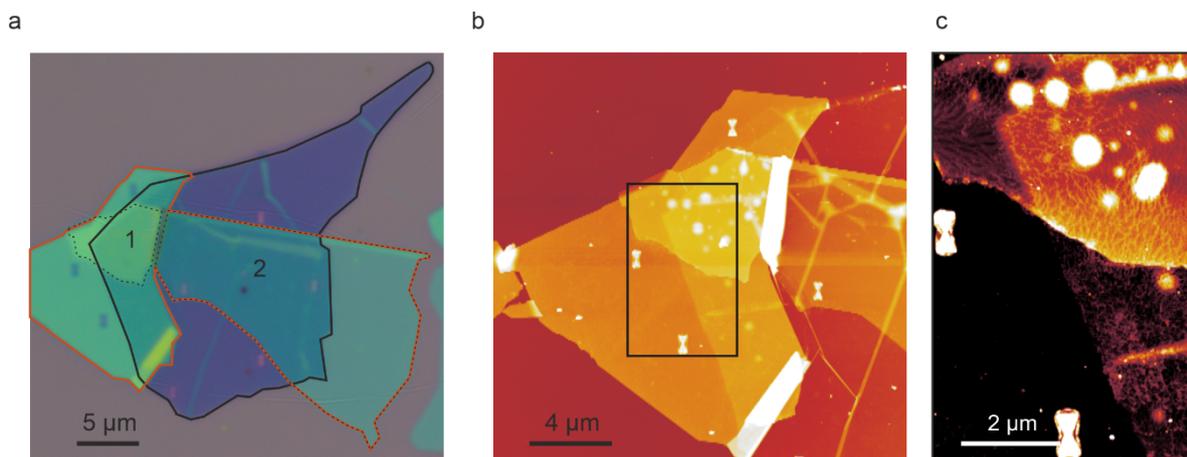


**Figure C.2 Sample H1: Single polymer fibers on a graphite/hBN gate where the sample was immersed a 0.2 wt.% solution.** a) Optical microscopy image of the finished stack with the bottom graphite electrode (black) and top hBN layer (red). b) AFM image after fiber deposition and c) zoom in of the black rectangle in b). The thickness of the hBN flake is 25 nm.

## C.1 Fabrication of single fiber transistors

After the fabrication of a graphite/hBN stack (see section 3.3) a local marker system to locate single polymer fibers using AFM and to align the contact layout was applied. As these small markers showed poor adhesion to the hBN surface and tended to rotate or dissolve, RIE was performed for 11 sec (recipe can be found in publication P4) after developing PMMA to embed the evaporated markers in hBN/graphite. Single polymer fibers were deposited in two different ways. One approach (see Figure C.2) is completely analogous as above with the exception that a 0.2 wt.% solution was used. Although this technique results in single polymer fibers on the hBN surface as can be clearly seen in the AFM images in Figure C.2 b-c), also large polymer clusters are formed. To assure that the large grains are indeed the OSC on top of hBN and not dirt or glue residues in between the graphite and hBN layer resulting from the stamping procedure, AFM images were taken after every single step for a different sample. Here the large grains were not observed until immersing the sample in the OSC solution. One possible explanation why these large clusters only form at the overlay of graphite and hBN could be a different surface energy induced by the underlying graphite layer. Nevertheless, single fibers on this sample were contacted for electrical characterization (sample H1).

To avoid large polymer clusters, a different approach was used for another stack (Figure C.3; sample H2). A solution of 0.05 wt.% was drop casted on the substrate. Subsequently the droplet was slowly blown over the graphite/hBN stack with nitrogen, resulting in a very thin remaining layer of the OSC solution. The sample was dried at room temperature and subsequently baked for 5 min at 80 °C. Here, no large polymer clusters can be seen in the AFM images. It has to be noted that the poor quality of small AFM images (see Figure C.3 c)) is probably related to a broken vacuum pump, which is necessary to fix the sample during AFM scanning.



**Figure C.3 Sample H2: Single polymer fibers on a graphite/hBN gate where an OSC solution was drop-casted on the sample.** (a) Optical microscopy image of the finished stack with the bottom graphite electrode (black) and top hBN layer (red). (b) AFM image after fiber deposition and (c) zoom into the black rectangle in (b). The thickness of the hBN flake is 11 nm in region 1 and 25 nm in region 2.

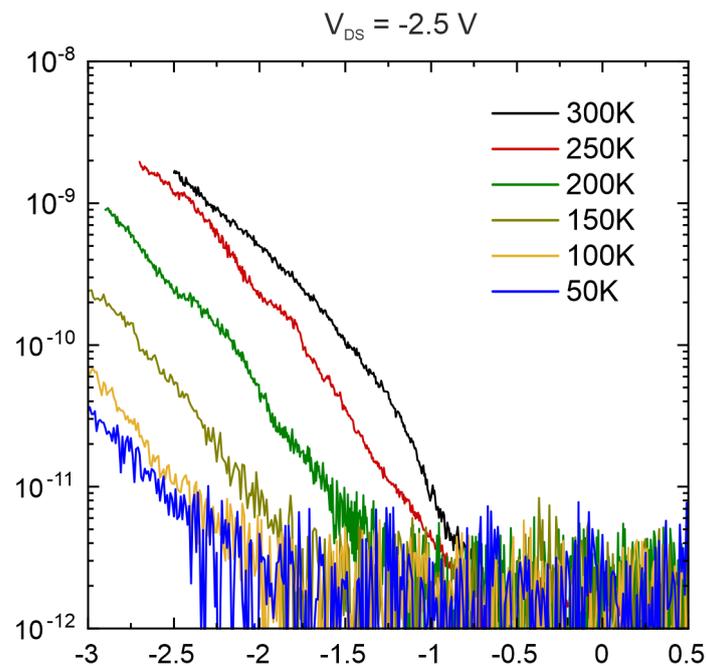
## C Supporting information: Single polymer fiber transistor

### C.2 Electrical characteristics of single fiber transistors

In this section, further measurement data not shown within the discussion in section 5 is presented. The additional data supports the presented results and is shown for completeness and reference.

#### Influences of contact OSC interface on electrical characteristics

The influence of the contacts in terms of contact resistances and tunnel barriers can be seen in Figure C.4 by comparing two measurements on the same transistor, where the source and drain configuration was exchanged between the first (solid lines) and the second (dashed lines) measurement. As can be clearly seen in both the output and transfer characteristics, the different in- and ejection barriers lead to different shapes and magnitudes of the measured currents.

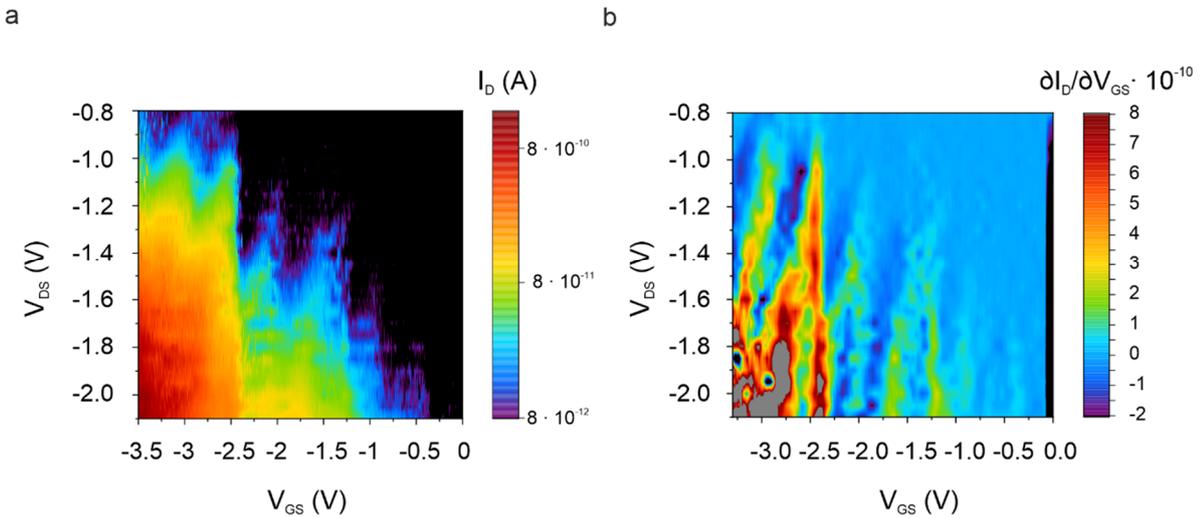


**Figure C.4** Transfer characteristics of a single PDPP fiber transistor with an  $\text{Al}_2\text{O}_3/\text{TDPA}$  gate (sample A1) for varying temperatures ( $p = 1.9 \times 10^{-7}$  mbar) measured at  $V_{DS} = -2.5$  V with a transport freeze-out at lower temperatures. Due to poor thermal coupling the given temperatures are not the real sample temperatures. The qualitative temperature behavior is still valid.

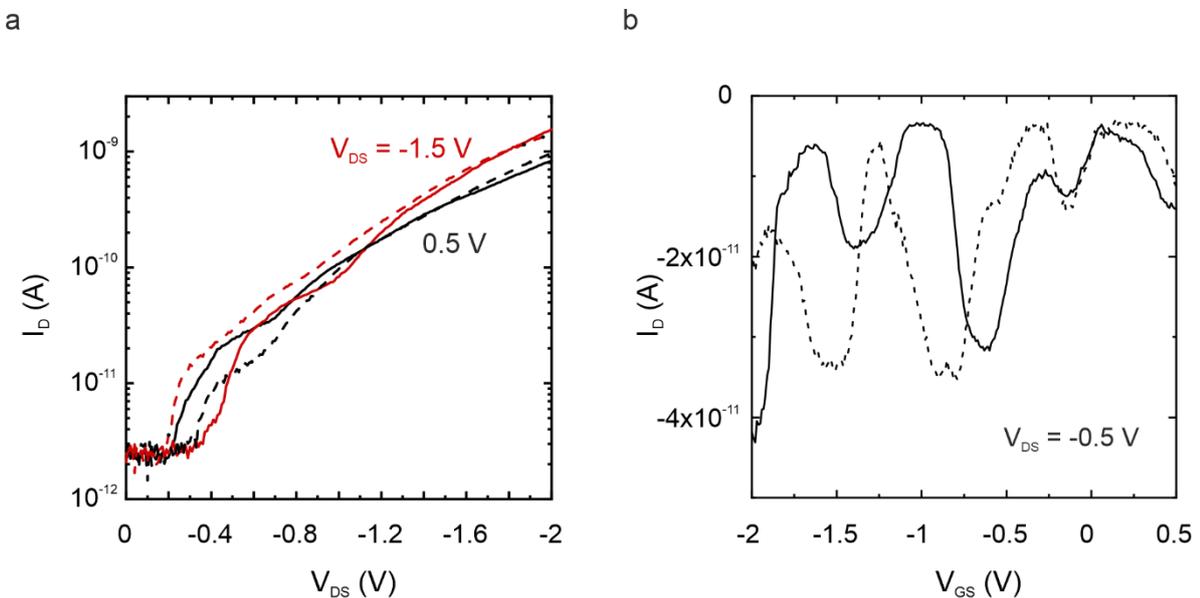
## C.2 Electrical characteristics of single fiber transistors

Coulomb blockade measurements in addition to section 5

Figure C.5 shows the first measurements of Coulomb diamonds for the same device as in Figure 5.6. However, the diamonds are only partially visible as a too small  $V_{DS}$  range was chosen.

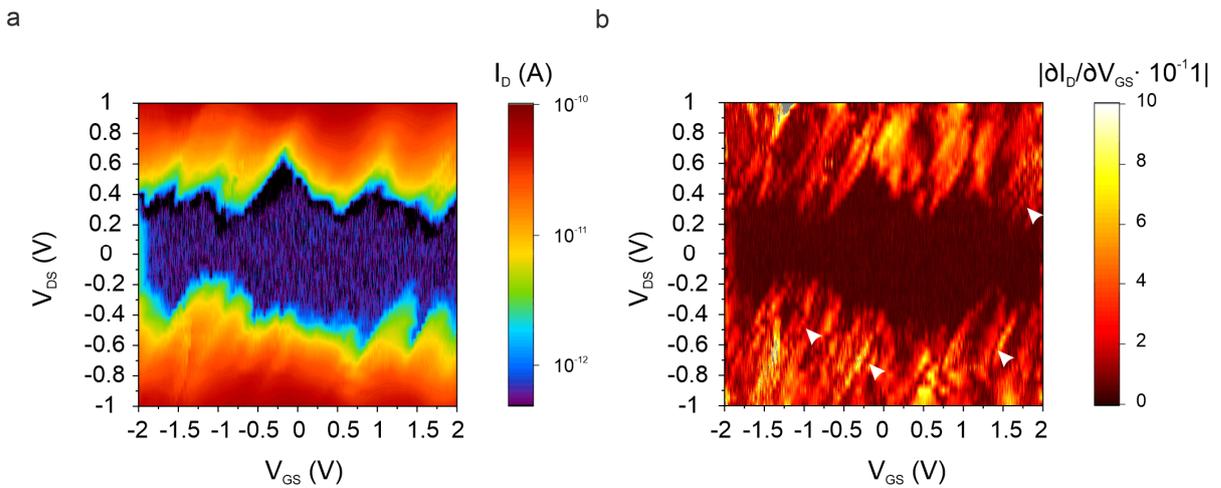


**Figure C.5** Current characteristics of the same device as in Figure 5.6 at  $T = 5.8$  K. a)  $(V_{GS}, V_{DS})$ -current map and b) differential conductance  $\partial I_D / \partial V_{GS}$ .



**Figure C.6** Influence of source and drain contacts on the electrical characteristics of a single PDPP fiber transistor on sample A2 measured at  $T = 10$  K ( $p = 1.6 \times 10^{-7}$  mbar). a) Output characteristics for two different  $V_{DS}$  and b) transfer characteristics for  $V_{DS} = -0.5$  V. The solid and dashed lines refer to an exchange of the source and drain electrodes.

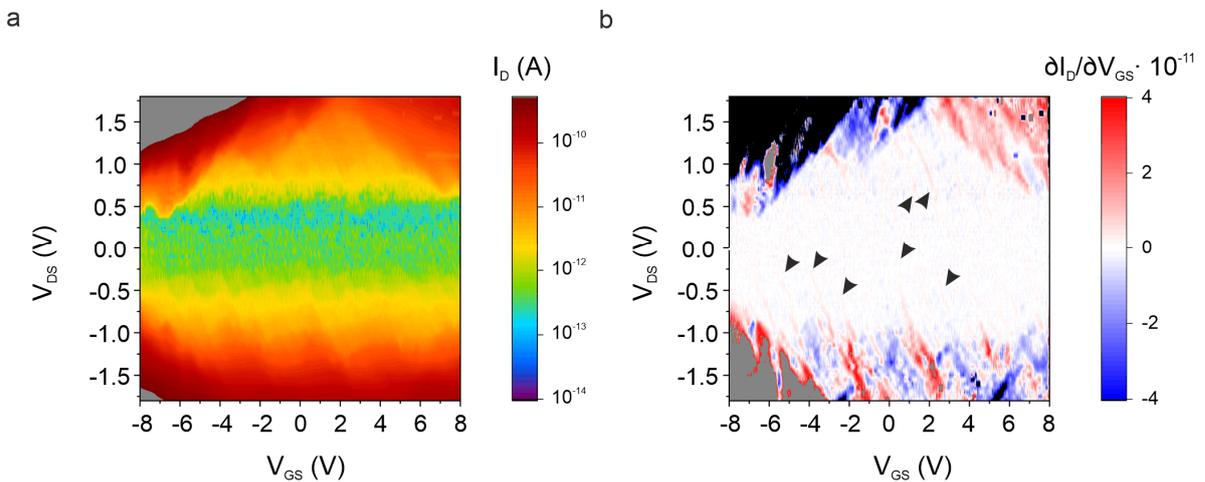
## C Supporting information: Single polymer fiber transistor



**Figure C.7 Coulomb blockade diamonds of a single PDPP fiber transistor on sample A2 measured at  $T = 5.5$  K ( $p = 1.7 \times 10^{-7}$  mbar).** ( $V_{GS}, V_{DS}$ )-current map and b) differential conductance  $\partial I_D / \partial V_{GS}$  as a function of  $V_{GS}$  and  $V_{DS}$ . Excited states are highlighted by white arrows.

In Figure C.7 another single fiber measurement on the same sample as in Figure 5.8 (sample A2) can be seen. Although a lot of excited states are visible, due to a larger disorder the individual Coulomb diamonds are not distinguishable in the differential-conductance  $\partial I_D / \partial V_{GS}$  map.

Figure C.8 shows another single fiber measurement on the same sample as in Figure 5.9 (sample H2) with a very asymmetric conductance for positive and negative  $V_{DS}$ .



**Figure C.8 Coulomb blockade diamonds of a single PDPP fiber transistor on sample H2 measured at  $T = 7$  K ( $p = 1.6 \times 10^{-7}$  mbar).** ( $V_{GS}, V_{DS}$ )-current map and b) differential conductance  $\partial I_D / \partial V_{GS}$  as a function of  $V_{GS}$  and  $V_{DS}$ . Excited states are highlighted by black arrows

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