Characterization and Optimization of the Prototype DEPFET Modules for the Belle II Pixel Vertex Detector

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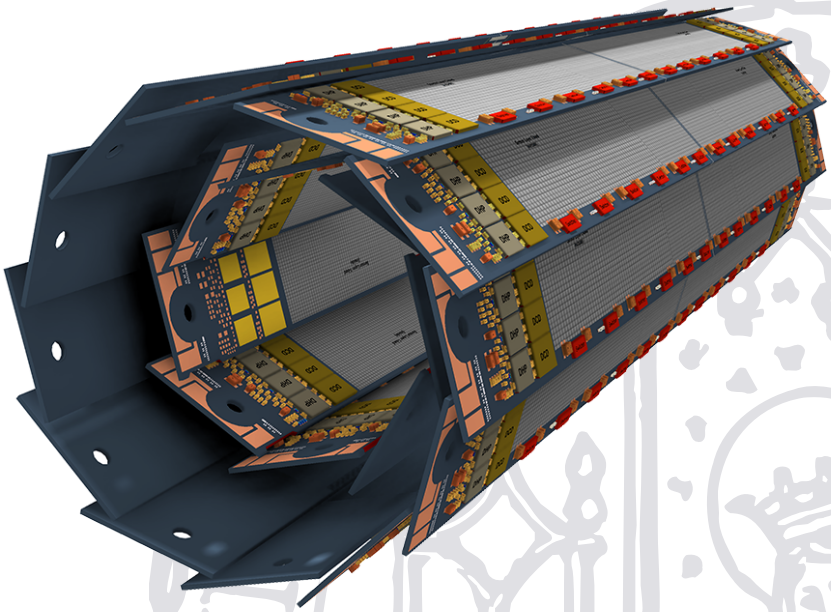

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Zusammenfassung

Der Elektron-Positron-Speicherring KEKB wurde von 1999 bis 2010 am Hochenergie- und Beschleunigerforschungszentrum KEK in Tsukuba (Japan) betrieben, wobei die Schwerpunktsenergie hauptsächlich dem Anregungszustand des $\Upsilon(4S)$-Teilchens (10.58 GeV) entsprach. KEKB erreichte während seiner Betriebszeit eine integrierte Luminosität von 1041 fb^{-1}. Mit dem Belle-Detektor wurden die Zerfälle von B-Mesonen untersucht, die die Theorie über den Ursprung der $\mathcal{CP}$-Verletzung im Standardmodell von Kobayashi und Maskawa bestätigten; dafür erhielten beide im Jahr 2008 den Nobelpreis. Der Speicherring KEKB wird zu SuperKEKB erneuert, um Antworten auf die vielen offenen Fragen des Standardmodells und möglicherweise "Neue Physik" jenseits des Standardmodells zu finden. Die Teilchenstrahlen werden auf etwa 50 Nanometer am Wechselwirkungspunkt kollimiert ("nanobeam scheme"), damit die weltweit höchste instantane Luminosität von KEKB um einen weiteren Faktor 40 auf $8\times10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ gesteigert werden kann. Die (physikalischen) Ziele des Projekts sind die präzise Vermessung der $\mathcal{CP}$-Verletzung und die Suche nach seltenen oder sogar "verbotenen" Zerfällen von B-Mesonen, um mögliche Abweichungen vom Standardmodell zu finden. Verschiedene Komponenten müssen von Belle erneuert werden (Belle II), um die hohe instantane Luminosität von SuperKEKB zu bewältigen. Nicht nur die Anzahl der Ereignisse nimmt zu, sondern auch der Untergrund, insbesondere der unvermeidbare Zwei-Photonen-Untergrundprozess.

Mit einem Siliziumvertexdetektor werden im Experiment die Zerfallsvertices der B-Mesonen analysiert. Der Vertexdetektor soll so nah wie möglich um das Strahlrohr platziert werden, damit Extrapolationsfehler der Zerfallsvertices minimiert werden. Da ein Siliziumstreifendetektor, wie er in Belle benutzt wurde, den hohen Untergrund im geringen Abstand zum Strahlrohr nicht bewältigen kann, wird ein neuartiger Pixel-Detektor (PXD) installiert, der aus monolitischen DEPFET (DEPletierter p-Kanal Feld Effekt Transistor) Pixel-Sensoren besteht. Der DEPFET-Sensor kann bis zu 75 µm gedünnt werden, um die Mehrfachstreuung zu minimieren, besitzt ein hohes Signal-Rausch-Verhältnis, verfügt über eine intrinsische Positionsausflösung von 15 µm, unterstützt schnelle Auslesezeiten von weniger als 20 µs und hat einen geringen Stromverbrauch. Der PXD besteht insgesamt aus 40 Sensor-Modulen, wobei jedes mit 14 ASICs für die Steuerung und Auslese bestückt ist. Die Module werden in zwei Lagen um das Strahlrohr montiert.

Die vorliegende Arbeit fokussiert sich auf die Charakterisierung und Optimierung der ersten Prototypen der finalen PXD-Module. Die kombinierte Kontroll- und Ausleseelektronik wurde auf Prototyp-Modulen untersucht, verbessert und optimiert: Sechs Switcher pro Modul schalten die Pixelzeilen nacheinander ein (rolling-shutter Modus / zeilenweiser Auslesemodus), um die signalverstärkten

Drainströme der DEPFET-Pixel zu messen und die Pixelzelle zurückzusetzen. Insgesamt messen 1000 ADCs auf jedem Modul die Drainströme mit einer PXD-Auslesefrequenz von 50 kHz. Damit die Pixel korrekt angesteuert werden, wurden Steuerungssequenzen für die Switcher simuliert und auf den Prototyp-Modulen getestet. Die systemrelevanten Aspekte, wie die inter-ASIC Kommunikation, Kontrollsequenzen und Synchronisationsprobleme wurden eingehend untersucht und optimiert. Zusätzlich wurden Messungen mit radioaktiven Quellen und Lasern durchgeführt, um die optimalen Operationsspannungen für verschiedene Betriebsmodi zu bestimmen.
Der zeilenweise Auslesemodus von 20 µs erscheint problematisch, wenn ein kurzzeitiger, periodischer Untergrund auftritt, beispielsweise während der Aufstockungsinjektion der Teilchenpakete in SuperKEKB. Um dieses Problem zu lösen, wurde ein neuer Arbeitsmodus vorgeschlagen und untersucht, welcher einen "gated" Betriebsmodus des Detektors ermöglicht. Dies schaltet den Pixel-Vertex-Detektor für eine kurze Zeitspanne (1–2 µs) blind, während der hohe Untergrund erwartet wird. Ein Prototyp-Modul wurde im "Gated Mode" betrieben; Ursachen von auftretenden Problemen wurden ausfindig gemacht. Die daraus resultierenden Verbesserungen trugen dem finalen Modul-Layout bei. Außerdem wurden zwei verschiedene Arten von Prototyp-Modulen erfolgreich in einer Strahltest-Kampagne betrieben. Die Ladungs-Cluster-Verteilungen, Positionsauflösung und Effizienzen wurden studiert, wobei deutlich wird, dass sich die Sensoren gut für den Betrieb in Belle II eignen.

Abstract

The Belle detector was located at the electron-positron collider KEKB in Tsukuba, Japan. It operated from 1999 to 2010, running mostly at the $\Upsilon(4S)$ resonance, and achieved an integrated luminosity of $1041\,\mathrm{fb}^{-1}$. The main research topic was the $\mathcal{CP}$ violation in the B meson system. The measured results on B meson decays confirmed the theory of Kobayashi and Maskawa (Nobel Prize 2008) on the origin of $\mathcal{CP}$ violation within the Standard Model.
Since the Standard Model nevertheless leaves many open questions, the upgrade of KEKB to SuperKEKB has the potential to find New Physics beyond the Standard Model. SuperKEKB will increase the world-record instantaneous luminosity of KEKB by a factor of 40 to $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ using the nano-beam scheme. The physics goals are the precise measurement of $\mathcal{CP}$ violation, searching for rare or even "forbidden" decays of B mesons and finding small deviations from the Standard Model with larger statistics and more precise measurements than ever before.
To cope with the large luminosity of SuperKEKB various components of Belle need to be upgraded to the Belle II detector. Given the high luminosity, not only the number of events increases but also the background, in particular, the inevitable two-photon process. To minimize the extrapolation errors of the decay vertices of the B mesons the vertex detector should be situated as close as possible to the beam pipe. A silicon strip detector, as used in Belle, is not able to cope with the high background at SuperKEKB. Therefore, a novel pixel vertex detector (PXD) will be installed, featuring monolithic sensors using the DEPFET (DEPleted p-channel Field Effect Transistor) technology. The sensors can be thinned down to only 75 µm to minimize multiple scattering, offer high signal-to-noise ratio, provide high intrinsic position resolution of ~ 15 µm, support fast readout within 20 µs and have low power consumption. The PXD consists of 40 sensors, each equipped with 14 custom-made ASICs for control and readout, which are mounted in two layers around the beam pipe.
This thesis focuses on the characterization and optimization of the first full-size prototypes of the final sensor modules for the PXD. The combined control and readout electronics was investigated, improved and optimized on prototype modules equipped with the complete set of ASICs: six Switchers per module enable the pixel rows subsequently (rolling shutter mode) to measure the signal-amplified Drain currents from the DEPFETs and reset the device. A total of 1000 ADCs on each module sample the Drain currents resulting in a readout frequency of 50 kHz for the PXD. Switcher control sequences were simulated and applied for the prototypes to control the pixels properly. The system-related aspects like the inter-ASIC communication, control sequences and synchronization issues were studied and optimized. Measurements with radioactive sources and lasers were performed to determine optimal voltages for the different operation modes.
The rolling shutter readout mode is problematic when transient intermittent high

background is present, for instance during the top-up injection of SuperKEKB. To address this issue a new readout mode is proposed and investigated, which allows a "gated" or shutter-controlled operation of the detector. This makes the detector blind for a certain time interval in which high background is expected. A prototype module was operated in the *Gated Mode*; causes of encountered problems were identified and improvements were proposed and applied to the module layout. Two different kinds of prototype modules were operated successfully in a beam test campaign. The cluster charge distributions, position resolutions and efficiencies were studied and prove that the sensor is well suited for the operation at Belle II.

Contents

Chapter 1

Introduction

> By convention ['nomos'] sweet is sweet, bitter is bitter, hot is hot, cold is cold, color is color; but in the truth there are only atoms and the void.
>
> *(Democritus 460 BC–360 BC [2])*

Joseph John Thomson discovered the *electron* in 1897, emerging from the atoms of the cathode material, by investigating the properties of the so-called cathode rays [3]. He proposed a model of the atom in which the entire mass and positive charge is distributed homogeneously inside the atom's volume. He compared electrons in the atom with raisins in a cake. Due to the mutual repulsion of the electrons, they would also be distributed homogeneously.
Around 1911, Ernest Rutherford performed experiments with Alpha particles (two-fold ionized Helium atoms) hitting a thin gold foil (about 1000 atomic layers thick) [4]. He observed that many Alpha particles passed the foil without deflection. Nevertheless, there were also a few particles which were deflected at larger angles; the angular distribution was compatible with scattering off of a point-like charge. In addition, he observed that the number of deflected particles increased with the thickness. He concluded that atoms consist of a small positive core and (compared to the core) huge (almost empty) shells where the electrons revolved to shield the positive nucleus. He proposed the name *proton* to refer to the core of the hydrogen atom. The protons were already indirectly discovered by Wilhelm Wien in 1898 [5, 6].
However, there were some inconsistencies regarding the assumption that the nucleus consists only of positive charges. For instance, the helium nucleus is four times heavier compared to the hydrogen nucleus. According to Rutherford's assumption, it should also have four-fold the charge, but it only has twice the charge of the hydrogen nucleus. This inconsistency was also observed for heavier nuclei. Moreover, isotopes were discovered, i.e., atoms of the same elements but different masses. Consequently, Rutherford assumed in 1920 that the nucleus has to consist not only of protons but also of so-called *neutrons* [7]. In 1932, his assistant, James Chadwick, shot Alpha particles at Beryllium, which emitted yet unknown neutral particles [8]. These particles hit a target of paraffin wax (which contains hydrogen), ejecting energetic protons. Those were detected in a gas-filled chamber by ionizing atoms. Chadwick calculated that the mass of the neutrons corresponds almost to the mass of the protons [9].

At the time, all matter consisted of these three *elementary* particles, namely protons, neutrons and electrons. Later, physicists discovered various other particles, such as mesons (π, K, etc.) and hyperon resonances (Δ, Λ, Σ etc.) in high energy scattering experiments. In 1964, Murray Gell-Mann and George Zweig proposed the theory of quarks (up, down and strange) to explain the *zoo* of the many particles [10, 11]. The deep inelastic scattering experiments, carried out in the years 1968–69 at SLAC, have revealed that the nucleon itself is composed of smaller constituents: the partons [12, 13]. Later, it turned out that the partons are the theoretically predicted quarks. In the following years, new quarks were predicted and experimentally found (charm, strange, top and bottom).
Furthermore, to these *strongly interacting* particles (the quarks), *weakly interacting* particles were found. These were two types of neutrinos and their charged partners, muon and tau, in addition to the electron and its associated neutrino.
The elementary particles are all summarized in the Standard Model of Particle Physics, which has been developed by collaborative effort, i.e., by experimental measurements and theoretical predictions. A quantum field theory describes the elementary particles and three fundamental interactions, namely the *strong*, the *weak* and the *electromagnetic interactions*. In spite of the tremendous success of the Standard Model, there are still unanswered questions. It neither explains the matter-dominated Universe nor the theory of gravitation. Besides, it does not incorporate *dark matter* nor the mysterious *dark energy*.
Sakharov stated that there are three necessary conditions for the evolution of a matter-dominated Universe [14]: the deviation from thermal equilibrium, the violation of baryon number and the violation of matter-antimatter symmetry (charge and charge-parity ($\mathcal{CP}$) symmetry). The violation of the $\mathcal{CP}$ symmetry, which was discovered in 1964 by Cronin and Fitch [15], could be integrated in the Standard Model by the *Cabibbo-Kobayashi-Maskawa (CKM)* formalism [16] in 1973. However, this formalism requires six quarks, while at that time only three quarks were known (up, down and strange). A fourth (charm) quark was already predicted in 1970 and found later in 1974 [17, 18], the bottom quark was discovered in 1977 [19] and the predicted top quark was discovered in 1995 [20]. The importance of studying the $\mathcal{CP}$ violation in the B meson sector was emphasized by many researchers [21, 22]. For that reason, two dedicated experiments were built: the BaBar experiment in the USA and the Belle experiment in Japan. The experimental foundation of $\mathcal{CP}$ violation in the B mesons was observed in 2001 at both experiments [23, 24]. Kobayashi and Maskawa were awarded the 2008 Nobel Prize in Physics for their correct theoretical model.
However, the $\mathcal{CP}$ violation included in the Standard Model by the CKM matrix is orders of magnitude too small to explain the matter-dominance in the Universe [25]. Consequently, there must be New Physics beyond the Standard Model which resolves the mystery of a matter-dominated Universe. It is believed that the New Physics is connected to new heavy particles with masses beyond the TeV scale.
To study New Physics beyond the Standard Model there are, in general, two approaches. One approach is the so-called *high energy frontier*, where new heavy particles could be detected directly at high center-of-mass energies ($\sim 14\,\text{TeV}$ as provided by the LHC at CERN). The other approach is the *intensity frontier*,

i.e., high luminosity in a high precision experiment, where small deviations from the Standard Model are measured with very high statistics and high precision. The SuperKEKB accelerator (upgrade of the KEKB accelerator) implements this intensity approach and offers an instantaneous luminosity of $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. Electrons and positrons collide at a center-of-mass energy of 10.58 GeV, the $\Upsilon(4S)$ resonance which decays dominantly into a B–$\overline{B}$ meson pair. The upgrade of the Belle detector to Belle II allows the full reconstruction of the decay products of the B mesons. Thus, one can also reconstruct missing energy and "invisible" decays. The Belle II experiment will provide precise reconstruction of the tracks and decay vertices. Therefore, the innermost detector will be as close as possible to the beam pipe around the interaction point to minimize the extrapolation errors on the B meson decay vertices. Consequently, it must withstand the increased background, mainly dominated by the two-photon process and the large radiation doses. Furthermore, it should be thin in order to minimize multiple scattering (which would harm precise reconstruction of the B meson vertices) of traversing particles, but at the same time it should detect the minimum ionizing particles. With the increased luminosity of SuperKEKB and the accompanied high background, the occupancy of a strip detector as used in Belle would be too large to resolve tracks of the particles. For those reasons, an additional two-layer pixel detector is installed close to the beam pipe. It incorporates roughly eight million active pixels in monolithic arrays, consisting of depleted p-channel field effect transistors (DEPFETs). The sensitive area is thinned to 75 µm and has a length of ≈ 90 mm parallel to the beam pipe (in the z-direction). Its pixel sizes between 50–85 µm offer a spatial resolution of ~ 14 µm. The entire pixel is read out in the rolling shutter mode within ~ 20 µs. The impact parameter resolution using the upgraded silicon vertex detector is improved by almost a factor of two [26].

This thesis focuses on the operation and characterization of the first prototype pixel sensors, which are equipped with all control and readout electronics. The functionality of the modules, the communication and synchronization between the 14 application-specific integrated circuits (ASICs) on the sensor, the controlling of the individual control and readout electronics, the proper data transmission up to the data acquisition system and the power supply distribution on the modules are studied. This requires the development of a large software framework to perform, record and analyze all characterization measurements of the complete system. Detailed measurements of the control and readout electronics are presented together with system-related aspects, which are crucial for a proper functionality of the entire detector system.
In addition to the laboratory analysis, the detector modules were operated successfully with the entire data acquisition chain foreseen for Belle II in a dedicated beam test campaign.

The structure of the thesis is summarized as follows:

Chapter 1 briefly discusses the physics goals at Belle II and introduces the pixel vertex detector. It motivates the studies which are presented in this thesis.

Chapter 2 introduces the physics at Belle II, in particular, the $\mathcal{CP}$ violation and the mathematical formalism. The task of the pixel detector and its contribution to the measurements of the charge parity violation are presented.

Chapter 3 covers the collider SuperKEKB. It describes the generation of the particles (electrons, positrons), the beam optic instruments (wiggler, focusing and bending magnets), the luminosity, the nano-beam scheme, the damping and storage rings, the injection scheme and its background. The operation schedule and its three phases ensuring a proper operation and stable environment for the Belle II experiment are covered. Furthermore, the sub-detector systems and their tasks are briefly described. The chapter closes with the interaction region, beam pipe and the surrounding vertex detector.

Chapter 4 starts with the requirements for the pixel vertex detector and lists the available technologies. The innermost detector consists of two layers of DEPFET pixel detector modules. Its concept, working principle and module layout are discussed. In addition to this, the control and readout electronics are introduced. Additionally, this chapter covers the data acquisition systems, the (intrinsic) noise sources contributing to the overall signal-to-noise ratio, the mechanical arrangement and the cooling concept.

Chapter 5 is dedicated to the first electrically functional modules of the full-size detector modules, which are fully equipped with all ASICs and passive components. They resemble the final module layout without DEPFETs pixels. They offer the possibility to practice the assembly of the various components, to operate the entire control and to study the readout electronics. Characterizations of the ASICs were performed and are presented. In addition to this, a small DEPFETs matrix was placed on top of the module and is operational. Dedicated measurements are shown.

Chapter 6 focuses on the full-size prototype sensors, which includes the DEPFET pixels with the final design layout. The fully working module is entirely characterized. Detailed measurements are presented. The parameters for the control and readout electronics were adjusted and the voltages for proper operation were optimized. Detailed investigations of the sensor and system response were performed. The prototypes were operated in different modes (as foreseen in the experiment), their (system) behaviors were thoroughly studied and improved.

Chapter 7 discusses the performance of two full-size prototype modules in an electron beam test campaign. The behavior of the sensors in terms of cluster charges, internal amplifications and efficiencies are summarized. The system integrity, the combination of the pixel detector (PXD) and silicon vertex detector (SVD) forming the vertex detector, was verified.

Chapter 8 summarizes the studies presented in this thesis and concludes their most important results. The system-related problems, results and an outlook are given.

Chapter 2

Physics at Belle II

2.1 Standard Model of Elementary Particle Physics

The Standard Model (SM) has been developed in the 20^{th} century by experimental measurements and theoretical predictions. It is a theory of the fundamental interactions (strong, weak and electromagnetic) of elementary particles (quarks and leptons). The forces between the elementary particles are mediated by the exchange of elementary field quanta (gluons, photons, the $W^{\pm}$ and Z^0 weak bosons and the Higgs particle). All elementary particles and field quanta of the SM are shown in Fig. 2.1.
The fundamental particles, i.e., particles that presumably do not consist of other particles, are called *elementary particles*. Particles can be further classified as either fermions or bosons. Fermions are particles with half-integer spin, e.g., the six quarks and the six leptons. Bosons are particles with integer spin ($S = 0, 1, 2$), e.g., the photon, the gluon and the weak bosons, $W^{\pm}$ and Z^0, and H.
All quarks and leptons are fermions with spin $S = \frac{1}{2}$. The quarks and leptons are divided into three generations. The up-type quarks (u, c, t) have an electric charge of $+\frac{2}{3}$ and the down-type quarks (d, s, b) have an electric charge of $-\frac{1}{3}$, in units of elementary charge. In addition, the quarks have a color charge (red, green or blue) and couple via the strong interaction. The electric charge of the three leptons (electron, muon and tauon) is -1, while the neutrinos are chargeless. All particles couple to the weak interaction, electrically charged particles couple in addition to the electromagnetic interaction.
In addition, a corresponding antiparticle exists for every quark and lepton, named antiquark and antilepton, respectively. The gauge bosons are introduced in the next section.

2.1.1 Interactions

The interaction between particles is described in the SM by the exchange of gauge bosons and its corresponding gauge theory, which is mathematically described by the product of the symmetry groups $\mathrm{SU(3)_C} \times \mathrm{SU(2)_L} \times \mathrm{U(1)_Y}$. The C in $\mathrm{SU}(3)_C$ denotes color and the L in $\mathrm{SU}(2)_L$ denotes to the interactions with left-handed states. Y in $\mathrm{U}(1)_Y$ denotes the hypercharge, which is given as:

$$Q = I_z + \frac{1}{2}Y$$

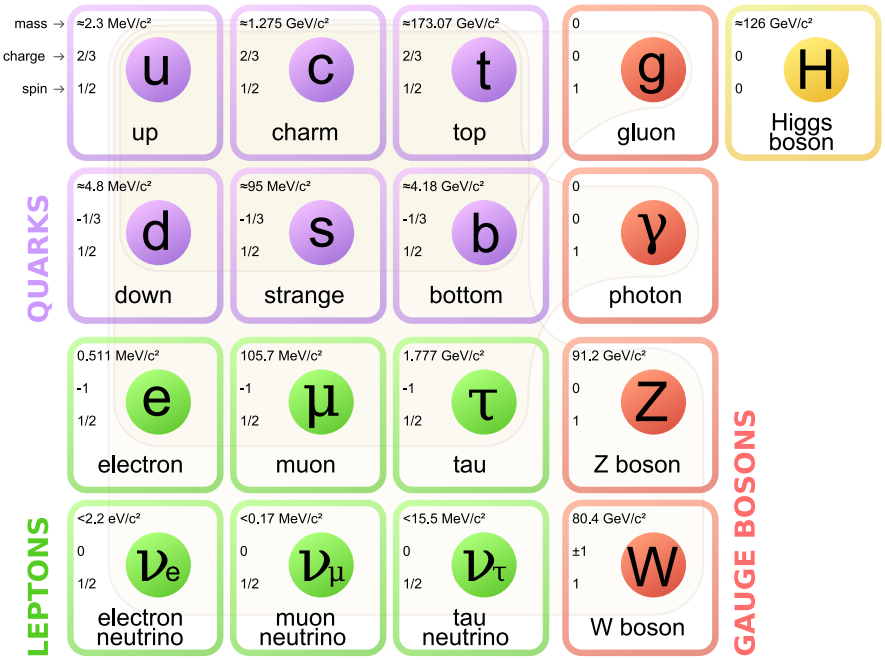


Figure 2.1: The Standard Model of elementary particles. It consists of three generations, six quarks, six leptons, four gauge bosons and the Higgs boson [27].

where Q is the electric charge of the particle and I_z denotes the z-component of the weak isospin.

The electroweak theory (EWT) unifies the weak and electromagnetic (EM) interactions and is described by the $\mathrm{SU(2)_L} \times \mathrm{U(1)_Y}$ symmetry group. The mediators of the weak interaction are the $W^{\pm}$ (for charged current interactions) and Z^0 (for neutral current interactions) gauge bosons in quantum flavordynamics (QFD).
The EM interaction is described by the quantum electrodynamics (QED). The mediator is the photon. The SU(2) group has three generators, therefore, three massless gauge bosons were expected. However, as was measured, the $W^{\pm}$ and Z^0 bosons do have mass [28] (see Fig. 2.1). Glashow, Weinberg and Salam published a series of papers in the 1960s using the concept of spontaneous symmetry breaking (SSB) of a local gauge invariant theory. Glashow et al. mathematically unified the electroweak and the electromagnetic theory with the $\mathrm{SU(2)_L} \times \mathrm{U(1)_Y}$ symmetry group. Thus, the properties of a full gauge invariant theory are conserved.
The strong interaction is described in quantum chromodynamics (QCD) using the $\mathrm{SU(3)_C}$ symmetry group, which has eight generators. The mediator of the strong interaction is the massless gluon, which couples to the quarks carrying color charge. The range of the interaction is directly connected to the mass of the exchanged bosons. Since the photon and graviton are massless, their range is infinite. In comparison, the Z^0 and $W^{\pm}$ ranges are limited in the order of 10^{-18} m to 10^{-15} m. The range of massive field quanta is described by the Yukawa potential

$$V_{\mathrm{Yukawa}}(r) \propto \frac{1}{r} e^{-mr} \tag{2.1.1}$$

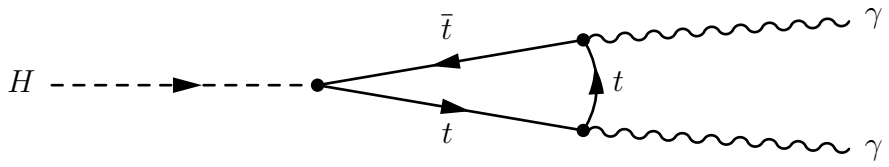


Figure 2.2: Feynman diagram of the decay of the Higgs boson to two photons with a fermion loop. The top quark provides the dominant contribution.

Table 2.1: Summary of the four interactions. The weak and electromagnetic theories are unified in the electroweak theory.

Interaction	**Strong**	**Weak**	**Electromagnetic**	**Gravity**
Theory	QCD	QFD	QED	GR
		EWT		
Mediator	gluon (g)	$W^{\pm}$, Z^0	photon (γ)	graviton (G)
Range [m]	10^{-15}	10^{-18}	∞	∞
Relative strength	1	10^{-5}	1/137	10^{-38}
Mass (GeV)	0	81.8, 92.6	0	0
Color charge	octet	none	none	none
Electric charge	0	± 1, 0	0	0

where m denotes the mass and r the distance to the exchanged quantum. Although gluons are massless, the range of the strong interaction amongst hadrons (see below) is limited to $\approx 10^{-15}$ m.

Higgs mechanism Peter Higgs introduced a scalar field [29], the *Higgs field*, ϕ, which preserves the gauge invariance and leads to a spontaneous symmetry breaking, allowing masses for the exchanged field quanta. Three of the four degrees of freedom (in the Higgs field) form the massive $W^{\pm}$ and Z^0 bosons. The remaining degree of freedom represents the Higgs boson and penetrates all space and interacts with quarks and leptons. The scalar particle boson, which was discovered in 2012 by ATLAS [30] and CMS [31], is presumably the long-sought Higgs boson. A Feynman diagram of a possible decay of the boson into two photons is shown in Fig. 2.2.

Gravity The Gravity is described in the general relativity (GR) by A. Einstein, which is not part of the SM. For the sake of completeness, the properties of the four interactions are summarized in Tab. 2.1 . GR is still a classical field theory, resisting the attempts to formulate it as a quantum theory.

2.1.2 Hadrons

In the physical world only bound systems of quarks, called hadrons, are observed. Hadrons are particles that are composed of either three quarks (baryons) or a

quark and an antiquark (mesons). They are bound together by the strong force. Most of the hadrons are very unstable with a lifetime of approximately 10^{-23} s [32], decaying by weak interaction, except the protons, which are stable (free neutrons have a lifetime of approximately 15 minutes).
The hadrons may be differentiated based upon the number of their (anti)quarks:

- **(Anti)Baryons** Baryons consist of three quarks. Each baryon has its corresponding antiparticle. Examples are nucleons, such as protons or neutrons. Protons consist of two up quarks and one down quark, while neutrons are composed of one up quark and two down quarks. Their corresponding antiparticles are the anti-protons and anti-neutrons. Furthermore, there are hyperons, i.e., particles which contain at least one strange quark, such as the Λ and Σ particles and any other combination of $q_i q_j q_k$ where i, j, k denote the five quarks (u, c, d, s, b). Hadrons containing top quarks do not exist, because the t quark decays before a hadron can be formed. All quarks can also be of the same type.

- **Mesons** Mesons are composed of one quark and one antiquark. Examples are the pions $\left(\pi^+(u\bar{d}),\ \pi^0(\frac{u\bar{u}-d\bar{d}}{\sqrt{2}}),\ \pi^-(d\bar{u})\right)$, kaons $\left(K^+(u\bar{s}),\ K^0(d\bar{s}),\ \overline{K}^0(s\bar{d}),\ K^-(s\bar{u})\right)$, D mesons $\left(D^+(c\bar{d}),\ D^0(c\bar{u}),\ \overline{D}^0(u\bar{c}),\ D^-(d\bar{c})\right)$ and B mesons $\left(B^+(u\bar{b}),\ B^0(d\bar{b}),\ \overline{B}^0(b\bar{d}),\ B^-(b\bar{u})\right)$.

2.2 Discrete Symmetries

Symmetries play an important role in physics. Conservation laws in classical physics (energy, momentum and angular momentum) correspond to symmetries for the equations of motion under canonical transformations (time, space translation and rotation). The physical laws do not change due to different time or spatial orientations. In 1918 Emmy Noether published her theorem stating that every continuous symmetry of a physical system is associated to a conservation law [33]. Important discrete symmetries in quantum mechanics are the charge conjugation $\mathcal{C}$, parity conjugation $\mathcal{P}$ and time conjugation $\mathcal{T}$.

2.2.1 Parity Conjugation

The parity conjugation mirrors the physical system in space at the origin. The parity operator, $\mathcal{P}$, acts on the spatial coordinates $\vec{r} = (x, y, z)$ but not on time.

$$\mathcal{P}\vec{r} \xrightarrow{\mathcal{P}} -\vec{r} \tag{2.2.1}$$

If the parity operator is applied twice on a wavefunction $\Psi(t, \vec{r})$, which describes the quantum state of a system, it coincides with its original state:

$$\mathcal{P}\mathcal{P}\,\Psi(\vec{r}, t) = \mathcal{P}\,\Psi(-\vec{r}, t) = \Psi(\vec{r}, t) \tag{2.2.2}$$

Thus, the equation $\mathcal{P}^2 = 1$ holds for the parity operator. Taking the normalization of the wavefunction into account, it follows that the $\mathcal{P}$ operator is unitary and hermitian.

The two vectors are differentiated as follows:

- *Axial vectors*, denoted by $\vec{a}$, are invariant under parity transformations. Examples are angular momentum ($\vec{L}$) and spin ($\vec{S}$).
- *Polar vectors*, denoted by $\vec{v}$, change their sign under parity conjugation. Polar vectors are, for instance, momentum ($\vec{p}$) or a space coordinate ($\vec{r}$).

Applying the parity operator $\mathcal{P}$ on both types of vectors results in:

$$\mathcal{P}\vec{a} = (+1)\vec{a} \qquad \mathcal{P}\vec{v} = (-1)\vec{v} \tag{2.2.3}$$

Axial vectors have a positive parity while the parity for polar vectors is negative. In addition to this, it is differentiated between pseudoscalars (p_s), i.e., the product of an axial vector and a polar vector ($p_s = \vec{v} \cdot \vec{a}$) and scalars ($s$), e.g., $s = \vec{v} \cdot \vec{v}$ or $s = \vec{a} \cdot \vec{a}$:

$$\mathcal{P}s = (+1)s \qquad \mathcal{P}p_s = (-1)p_s \tag{2.2.4}$$

In quantum mechanics, the wave function $\Psi(\vec{r})$ can be separated into radial, $R(r)$, and angular, $\mathrm{Y}_l^m(\Theta, \phi)$, components, satisfying the eigenvalue equation:

$$\mathcal{P}\,\Psi(\vec{r}) = \Psi(-\vec{r}) = \eta_{\mathcal{P}}\,\Psi(\vec{r}) \tag{2.2.5}$$

By definition, fermions have positive ($\eta_{\mathcal{P}} = 1$) intrinsic parity and their antiparticles have negative ($\eta_{\mathcal{P}} = -1$) intrinsic parity. Mesons, therefore, have an intrinsic parity of $\eta_{\mathcal{P}} = -1$. Applying the parity operator ($\mathcal{P}(\,\Psi(\vec{r})$) results in:

$$\begin{aligned} &\mathcal{P}R(r) = R(r) \\ &\mathcal{P}\mathrm{Y}_\mathrm{l}^\mathrm{m}(\theta, \psi) = \mathrm{Y}_\mathrm{l}^\mathrm{m}(\pi - \theta, \pi + \phi) = (-1)^\mathrm{l}\mathrm{Y}_\mathrm{l}^\mathrm{m}(\theta, \phi) \end{aligned} \tag{2.2.6}$$

A detailed mathematical derivation of eq. (2.2.6) is given in app. A.1.
For this reason, the parity eigenvalue $\eta_{\mathcal{P}}$ for a meson, consisting of a quark-antiquark bound state ($|q_i\overline{q}_j\rangle$) with an angular momentum $|\vec{L}|$, can be written as:

$$\mathcal{P}|q_i\overline{q}_j\rangle = \eta_{\mathcal{P}}|q_i\overline{q}_j\rangle \quad \Rightarrow \quad \eta_{\mathcal{P}} = \eta_q\eta_{\overline{q}}(-1)^L = (-1)^{L+1} \tag{2.2.7}$$

where η_q denotes the quark parity and $\eta_{\overline{q}}$ the antiquark parity.

2.2.2 Charge Conjugation

The charge conjugation transforms a particle $|k\rangle$ with charge q into its antiparticle $|\overline{k}\rangle$ of charge $-q$. The charge operator $\mathcal{C}$ acts on the charge of the particle but leaves the mass, momentum, $\vec{p}$, and spin, $\vec{S}$, invariant. It inverts the electric charge, baryon number, lepton number and flavor (such as topness, bottomness, charm and strangeness). The charge conjugation operator $\mathcal{C}$ is unitary, i.e., $\mathcal{C}\mathcal{C}^\dagger = \mathbb{1}$. Applying it twice results in the initial particle

$$\mathcal{C}^2|\vec{p}, \vec{S}, k\rangle = |\vec{p}, \vec{S}, k\rangle \tag{2.2.8}$$

Only particles that coincide with their antiparticles ($|k\rangle = |\overline{k}\rangle$) are eigenstates of the $\mathcal{C}$ operator. Examples are the photon (γ) or the neutral pion (π^0). The eigenvalues are $\eta_\mathcal{C} = \pm 1$. The photon is a self-conjugate, since the components of the magnetic field and the vector potential change their signs under charge conjugation. Therefore, the charge conjugation is negative ($\eta_\mathcal{C} = -1$). For a system of n photons the eigenvalue is calculated by:

$$\mathcal{C}|n\gamma\rangle = (-1)^n|n\gamma\rangle \tag{2.2.9}$$

For a neutral pion, the following equation holds:

$$\mathcal{C}|\pi^0\rangle = (+1)|\pi^0\rangle \tag{2.2.10}$$

For a neutral fermion-antifermion system, the charge parity is calculated by:

$$\mathcal{C}|f\overline{f}\rangle = \eta_\mathcal{C}|f\overline{f}\rangle \tag{2.2.11}$$

with $\eta_\mathcal{C} = (-1)^{L+S}$, where L denotes the orbital angular of the $f\overline{f}$ system momentum and S is the total spin.

2.2.3 Time Reversal

The time reversal reflects t into $-t$ ($\mathcal{T} : t \mapsto -t$). Where $\vec{p}$ is the momentum and $\vec{L}$ the angular momentum, the transformations result in:

$$\vec{p} \xrightarrow{\mathcal{T}} -\vec{p} \qquad \vec{L} \xrightarrow{\mathcal{T}} -\vec{L} \tag{2.2.12}$$

On a macroscopic scale, a system is not invariant under the time reversal transformation. The second law of thermodynamics, which states that the total entropy of an isolated system increases over time, does not lead to symmetry of a system under time reversal (for instance, the destruction of a vase). However, a microscopic system can be invariant under time reversal.

2.2.4 Charge-Parity Symmetry

The combined conjugation of charge and parity is called $\mathcal{CP}$ conjugation. Assuming a generic state $|k, \vec{p}, \vec{S}\rangle$, where k denotes the particle, $\vec{p}$ the momentum and $\vec{S}$ the spin and applying the $\mathcal{CP}$ operators yields:

$$\mathcal{CP}|\vec{p}, \vec{S}, k\rangle = \eta_{\mathcal{CP}}|-\vec{p}, \vec{S}, \overline{k}\rangle \tag{2.2.13}$$

Examples for $\mathcal{CP}$ eigenstates are:

$$\begin{aligned} \mathcal{CP}|\pi^0\pi^0\rangle = +1|\pi^0\pi^0\rangle \qquad & \mathcal{CP}|\pi^0\pi^0\pi^0\rangle = +1|\pi^0\pi^0\pi^0\rangle \\ |K_1\rangle = \frac{1}{\sqrt{2}}(|K^0\rangle - |\overline{K}^0\rangle) \Rightarrow \mathcal{CP}|K_1\rangle &= +1|K_1\rangle \\ |K_2\rangle = \frac{1}{\sqrt{2}}(|K^0\rangle + |\overline{K}^0\rangle) \Rightarrow \mathcal{CP}|K_2\rangle &= -1|K_2\rangle \end{aligned} \tag{2.2.14}$$

The parity and charge (if possible) quantum number are often denoted by $J^{\mathcal{PC}}$. For instance, for the neutral pion in the ground state ($L = 0$, $S = 0$, $\Rightarrow J = 0$) the values $\eta_{\mathcal{P}} = (-1)^{L+1} = -1$ and $\eta_{\mathcal{C}} = (-1)^{L+S} = +1$ are calculated, resulting in $J^{\mathcal{PC}} = 0^{-+}$.

2.2.5 $\mathcal{CPT}$ theorem

The combination of charge conjugation, parity conjugation and time reversal ($\mathcal{CPT}$) is conserved in any quantum field theory which is invariant under Lorentz transformation with a hermitian Hamiltonian[1] [35–37]. The $\mathcal{CPT}$ theorem has consequences such as the existence of antiparticles. Moreover, it states that the masses and the lifetimes of particles and their corresponding antiparticles are the same [38]. As a direct consequence, if $\mathcal{CPT}$ is violated, the Lorentz invariance would be also violated [39]. $\mathcal{T}$ violation is a direct consequence of the $\mathcal{CP}$ violation assuming the conservation of $\mathcal{CPT}$.

2.2.6 Symmetry experiments

Parity violating experiment Based on the theoretical argument by Lee and Yang [40] that parity might be violated ($\Theta - \tau$ *puzzle*), the Wu experiment in 1956 showed that parity is indeed violated [41]. The decay products of cobalt nuclei were studied in a magnetic field. The spins were pointing in the positive z-direction.

$$^{60}_{27}\mathrm{Co} \longrightarrow {}^{60}_{28}\mathrm{Ni}^{*} + e^{-} + \overline{\nu}_e + 2\gamma \tag{2.2.15}$$

The $^{60}_{27}$Co nucleus has the spin $S_z = +5$ in z-direction, the nucleus $^{60}_{28}\mathrm{Ni}^{*}$ has the spin $S_z = +4$ in the same direction. The electron and the antineutrino have the spin $S = +\frac{1}{2}$. The spins of the electron and the antineutrino point in the same direction due to the conservation of angular momentum. The external magnetic field determines the spin direction of the emitted electrons and neutrinos.

If parity were conserved, the probability of detecting electrons with positive and negative helicity would be the same. Wu observed the angular distribution of the electrons

$$W(\Theta) = 1 - \alpha\vec{p}\cos\Theta \qquad (\text{with } \alpha > 0.7) \tag{2.2.16}$$

where $\alpha \simeq v/c$, v is the velocity of the emitted electron, c is the speed of light and Θ is the angle between the emitted electron and the polarization vector ($\vec{p}$), i.e., the polarization axis of the cobalt nuclei (see Fig. 2.3).

$\mathcal{CP}$ violating experiment Cronin and Fitch discovered the $\mathcal{CP}$ violation in the neutral kaon system in 1964 [15]. It will be explained in more detail later when the mathematical formalism is introduced. (see Sect. 2.6).

[1] The $\mathcal{CPT}$ theorem can be extended to non-hermitian Hamiltonians and unstable states [34].

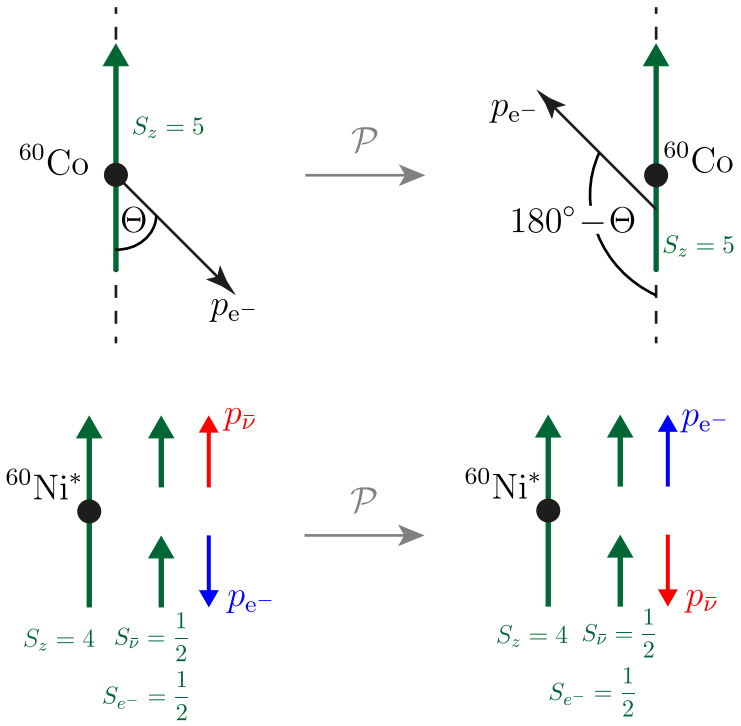


Figure 2.3: The ^{60}Co nucleus decays into ^{60}Ni* by emitting an antineutrino and an electron. Due to the conservation of angular momentum, the spin points into the positive z-direction. The scenario shown on the right has not been observed. However, a few events have been detected, since the polarization of the nuclei could not be achieved for all atoms.

2.3 Quark Mixing and $\mathcal{CP}$ violation

When Cabibbo published his paper on "Unitary Symmetry and Leptonic Decays" in 1963 [42], only three quarks were known, i.e., the up, down and strange quarks. The doublet scheme of the quarks, as it is known today, was not established yet. According to the "strange" behavior in the decays of $\pi^+ \to \mu^+\nu_\mu$ and $K^+ \to \mu^+\nu_\mu$, a "weaker" transition from $s \to u$ relative to $d \to u$ was proposed to explain the relative lifetimes of π^+ and K^+ (the K^+ lived "too long," therefore, called "strange"). Cabibbo introduced a theory about the flavor transitions by defining the mixing angle, the *Cabibbo angle* ($\Theta_c = 13.04 \pm 0.05\,°$), resulting in a $SU(2)$ doublet:

$$\begin{pmatrix} u \\ d' \end{pmatrix} = \begin{pmatrix} u \\ d\cos\Theta_c + s\sin\Theta_c \end{pmatrix} \tag{2.3.1}$$

Feynman diagrams showing the transitions from the d and s to the u quark, including the Cabibbo angle, Θ_c, are shown in Fig. 2.4.

There was, however, still another theoretical mystery with the strange K mesons. According to the theoretical model introduced above, a transition from an s quark to a d quark by a virtual Z^0 should be allowed. The decays $K \to \mu^+\mu^-$ should be approximately the same as $K^+ \to \mu^+\nu_\mu$. However, as it turned out experimentally,

(a) The down quark has a coupling to the up quark by the W^- boson corresponding to $\cos\Theta_c$.

(b) The strange quark has a coupling to the up quark by the W^- boson corresponding to $\sin\Theta_c$.

Figure 2.4: Feynman diagrams showing the transition from an (up-) down-type quark to a (down-) up-type quark by a $W^\pm$ boson.

the branching ratio is [32]:

$$\frac{\Gamma(K^0 \to \mu^-\mu^+)}{\Gamma(K^+ \to \mu^-\nu_\mu)} \approx 10^{-8} \tag{2.3.2}$$

Glashow, Iliopoulos and Maiani postulated the charm quark to explain the highly suppressed flavor-changing neutral current (FCNC) decay of $K^0 \to \mu^-\mu^+$ [17]. This forms a second doublet:

$$\begin{pmatrix} c \\ s' \end{pmatrix} = \begin{pmatrix} c \\ s\cos\Theta_c - d\sin\Theta_c \end{pmatrix} \tag{2.3.3}$$

The second term in eq. (2.3.3) also has a mixing term as eq. (2.3.1). The transitions between the quark flavors could be mathematically described by a 2×2 matrix. The flavor eigenstates are expressed as a linear combination of the mass eigenstates. The theoretical predicted charm quark was found experimentally in 1974 [18, 43].

$$\begin{pmatrix} d' \\ s' \end{pmatrix} = V \begin{pmatrix} d \\ s \end{pmatrix} \quad \text{with} \quad V = \begin{pmatrix} V_{ud} & V_{us} \\ V_{cd} & V_{cs} \end{pmatrix} = \begin{pmatrix} \cos\Theta_c & \sin\Theta_c \\ -\sin\Theta_c & \cos\Theta_c \end{pmatrix} \tag{2.3.4}$$

In 1973, the matrix was extended by Kobayashi and Maskawa [16], known as the CKM matrix, in order to describe mathematically the $\mathcal{CP}$ violation within the SM. This matrix is expressed as:

$$\underbrace{\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix}}_{\text{flavor eigenstates}} = \underbrace{\begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix}}_{\text{CKM matrix}} \underbrace{\begin{pmatrix} d \\ s \\ b \end{pmatrix}}_{\text{mass eigenstates}} \tag{2.3.5}$$

Kobayashi and Maskawa introduced a third generation of quarks (bottom and top), which were discovered in 1977 [19] and 1994 [20], respectively. A sketch of the flavor transition from the u quark to the d' quark as superposition of three mass eigenstates with Feynman diagrams is shown in Fig. 2.5. The CKM matrix is a complex 3×3 matrix that nominally has 18 free parameters. The unitarity condition reduces them to nine degrees of freedom, three angles and six phases.

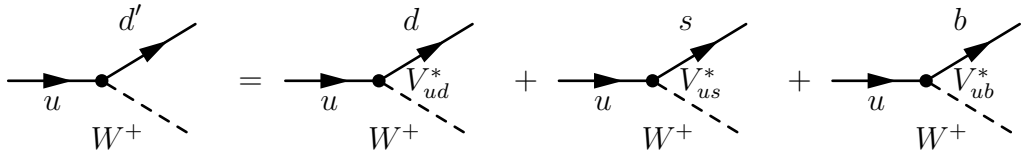


Figure 2.5: Feynman diagrams of the flavor transition of the u quark to the d, s and b quarks. The quark flavor eigenstate d' is the superposition of quark mass eigenstates d, s and b.

These are further reduced to four parameters, three angles and only one complex phase. A detailed mathematical description of reducing the 18 free parameters to four is given in app. A.2. The other five phases are absorbed in the (free selection of the phases of the) quark fields.

The CKM matrix has four free parameters: three rotations in orthogonal planes and one complex phase. Thus, the matrix can be re-written as the product of three rotation matrices, where c_{ij}, s_{ij} denote the cosine and sine of the corresponding angles:

$$\begin{aligned} V_{\text{CKM}} &= R_{23}R_{13}R_{12} \\ &= \begin{pmatrix} 1 & 0 & 0 \\ 0 & c_{23} & s_{23} \\ 0 & -s_{23} & c_{23} \end{pmatrix} \begin{pmatrix} c_{13} & 0 & s_{13}\mathrm{e}^{-\mathrm{i}\delta} \\ 0 & 1 & 0 \\ -s_{13}\mathrm{e}^{\mathrm{i}\delta} & 0 & c_{13} \end{pmatrix} \begin{pmatrix} c_{12} & s_{12} & 0 \\ -s_{12} & c_{12} & 0 \\ 0 & 0 & 1 \end{pmatrix} \\ &= \begin{pmatrix} c_{13} & 0 & s_{13}\mathrm{e}^{-\mathrm{i}\delta} \\ -s_{23}s_{13}\mathrm{e}^{-\mathrm{i}\delta} & c_{23} & s_{23}c_{13} \\ -s_{13}c_{23}\mathrm{e}^{\mathrm{i}\delta} & s_{23} & c_{23}c_{13} \end{pmatrix} \begin{pmatrix} c_{12} & s_{12} & 0 \\ -s_{12} & c_{12} & 0 \\ 0 & 0 & 1 \end{pmatrix} \\ &= \begin{pmatrix} c_{13}c_{12} & c_{13}s_{12} & s_{13}\mathrm{e}^{-\mathrm{i}\delta} \\ -c_{12}s_{23}s_{13}\mathrm{e}^{-\mathrm{i}\delta} - s_{12}c_{23} & -s_{12}s_{13}s_{23}\mathrm{e}^{-\mathrm{i}\delta} + c_{12}c_{23} & s_{23}c_{13} \\ -c_{12}s_{13}c_{23}\mathrm{e}^{\mathrm{i}\delta} + s_{12}s_{23} & -s_{13}s_{12}c_{23}\mathrm{e}^{\mathrm{i}\delta} - s_{23}c_{12} & c_{23}c_{13} \end{pmatrix} \end{aligned}$$

Only if the complex phase $\delta \neq 0$, the $\mathcal{CP}$ violation (see Sect. 2.7) is manifest in the quark transition.

2.3.1 Wolfenstein parametrization

Wolfenstein introduced a parametrization given as [44]:

$$\begin{aligned} &\lambda = s_{12} \equiv \sin\Theta_{\text{c}}, \quad A = \frac{s_{23}}{s_{12}^2}, \quad \rho = \frac{s_{13}}{s_{12}s_{23}}\cos\delta, \quad \eta = \frac{s_{13}}{s_{12}s_{23}}\sin\delta \\ \Rightarrow &s_{12} = \lambda, \quad s_{23} = A\lambda^2, \quad s_{13}\mathrm{e}^{-\mathrm{i}\delta} = A\lambda^3(\rho - \mathrm{i}\eta) \end{aligned} \tag{2.3.6}$$

where η incorporates the $\mathcal{CP}$ violating phase. The sine of the Cabibbo angle is $\lambda = \sin\Theta_{\text{c}} \approx 0.23$. The CKM matrix is written in this parametrization as:

$$V_{\text{CKM}} = \begin{pmatrix} 1-\frac{\lambda^2}{2} & \lambda & A\lambda^3(\rho-\mathrm{i}\eta) \\ -\lambda & 1-\frac{\lambda^2}{2} & A\lambda^2 \\ A\lambda^3(1-\rho-\mathrm{i}\eta) & -A\lambda^2 & 1 \end{pmatrix} + \mathcal{O}(\lambda^4) \tag{2.3.7}$$

Due to the smallness of the Cabibbo angle λ, the diagonal elements are very close to unity. The off-diagonal elements are smaller $\big(\mathcal{O}(\lambda),\ \mathcal{O}(\lambda^2)\big)$, whereas the transitions across two generations are almost zero $\big(\mathcal{O}(\lambda^3)\big)$. The other three coefficients A, ρ and η are $\mathcal{O}(1)$. Defining the parameters $\overline{\rho}$ and $\overline{\eta}$, where $\mathcal{O}(\lambda^4)$ is included in the parametrization, as

$$\overline{\rho} = \rho\Big(1-\frac{\lambda^2}{2}\Big) \qquad \overline{\eta} = \eta\Big(1-\frac{\lambda^2}{2}\Big) \tag{2.3.8}$$

yields the relations:

$$\overline{\rho} + \mathrm{i}\overline{\eta} = -\frac{V_{ud}V_{ub}^*}{V_{cd}V_{cb}^*} \tag{2.3.9}$$

2.3.2 Unitary Triangle

Applying the unitarity condition to the CKM matrix yields six independent equations each:

$$\begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \begin{pmatrix} V_{ud}^* & V_{cd}^* & V_{td}^* \\ V_{us}^* & V_{cs}^* & V_{ts}^* \\ V_{ub}^* & V_{cb}^* & V_{tb}^* \end{pmatrix} = \delta_{ij} \qquad \begin{pmatrix} V_{ud}^* & V_{cd}^* & V_{td}^* \\ V_{us}^* & V_{cs}^* & V_{ts}^* \\ V_{ub}^* & V_{cb}^* & V_{tb}^* \end{pmatrix} \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} = \delta_{ij}$$

$$\begin{array}{rcl}
\Rightarrow & V_{ud}V_{cd}^* + V_{us}V_{cs}^* + V_{ub}V_{cb}^* = 0 & \Rightarrow \quad V_{ud}^*V_{us} + V_{cd}^*V_{cs} + V_{td}^*V_{ts} = 0 \\
\Rightarrow & V_{ud}V_{td}^* + V_{us}V_{ts}^* + V_{ub}V_{tb}^* = 0 & \Rightarrow \quad V_{ud}^*V_{ub} + V_{cd}^*V_{cb} + V_{td}^*V_{tb} = 0 \\
\Rightarrow & V_{cd}V_{ud}^* + V_{cs}V_{us}^* + V_{cb}V_{ub}^* = 0 & \Rightarrow \quad V_{us}^*V_{ud} + V_{cs}^*V_{cd} + V_{ts}^*V_{td} = 0 \\
\Rightarrow & V_{cd}V_{td}^* + V_{cs}V_{ts}^* + V_{cb}V_{tb}^* = 0 & \Rightarrow \quad V_{us}^*V_{ub} + V_{cs}^*V_{cb} + V_{ts}^*V_{tb} = 0 \\
\Rightarrow & V_{td}V_{ud}^* + V_{ts}V_{us}^* + V_{tb}V_{ub}^* = 0 & \Rightarrow \quad V_{ub}^*V_{ud} + V_{cb}^*V_{cd} + V_{tb}^*V_{td} = 0 \\
\Rightarrow & V_{td}V_{cd}^* + V_{ts}V_{cs}^* + V_{tb}V_{cb}^* = 0 & \Rightarrow \quad V_{ub}^*V_{us} + V_{cb}^*V_{cs} + V_{tb}^*V_{ts} = 0
\end{array}$$

These equations represent closed triangles in the complex plane. Their areas are all the same, given as $A_{\text{triangle}} = \frac{1}{2}J \approx A^2\lambda^6\eta$, where J denotes the *Jarlskog* parameter [45]. The angles and lengths of the triangles are determined from measurements of proper decays, which is discussed in more detail in Sect. 2.11. In the following section, it will be shown that the $\mathcal{CP}$ violation in the neutral B meson system is large compared to other neutral meson systems. This is due to the non-degenerate unitary triangle, i.e., the large angles (none of the angles is small). The neutral B^0 ($\overline{B}^0$) consists of a d ($\overline{d}$) and $\overline{b}$ (b) quark, i.e., it is a $d-b$ system. Choosing the appropriate equation (and performing the complex conjugation) yields:

$$\begin{array}{ccccccc} V_{ud}V_{ub}^* & + & V_{cd}V_{cb}^* & + & V_{td}V_{tb}^* & = 0, \\ \mathcal{O}(\lambda^3) & + & \mathcal{O}(\lambda^3) & + & \mathcal{O}(\lambda^3) & & \end{array} \tag{2.3.10}$$

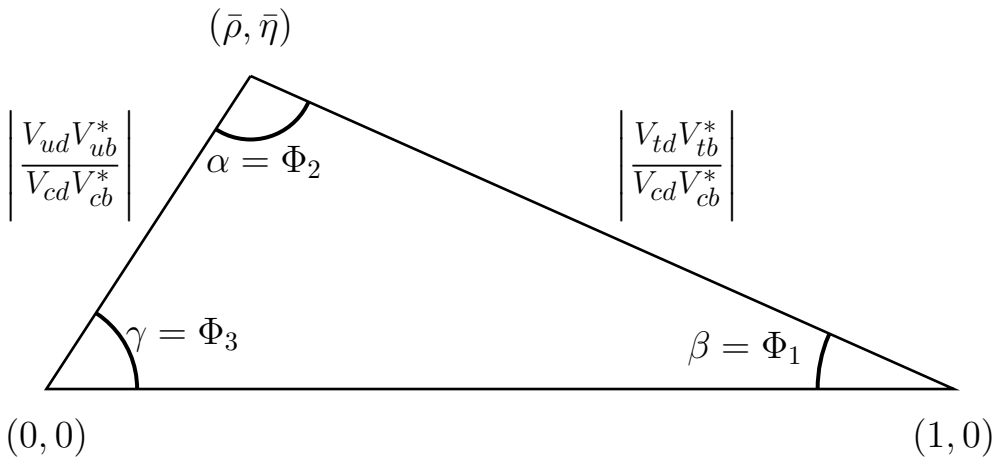


Figure 2.6: Unitarity triangle of eq. (2.3.10) of the b quark transition. The first row and the third column are divided by $V_{cd}V_{cb}^*$. All sides of the triangles are of $\mathcal{O}(1)$.

All terms have the same the equal powers of λ. Dividing it by $V_{cd}V_{cb}^*$ results in:

$$\underbrace{\frac{V_{ud}V_{ub}^*}{V_{cd}V_{cb}^*}}_{-(\bar{\rho}+\mathrm{i}\bar{\eta})} + 1 + \frac{V_{td}V_{tb}^*}{V_{cd}V_{cb}^*} = 0. \tag{2.3.11}$$

This equation is sketched in the complex plane in Fig. 2.6.

The angles are given as[2]:

$$\beta = \arg\left(-\frac{V_{cd}V_{cb}^*}{V_{cd}V_{cb}^*}\right), \quad \alpha = \arg\left(-\frac{V_{td}V_{tb}^*}{V_{ud}V_{ub}^*}\right), \quad \gamma = \arg\left(-\frac{V_{ud}V_{ub}^*}{V_{cd}V_{cb}^*}\right), \tag{2.3.12}$$

They are obtained from $\mathcal{CP}$ asymmetry measurements in proper chosen decay channels of the B meson. Since the triangle is normalized to unity in the real axis, it is only necessary to measure two quantities to determine the triangle. Measuring both sides and the three angles results in an over constrained test of the SM. If the triangle were not closed in the complex plane, it would give a hint to physics beyond the SM. One example is that there could be even more than three quark generations.

Another triangle is obtained for the $|B_s^0\rangle = |s\bar{b}\rangle$, $|\overline{B}_s^0\rangle = |\bar{s}b\rangle$ system.

$$\begin{array}{ccccccc} V_{us}V_{ub}^* & + & V_{cs}V_{cb}^* & + & V_{ts}V_{tb}^* & = 0. \\ \mathcal{O}(\lambda^4) & + & \mathcal{O}(\lambda^2) & + & \mathcal{O}(\lambda^2) & \end{array} \tag{2.3.13}$$

[2]Kobayashi and Maskawa introduced the original notation Φ_1, Φ_2, Φ_3, which is followed by the Belle II experiment. Now, the angles are also commonly named β, α, γ, as in BaBar and LHCb.

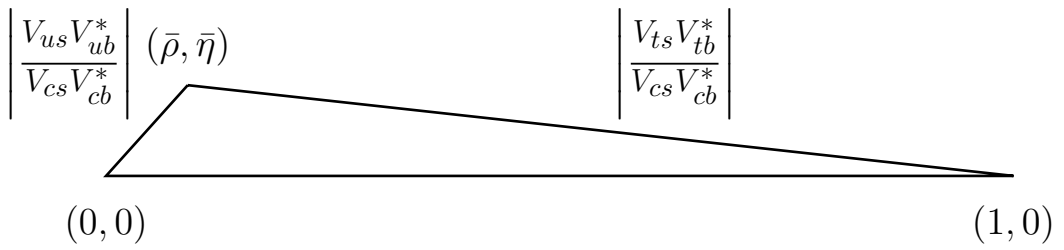


Figure 2.7: Unitarity triangle of eq. (2.3.13). The first row and the third column are divided by $V_{cs}V_{cb}^*$: One side of the triangle has a different power of λ compared to the other two.

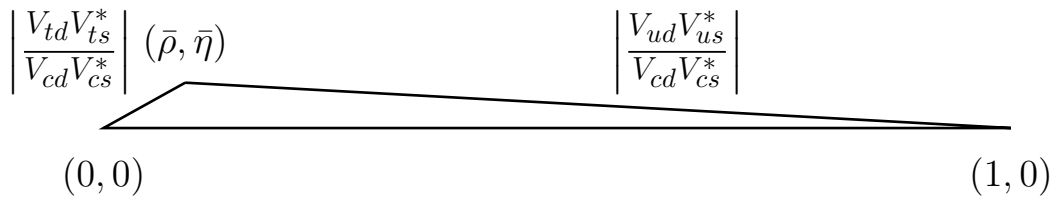


Figure 2.8: Unitarity triangle of eq. (2.3.15). The first row and the third column are divided by $V_{cd}V_{cs}^*$: One side of the triangle has a different power of λ compared to the other two.

Dividing eq. (2.3.13) by $V_{cs}V_{cb}^*$ yields:

$$\frac{V_{us}V_{ub}^*}{V_{cs}V_{cb}^*} + 1 + \frac{V_{ts}V_{tb}^*}{V_{cs}V_{cb}^*} = 0 \tag{2.3.14}$$

The corresponding unitarity triangle is shown in Fig. 2.7.
Choosing the neutral kaon system ($|K^0\rangle = |d\bar{s}\rangle$, $|\overline{K}^0\rangle = |\bar{d}s\rangle$), i.e., the $d-s$ system the equation of the unitary triangle is given as:

$$\begin{array}{ccccccc} V_{ud}V_{us}^* & + & V_{cd}V_{cs}^* & + & V_{td}V_{ts}^* & = 0. \\ \mathcal{O}(\lambda) & + & \mathcal{O}(\lambda) & + & \mathcal{O}(\lambda^5) & \end{array} \tag{2.3.15}$$

Dividing eq. (2.3.15) by $V_{cd}V_{cs}^*$ results in:

$$\frac{V_{ud}V_{us}^*}{V_{cd}V_{cs}^*} + 1 + \frac{V_{td}V_{ts}^*}{V_{cd}V_{cs}^*} = 0 \tag{2.3.16}$$

The equation is shown in Fig. 2.8. The different powers of λ ($\mathcal{O}(\lambda)$ and $\mathcal{O}(\lambda^5)$) degenerate the triangle. Thus, the $\mathcal{CP}$ violation is small since the angles are small. The $\mathcal{CP}$ violation in the neutral kaon system is very small and difficult to measure. Since the parameters of the CKM matrix cannot be theoretically calculated they are determined by measurements. The magnitudes of the matrix elements are [32]:

$$\begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} = \begin{pmatrix} 0.97425 \pm 0.00022 & 0.2253 \pm 0.0008 & (4.13 \pm 0.49) \cdot 10^{-3} \\ 0.225 \pm 0.008 & 0.986 \pm 0.016 & (41.1 \pm 1.3) \cdot 10^{-3} \\ (8.4 \pm 0.6) \cdot 10^{-3} & (40.0 \pm 2.7) \cdot 10^{-3} & 1.021 \pm 0.032 \end{pmatrix}$$

2.4 Neutral meson mixing

In the following section, the particle X^0 denotes one of the neutral mesons K^0, B^0, B_s^0, D^0. It is a pseudoscalar, i.e., $J^P = 0^-$ (see Sect. 2.2.1), where $J = L + S$ denotes the sum of the angular momentum and the spin. The mesons consist of two quarks $|q_i\overline{q}_j\rangle$. As already stated previously, the parity and charge conjugation operators result in

$$\mathcal{P}|q_i\overline{q}_j\rangle = (-1)^{L+1}|q_i\overline{q}_j\rangle \qquad \mathcal{C}|q_i\overline{q}_j\rangle = (-1)^{L+S}|q_i\overline{q}_j\rangle,$$

where L denotes the orbital momentum and S the total spin.
The states $|X^0\rangle$ and $|\overline{X}^0\rangle$ are called *flavor eigenstates*. X^0 denotes a neutral meson, $\overline{X}^0$ is its antiparticle. The charge and parity symmetries of the this system are studied by applying the operators, introduced in Sect. 2.2:

$$\mathcal{P}|X^0\rangle = -|X^0\rangle \qquad \mathcal{P}|\overline{X}^0\rangle = -|\overline{X}^0\rangle \tag{2.4.1}$$

$$\mathcal{C}|X^0\rangle = |\overline{X}^0\rangle \qquad \mathcal{C}|\overline{X}^0\rangle = |X^0\rangle \tag{2.4.2}$$

$$\mathcal{CP}|X^0\rangle = -|\overline{X}^0\rangle \qquad \mathcal{CP}|\overline{X}^0\rangle = -|X^0\rangle \tag{2.4.3}$$

The weak interaction does not conserve the flavor of the particles. Oscillations of the neutral meson to its corresponding antiparticle can occur, i.e., $|X^0\rangle \leftrightarrow |\overline{X}^0\rangle$ transitions. These are second order processes, i.e., the quantum number changes $\Delta F = 2$. The Feynman diagrams (box diagrams) for the oscillations in neutral B mesons, neutral kaons and neutral D mesons are shown in Figs. 2.9 to 2.12.

The mass eigenstates are different than the flavor eigenstates. Thus, the Hamiltonian can be split into a flavor invariant strong Hamiltonian, $\mathcal{H}_\mathrm{s}$, with the eigenstates $|X^0\rangle$ and $|\overline{X}^0\rangle$, and a non-flavor invariant electroweak Hamiltonian $\mathcal{H}_\text{el-weak} = \mathcal{H}_\mathrm{EM} + \mathcal{H}_\mathrm{weak}$ with a mixing of the flavor eigenstates $\{|X^0\rangle, |\overline{X}^0\rangle\}$[3].
A general state $|\psi(t)\rangle$ is assumed, which is a superposition of $|X^0\rangle$ and $|\overline{X}^0\rangle$. The decays of the initial mesons with any number of particles $\psi_n|n\rangle$ are neglected. The time evolution of the system is given by the linear combination of the eigenstates of the strong interaction Hamiltonian, $\mathcal{H}_\mathrm{s}$:

$$|\psi(t)\rangle = \psi_1(t)|X^0\rangle + \psi_2(t)|\overline{X}^0\rangle \tag{2.4.4}$$

where $\mathcal{H}_\mathrm{s}|X^0\rangle = m|X^0\rangle$ and $\mathcal{H}_\mathrm{s}|\overline{X}^0\rangle = m|\overline{X}^0\rangle$ and m denotes the mass.
The effective 2×2 Hamiltonian $\boldsymbol{\mathcal{H}}_\text{eff}$ which governs the time evolution is the sum of the strong, electromagnetic and weak interaction Hamiltonians, i.e.,

$$\boldsymbol{\mathcal{H}}_\text{eff} = \boldsymbol{\mathcal{H}}_\mathrm{s} + \boldsymbol{\mathcal{H}}_\mathrm{EM} + \boldsymbol{\mathcal{H}}_\mathrm{weak} = \boldsymbol{M} - \frac{\mathrm{i}}{2}\boldsymbol{\Gamma}, \tag{2.4.5}$$

[3] If the $\mathcal{CP}$ symmetry were not violated for the weak Hamiltonian, the mass eigenstates would be the $\mathcal{CP}$ eigenstates. Applying the $\mathcal{CP}$ operators they would transform into their own states with the $\mathcal{CP}$ eigenvalues ± 1.

where $\boldsymbol{M} \in \mathbb{R}^{2\times2}$ denotes the mass matrix and $\frac{\mathrm{i}}{2}\boldsymbol{\Gamma} \in \mathbb{C}^{2\times2}$, $\boldsymbol{\Gamma}$ is the decay matrix. The mass and decay matrices are Hermitian:

$$\boldsymbol{M} = \frac{1}{2}(\boldsymbol{\mathcal{H}}_{\text{eff}} + \boldsymbol{\mathcal{H}}_{\text{eff}}^{\dagger}) = \boldsymbol{M}^{\dagger} \qquad \boldsymbol{\Gamma} = (\boldsymbol{\mathcal{H}}_{\text{eff}} - \boldsymbol{\mathcal{H}}_{\text{eff}}^{\dagger})\mathrm{i} = \boldsymbol{\Gamma}^{\dagger} \tag{2.4.6}$$

The Hamiltonian $\mathcal{H}_{\text{eff}}$ is not Hermitian (due to the imaginary component). Furthermore, it neglects the final states and does not conserve probability (otherwise the mesons would only oscillate but never decay). Rewriting eq. (2.4.5) yields:

$$\boldsymbol{\mathcal{H}} = \boldsymbol{M} - \frac{\mathrm{i}}{2}\boldsymbol{\Gamma} = \begin{pmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{pmatrix} - \frac{\mathrm{i}}{2}\begin{pmatrix} \Gamma_{11} & \Gamma_{12} \\ \Gamma_{21} & \Gamma_{22} \end{pmatrix} = \begin{pmatrix} M_{11} & M_{12} \\ M_{12}^{*} & M_{22} \end{pmatrix} - \frac{\mathrm{i}}{2}\begin{pmatrix} \Gamma_{11} & \Gamma_{12} \\ \Gamma_{12}^{*} & \Gamma_{22} \end{pmatrix} \tag{2.4.7}$$

where the diagonal elements $H_{ii} \in \{M_{ii}, \Gamma_{ii}\}$ are flavor-conserving transitions, and the off-diagonal elements $M_{ij}, \Gamma_{ij},\ i \neq j$ represent the flavor-changing transitions.

Using the $\mathcal{CPT}$ invariance, it can be derived for the diagonal elements that the masses and lifetimes of the antiparticle and particle are identical:

$$M = M_{11} = M_{22}, \quad \Gamma = \Gamma_{11} = \Gamma_{22} \quad \Rightarrow \quad \mathcal{H} = \mathcal{H}_{11} = \mathcal{H}_{22} \tag{2.4.8}$$

If $\mathcal{CP}$ or $\mathcal{T}$ is conserved, it holds for the off-diagonal elements element-wise, i.e., for the real and imaginary components separately:

$$\mathcal{H}_{21}^{*} = M_{12}^{*} - \frac{\mathrm{i}}{2}\Gamma_{12}^{*} \tag{2.4.9}$$

This is valid, since the imaginary components of the diagonal elements of the mass and decay matrices vanish. Calculating the eigenvalues and eigenvectors yields[4]:

$$\lambda_{1,2} = \mathcal{H} \pm \sqrt{\mathcal{H}_{12}\mathcal{H}_{21}} = M - \frac{\mathrm{i}}{2}\Gamma \pm \sqrt{(M_{12} - \frac{\mathrm{i}}{2}\Gamma_{12})(M_{12}^{*} - \frac{\mathrm{i}}{2}\Gamma_{12}^{*})} \tag{2.4.10}$$

Literature often defines the ratio[5]:

$$\frac{q}{p} = \sqrt{\frac{\mathcal{H}_{21}}{\mathcal{H}_{12}}} = \sqrt{\frac{M_{12}^{*} - \frac{i}{2}\Gamma_{12}^{*}}{M_{12} - \frac{i}{2}\Gamma_{12}}} \neq \sqrt{\frac{\mathcal{H}_{12}^{*}}{\mathcal{H}_{12}}} \tag{2.4.11}$$

Furthermore, the normalization is given as:

$$p^2 + q^2 = 1 \tag{2.4.12}$$

If $\mathcal{CP}$ is conserved, then M_{12} and Γ_{12} are real and the relation $p = 1 = q$ is valid. In contrast, if $\mathcal{CP}$ is violated, the ratio $\frac{q}{p} \simeq e^{\mathrm{i}\delta}$ holds, where δ denotes the complex phase.

[4]The detailed calculation can be found in app. A.3.1.

[5]The inequality is given by the fact that $\mathcal{H}_{21}{*} = \left(M_{21} - \frac{\mathrm{i}}{2}\Gamma\right)^{*} = M_{21}^{*} + \frac{\mathrm{i}}{2}\Gamma^{*} \neq M_{21}^{*} - \frac{\mathrm{i}}{2}\Gamma^{*}$.

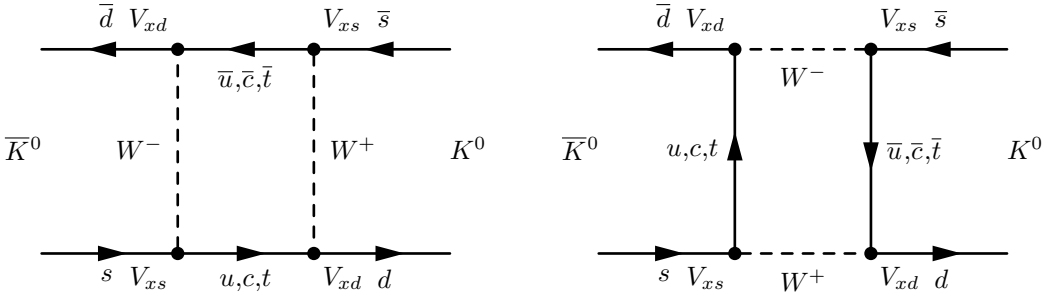


Figure 2.9: Leading Feynman diagrams contributing to the K^0 oscillations with the CKM matrix elements V_{xd}, V_{xs} where $x = u, c, t$.

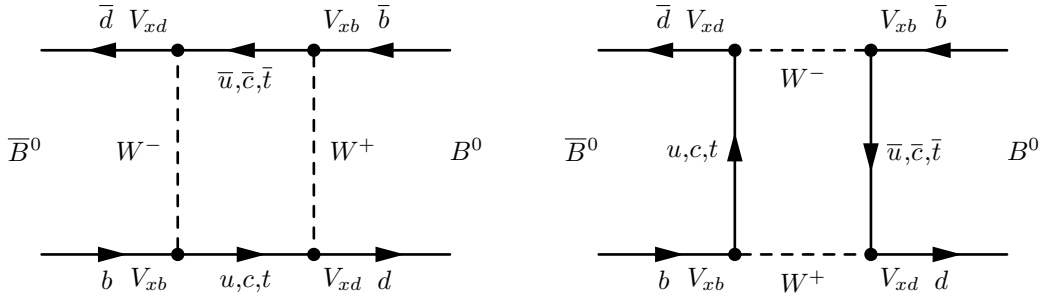


Figure 2.10: Leading Feynman diagrams contributing to the B^0 meson oscillations with the CKM matrix elements V_{xd}, V_{xb} where $x = u, c, t$.

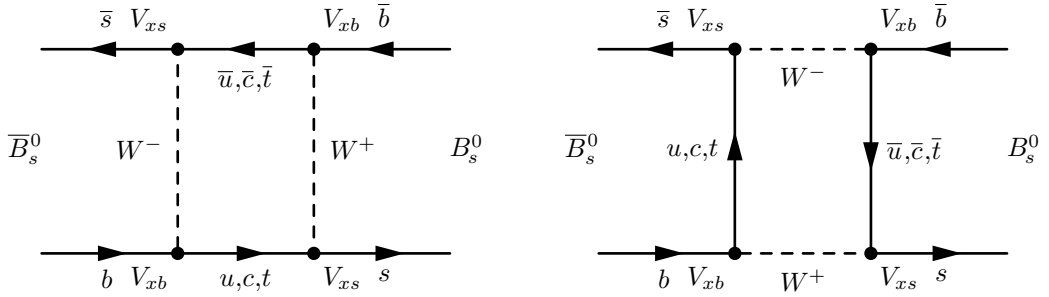


Figure 2.11: Leading Feynman diagrams contributing to the strange B_s^0 meson oscillations with the CKM matrix elements V_{xs}, V_{xb} where $x = u, c, t$.

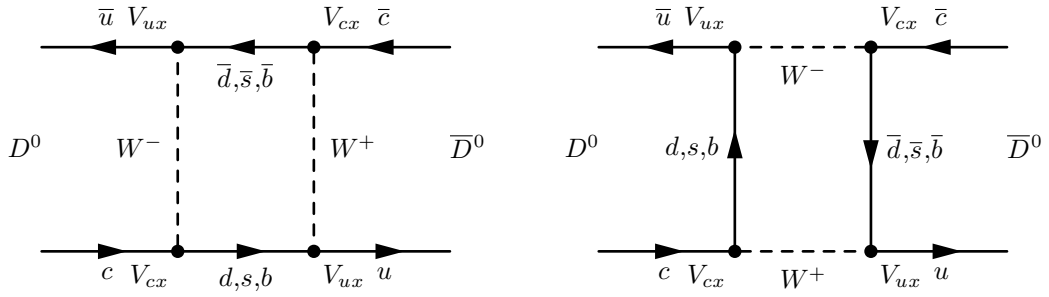


Figure 2.12: Leading Feynman diagrams contributing to the D^0 meson oscillations with the CKM matrix elements V_{ux}, V_{cx} where $x = d, s, b$.

2.5 Time Evolution

Equation (2.4.4) will be used for calculating the time evolution.
The time evolution of this quantum system is given by the Schrödinger equation.

$$\begin{aligned} \mathrm{i}\hbar\frac{\partial}{\partial t}|\psi(t)\rangle &= \mathcal{H}|\psi(t)\rangle \\ \mathrm{i}\hbar\frac{\partial}{\partial t}\big(\psi_1(t)|X^0\rangle + \psi_2(t)|\overline{X}^0\rangle\big) &= \mathcal{H}\big(\psi_1(t)|X^0\rangle + \psi_2(t)|\overline{X}^0\rangle\big) \end{aligned} \tag{2.5.1}$$

The solution of the Schrödinger equation is given as:

$$|\psi(t)\rangle = \mathrm{e}^{-\mathrm{i}\lambda t}|\psi(0)\rangle \tag{2.5.2}$$

The masses and the decay rates from the eigenvalues $\lambda_{1,2}$ from eq. (2.4.10) are defined as:

$$m_n = \Re(\lambda_n) \qquad \Gamma_n = -2\Im(\lambda_n) \qquad n \in \{1,2\} \tag{2.5.3}$$

Moreover, the eigenvectors of eq. (2.4.7) to the associated eigenvalues eq. (2.4.10) are[6]:

$$EV_1 = \begin{pmatrix} -q \\ p \end{pmatrix} \qquad EV_2 = \begin{pmatrix} q \\ p \end{pmatrix} \tag{2.5.4}$$

Hence, the solution is given as:

$$|X_1\rangle = p|X^0\rangle - q|\overline{X}^0\rangle \tag{2.5.5}$$

$$|X_2\rangle = p|X^0\rangle + q|\overline{X}^0\rangle \tag{2.5.6}$$

And the time evolution of the system follows as:

$$\begin{aligned} |X_1(t)\rangle &= \mathrm{e}^{-\mathrm{i}(m_1-\frac{\mathrm{i}}{2}\Gamma_1)t}\left(p|X^0(0)\rangle - q|\overline{X}^0(0)\rangle\right) \\ |X_2(t)\rangle &= \mathrm{e}^{-\mathrm{i}(m_2-\frac{\mathrm{i}}{2}\Gamma_2)t}\left(p|X^0(0)\rangle + q|\overline{X}^0(0)\rangle\right) \end{aligned}$$

In the following, the notation $X^0(0) = X^0$ and $\overline{X}^0(0) = \overline{X}^0$ are applied. Consequently, using this notation the states $|X^0(t)\rangle$ and $|\overline{X}^0(t)\rangle$ are expressed as[7]:

$$|X^0(t)\rangle = g^+|X^0\rangle + \frac{q}{p}g^-|\overline{X}^0\rangle \tag{2.5.7}$$

$$|\overline{X}^0(t)\rangle = \frac{p}{q}g^-|X^0\rangle + g^+|\overline{X}^0\rangle, \tag{2.5.8}$$

where the following relations are used:

$$g^+ = \frac{1}{2}\left(\mathrm{e}^{-\mathrm{i}(m_2+\frac{\mathrm{i}}{2}\Gamma_2)t} + \mathrm{e}^{-\mathrm{i}(m_1+\frac{\mathrm{i}}{2}\Gamma_1)t}\right) \tag{2.5.9}$$

[6] A detailed derivation is given in app. A.3.2.
[7] Detailed calculation is given in app. A.4.

$$g^- = \frac{1}{2}\left(\mathrm{e}^{-\mathrm{i}(m_2+\frac{\mathrm{i}}{2}\Gamma_2)t} - \mathrm{e}^{-\mathrm{i}(m_1+\frac{\mathrm{i}}{2}\Gamma_1)t}\right) \tag{2.5.10}$$

Calculating the products of the functions, $g^{\pm}$, yields[8]:

$$g^{\pm^*}g^{\pm} = \frac{1}{2}\mathrm{e}^{-\Gamma t}\left(\cosh\left(\frac{\Delta\Gamma t}{2}\right) \pm \cos(\Delta m t)\right) \tag{2.5.11}$$

$$g^{+^*}g^{-} = \frac{1}{2}\mathrm{e}^{-\Gamma t}\left(-\sinh\left(\frac{\Delta\Gamma t}{2}\right) + \mathrm{i}\sin(\Delta m t)\right) \tag{2.5.12}$$

$$g^{+}g^{-^*} = \frac{1}{2}\mathrm{e}^{-\Gamma t}\left(-\sinh\left(\frac{\Delta\Gamma t}{2}\right) - \mathrm{i}\sin(\Delta m t)\right) \tag{2.5.13}$$

Defining $M = \frac{m_1+m_2}{2}$, $\Delta m = m_1 - m_2$, $\Gamma = \frac{\Gamma_1+\Gamma_2}{2}$ and $\Delta\Gamma = \Gamma_2 - \Gamma_1$, $g^{\pm}$ is:

$$\begin{aligned} g^{\pm} &= \frac{1}{2}\left(\mathrm{e}^{-\mathrm{i}m_2 t - \frac{\Gamma_2}{2}t} \pm \mathrm{e}^{-\mathrm{i}m_1 t - \frac{\Gamma_1}{2}t}\right) \\ &= \frac{1}{2}\mathrm{e}^{-\mathrm{i}Mt}\left(\mathrm{e}^{\mathrm{i}\frac{\Delta m}{2}t - \frac{\Gamma_2}{2}t} \pm \mathrm{e}^{-\mathrm{i}\frac{\Delta m}{2}t - \frac{\Gamma_1}{2}t}\right) \\ &= \frac{1}{2}\mathrm{e}^{-\mathrm{i}Mt}\mathrm{e}^{-\frac{\Gamma}{2}t}\left(\mathrm{e}^{\mathrm{i}\frac{\Delta m}{2}t}\mathrm{e}^{-\frac{\Delta\Gamma}{4}t} \pm \mathrm{e}^{-\mathrm{i}\frac{\Delta m}{2}t}\mathrm{e}^{\frac{\Delta\Gamma}{4}t}\right) \end{aligned} \tag{2.5.14}$$

The probability to obtain a final state of $|X^0\rangle$ or $|\overline{X}^0\rangle$ is:

$$\mathcal{P}_{X^0\to X^0} = |\langle X^0|X^0(t)\rangle|^2 = |g^+|^2 = \frac{1}{2}\mathrm{e}^{-\Gamma t}\left(\cosh\left(\frac{\Delta\Gamma t}{2}\right) + \cos(\Delta m t)\right)$$

$$\mathcal{P}_{\overline{X}^0\to\overline{X}^0} = |\langle \overline{X}^0|\overline{X}^0(t)\rangle|^2 = |g^+|^2 = \frac{1}{2}\mathrm{e}^{-\Gamma t}\left(\cosh\left(\frac{\Delta\Gamma t}{2}\right) + \cos(\Delta m t)\right)$$

$$\mathcal{P}_{X^0\to\overline{X}^0} = |\langle X^0|\overline{X}^0(t)\rangle|^2 = \left|\frac{q}{p}g^-(t)\right|^2 = \left|\frac{q}{p}\right|^2\frac{1}{2}\mathrm{e}^{-\Gamma t}\left(\cosh\left(\frac{\Delta\Gamma t}{2}\right) - \cos(\Delta m t)\right)$$

$$\mathcal{P}_{\overline{X}^0\to X^0} = |\langle \overline{X}^0|X^0(t)\rangle|^2 = \left|\frac{p}{q}g^-(t)\right|^2 = \left|\frac{p}{q}\right|^2\frac{1}{2}\mathrm{e}^{-\Gamma t}\left(\cosh\left(\frac{\Delta\Gamma t}{2}\right) - \cos(\Delta m t)\right)$$

The probabilities, $\mathcal{P}$, of the flavor mixings must be equal to conserve $\mathcal{CP}$ symmetry during the oscillations of the neutral mesons, i.e., $\mathcal{P}_{X^0\to\overline{X}^0} = \mathcal{P}_{\overline{X}^0\to X^0}$. Hence, $\left|\frac{p}{q}\right|^2 = \left|\frac{q}{p}\right|^2$, resulting in $\frac{p}{q} = \pm\frac{q}{p}$. If $\frac{p}{q} \in \mathbb{R} \Rightarrow \frac{p}{q} = 1$.
In the case that the probabilities of the oscillations are not the same, known as the *indirect $\mathcal{CP}$ violation*, which is discussed in Sect. 2.7.2, the ratio $\frac{q}{p} \simeq e^{i\delta}$ is a complex value.
The flavor oscillations for different mesons (K^0, B^0, B_s^0, D^0) are shown in Fig. 2.13. An overview of the mesons is presented in Tab. 2.2. According to [32, 47], the definition of $x = \frac{\Delta m}{\Gamma}$ and $y = \frac{\Delta\Gamma}{2\Gamma}$ with $\Delta m = M_\mathrm{H} - M_\mathrm{L}$, $\Delta\Gamma = \Gamma_\mathrm{L} - \Gamma_\mathrm{H}$ and $\Gamma = \frac{1}{2}(\Gamma_\mathrm{H} + \Gamma_\mathrm{L})$ are used. M_L denotes the light mass eigenstate and M_H is the heavy mass eigenstate.
The frequency of the oscillations is due to the mass difference Δm, divided by the average of the decay rates Γ.

[8] Detailed calculations are given in app. A.5.

Table 2.2: Properties for K^0, B^0, B_s^0 and D^0 meson oscillations.

Property	K^0	B^0
Δm in eV	$(3.484 \pm 0.006) \cdot 10^{-6}$	$(3.356 \pm 0.020) \cdot 10^{-4}$
$\tau_{\mathrm{H}} = \frac{1}{\Gamma_H}$ in s	$(0.8954 \pm 0.0004) \cdot 10^{-10}$	$(1.520 \pm 0.004) \cdot 10^{-12}$
$\tau_L = \frac{1}{\Gamma_L}$ in s	$(5.1116 \pm 0.021) \cdot 10^{-8}$	
$\Delta\Gamma$ in s^{-1}	$-1.11 \cdot 10^{10}$	< 0.001 [46]
$x = \frac{\Delta m}{\Gamma}$	0.947	0.775
$y = \frac{\Delta\Gamma}{2\Gamma}$	-0.997	< 0.001

Property	B_s^0	D^0
Δm in eV	$(1.11688 \pm 0.0014) \cdot 10^{-2}$	$6.25^{+2.70}_{2.90} \cdot 10^{-6}$
$\tau_{\mathrm{H}} = \frac{1}{\Gamma_H}$ in s	$(1.510 \pm 0.005) \cdot 10^{-12}$	$(410.1 \pm 1.5) \cdot 10^{-13}$
$\tau_L = \frac{1}{\Gamma_L}$ in s		
$\Delta\Gamma$ in s^{-1}	$(0.082 \pm 0.007) \cdot 10^{12}$	$3.15 \cdot 10^{10}$
$x = \frac{\Delta m}{\Gamma}$	26.86	0.004
$y = \frac{\Delta\Gamma}{2\Gamma}$	0.062	0.006

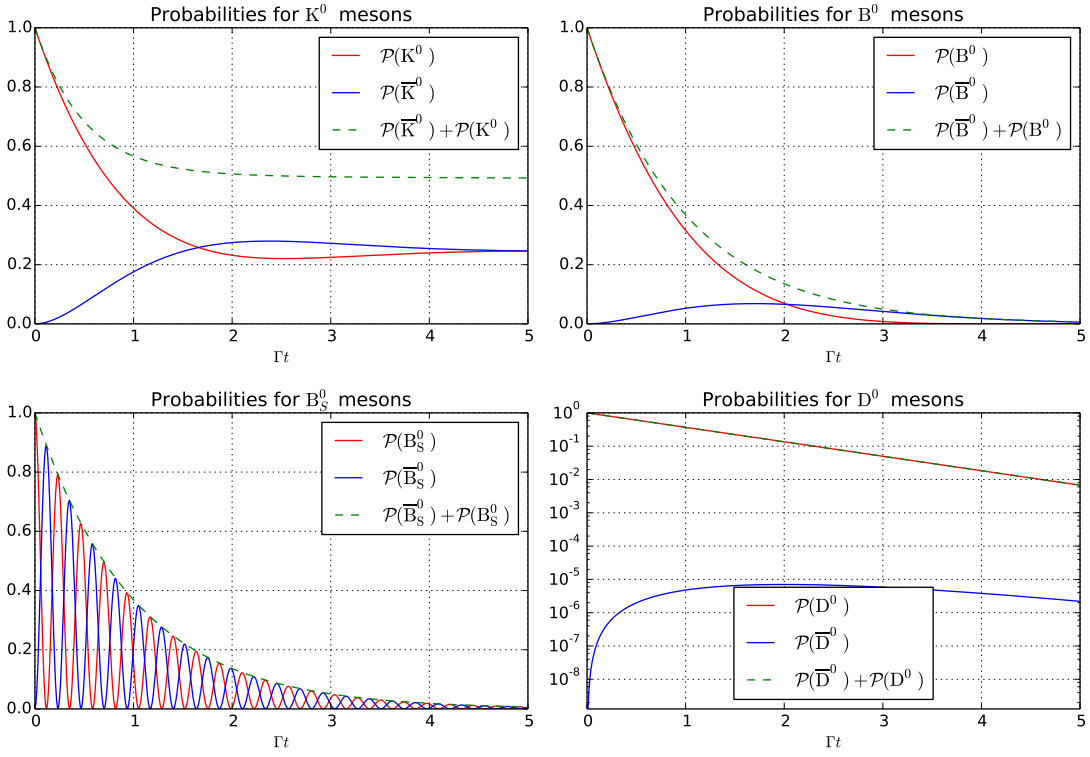


Figure 2.13: Probability of finding a meson in its flavor eigenstate as a function of the decay time, given by the probability $\mathcal{P} = \frac{1}{2}\mathrm{e}^{-\Gamma t}(\cosh(\frac{\Delta\Gamma t}{2}) \pm \cos(\Delta m t))$. The differences are explained by the parameters in Tab. 2.2.

The mass differences, Δm, and decay differences, $\Delta\Gamma$, are difficult to estimate for kaons and D mesons, since the off diagonal elements M_{12} and Γ_{12} are dominated by long distance contributions [48].

2.6 Cronin and Fitch Experiment

In this section, the $\mathcal{CP}$ violation is explained in the neutral kaon system, discovered by Cronin and Fitch. The neutral kaon, K^0, consists of the two quarks $d\bar{s}$, and has the *Strangeness* quantum number $\tilde{S} = 1$. The antikaon $\overline{K}^0$ is composed of the two quarks $\bar{d}s$ and has $\tilde{S} = -1$. Both particles $(K^0\overline{K}^0)$ are bosons with spin $S = 0$.
In strong decays, the flavor is conserved. Since the kaon is the lightest particle containing an s quark, it cannot decay via the strong interaction. Thus, it has to decay via the weak force where the strangeness quantum number is not conserved[9]. The states $|K^0\rangle$ and $|\overline{K}^0\rangle$ are called *flavor eigenstates*. The charge and parity symmetries of the neutral (anti)kaons are studied by applying the operators, introduced in Sect. 2.2:

$$\mathcal{P}|K^0\rangle = -|K^0\rangle \qquad \mathcal{P}|\overline{K}^0\rangle = -|\overline{K}^0\rangle \tag{2.6.1}$$

$$\mathcal{C}|K^0\rangle = \mathcal{C}|d\bar{s}\rangle = |\bar{d}s\rangle = |\overline{K}^0\rangle \qquad \mathcal{C}|\overline{K}^0\rangle = |K^0\rangle \tag{2.6.2}$$

$$\mathcal{CP}|K^0\rangle = -|\overline{K}^0\rangle \qquad \mathcal{CP}|\overline{K}^0\rangle = -|K^0\rangle \tag{2.6.3}$$

The flavor is not conserved in the weak interaction. The $\mathcal{CP}$ eigenstates are expressed as linear combination of the flavor eigenstates:

$$|K_1\rangle = \frac{1}{\sqrt{2}}\left(|K^0\rangle - |\overline{K}^0\rangle\right) \tag{2.6.4}$$

$$|K_2\rangle = \frac{1}{\sqrt{2}}\left(|K^0\rangle + |\overline{K}^0\rangle\right) \tag{2.6.5}$$

Applying the $\mathcal{CP}$ operator yields:

$$\mathcal{CP}|K_1\rangle = \mathcal{CP}\frac{1}{\sqrt{2}}\left(|K^0\rangle - |\overline{K}^0\rangle\right) = \frac{1}{\sqrt{2}}\left(-|\overline{K}^0\rangle + |K^0\rangle\right) = |K_1\rangle \tag{2.6.6}$$

$$\mathcal{CP}|K_2\rangle = \mathcal{CP}\frac{1}{\sqrt{2}}\left(|K^0\rangle + |\overline{K}^0\rangle\right) = \frac{1}{\sqrt{2}}\left(-|\overline{K}^0\rangle - |K^0\rangle\right) = -|K_2\rangle \tag{2.6.7}$$

Neutral kaons decay mostly into pions ($\sim 99.89\,\%$ of K_S^0 decay to two pions; $\sim 32.06\,\%$ of K_L^0 decay to three pions [32]). The angular momentum $\vec{L} = 0$ for two pions is conserved. Moreover, for three pions the relation $\vec{L_1} \oplus \vec{L_2} = 0 \Leftrightarrow \vec{L_1} = \vec{L_2}$ holds.

[9] The quantum number is not conserved due to the charged weak interaction where $W^{\pm}$ bosons are involved.

Applying the parity and charge conjugation operators yields:

$$K^0 \to \pi^0\pi^0 : \begin{cases} \mathcal{P}(\pi^0\pi^0) \Rightarrow \eta_\mathcal{P} = (-1)(-1)(-1)^{|\vec{L}|} = 1 \\ \mathcal{C}(\pi^0\pi^0) \Rightarrow \eta_\mathcal{C} = (+1)(+1) = 1 \end{cases}$$
$$\Rightarrow \mathcal{CP}(\pi^0\pi^0) \Rightarrow \eta_\mathcal{CP} = 1$$
$$K^0 \to \pi^+\pi^- : \begin{cases} \mathcal{P}(\pi^+\pi^-) \Rightarrow \eta_\mathcal{P} = (-1)(-1)(-1)^{|\vec{L}|} = 1 \\ \mathcal{C}(\pi^+\pi^-) \Rightarrow \eta_\mathcal{C} = (-1)(-1) = 1 \end{cases}$$
$$\Rightarrow \mathcal{CP}(\pi^+\pi^-) \Rightarrow \eta_\mathcal{CP} = 1$$
$$K^0 \to \pi^0\pi^0\pi^0 : \begin{cases} \mathcal{P}(\pi^0\pi^0\pi^0) \Rightarrow \eta_\mathcal{P} = (-1)(-1)(-1)(-1)^{|\vec{L}_1|}(-1)^{|\vec{L}_2|} = -1 \\ \mathcal{C}(\pi^0\pi^0\pi^0) \Rightarrow \eta_\mathcal{C} = (+1)(+1)(+1) = 1 \end{cases}$$
$$\Rightarrow \mathcal{CP}(\pi^0\pi^0\pi^0) \Rightarrow \eta_\mathcal{CP} = -1$$
$$K^0 \to \pi^+\pi^-\pi^0 : \begin{cases} \mathcal{P}(\pi^+\pi^-\pi^0) \Rightarrow \eta_\mathcal{P} = (-1)(-1)(-1)(-1)^{|\vec{L}_1|}(-1)^{|\vec{L}_2|} = -1 \\ \mathcal{C}(\pi^+\pi^-\pi^0) \Rightarrow \eta_\mathcal{C} = (-1)(-1)(+1)^{L_1} \end{cases}$$
$$\Rightarrow \mathcal{CP}(\pi^+\pi^-\pi^0) \Rightarrow \eta_\mathcal{CP} = -1(-1)^{|\vec{L}_1|}$$

Using the $\mathcal{CP}$ operator yields (a schematic is shown in Fig. 2.14):

$$\mathcal{CP}|K_1\rangle = +|K_1\rangle \quad \Rightarrow \quad |K_1\rangle \to |\pi\pi\rangle \Rightarrow \quad \mathcal{CP} \text{ even} \tag{2.6.8}$$
$$\mathcal{CP}|K_2\rangle = -|K_2\rangle \quad \Rightarrow \quad |K_2\rangle \to |\pi\pi\pi\rangle \Rightarrow \quad \mathcal{CP} \text{ odd} \tag{2.6.9}$$

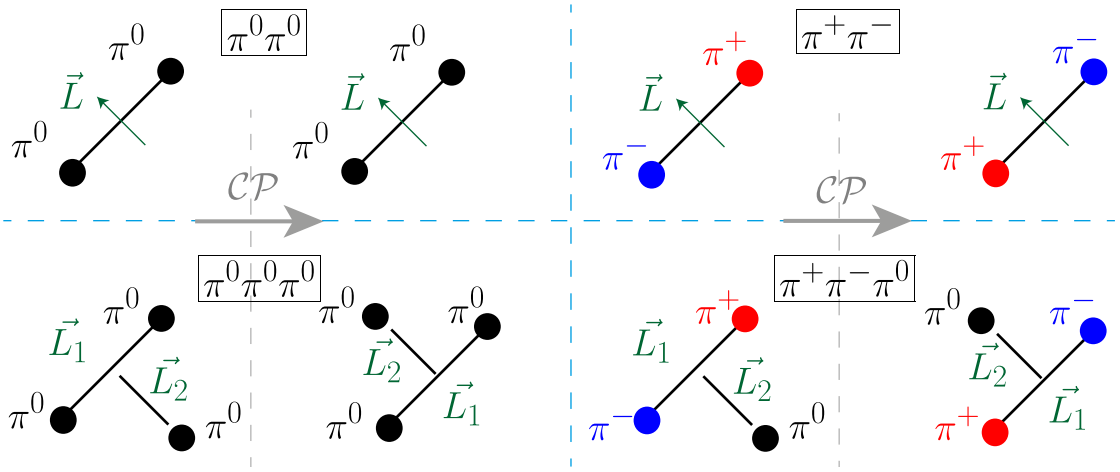


Figure 2.14: Application of the $\mathcal{CP}$ operator on two- and three-pion systems.

Cronin and Fitch performed an experiment in 1964 investigating the decays of neutral kaons [15]. They discovered the $\mathcal{CP}$ violation and were awarded the Nobel Prize in 1980. They had a beam consisting of two types of kaons. The particles have different life-times ($\tau_\mathrm{L} = 5.2 \cdot 10^{-8}\,\mathrm{s}$, $\tau_\mathrm{S} = 0.89 \cdot 10^{-10}\,\mathrm{s}$ [32]). After passing a 57 foot (17.34 m) long beam pipe the decay products of the kaons were detected. If $\mathcal{CP}$ were conserved, only the decay into three pions would be observed because the short-lived kaons would have all decayed before reaching the end of the pipe.

In that case, the mass eigenstates correspond to the $\mathcal{CP}$ eigenstates:

$$|K_S^0\rangle = |K_1\rangle \qquad |K_L^0\rangle = |K_2\rangle \tag{2.6.10}$$

However, Cronin and Fitch observed 45±9 out of 22700 events where kaons decayed into $\pi^+\pi^-$, which corresponds to a fraction:

$$\frac{\#(K^0 \to \pi\pi)}{\#(K^0 \to \pi\pi\pi)} = 2.3 \cdot 10^{-3} \tag{2.6.11}$$

They observed the $\mathcal{CP}$ violation since a small fraction of the two-pion decay was observed at the end of the pipe. A sketch is shown in Fig. 2.15.

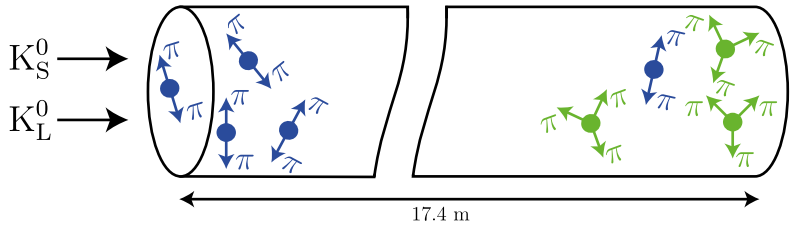


Figure 2.15: Sketch of the Cronin and Fitch experimental setup. A beam consisting of two types of kaons (K_S^0 and K_L^0) is injected into a beam pipe. All K_S^0 decay at the beginning of the pipe. It was expected to observe only three pion decays in the end. The $\mathcal{CP}$ violation was shown by detecting two pion decays at the end of the pipe,

Thus, neither the state $|K_2\rangle$ is a pure state of $|K_L^0\rangle$ nor $|K_1\rangle$ is a pure state of $|K_S^0\rangle$. A complex mixing parameter ε, $|\varepsilon| \sim 2 \times 10^{-3}$ is introduced:

$$|K_L^0\rangle = \frac{1}{\sqrt{1+|\varepsilon|^2}}\left(|K_2\rangle + \varepsilon|K_1\rangle\right) \tag{2.6.12}$$

$$|K_S^0\rangle = \frac{1}{\sqrt{1+|\varepsilon|^2}}\left(|K_1\rangle + \varepsilon|K_2\rangle\right) \tag{2.6.13}$$

To conserve the $\mathcal{CP}$ symmetry, the mixing parameter must be zero and the weak eigenstates would be pure $\mathcal{CP}$ eigenstates.
Expressing $|K_L^0\rangle$ and $|K_S^0\rangle$ in terms $|K^0\rangle$ and $|\overline{K}^0\rangle$ result in[10]:

$$\begin{aligned} |K_L^0\rangle &= p|K^0\rangle + q|\overline{K}^0\rangle \\ |K_S^0\rangle &= p|K^0\rangle - q|\overline{K}^0\rangle \end{aligned} \tag{2.6.14}$$

Using the notation for p and q:

$$\frac{p}{q} = \frac{1+\varepsilon}{1-\varepsilon} \qquad p = \frac{1+\varepsilon}{\sqrt{2(1+\varepsilon)}} \qquad q = \frac{1-\varepsilon}{\sqrt{2(1+\varepsilon)}} \tag{2.6.15}$$

[10]For detailed calculation, see app. A.6.1 and app. A.6.2.

For this reason, $|K^0\rangle$ and $|\overline{K}^0\rangle$ are expressed as follows[11]:

$$|K^0\rangle = \frac{|K_L^0\rangle + |K_S^0\rangle}{2p} \qquad |\overline{K}^0\rangle = \frac{|K_L^0\rangle - |K_S^0\rangle}{2q} \tag{2.6.16}$$

To conclude:

- **Flavor eigenstates** (also named **strong eigenstates**):

$$|K^0\rangle \text{ and } |\overline{K}^0\rangle$$

- $\boldsymbol{\mathcal{CP}}$ **eigenstates** are a linear combination of flavor eigenstates:

$$|K_1\rangle = \frac{1}{\sqrt{2}}(|K^0\rangle - |\overline{K}^0\rangle) \text{ and } |K_2\rangle = \frac{1}{\sqrt{2}}(|K^0\rangle + |\overline{K}^0\rangle)$$

- **Weak eigenstates** (also known as **mass eigenstates**) are a combination of flavor eigenstates:

$$|K_L^0\rangle = p|K^0\rangle + q|\overline{K}^0\rangle \text{ and } |K_S^0\rangle = p|K^0\rangle - q|\overline{K}^0\rangle$$

  It can be also expressed as a combination of $\mathcal{CP}$ eigenstates:

$$|K_L^0\rangle = \frac{1}{\sqrt{1+|\varepsilon|^2}}\left(|K_2\rangle + \varepsilon|K_1\rangle\right) \text{ and } |K_S^0\rangle = \frac{1}{\sqrt{1+|\varepsilon|^2}}\left(|K_1\rangle + \varepsilon|K_2\rangle\right)$$

2.7 Types of $\mathcal{CP}$ violation

Three different types of $\mathcal{CP}$ violation are discussed in this section. The general X mesons are used in this section to illustrate the different types. The four amplitudes $A_f, \overline{A}_f, A_{\overline{f}}$ and $\overline{A}_{\overline{f}}$ describe the transition of the (anti)meson to the final state $|f\rangle$ and $|\overline{f}\rangle$:

$$\begin{aligned} A_f &= A(X \to f) = \langle f|\mathcal{H}|X\rangle & \overline{A}_f &= A(\overline{X} \to f) = \langle f|\mathcal{H}|\overline{X}\rangle \\ A_{\overline{f}} &= A(X \to \overline{f}) = \langle \overline{f}|\mathcal{H}|X\rangle & \overline{A}_{\overline{f}} &= A(\overline{X} \to \overline{f}) = \langle \overline{f}|\mathcal{H}|\overline{X}\rangle \end{aligned} \tag{2.7.1}$$

[11] For a detailed calculation refer to app. A.6.3.

2.7.1 Direct $\mathcal{CP}$ violation

The $\mathcal{CP}$ violation in decay, also called *direct* $\mathcal{CP}$ *violation*, is defined by an asymmetry of the decay amplitudes (and decay rates) of the meson X and its antiparticle $\overline{X}$ into the final states $(f,\ \overline{f})$. A sketch is shown in Fig. 2.16. Mathematically, the direct $\mathcal{CP}$ violation is expressed by:

$$\Gamma(X \to f) \neq \Gamma(\overline{X} \to \overline{f}) \tag{2.7.2}$$

$$\left|\frac{\overline{A}_{\overline{f}}}{A_f}\right| \neq 1 \tag{2.7.3}$$

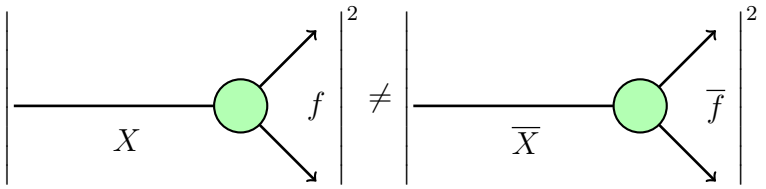


Figure 2.16: Sketch of the direct $\mathcal{CP}$ violation. The green dots depicts the decays [47].

The amplitude A consists of three parts: The weak-phases, ϕ_i, which change their signs under $\mathcal{CP}$ transformations, the strong phases, δ_i, which conserve their signs under $\mathcal{CP}$ transformations and the magnitudes A_i. The amplitudes A_f and $\overline{A}_{\overline{f}}$ are given as (see eq. (2.7.1)):

$$A_f = \sum_i A_i e^{\mathrm{i}(\delta_i+\phi_i)} \qquad \overline{A}_{\overline{f}} = \sum_i A_i e^{\mathrm{i}(\delta_i-\phi_i)} \tag{2.7.4}$$

The $\mathcal{CP}$ violation in the decay occurs only if there are different weak and strong phases from at least two terms:

$$|A_f|^2 - |\overline{A}_{\overline{f}}|^2 = 2\sum_{i,j} A_i A_j \sin(\phi_i - \phi_j)\sin(\delta_i - \delta_j) \tag{2.7.5}$$

The $\mathcal{CP}$ violation can be observed in the decay of charged B mesons:

$$\frac{1-|\overline{A}/A|^2}{1+|\overline{A}/A|^2} = \frac{\Gamma(B^+ \to f) - \Gamma(B^- \to \overline{f})}{\Gamma(B^+ \to f) + \Gamma(B^- \to \overline{f})} \tag{2.7.6}$$

2.7.2 $\mathcal{CP}$ violation in Mixing

$\mathcal{CP}$ violation in mixing, which is also called *indirect* $\mathcal{CP}$ *violation*, occurs if the mass eigenstates do not coincide with the $\mathcal{CP}$ eigenstates. Hence, there is an asymmetry in the flavor changing oscillations that is caused by the off-diagonal elements in the Hamiltonian, $\mathcal{H}_{ij}, i \neq j$. A sketch is shown in Fig. 2.17. A Feynman diagram

is shown in Fig. 2.18. The indirect $\mathcal{CP}$ violation is mathematically expressed as:

$$\left|\frac{q}{p}\right| \neq 1 \tag{2.7.7}$$

$$\text{mass eigenstates} \neq \mathcal{CP} \text{ eigenstates} \tag{2.7.8}$$

$$\mathcal{P}_{\text{probability}}(X \to \overline{X}) \neq \mathcal{P}_{\text{probability}}(\overline{X} \to X) \tag{2.7.9}$$

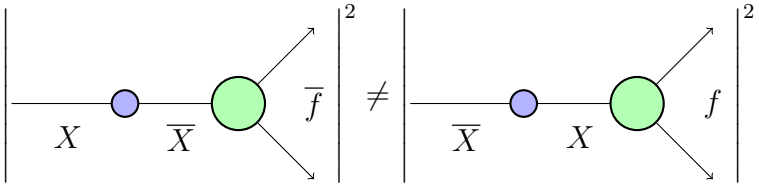


Figure 2.17: Sketch of the indirect $\mathcal{CP}$ violation. The blue dots depict the flavor oscillations. The decays are shown by the green dots [47].

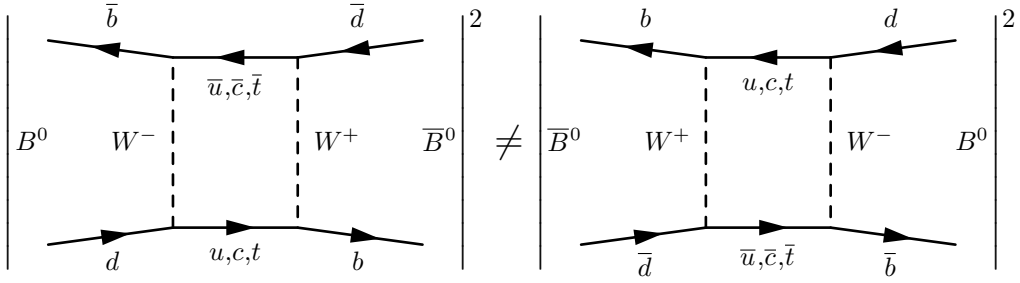


Figure 2.18: Indirect $\mathcal{CP}$ violation in the $B^0 \leftrightarrow \overline{B}^0$ oscillation.

2.7.3 $\mathcal{CP}$ violation in interference between mixing and decay

In addition to the previous $\mathcal{CP}$ violations, an interference of both the decay with and without mixing to the same final $\mathcal{CP}$ eigenstate $|f_{\mathcal{CP}}\rangle$, can occur. The possible decay chains $X \to f$ and $\overline{X} \to f$ interfere, which could result in a $\mathcal{CP}$ violation. This interference is mathematically expressed as:

$$\Im(\lambda) \neq 0, \qquad \lambda = \eta_{f\mathcal{CP}} \frac{q}{p} \frac{\overline{A}_{\overline{f}_{\mathcal{CP}}}}{A_{f_{\mathcal{CP}}}} = \frac{q}{p} \frac{\overline{A}_{f_{\mathcal{CP}}}}{A_{f_{\mathcal{CP}}}} \neq 1 \tag{2.7.10}$$

$$\Gamma(X_{(\rightsquigarrow \overline{X})} \to f)(t) \neq \Gamma(\overline{X}_{(\rightsquigarrow X)} \to f)(t) \tag{2.7.11}$$

where $\eta_{f\mathcal{CP}} = \pm 1$ is the $\mathcal{CP}$ eigenvalue of the state $f_{\mathcal{CP}}$. The $\mathcal{CP}$ violation in the decay (see eq. (2.7.3)) and the $\mathcal{CP}$ violation in the mixing (see eq. (2.7.7)) both contribute to eq. (2.7.10). The interference in the $\mathcal{CP}$ violation occurs in the time-dependent asymmetry of neutral mesons which decay into their $\mathcal{CP}$ eigenstates. The formula is given in eq. (2.9.5). The sketch is shown in Fig. 2.19.

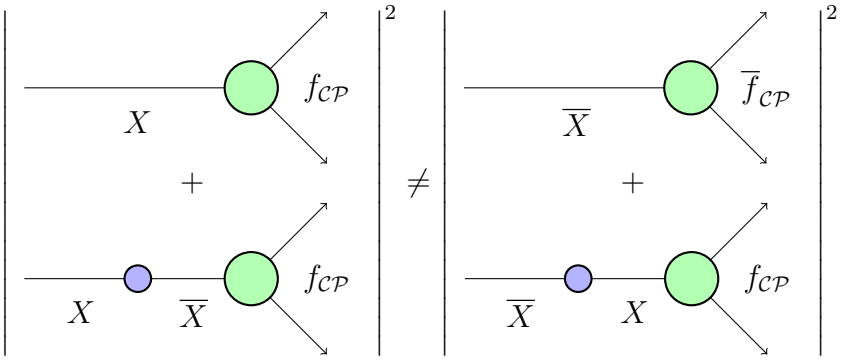


Figure 2.19: $\mathcal{CP}$ violation in the interference between the direct and indirect $\mathcal{CP}$ violation. The blue dots depict the flavor oscillations. The decays are shown by the green dots [47].

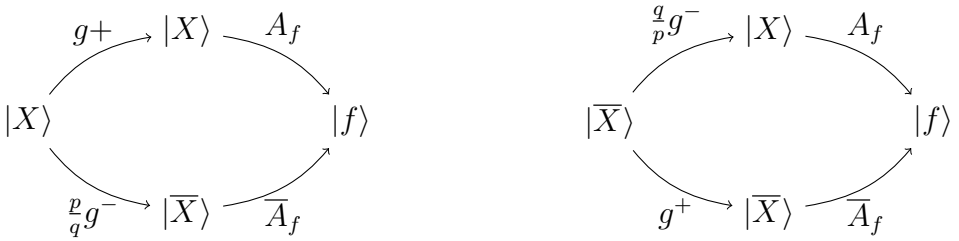


Figure 2.20: The decay of the initial mesons $X, \overline{X}$ by either directly decaying into the final state f or oscillating, where $g^{\pm}$ is defined in eq. (2.5.14), the decay amplitudes are defined in eq. (2.7.1) and the ratio q/p is given in eq. (2.4.11).

An overview of the decay from the initial $|X\rangle$ or $|\overline{X}\rangle$ meson into the final state $|f\rangle$ is shown in Fig. 2.20.

2.8 Neutral B Meson system

For neutral B mesons the two mass eigenstates have almost the same lifetimes $\Gamma_1 \approx \Gamma_2$, since the element Γ_{12} is CKM-suppressed. This is due to the large number of decay channels and the large mass in contrast to the neutral kaon system. Consequently, their difference, $\Delta\Gamma$, can be ignored ($\Delta\Gamma \approx 0$) The ratio $\frac{|\Gamma_1 - \Gamma_2|}{\Gamma}$ is approximately < 0.001 [46].
Moreover, $\mathrm{e}^{-\mathrm{i}Mt} = 1$ is chosen by phase convention. As a result, eq. (2.5.14) yields:

$$g^{\pm} = \mathrm{e}^{-\frac{\Gamma}{2}t}\frac{\mathrm{e}^{\mathrm{i}\Delta mt/2} \pm \mathrm{e}^{-\mathrm{i}\Delta mt/2}}{2} = \begin{cases} \mathrm{e}^{-\frac{\Gamma}{2}t}\cos\left(\frac{\Delta mt}{2}\right) \\ \mathrm{i}\mathrm{e}^{-\frac{\Gamma}{2}t}\sin\left(\frac{\Delta mt}{2}\right) \end{cases} \tag{2.8.1}$$

The oscillations between the B mesons ($B^0 \leftrightarrow \overline{B}^0$) shown in Fig. 2.10 are dominated by the virtual top quark[12] and Glashow-Iliopoulos-Maiani (GIM) cancella-

[12]This corresponds to the V_{tb} element in the CKM matrix, which was introduced in Sect. 2.3.

tions [49]. This leads to the ratio $\left|\frac{p}{q}\right| = 1$, i.e., there is no direct $\mathcal{CP}$ violation in mixing for $B^0\overline{B}^0$ mesons.
The time evolutions for the flavor eigenstates of the neutral B mesons $|B^0(t)\rangle$ and $|\overline{B}^0(t)\rangle$ yield, using eq. (2.5.7)), eq. (2.5.8) and eq. (2.8.1):

$$|B^0(t)\rangle = \mathrm{e}^{-\frac{\Gamma}{2}t}\left(\cos\left(\tfrac{\Delta mt}{2}\right)|B^0\rangle + \tfrac{q}{p}\mathrm{i}\sin\left(\tfrac{\Delta mt}{2}\right)|\overline{B}^0\rangle\right) \tag{2.8.2}$$

$$|\overline{B}^0(t)\rangle = \mathrm{e}^{-\frac{\Gamma}{2}t}\left(\cos\left(\tfrac{\Delta mt}{2}\right)|\overline{B}^0\rangle + \tfrac{p}{q}\mathrm{i}\sin\left(\tfrac{\Delta mt}{2}\right)|B^0\rangle\right) \tag{2.8.3}$$

Hence, the probabilities to have a pure state of $|B^0\rangle$ and $|\overline{B}^0\rangle$, respectively depending on the initial states, are calculated as:

$$\mathcal{P}_{B^0\to B^0} = |\langle B^0|B^0(t)\rangle|^2 = \tfrac{1}{2}\mathrm{e}^{-\Gamma t}\big(1+\cos(\Delta mt)\big) \tag{2.8.4}$$

$$\mathcal{P}_{\overline{B}0\to\overline{B}0} = |\langle \overline{B}^0|\overline{B}^0(t)\rangle|^2 = \tfrac{1}{2}\mathrm{e}^{-\Gamma t}\big(1+\cos(\Delta mt)\big) \tag{2.8.5}$$

$$\mathcal{P}_{B^0\to\overline{B}0} = |\langle B^0|\overline{B}^0(t)\rangle|^2 = \tfrac{1}{2}\left(\tfrac{p}{q}\right)^2\mathrm{e}^{-\Gamma t}\big(1-\cos(\Delta mt)\big) \tag{2.8.6}$$

$$\mathcal{P}_{\overline{B}0\to B^0} = |\langle \overline{B}^0|B^0(t)\rangle|^2 = \tfrac{1}{2}\left(\tfrac{q}{p}\right)^2\mathrm{e}^{-\Gamma t}\big(1-\cos(\Delta mt)\big) \tag{2.8.7}$$

The probabilities to find a meson in its flavor eigenstate are plotted in Fig. 2.13. According to Tab. 2.2, the ratio is $\frac{\Delta m}{\Gamma} = 0.775 \pm 0.006$ for neutral B mesons. Hence, they mostly decay before changing their flavor.

2.9 Time dependent decay amplitude

The four decay amplitudes of a given initial particle $(B^0, \overline{B}^0)$ decaying into the final state $(f, \overline{f})$ are defined by:

$$\begin{aligned} A_f &= A(B^0\to f) = \langle f|\mathcal{H}|B^0\rangle & \overline{A}_f &= A(\overline{B}^0\to f) = \langle f|\mathcal{H}|\overline{B}^0\rangle \\ A_{\overline{f}} &= A(B^0\to \overline{f}) = \langle \overline{f}|\mathcal{H}|B^0\rangle & \overline{A}_{\overline{f}} &= A(\overline{B}^0\to \overline{f}) = \langle \overline{f}|\mathcal{H}|\overline{B}^0\rangle \end{aligned} \tag{2.9.1}$$

The decay amplitudes for neutral B mesons are obtained by using eq. (2.8.2) and eq. (2.8.3):

$$\begin{aligned} A(t) = \langle f|B^0(t)\rangle &= \mathrm{e}^{-\frac{\Gamma}{2}t}\left(A_f\cos\left(\tfrac{\Delta mt}{2}\right) + \mathrm{i}\frac{q}{p}\frac{\overline{A}_f}{A_f}A_f\sin\left(\tfrac{\Delta mt}{2}\right)\right) \\ &= A_f\mathrm{e}^{-\frac{\Gamma}{2}t}\left(\cos\left(\tfrac{\Delta mt}{2}\right) + \mathrm{i}\lambda\sin\left(\tfrac{\Delta mt}{2}\right)\right) \\ \overline{A}_f(t) = \langle f|\overline{B}^0(t)\rangle &= \mathrm{e}^{-\frac{\Gamma}{2}t}\left(\overline{A}_f\cos\left(\tfrac{\Delta mt}{2}\right) + \mathrm{i}\frac{p}{q}\frac{A_f}{\overline{A}_f}\overline{A}_f\sin\left(\tfrac{\Delta mt}{2}\right)\right) \\ &= \overline{A}_f\mathrm{e}^{-\frac{\Gamma}{2}t}\left(\cos\left(\tfrac{\Delta mt}{2}\right) + \frac{\mathrm{i}}{\lambda}\sin\left(\tfrac{\Delta mt}{2}\right)\right), \end{aligned}$$

where λ is defined by:

$$\lambda = \frac{q}{p}\frac{\bar{A}_f}{A_f} \tag{2.9.2}$$

Assuming, $\Delta\Gamma = 0$, it follows that $\cosh(0) = 1$ and $\sinh(0) = 1$. Consequently, the decay rates ($\Gamma = |\langle f|B\rangle|^2$) are given as[13]:

$$\Gamma_{B^0\to f} = \frac{1}{2}|A_f|^2 \mathrm{e}^{-\Gamma t}\left(1 + |\lambda|^2 + (1-|\lambda|^2)\cos(\Delta m t) - 2\Im(\lambda)\sin(\Delta m t)\right) \quad (2.9.3)$$

$$\Gamma_{\overline{B}^0\to f} = \frac{1}{2}|A_f|^2 \left|\frac{p}{q}\right|^2 \mathrm{e}^{-\Gamma t}\left(1 + |\lambda|^2 - (1-|\lambda|^2)\cos(\Delta m t) - 2\Im(\lambda)\sin(\Delta m t)\right) \quad (2.9.4)$$

In order to calculate the asymmetry of the decay rates between B mesons and anti B mesons, the differences are divided by the sum of these decay rates, mathematically expressed as:

$$\begin{aligned} a_{\mathcal{CP}} &= \frac{\Gamma(\overline{B}^0(t)\to f) - \Gamma(B^0(t)\to f)}{\Gamma(\overline{B}^0(t)\to f) + \Gamma(B^0(t)\to f)} \\ &= \frac{2(|\lambda|^2-1)\cos(\Delta m t) + 4\Im(\lambda)\sin(\Delta m t)}{2(\lambda^2+1)} \\ &= \underbrace{\frac{\lambda^2-1}{\lambda^2+1}}_{\mathcal{A}_{\mathcal{CP}}}\cos(\Delta m t) + \underbrace{\frac{2\Im(\lambda)}{\lambda^2+1}}_{\mathcal{S}_{\mathcal{CP}}}\sin(\Delta m t) \end{aligned}$$

$$\boxed{a_{\mathcal{CP}} = \mathcal{A}_{\mathcal{CP}}\cos(\Delta m t) + \mathcal{S}_{\mathcal{CP}}\sin(\Delta m t)} \quad (2.9.5)$$

The rates to the conjugate state are given by the same equation: substituting f with $\overline{f}$ and the parameter λ with $\lambda_{\overline{f}} = q/p \cdot \overline{A}_{\overline{f}}/A_{\overline{f}}$.

2.10 Advantages of neutral B meson system

Searching for violations of the $\mathcal{CP}$ symmetry, the neutral B meson system offers several advantages:

- B mesons (B^+, B^-, B^0, $\overline{B}^0$) are composed of a heavy b quark and either a light u or light d quark. Theoretical calculations are simpler for those mesons consisting of a heavy and a light quark compared to mesons which consist of two quarks with the same mass.
- B mesons oscillate ($B \leftrightarrow \overline{B}$) in time with low frequency, see Fig. 2.13. Thus, time dependent effects of the $\mathcal{CP}$ violation can be studied by analyzing the decays of the B mesons in electron-positron colliders.
- B mesons can be exclusively produced in a very clean environment at the $\Upsilon(4S)$ state with electron-positron colliders. B mesons can be also produced in hadron colliders together with many hadrons, which results in a non-clean environment. The electron-positron and hadron colliders are discussed in more detail in Sect. 2.12.

[13] A detailed calculation for neutral mesons in general is performed in app. A.7.

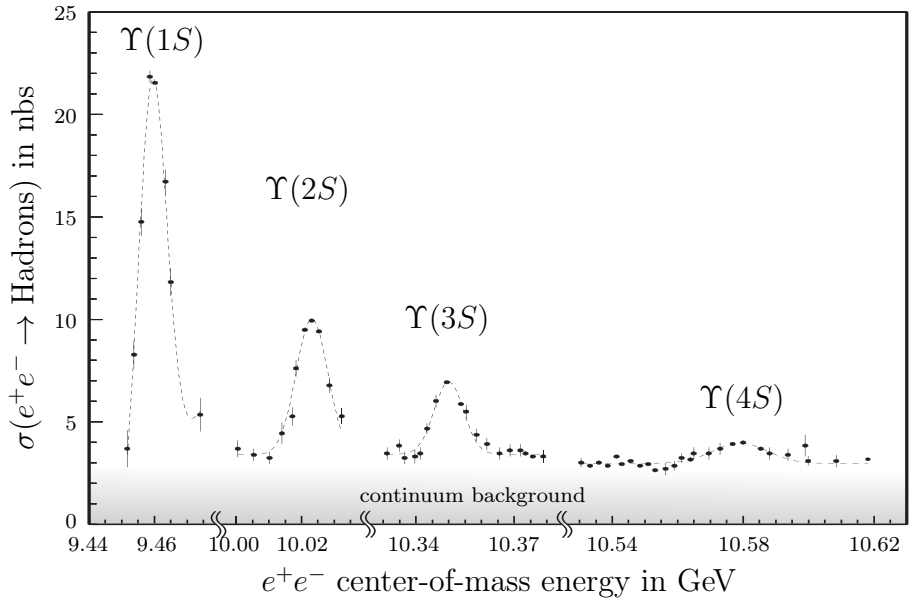


Figure 2.21: Hadronic cross-section for e^+e^- collisions as function of the e^+e^- center-of-mass [50] energy.

2.11 Production of B Mesons and Measurements of $\mathcal{CP}$ violation

2.11.1 Production of B Mesons

The Upsilon (Υ) resonances are states of the bound $b\bar{b}$ quarkonium (see Fig. 2.21). A quarkonium state is a meson, which consists of a quark and its antiquark ($q\overline{q}$). In comparison to the $\Upsilon(4S)$ state, the three resonances, the ground state $\Upsilon(1S)$ and the first two radially excited states $\Upsilon(2S), \Upsilon(3S)$, have too little energy to create a pair of free B mesons. The mass of the charged B meson is $5279.26\,\mathrm{MeV}/c^2$, whereas the mass of the neutral B meson is $5279.58\,\mathrm{MeV}/c^2$ [32].
The third radially excited state ($\Upsilon(4S)$) has sufficient energy to create a B meson pair (see Fig. 2.22). In the energy ranges of the Υ resonances, there is a continuum background, $e^-e^+ \to q\overline{q}$, where q can be an up, down, strange or charm quark. The ratio of the continuum to the resonance for the $\Upsilon(4S)$ is $3:1$ [50].
The $\Upsilon(4S)$, being produced in electron-positron annihilation, has the quantum numbers of the photon $J^{\mathcal{PC}} = 1^{--}$. Due to the conservation of the angular momentum, the two produced B mesons ($J^{\mathcal{P}} = 0^-$) must be in a P-wave ($L = 1$)[14] [48]. Producing B mesons at the $\Upsilon(4S)$ resonance has several advantages. The $\Upsilon(4S)$ resonance decays mostly into $B\overline{B}$ pairs ($> 96\,\%$) with almost equal branching ratios $\Gamma(B^+B^-)/\Gamma(B^0\overline{B}^0) \approx 1.06 \pm 0.03$ [32]. The events are clean since only a single pair of B mesons is produced in one event ($\Upsilon(4S) \to B\overline{B}$). The two B mesons can never have the same flavor simultaneously, i.e., the states B^0B^0 or $\overline{B}^0\overline{B}^0$ never

[14] (The total angular momentum of the $\Upsilon(4S)$ resonance is $J = 1$. The B mesons have both spin $S = 0$. To conserve the total angular momentum $J = L + S$, the orbital momentum of the created $B\overline{B}$ pair must be $L = 1$, which corresponds to a P-wave.

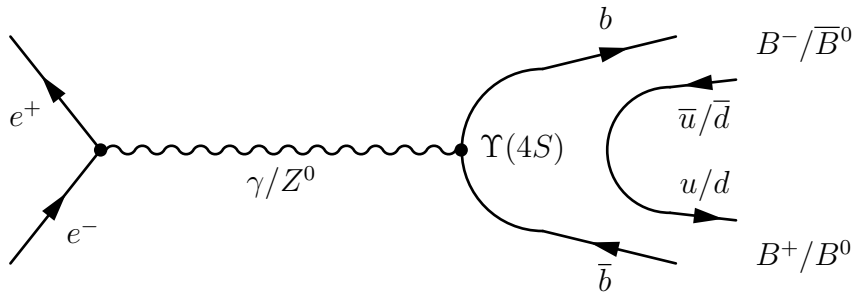


Figure 2.22: The $B\overline{B}$ production at the $\Upsilon(4S)$ resonance by electron-positron annihilation.

occur as long as one of them does not decay according to Bose-Einstein statistics. However, the flavors of the B mesons can oscillate as they evolve in time. B_1^0 and B_2^0 denote the two created neutral B mesons, which are in an orthogonal state. Then, the overall state is described by the anti-symmetric wave function Ψ of the quantum-entangled $B\overline{B}$ pair:

$$|\,\Psi(t_1,t_2)\rangle = \frac{1}{\sqrt{2}}\big(|B_1^0(t_1)\rangle|\overline{B}_2^0(t_2)\rangle - |\overline{B}_1^0(t_1)\rangle|B_2^0(t_2)\rangle\big) \tag{2.11.1}$$

The life-time of the neutral B mesons is approximately 1.52 ps [32]. Consider the case when one B meson decays into a $\mathcal{CP}$ eigenstate (called $B_{\mathcal{CP}}$) and the other B meson (called B_{tag}) decays first.

The first neutral B meson decays[15] at time t_1. Assuming this is identified with $\overline{B}^0$ ($\bar{d}b$) at time $t_1 = t_{\text{tag}}$, the other neutral B meson must be a B^0 ($d\bar{b}$) at t_1 and vice versa. Thus, the second B meson can freely oscillate, i.e., evolve in time until it decays at $t_2 = t_{\mathcal{CP}}$.

The time difference $\Delta t = t_{\mathcal{CP}} - t_{\text{tag}}$ and the information about the flavor of B_{tag} is used in order to obtain the $\mathcal{CP}$ parameters describing their asymmetry.

The probability density function $\mathcal{P}(\Delta t, \tilde{q})$ to find a $\mathcal{CP}$ eigenstate at the time difference Δt, depending on the flavor of the tagged B meson ($B_{\text{tag}} = B^0 \Rightarrow \tilde{q} = +1$, $B_{\text{tag}} = \overline{B}^0 \Rightarrow \tilde{q} = -1$), is given as[16]:

$$\mathcal{P}(\Delta t, \tilde{q}) = \frac{e^{-\Gamma|\Delta t|}}{4\tau_{B^0}}\Big[1 + \tilde{q}\big[\mathcal{A}_{\mathcal{CP}}\cos(\Delta m \Delta t) + \mathcal{S}_{\mathcal{CP}}\sin(\Delta m \Delta t)\big]\Big] \tag{2.11.2}$$

Figure 2.23 shows the probabilities for different arbitrily chosen values $\mathcal{A}_{\mathcal{CP}}$ and $\mathcal{S}_{\mathcal{CP}}$, which results in an $\mathcal{CP}$ asymmetry $a_{\mathcal{CP}}$ (see eq. (2.9.5)). The B mesons (created in the $\Upsilon(4S)$ decay) have a very small momentum of approximately 300 MeV/c in the laboratory frame [51]. The key feature of the B factories is to have asymmetric beam energies ($E_{e^+} \neq E_{e^-}$) in order to give the created particles a boost $\beta\gamma$. Due to this boost, the measurement of the time difference of the decays (Δt) is translated into a difference in decay lengths Δz. On average, the difference in

[15] Here B_{tag} is assumed to decay first ($t_{\text{tag}} < t_{\mathcal{CP}}$) but the discussion is also valid when $B_{\mathcal{CP}}$ decays first ($t_{\mathcal{CP}} < t_{\text{tag}}$).

[16] The derivation is discussed in detail in app. A.8.

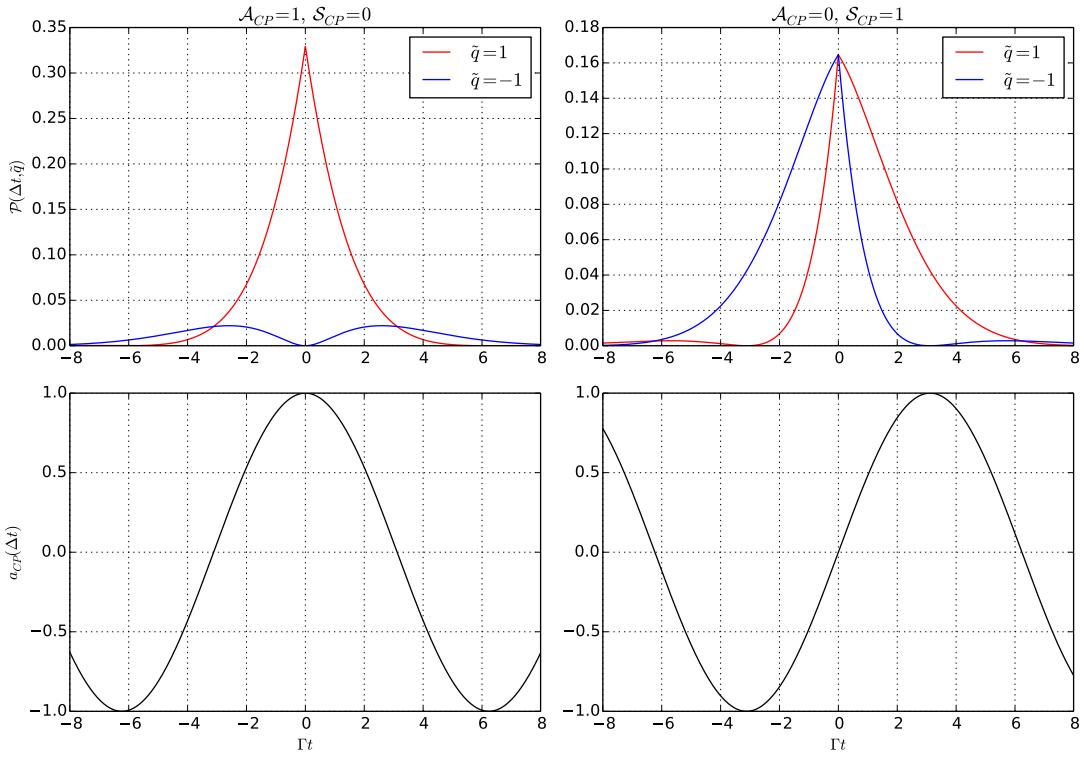


Figure 2.23: Upper part: Probabilitiy density and asymmetry for $B^0\overline{B}^0$ mesons, $\Gamma \approx 0.658$, $\Delta m \approx 0.504$; Lower Part: Asymmetry function, compare to eq. (2.9.5).

decay lengths is:

$$\Delta z = \Delta t \beta\gamma c \tag{2.11.3}$$

where $\gamma = \frac{1}{\sqrt{1-\beta^2}}$ is the Lorentz factor, c is the speed of light and $\beta = \frac{v}{c}$. In the KEKB collider, the beam energy for the electrons was 8 GeV and the beam energy for the positrons was 3.5 GeV [51]. The corresponding boost is:

$$\beta\gamma = \frac{E_{e^-} - E_{|e^+}}{\sqrt{s}} = \frac{E_{e^-} - E_{e^+}}{\sqrt{4E_{e^-}E_{e^+}}} = \frac{(8 - 3.5)\,\text{GeV}}{10.58\,\text{GeV}} = 0.42, \tag{2.11.4}$$

where s denotes the center-of-mass energy. Hence, the average decay length difference (for $\Delta t \approx 1.5$ ps) is around 188 µm. In contrast to its predecessor, SuperKEKB has beam energies of $E_{e^+} = 4.0$ GeV and $E_{e^-} = 7.0$ GeV (see Sect. 3.2.6), corresponding to a boost of $\beta\gamma = 0.28$. The decay length difference is reduced, resulting in an average of around 125 µm (see Fig. 2.24). In order to resolve the small decay length difference, a high resolution vertex detector is required. Detailed discussions about the requirements of the vertex detector will be discussed in Sect. 4.1.

2.11.2 Previous Measurements

The experiments BaBar (at PEP-II) and Belle (at KEKB) analyzed the decay products and the properties of the created B mesons. The achievements of the

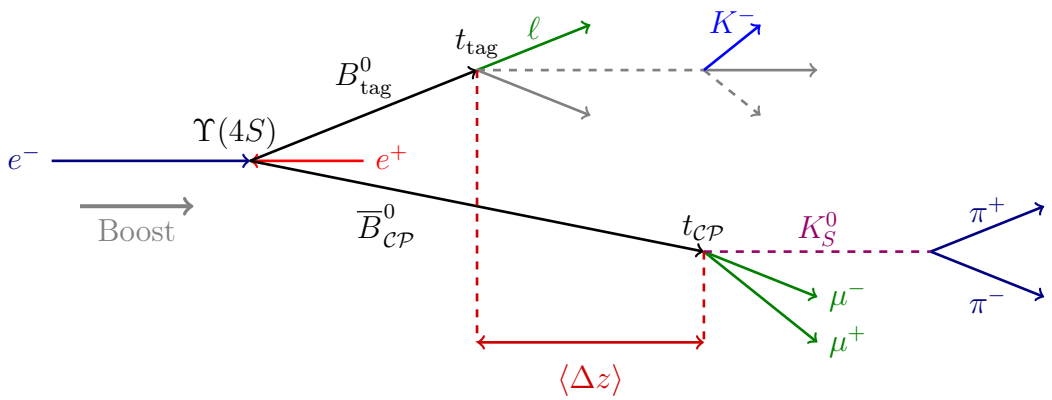


Figure 2.24: Production of two neutral B mesons at the $\Upsilon(4S)$ resonance. ${B^0}_{\text{tag}}$ and ${\overline{B}^0}_{\mathcal{CP}}$ are entangled until the decay at t_{tag}. The time difference Δt is translated to a length difference, which for SuperKEKB is $\Delta z \approx 125\,\mu\text{m}$ on average.

experiments include: the measurements of the angles in the unitarity triangle, the V_{cb} and V_{ub} CKM matrix elements, the study of leptonic and semileptonic B meson decays, precise measurements of D^0 mixing, τ physics, B physics at the Υ(5S), two-photon physics and new resonances [52].
Table 2.3 shows four decay channels which allows the determination of the three angles and the two sides of the unitarity triangle. The present status of the measurements of the parameters of the unitarity triangle is shown in Fig. 2.25.

Table 2.3: Decay channels to measure the angles β, α and γ.

β	$B^0 \to J/\psi K^0_S$, $B^0 \to \eta_C K^0_S$,	$B^0 \to J/\psi K^0_L$, $B^0 \to J/\psi K^{*0}$	$B^0 \to \Psi(2S) K^0_S$,	$B^0 \to \chi_{1C} K^0_L$,
α	$B \to \pi^+\pi^-$,	$B \to \rho\pi^-$,	$B \to \rho\rho$	
γ	$B \to D^{(*)}K^{(*)}$,	$B^0 \to D^- K^0 \pi^+$,	$B^0 \to D^{(*)}\pi$,	$B^0 \to D^{(*)}\rho$
$\left\lvert\frac{V_{ud}V^*_{ub}}{V_{cd}V^*_{cb}}\right\rvert$	$B \to \pi\ell\nu$,	$B \to X_u\ell\nu$,	$B \to \rho\ell\nu$	
$\left\lvert\frac{V_{td}V^*_{tb}}{V_{cd}V^*_{cb}}\right\rvert$	$B \to D^{(*)}\ell\nu$,	$B \to DX\ell\nu$,	$B \to \rho\ell\nu$,	$B \to D^*\ell\nu$

- The angles β and α are measured using the decay channels of the neutral B mesons ($B^0\overline{B}^0$) shown in Tab. 2.3. The angle γ is measured using the decay channels of charged B mesons (B^+B^-). In order to calculate the sides of the triangle, the branching ratios of the corresponding semileptonic decays need to be measured.
- The *Golden channel* for measuring the $\mathcal{CP}$ asymmetry is the decay channel of the neutral B mesons $B^0 \to J/\psi K^0_S$, (where the amplitude of the asymmetry is directly related to $\sin(2\beta)$). It is called "Golden channel" because the branching ratio is large and has a clean low background signature. It provides a clean environment to measure β of the unitarity triangle.

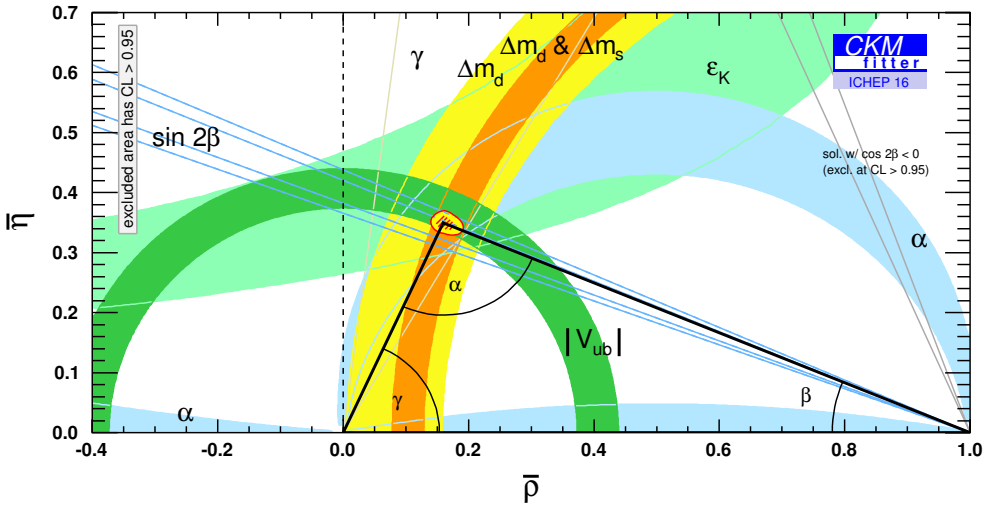


Figure 2.25: Constraints on the unitarity triangle in the complex plane [53].

2.11.3 Physics beyond the Standard Model and future Measurements

The SM is well verified by all experimental tests. It is a very sophisticated model that accurately describes the interactions of the elementary particles. However, there are several open issues which cannot be explained, resulting in an incomplete description of reality.

- **Mass:** Mass and gravity are not described in the SM. The gravity is not included. The masses enter as free parameters of the SM.
- **Three generations:** The SM includes three generations (also called families) and three fundamental forces (compare with Fig. 2.1). These particles were partially theoretically predicted and had been observed. The SM does not explain why there are exactly three families. There could be even more.
- **Many free parameters:** The SM has 19 free parameters, which can only be determined by experimental measurements. Those parameters include the masses of the six quarks and three leptons (electron, muon and tau), three mixing angles, the $\mathcal{CP}$ violating phase (see Sect. 2.3), three gauge couplings, the QCD vacuum angle, the Higgs vacuum expectation value and the Higgs mass. Adding the mixing angles and masses of the neutrinos further increases the number of parameters.
- **Matter-Antimatter asymmetry in the universe:** The $\mathcal{CP}$ violation has been discovered in the neutral kaon system by Cronin and Fitch in 1964 [15]. $\mathcal{CP}$ violation can only be explained in the SM if the CKM matrix, introduced by Kobayashi and Maskawa, includes a complex phase (compare to Sect. 2.3). The universe is dominated by matter over antimatter. Although the $\mathcal{CP}$ violation is one of three necessary conditions for the evolution of a matter-dominated universe [14], the complex phase of the CKM matrix

(which allows $\mathcal{CP}$ violation) is orders of magnitudes too small to explain the matter-dominance.

- **Dark matter and dark energy:** Dark matter and dark energy are not described in the SM. According to the measurements of Wilkinson Microwave Anisotropy Probe (WMAP), only about 5 % of the universe's entire energy is of baryonic origin [54]. The rest is a composition of dark energy and dark matter which has not been observed so far.
- **Interaction strength:** There does not exist any information about the strength of the weak and strong interaction. For instance, the strong interaction is around 10^{32} stronger compared to the weak interaction (summarized in Tab. 2.1). There is no theory that provides a suitable explanation.
- **Unification:** The weak and EM interactions could be unified to the electroweak interaction, mathematically expressed by the SU(2) × U(1) symmetry groups. In contrast, the strong and the electroweak interactions are not (yet) unified. Starting in 1974, the grand unified theory (GUT) tries to unify them [55, 56]. The experimental verification requires very high energies (10^{24} eV), at which the strength of the different interactions would be approximately the same and thus be unified. Since those large energies are technically not feasible to reach with particle accelerators (to date), another approach is to study the decay of protons (which has not been observed yet).

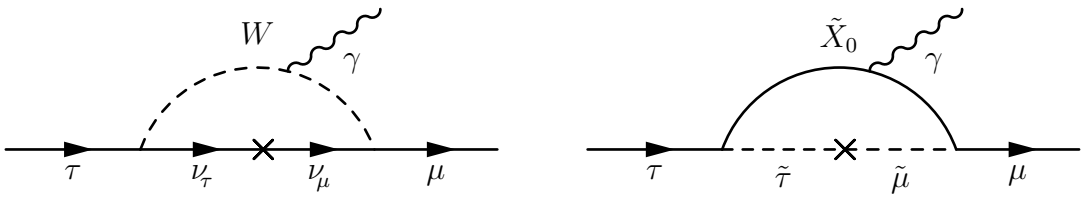
Future experiments seek to give answers to those questions. There are two approaches:

1. One approach is to operate at the energy frontier of the LHC with the ATLAS [57] and CMS [58] experiments. The masses of undiscovered particles are assumed to be quite large. Even the upgrades of the LHC do not reach the energy scales needed to directly produce those particles. B mesons are also produced in pp collisions. They are studied in the LHCb experiment (see Sect. 2.12).
2. Another approach is the luminosity frontier (including LHCb), operated by B factories, like the SuperKEKB with its Belle II detector (there were also other facilities like BaBar). At low energies, New Physics could manifest in form of signatures of new processes (by virtual effects) in flavor physics that deviate from the Standard Model.

Both approaches are complementary. More details are given in Sect. 2.12.
The Belle II New Physics discovery potentials are:

- New Physics could be found if the precise measurements lead to a non-closing unitarity triangle.
- Taking minimal flavor-violating New Physics (NP) with weak couplings to the fermions, new particles below 100 GeV could be found (e.g. see [59]). The weak coupling to fermions are in the order of the weak gauge couplings.
- The lepton flavor violating τ decays are interesting because they are sensitive to NP. The process of the charged lepton flavor violation is highly suppressed

in the SM by approximately 10^{-54}. The change of the flavor in leptons can occur due to the mass of neutrinos. The upper limit from Belle for the processes $\tau \to \mu\gamma$, $\tau \to \mu\mu\mu$ and $\tau \to \mu\eta$ are of order 10^{-8}, while in the successor Belle II experiment it will be of order 10^{-9}. The observation of the charged current flavor violation would be a clear hint to NP beyond the SM. A new virtual particle in the loop could occur. Feynman graphs for the transition in and beyond the Standard Model are shown in Fig. 2.26.



(a) Feynman diagram for $\tau \to \mu\gamma$ in the Standard Model, which is suppressed by 10^{-54}.

(b) Feynman diagram for $\tau \to \mu\gamma$ beyond the Standard Model.

Figure 2.26: Charged lepton flavor violation from a tauon to a muon. The observation would be a clear indication to New Physics.

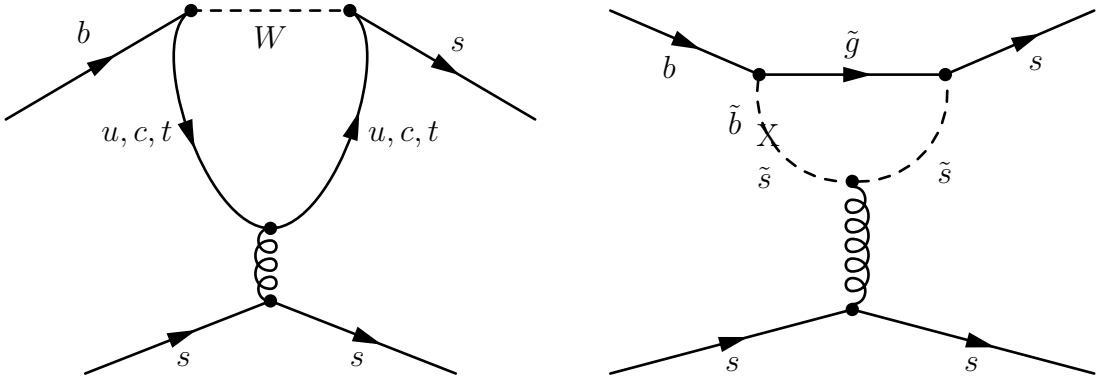
- B mesons also decay into tauons ($B \to D^*\tau\nu_\tau$). The masses of the quarks, leptons and gauge bosons are acquired by the Higgs mechanism. Since the tauon is the heaviest lepton, it is assumed to couple stronger to the Higgs field compared to the electron and muon. Electrical neutral and charged Higgs bosons theoretically exist in extensions of the SM (the two Higgs doublet models). Since the B meson and the decay products include heavy quarks, this decay channel may be sensitive to measure Higgs effects. The ratio of the branching fractions

$$\mathcal{R}(D^{(*)}) = \frac{\Gamma(B \to D^{(*)}\tau\nu_\tau)}{\Gamma(B \to D^{(*)}\ell\nu)}$$

  with $\ell = e, \mu$ can be calculated quite precisely in the SM. However, measured branching fractions (in Belle and BaBar) exceed predictions in the SM by 3.4σ [60]. The Belle II experiment will contribute resolving this tension.

- There are tensions in the measurements of the angle β in the unitary triangle. Measurements of the decay $B \to J/\psi K_S^0$ and from the penguin process $b \to sq\overline{q}$ show differences up to 3σ [61, 62]. This could be due to a new $\mathcal{CP}$ phase. Belle II will resolve those discrepancies.

- New, yet undiscovered particles could be found that are involved in internal loops such as in FCNCs [63] (see Fig. 2.27). They only exist beyond the tree level in the SM and are strongly suppressed by the GIM mechanism (see Fig. 2.27a). The FCNCs can be studied in Belle II by analyzing hadronic decays ($b \to sq\overline{q}$), radiative decays ($b \to s\gamma$), and semileptonic decays ($b \to s\ell^+\ell^-$). The b quark is the third quark generation (see Fig. 2.1); there could be physical processes which include the other two quark generations. Hence,



(a) "Penguin" diagram illustrates the down-type quark transition in the SM beyond the tree level.

(b) Transition of the quark in physical processes beyond the SM. This changes the observables, such as the angles in the unitarity triangle.

Figure 2.27: Transition from $b \to s$ in the Standard Model and beyond.

NP contributions could be found in highly suppressed penguin decays in the SM. For instance, new virtual particles could occur in these processes that extend the SM.

The new SuperKEKB factory will deliver a luminosity 50 times larger than its predecessor, KEKB. This will substantially improve the precision of the measurements and allow the observation of highly suppressed physical processes, opening a new window on the search of New Physics in the flavor sector.

2.12 LHCb and Belle II

B mesons can be produced in large numbers either by hadronic collisions at very high energies or by electron-positron collisions with a defined center-of-mass energy at the production threshold 10.58 GeV.
The LHCb experiment [64], located at the LHC at CERN, is dedicated to the study of b hadrons, $\mathcal{CP}$ violation and rare decays of B_d, B_s and D mesons. In the LHC, the protons collide at the center-of-mass energy of 13 TeV with a large $b\bar{b}$ production cross-section of approximately 500 µb. This production cross-section is much larger compared to SuperKEKB ($\sim$ 1 nb). Thus, more statistics allow gaining more information about rare decays.
The luminosity is reduced (by adjusting the beam focus at the interaction point) to lower the detector occupancy and simplify the reconstruction of the events. Single proton-proton interactions per bunch crossing are favorable. The large amount of additionally produced particles (*underlying event*) complicate the reconstruction of the $B\overline{B}$ pairs (tagging). An efficient trigger is required to select the events containing B mesons. The trigger efficiency is 0.1–10 % depending on the decay channel [65].

At the LHC, $b\bar{b}$ production is mainly due to gluon-gluon fusion, which are emitted from the quarks within the colliding protons. In general, the energies of the two colliding gluons are different so that the $B\overline{B}$ system is boosted either in the forward or backward direction [66]. The LHCb detector only covers the forward region. Consequently, only approximately 35 % of all produced $b\bar{b}$ pairs are covered by the LHCb detector [65]. Neutral final states (e.g., containing neutrinos or photons) are difficult to study due the large amount of additionally produced particles. However, the enormous boost results in an excellent spatial resolution; the flight distance of the B mesons is approximately 1 cm which corresponds to a decay-time resolution of ~ 50 fs [65]. Thus, the time-dependent $\mathcal{CP}$ violation in the B_s system (with a high flavor changing oscillation frequency) can be investigated precisely.
In conclusion, the advantages of the LHCb are the huge cross-section, the high resolution of the decay-time and the time-dependent analysis of the high frequent oscillating B_s mesons and other hadrons containing b quarks.
For the Belle II detector at SuperKEKB, on the other hand, the center-of-mass energy is well-known (10.58 GeV). A clean environment with low background is provided since the $\Upsilon(4S)$ resonance decays into two B mesons only. Missing energy modes can be reconstructed using the other (tag) B meson, for instance, the leptonic decay $B \to \tau\nu$ or even invisible B decays ($B \to \nu\overline{\nu}$) can be studied.
Both approaches, the LHCb and the Belle II experiments, are therefore complementary in the search for New Physics beyond the Standard Model.

Chapter 3

SuperKEKB and Belle II

3.1 Motivation

B factories are electron positron colliders which operate at the $\Upsilon(4S)$ resonance (at 10.58 GeV). This energy is slightly above the threshold to create pairs of B mesons. Examples are the PEP-II accelerator at SLAC and the accelerator KEKB, built in the 1990s.

The experiments BaBar (at SLAC) and the predecessor experiment of Belle II, the Belle detector, analyze the decay products and the properties of the B mesons. Both experiments proved the correctness of the Kobayashi-Maskawa theory and thus contributed significantly to their Nobel prize award. The experiments furthermore are credited with many physical achievements, such as the measurements on D^0 mixing, τ physics, B physics at the Υ(5S), two-photon physics and exotic hadron resonances [52].

The 50 times larger amount of data samples expected by SuperKEKB allows increasing the precision of the measurements and also reducing the systematical uncertainties. Furthermore, new measurements of flavor physics processes beyond the SM could emerge, such as FCNCs. In the SM, the FCNCs are not allowed at tree level, but they can occur via loop diagrams which are strongly suppressed. In addition, new elementary particles, such as charged Higgs bosons, could be detected. The sensitivity to New Physics beyond the Standard Model and the indirect observation of new particles in quantum loops depends on the size of the data sample, i.e., the luminosity of the accelerator and the detector performance.

This chapter starts with a short introduction to the KEKB and SuperKEKB accelerators. The nano-beam scheme, which allows for the tremendous increase of luminosity, will be described. Furthermore, the generation of the electrons and positrons, the beam optics and the injection scheme are discussed. The schedule for the commissioning of the accelerator is briefly given. In the next section, the upgrade of the various sub-detectors of the Belle II detector and the interaction region are presented.

3.2 SuperKEKB

3.2.1 Particle Accelerator

KEKB was an asymmetric electron positron collider with two storage rings, the high energy ring (HER) for electrons and low energy ring (LER) for positrons, located at the KEK accelerator center in Tsukuba Japan. It operated for more than ten years, from December 1998 until June 2010 [67, 68]. It achieved the world-record peak luminosity of $2.108 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ and integrated luminosity of $1041\,\mathrm{fb}^{-1}$.
The center-of-mass energy chosen was primarily ($711\,\mathrm{fb}^{-1}$) $10.58\,\mathrm{GeV}$, corresponding to the $\Upsilon(4S)$ resonance [69, 70]. This resonance is the lightest state of two bound bottom quarks decaying into two B mesons. The groundbreaking ceremony of the upgrade project, SuperKEKB, was on November 18, 2011. SuperKEKB aims at a target instantaneous luminosity of $\mathcal{L} = 8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ covering the energy spectrum of the Υ(1S) to the Υ(6S) resonances [71]. To achieve this, the nano-beam scheme was used. The first stored and circulating positron and electron beams were achieved on February 10, 2016 and on February 26, 2016, respectively [72]. A sketch of SuperKEKB is shown in Fig. 3.1. The coordinate system used in this chapter is also shown in Fig. 3.1. The z-axis is the bisector of the electron and the positron beam directions. The x-axis is perpendicular to the motion of the particles pointing "outward". The y-axis is orthogonal to the x- and z-axes.

3.2.2 Luminosity and nano-beam scheme

Colliding two beams head-on and analyzing the resulting products is very challenging. The density of particle beams is very low (compared to solid states), therefore direct collisions are rather rare. The number of collisions per second ($\frac{\mathrm{d}N}{\mathrm{d}t}$)is expressed by

$$\frac{\mathrm{d}N}{\mathrm{d}t} = \sigma_\mathrm{p} \cdot \mathcal{L} \tag{3.2.1}$$

where σ_p denotes the cross-section of particles and $\mathcal{L}$ the luminosity[1], which indicates the probability of the particle collisions of the two opposite beams. It is calculated as [73]:

$$\mathcal{L} = \frac{N_{e^+} N_{e^-} f_\mathrm{c}}{4\pi\sigma_x\sigma_y} R_\mathrm{L} \tag{3.2.2}$$

where N_{e^+} and N_{e^-} denote the number of positrons and electrons respectively, f_c is the collision frequency, $\sigma_{x,y}$ are the root mean squares (RMS) values of the transverse beam shapes and R_L is the luminosity reduction factor (the derivation is given in [74]).
Equation (3.2.2) states that the luminosity can be increased by adding more particles (N) to the bunches, increasing the collision frequency (f_c) and decreasing the size of the beams (σ_x, σ_y).

[1] The performance of a particle collider is measured by the luminosity.

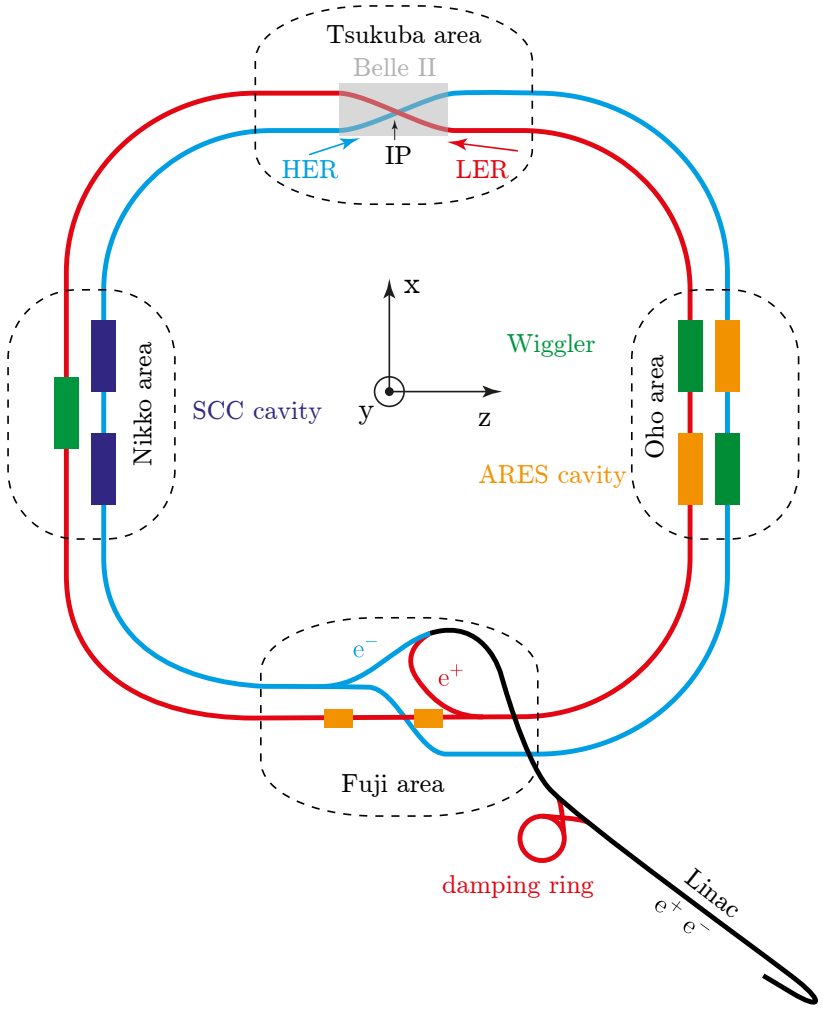


Figure 3.1: SuperKEKB e^+e^- collider. It consists of the linear accelerator (linac) for particle injection, an additional damping ring for the positrons and two independent storage rings for the two types of charged particles. The beams collide at the IP in the Tsukuba hall.

The number of events collected over a certain time interval $[t_0, T]$ is given by

$$N = \sigma_{\mathrm{p}} \int_{t_0}^{T} \mathcal{L} \, \mathrm{d}t' = \sigma_{\mathrm{p}} \cdot \mathcal{L}_{\mathrm{int}} \tag{3.2.3}$$

where the expression $\mathcal{L}_{\mathrm{int}} = \int_{t_0}^{T} \mathcal{L} \, \mathrm{d}t'$ is called *integrated luminosity*.

The instantaneous luminosity can be also written as:

$$\mathcal{L} = \frac{\gamma_{e^\pm}}{2er_e} \left(1 + \frac{\sigma_y}{\sigma_x}\right) \left(\frac{I_{e^\pm} \xi_{y,e^\pm}}{\beta_y}\right) \left(\frac{R_{\mathrm{L}}}{R_{\xi_{x,y}}}\right) \tag{3.2.4}$$

where $\gamma_{e^\pm}$ denotes the Lorentz factor of the beam particles, e the elementary charge, r_e the classical electron radius, $\sigma_{x,y}$ the beam size, $I_{e^\pm}$ the electron and positron beam current, β_y the vertical beta function at the IP, R_{L}/R_{ξ_y} the ratio

of the luminosity reduction factor and the tune shift reduction factor, and $\xi_{y,e^\pm}$ is the beam-beam tune shift parameter in x- and y-direction, given by:

$$\xi_{x,y,e^\pm} = \frac{r_e}{2\pi\gamma_{e^\pm}} \frac{N_{e^\pm}\beta_{e^\pm,x,y}}{\sigma_{x,y}(\sigma_x + \sigma_y)} R_{\xi_{x,y}} \tag{3.2.5}$$

where $\beta_{e^\pm,x,y}$ denotes the betatron function in x and y. The beam-beam parameter describes the betatron tune shift of the bunch center. It is caused by the focusing force of the other beam [75]. The luminosity reduction factor R_L is given by [76]:

$$R_\mathrm{L} = \frac{\beta_y}{\sigma_z\sqrt{\pi}} \exp\left(\frac{\beta_y^2}{2\sigma_z^2}\left[1 + \left(\frac{\sigma_z}{\sigma_x}\tan\frac{\Theta_c}{2}\right)^2\right]\right) K_0\left(\frac{\beta_y^2}{2\sigma_z^2}\left[1 + \left(\frac{\sigma_z}{\sigma_x}\tan\frac{\Theta_c}{2}\right)^2\right]\right) \tag{3.2.6}$$

where σ_z is the bunch length, Θ_c is the crossing angle, shown in Fig. 3.2, and K_0 is the Bessel function. Moreover, the beam-beam parameter is expressed by [76]:

$$R_{\xi_y} = \int \mathrm{d}z' \rho(z') \sqrt{1 + \left(\frac{S}{\beta_y}\right)^2} f_y\left(z' \tan\frac{\Theta_c}{2}, \sigma_x(S), \sigma_y(S)\right) \tag{3.2.7}$$

where $S = (z^* - z')/2$, z^* is a coordinate after a Lorentz transformation to the head-on collision, ρ is the density distribution in z-direction and f_y is the Montague's function [77].
The luminosity reduction factor is mainly due to the beam-beam interactions and the finite crossing angle, Θ_c, (bunches do not collide head-on, hence the geometric overlap is reduced). A particle bunch circulating in beam pipes creates EM fields which act on the opposite, colliding bunch. This effect is known as *beam-beam* interaction. A large crossing-angle of the two beams of 83 mrad is used to prevent multiple beam-beam interactions. The beams should only collide at the IP. Furthermore, geometrical effects also contribute the luminosity reduction. If the betatron functions, β_x and β_y, are smaller compared to the bunch length σ_z, the luminosity decreases due to the variations of the transverse beam size along the bunch. This is known as the *hourglass effect* [78].

A flat ($\sigma_y \ll \sigma_x$) beam is chosen in the accelerator plane due to physical feasibility (synchrotron radiation), although the luminosity would be increased by round beams according to eq. (3.2.4). Since $\sigma_y \ll \sigma_x$, the luminosity (eq. (3.2.4)) can be rewritten as:

$$\mathcal{L} \approx \frac{\gamma}{2er_e}\left(\frac{I\xi_y}{\beta_y}\right)\left(\frac{R_\mathrm{L}}{R_{\xi_y}}\right) \tag{3.2.8}$$

In order to achieve a high luminosity, according to eq. (3.2.8), the beam currents must be large, the beam-beam parameter ξ_y must be large and the vertical β_y function at the IP is required to be small. The transverse beam size $\sigma_{x,y}$ depends on the betatron function ($\beta_{x,y}$) and the emittance ($\varepsilon_{x,y}$) (which is introduced in Sect. 3.2.4):

$$\sigma_{x,y} = \sqrt{\beta_{x,y}\ \varepsilon_{x,y}} \tag{3.2.9}$$

The basic idea of the *nano-beam* scheme, proposed in [79], is to have small emittance, a small betatron function at the IP compared to the length of the bunch, i.e., $\beta_y \ll \sigma_z$ and a very large Piwinksi angle, which is defined by:

$$\Phi = \frac{\Theta_c \sigma_z}{\sigma_x} \tag{3.2.10}$$

For SuperKEKB, the bunch length is approximately 5–6 mm and the transverse sizes are approximately 10 µm × 50 nm. According to Fig. 3.2, the beam overlap is determined by $d \sim \frac{\sigma_x}{2\Theta_c}$, not by σ_z. Moreover, in order to avoid the hourglass effect, the requirements $\frac{\sigma_x}{2\Theta_c} \lesssim \beta_y$ and $\beta_y \geq \sigma_z$ must be fulfilled. The overlap region is approximately $\sigma_x / 2\Theta_c \sim 300\,\mu\text{m}$. For SuperKEKB, the betatron function β_y is chosen to be 0.30 mm, which increases the luminosity by roughly a factor of 20 [80]. Furthermore, the beam current is increased, resulting in an additional doubling of the instantaneous luminosity. Further increase of the beam current, by adding more particles, results in unstable beams due to intra-beam scattering (discussed in Sect. 3.2.5), transverse mode coupling instabilities and longitudinal microwave instabilities. Hence, it is around a factor of 40 larger compared to its predecessor, resulting in $\mathcal{L} = 8 \times 10^{35}\,\text{cm}^{-2}\,\text{s}^{-1}$. All of the machine parameters are listed in Tab. 3.1.

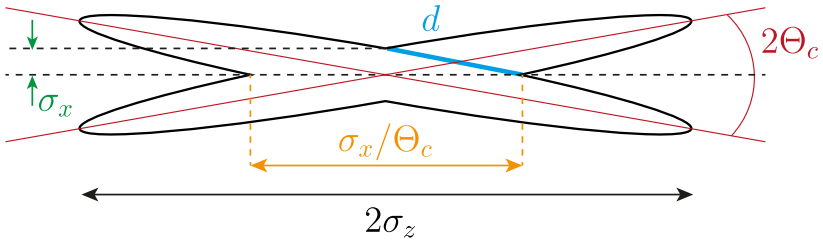


Figure 3.2: Electron and positron beam (bunch) crossing in the nano-beam scheme.

3.2.3 Particle Generation and Linac

SuperKEKB requires electron and positron bunches of high charge (5 nC for electrons and 4 nC for positrons [81]) and low emittance (see eq. (3.2.9)) – for electrons: 200 to 20 mm-mrad and for positrons: 2100 to 6 mm-mrad [82]) in order to achieve the high luminosity.

Electrons: An Ytterbium-doped laser generates 30 ps high-peaked energy pulses with a center wavelength of 259 nm [83, 84]. The pulses hit an Ir_5Ce photocathode (with a diameter of 6 mm) and create electrons by the photoelectric effect. Iridium cerium (Ir_5Ce) has been favored instead of Lanthanum hexaboride (LaB_6) due to its high emission (high quantum efficiency) and long lifetime. [82]. The generated electron bunches have a total charge of around 5 nC, corresponding to 3×10^{10} particles.
They are accelerated by a linear accelerator to 1.5 GeV, bent in the J-ARC and afterwards further accelerated to 7 GeV before they enter the HER (see Fig. 3.3). The gradient of the accelerating field must be more than 100 MeV/m in order to

Table 3.1: SuperKEKB machine parameters for the low energy ring (LER) and for the high energy ring (HER) [80].

	LER	HER	
Energy	4.0	7.0	GeV
Current	3.6	2.6	A
Number of bunches	2500		
Bunch Current	1.44	1.04	mA
Circumference	3016		m
Emittance ε_x	3.2(1.9)	4.6(4.4)	nm
Emittance ε_y	8.64(2.8)	12.9(1.5)	pm
Coupling	0.27	0.28	
Beta function β_x	32	25	mm
Beta function β_y	0.27	0.30	mm
Crossing angle ($2\Theta_c$)	83		mrad
Beam-beam parameter ξ_x	0.0028	0.0012	
Beam-beam parameter ξ_y	0.0881	0.0807	
Luminosity $\mathcal{L}$	8×10^{35}		$\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$

avoid beam expansion (i.e., higher emittance) by space charge effects for the low velocity regions [85].

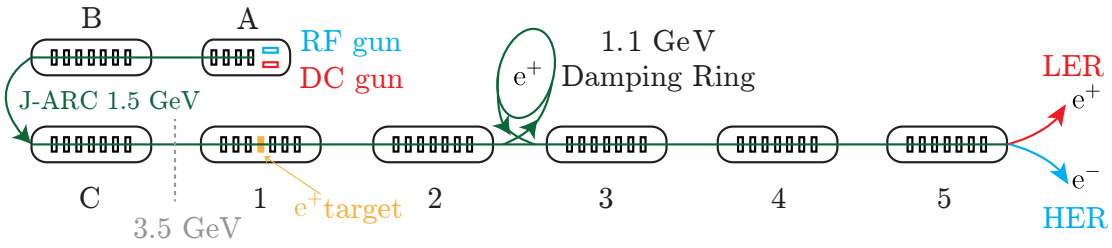


Figure 3.3: Injector of SuperKEKB. It consists of the low emittance RF gun and a DC gun for electron and positron beams. An additional damping ring for the positrons is necessary in order to reduce the emittance to a sufficient level. After additional acceleration, the bunches are injected into LER and HER.

Positrons: The positrons are generated as secondary particles. A highly-charged (10 nC) electron beam is accelerated to 3.5 GeV using a DC gun [81]. The electron bunches (to generate positrons) are accelerated within the same linac which is used for the electrons. The accelerated electron beam hits a 14 mm thick amorphous tungsten target and thus creates bremsstrahlung [86]. The resulting highly energetic photons convert into electron-positron pairs. A sketch is shown in Fig. 3.4. The electrons and positrons are separated in a chicane, which is an arrangement of solenoids creating large magnetic fields, also called *capture section*, to obtain a pure positron beam. The beam cannot be directly accelerated and injected into the LER due to the large emittance, which is not suitable for the nano-beam scheme. Therefore, an additional 1.1 GeV damping ring (DR) was built in order to cool

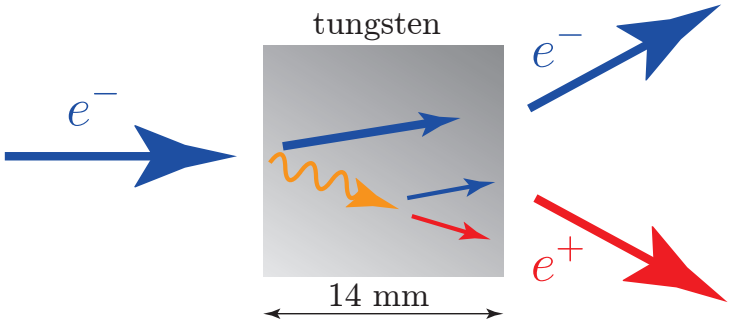


Figure 3.4: Sketch of the generation of positrons. The electron beam hits the amorphous tungsten target. The decelerated electrons create high energetic γ photons by bremsstrahlung. These interact with the nuclei in the target and create electron positron pairs, which are separated by a magnetic field afterwards.

down the transverse momentum component by synchrotron radiation; hence, the bunches decrease their emittance from 1700 nm to 42.5 nm, i.e., roughly a factor of 40, such that the positrons can be injected without significant loss into the storage ring [87]. Afterwards, the positron beam is re-injected into the main linac, further accelerated to 4 GeV and transferred into the LER.

Both particle bunches use the same linear accelerator before being injected into the LER and HER, respectively. They are accelerated alternately, which is discussed in Sect. 3.2.7. A sketch is shown in Fig. 3.3.

3.2.4 Storage Rings

SuperKEKB has two large independent storage rings for electrons and for positrons. In order to guide the particles, beam optics are required.

Beam Optics Having created electrons (or positrons) they need to be guided along a pre-defined trajectory in a clean and evacuated beam pipe to the IP surrounded by the Belle II detector. Therefore, it is necessary that there be:

- **Normal conducting dipole bending magnets** guide the particle bunches around the arcs. Passing particles are deflected by the Lorentz force and are guided to their predefined trajectory.
- **Focusing magnets / collimators** are used to focus the beam and counteract the forces which expand the bunches. Therefore, several quadrupole magnets are usually used in sequence [88]. All particles within an electron (or positron) bunch are affected by the magnetic forces. Hence, the electrons move towards the ideal design orbit and perform radial and transverse oscillations, called *betratron oscillations*.
- **Superconducting quadrupole magnets:** The superconducting final focus quadruple magnet system (QCS) consists of eight quadrupoles arranged in two quadrupole doublets, which are aligned on the beam line [89]. Figure 3.5 shows the arrangement. Two quadrupoles for each beam (LER and HER)

are installed on the left and right side of the IP as viewed from the center of the SuperKEKB accelerator ring. The quadrupole magnets are based on NbTi/Cu Rutherford type cable [89]. The magnet focusing system is cooled to 4.2 K in two horizontal cryostats (left and right of the IP) consisting of a liquid helium (LHe) vessel, which is thermally shielded by liquid nitrogen (LN_2) [89]. The quadrupoles QC1P and QC1E, which are closest to the IP, have an inner diameter of 25 mm (33 mm) and a magnetic length of 334 mm (373 mm). They create magnetic field gradients of 70 T/m [89]. The QC1E and QC2P have a permendur yoke, while the yoke of QC2E is iron. Iron is sufficient to reduce the leakage field to the positron beam line to a negligible value [90]. The QC1P does not have a yoke since the compensation solenoids integrally cancel the Belle II solenoid field [91].
The QCS is located inside the solenoid, which creates a uniform 1.5 T field. In order to counteract the deflection, compensation solenoids (ESL and ESR) are installed which guide the beam to the IP. In addition, each quadrupole is equipped with corrector coils to control the field precisely and compensate for the errors [89, 92]. The QCS focuses the bunches to 10 µm × 50 nm in the transverse direction at the IP.

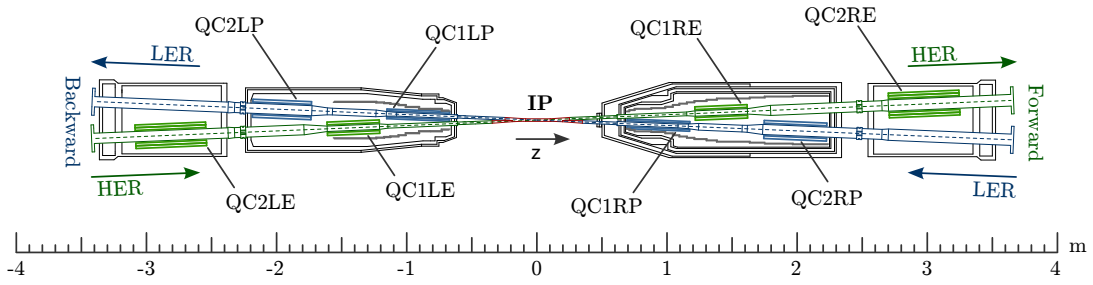


Figure 3.5: Interaction Region of SuperKEKB. The final focusing magnets, denoted by "QC⟨number⟩L/R PE" are installed around the interaction point [93].

- **RF Cavities** compensate for the beam energy loss by synchrotron radiation. The longitudinal electric fields within the cavities are used to adjust the energies of the incoming particles. Due to a proper phase adjustment between the electric field and the passing bunch, the bunch is longitudinally compressed, and the electrons (or positrons) start to oscillate in the longitudinal direction caused by the restoring force of the electric field. These are called *synchrotron oscillations*. One distinguishes between the two types of RF cavities as follows:
  SCC cavities: Eight Single-Cell superconducting Cavities (SCC) are placed in the HER [94, 95]. They are Pure-Niobium resonators, each with an RF voltage of approximately 1.5 MV.
  ARES cavities: Accelerator Resonantly coupled with Energy Storage (ARES) is a three-cavity system of high-purity copper resonators operated at around 0.5 MV [96, 97]. In total there are 22 ARES cavities placed in the LER and eight ARES cavities in the HER.

The time and spatial evolution of the beam under the influence of the devices mentioned above is called *beam optics*.

Emittance The emittance is defined as the occupied volume of the particle bunch in the transverse position-momentum phase space. The particle bunch is mathematically described by a second order homogeneous differential equation [74]:

$$\frac{\mathrm{d}^2 h}{\mathrm{d}s^2} + k(s)h(s) = 0 \tag{3.2.11}$$

where $h(s)$ is a function describing the transverse trajectory relative to the design orbit and $k(s)$ is the strength of the quadrupole focusing system, which fulfills the periodic relation $k(s) = k(s+u)$ with u being the size of the periodic magnetic lattice around the entire accelerator ring. The function $h(s)$ is an oscillation around the orbit depending on phase and position, which is called *betatron oscillation*. The derivation is given in [74]. The solution and its derivative are

$$h(s) = \sqrt{\varepsilon}\sqrt{\beta(s)}\cos\big(\Psi(s) + \Phi(s)\big) \tag{3.2.12}$$

$$h'(s) = -\frac{\sqrt{\varepsilon}}{\sqrt{\beta(s)}}\big[\alpha\cos(\Psi(s)+\Phi) + \sin(\Psi(s)+\Phi)\big] \tag{3.2.13}$$

where ε denotes the *emittance*, which is proportional to the area in the transverse phase space (see Fig. 3.6), $\beta(s)$ is the betatron function which describes the amplitude of the oscillation and $\Psi(s) = \int_0^s \frac{1}{\beta(t)}\mathrm{d}t$ is the betatron oscillation phase. $\sqrt{\varepsilon\beta(s)}$ and $\Phi(s)$ are determined by boundary conditions. Rewriting eq. (3.2.11) by defining $\gamma(s) := \frac{1+\alpha(s)}{\beta(s)}$ and $\alpha(s) := -\frac{\beta'(s)}{2}$, one obtains:

$$\gamma(s)h^2(s) + 2\alpha(s)h(s)h'(s) + \beta(s)h'^2(s) = \varepsilon \tag{3.2.14}$$

The mathematical derivations are given in app. B.1 and app. B.2. This equation is a rotated ellipse as shown in Fig. 3.6. Hence, the envelope of the particle trajectories (i.e., the width) is given by $\sigma(s) = \sqrt{\varepsilon\beta(s)}$, which is shown in Fig. 3.7. Moreover, the divergence of the beam is calculated by $\sigma'(s) = \sqrt{\frac{\varepsilon}{\beta(s)}}$.

Liouville Theorem Every phase space volume element (i.e., the phase space density) for a Hamiltonian system remains constant [98]. In classical mechanics, it is a fundamental theorem which has been adopted to quantum mechanics. Hence, the Liouville theorem is applicable if the interaction between the particles (such as EM interaction) is ignored [99]. If the particles behave according to the canonical equations of motion, the area of the ellipse in the phase space (see Fig. 3.6), which is proportional to the emittance, keeps constant over time. Hence, the beam emittance is an invariant of the particle movements along the accelerator orbit.
Taking the interactions between the particles such as intra-beam scattering and space charge effects within a bunch into account, this theorem is not valid any-

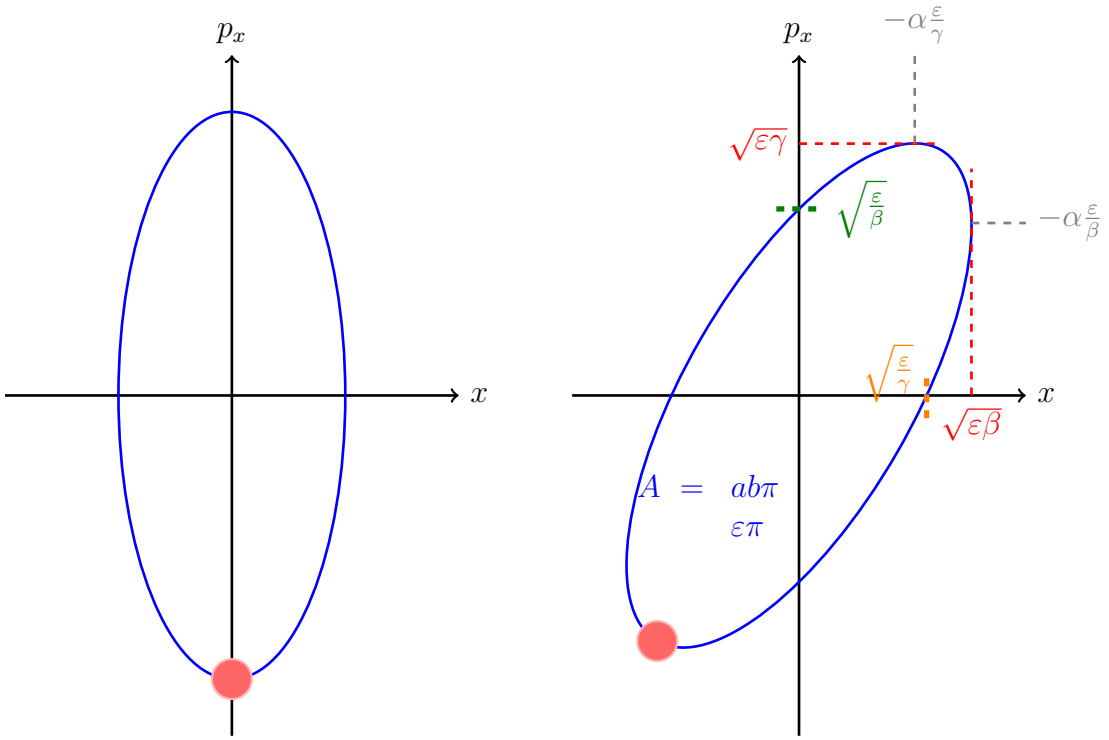


Figure 3.6: Time evolution of ellipse for particles in phase space in the $x - p_x$ (position-momentum) plane. The purple dot represent a particle in the phase space for different times $t = 0$ and $t > 0$.

more [100]. There is a possibility to decrease the emittance, for instance, by synchrotron radiation.

Synchrotron Radiation Particles, which are guided on an ideal orbit, perform longitudinal and transverse oscillations (synchrotron oscillations and betatron oscillations). However, electrons (and positrons) emit *synchrotron radiation* when they get deflected, i.e., they lose energy. The energy loss is compensated by the RF cavities. The phase space density is not conserved due to the emitted synchrotron radiation. This radiation damps the oscillations of the particles around the design (ideal) orbit. The emission of photons acts as a friction force on the particles [99]. It points to the opposite direction of the particles' motion. Hence, the phase space of the particles is damped and the oscillations decrease [101]. Consequently, the emittance is also decreased. This mechanism is called *beam cooling* or *synchrotron radiation (SR)* cooling. However, the damping is bounded to a lower limit since synchrotron radiation is emitted by photons of discrete energy, which is called *quantum fluctuations* in energy loss [102]. If the synchrotron radiative effects and the excitations by the RF are in a statistical equilibrium, the density of the bunch is given by statistically stationary Gaussian distributions in radial and longitudinal directions.

Storage Ring SuperKEKB has two storage rings: one, for electrons HER (7 GeV) and another one for positrons LER (4 GeV). The beams inside the storage

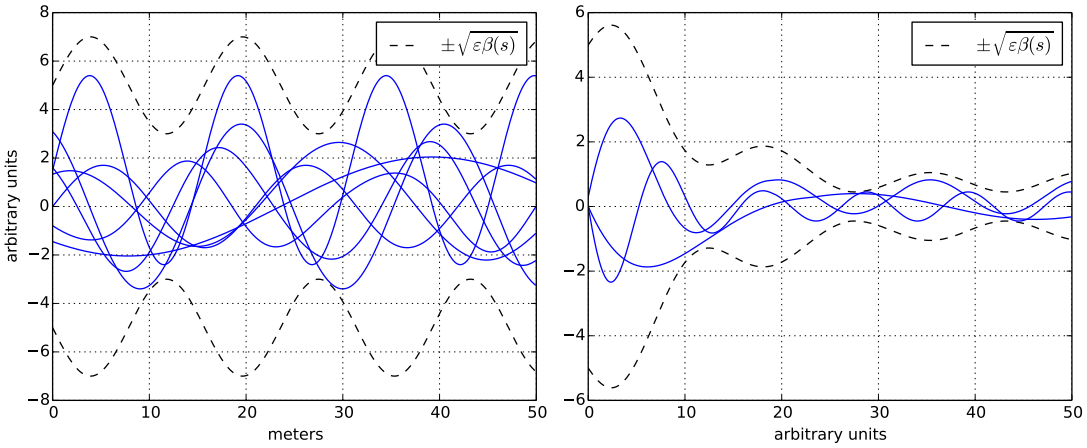


Figure 3.7: Betatron oscillations bounded by the envelope $\sqrt{\varepsilon\beta(s)}$. Left: Many particles oscillating differently. Right: Oscillations' development within the damping ring; the amplitude decreases proportionally to the emittance.

rings are bounded close to circular orbits and focused to very tiny bunch sizes near the IP in order to increase the luminosity. The beam optic instruments within the rings must be adjusted very accurately. However, none of the existing storage rings are perfect in terms of magnet alignment and created fields. Hence, some particles leave the acceptable deflection from their ideal orbit and are lost. This leads to finite lifetimes by colliding with the wall of the beam pipe.

3.2.5 Background and particle loss

The beam lifetime, limited by particle loss, is very crucial for the detector. In this subsection, the particle loss and the corresponding background effects in the Belle II detector are discussed.

Misalignment Misaligned beam magnets result in deviations from the ideal particle trajectories. Operation failures of power supplies controlling the bending magnets, cavities or quadrupoles also lead to unexpected beam loss.

Betatron oscillations As already discussed in the previous sections, betatron oscillations describe the transverse oscillations of the charged particle within a bunch. Bunches are stabilized and focused in the beam optic instruments, such as the focusing quadrupoles. If the betatron amplitudes become too large, particles also hit the beam pipe and disappear.

Synchrotron oscillations Synchrotron oscillations are the longitudinal oscillations along the beam in the z-direction, as described in the previous section. Particles with less energy compared to the nominal energy (E_{nominal}) are located in the tail of the bunch; particles with more energy travel in the front part. The

deflection by bending magnets depends on the energy of the particle, i.e., a particle with $E < E_{\text{nominal}}$ is more deflected compared to a particle with $E > E_{\text{nominal}}$. As a consequence, they start to oscillate transversely, that is to say they perform additional betatron oscillations.

Beam-gas scattering Stored particles scatter with residual gas molecules within the vacuum chamber. A fraction of the particles within the bunch scatter elastically and are deflected. Thus, they increase their betatron oscillation amplitudes and may be lost. There are also inelastic collisions, i.e., the charged particles within the bunch either transfer their kinetic energy to residual gas molecules (and hence lose their kinetic energy) or are deflected by the nucleus and emit photons by bremsstrahlung.

Touschek effect As already described in the previous section, the charged particles within a bunch oscillate in longitudinal (synchrotron oscillations) and perpendicular directions (betatron oscillations). Due to the oscillations, Coulomb interactions with other particles within the same bunch (*intra-bunch scattering*) occur, i.e., elastic scattering. Thus, the particle energies change, resulting in deviations from the bunch energy. The bunch size increases in all three dimensions and thus the emittance increases as well.
If a particle scatters with another one in the same bunch and transfers its momentum in the longitudinal direction, it either becomes decelerated or accelerated such that it leaves the bunch. This effect is called the *Touschek effect*. Particles are also lost since they leave their ideal trajectory and hit the beam pipe.
The scattering rate of the Touschek effect is [103]:

$$S \propto \frac{I^2}{E^3 \sigma_y} \tag{3.2.15}$$

where I denotes the bunch current, E the beam energy and σ_y the beam size.
If the particles hit the beam pipe, they do not only create EM showers but also neutrons (nuclear spallation).

Radiative Bhabha scattering A major contribution to the background in the Belle II detector is the *radiative Bhabha* scattering:

$$e^+e^- \longrightarrow e^+e^- (\gamma)$$

Since the majority of the scattering angles are very small, they mostly do not pass the Belle II detector. However, the emitted photons propagate along the beam pipe until they hit a magnet of the beam optic instruments. Neutrons are created which in turn may hit the Belle II detector. In order to prevent this, additional neutron shields are installed within Belle II. Simulations showed that the QCS over-bend the scattered electrons and positrons. Only a small fraction of highly energetic particles are lost within the detector. Therefore, background

from scattered positrons and electrons within the Belle II detector is expected to be small [104].

Two-photon process The two-photon process

$$e^+e^- \longrightarrow e^+e^- + \text{“}\gamma\gamma\text{”} \longrightarrow e^+e^-e^+e^-$$

is the dominating irreducible QED background effect for the PXD, since it is located very close to the beam pipe. Since the momenta of the secondary particles are rather small, they are mostly confined within the innermost part of the Belle II detector, i.e., the PXD. The two-photon process is much less severe for the sub-detectors at larger radii.

Synchrotron radiation SR is created when a light charged particle is accelerated. SR is emitted in every circular accelerator since the beam is guided around the arcs by the bending magnets.
The final focusing magnet system, which squeezes the bunch, is located close to the IP (see Fig. 3.5). Due to the strong deflection of the electrons and positrons, SR is emitted. One distinguishes the SR as:

- *direct (upstream) SR*, which are photons directly created from the incoming beam caused by the bending of the charged particles at the QCS and hit the detector directly.
- *backscattered (downstream) SR*, created by photons which are generated by the deflection of the outgoing beam. The emitted photons are reflected at the surface of the beam pipe or on other machine elements and scatter back into the detector. The back-scattering involves mainly three processes: Rayleigh scattering, Compton scattering and photoabsorption followed by X-ray fluorescence [105].

The four quadrupole magnets, which are installed around the IP for the nano-scheme beam, centers the beam trajectories resulting in less deflection, which in turn causes less SR. In order to counteract the SR and to protect the vertex detector (VXD), the inner surface of the beam pipe is coated with a 10 µm thin layer of gold, which absorbs the low energetic photons [85, 104]. Hence, the hit rate (occupancy) of the VXD is greatly reduced. The details are discussed in Sect. 3.4.

3.2.6 Beam energies

The beam energies in SuperKEKB with the nano-beam scheme are less asymmetric (4.0 GeV and 7.0 GeV) compared to KEKB (3.5 GeV and 8.0 GeV). SuperKEKB is the world's first accelerator which implements the nano-beam scheme. This results in a reduced boost, already described in Sect. 2.11. In the nano-beam scheme, the Touschek effect in the LER lowers the beam lifetime substantially. In order to counteract this effect, the beam energy in the LER was increased to 4.0 GeV. Reducing the beam asymmetry yields a decreased boost. In conclusion, it is necessary to find the compromise in optimal beam energies to keep the Touschek effect small while achieving a large boost to resolve the decay length difference.

3.2.7 Injection scheme

Electron and positron bunches are continuously injected to counteract against the short beam life time, i.e., the particle loss due to the effects discussed in the previous section (top-up mode). The injection frequency is 25 Hz for both electrons and positrons resulting in a total injection frequency of 50 Hz, i.e., every 20 ms new particles are pushed into the HER and LER, respectively. The criterion for the bunch selections (which are spaced by 100 ns) is the lowest sum of beam currents within all bunch pairs in the storage ring.

In SuperKEKB, the *betatron injection* scheme will be used. The injection of new particles into an existing stored bunch is realized by kicker magnets and a septum magnet in order to minimize the angle, α, between the trajectories of the newly injected bunch and the existing, circulating bunch (see Fig. 3.8). Kicker magnets produce rectangular fast pulses in order to guide the stored bunches in the direction of the newly injected bunches (*orbit bump*). For SuperKEKB, the kicker magnet consists of a conventional lumped magnet with a window-frame ferrite core [106]. The peak current of 2000 A, with a pulse width of 2 µs, creates a magnetic field of 0.05 T [107]. In addition, a septum magnet is relatively low pulsed and thus provides a very strong magnetic field. It bends the trajectories of the injected bunches towards the trajectory of the stored ones. The septum separates the two field regions, the strong field for the beam injection and low fringe fields of the orbit bump in order to not influence the stored, circulating bunches [108]. The principle of the septum magnets for SuperKEKB can be found in [109]. The trajectory of the injected bunches and the stored bunches intersect, both with the same kinetic energy. The injected bunches start to perform betatron oscillations around the circulating, stored beam, cooling into their host bunches by SR. Due to the initially large betatron amplitudes the bunches to be filled-up lose particles around the ring by collisions with the beam pipe. These bunches are called *noisy bunches*.
The collisions with the beam pipe result in secondary particles, which in turn create strong background in Belle II. The beam efficiency due to this effect and the corresponding particle loss is estimated to be only around 24 % [110].
The damping time of the betatron oscillations of the particles in KEKB were approximately 4 ms, while the revolution time is 10 µs. Assuming the same damping time for SuperKEKB 20 % of the total data collection time is "contaminated" by damping.
Special operation modes for the sub-detectors have been developed in order to overcome this problem: They switch into a "blind" mode for around 1–2 µs when those noisy bunches are passing. Special attention has to be paid to the PXD using the rolling shutter readout. While other sub-detectors stop their readout for a short time, the charge collection of PXD sensors cannot be stopped. Hence, a special operation mode of the PXD, called *Gated Mode* has been developed. This will be discussed in Sect. 6.12. A sketch of the noisy bunches and their damping time is shown in Fig. 3.9.

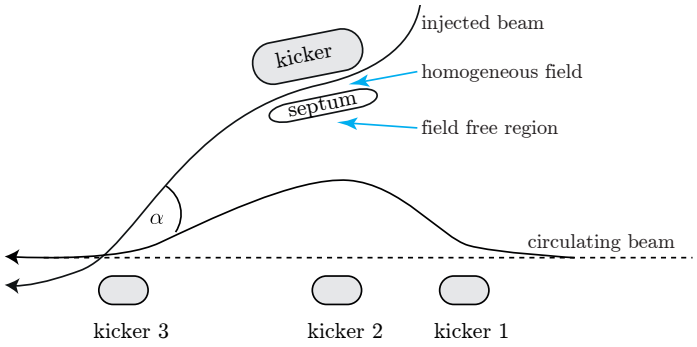


Figure 3.8: Betatron injection scheme. The injected bunch has the same energy as the stored one. It performs betatron oscillations.

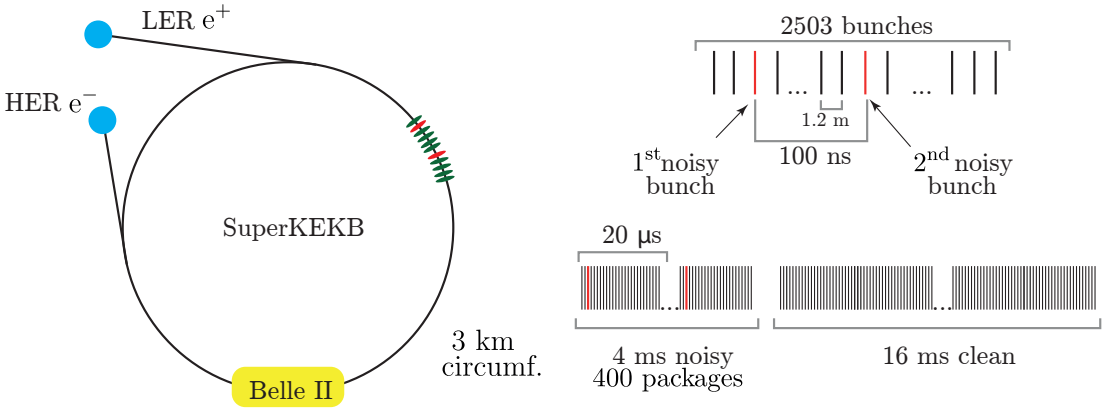


Figure 3.9: SuperKEKB injection scheme. The total injection frequency is 50 Hz (every 20 ms) where two bunches in a distance of 100 ns are filled up. They are shown as the red lines. The damping takes approximately 4 ms.

3.2.8 Schedule

The preparations for a stable experiment in order to perform physics runs are divided into three phases.

Phase 1 (∼ February 2016 for 5 months) In the first phase, the initial commissioning of SuperKEKB was done, i.e., the accelerator needed to be tuned in order to establish high quality vacuum in the beam pipe (vacuum scrubbing). The surfaces of the new beam pipes were "cleaned" by synchrotron radiation. This process took around one month with beam currents of up to 1 A [111]. The accelerator ran without the final focus superconducting quadropole and without the Belle II detector. Most of the pipes from the HER could be reused, whereas 90 % of the beam pipes from KEKB's LER have been renewed. Furthermore, background studies are performed in the "Beam Exorcisms for A STable belle experiment" (BEAST)-phase. Consistency between the simulations and measurements were cross-checked to guarantee a safe environment for the Belle II detector. Therefore, several independent sub-detectors were mounted around the beam pipe in order to study the different components of the background. The sub-detectors for BEAST are listed below.

- Scintillation light and waveform sensors (CLAWS) [112] (8 sensors): Consists of plastic scintillator with silicon photomultiplier readout. Measures the delay between trigger and particles at the IP and the damping time of newly injected bunches
- Diamond sensors (4 sensors): Determination of the total ionizing dose
- Positive intrinsic negative (PIN) diodes (64 sensors): Measurement of X-ray and ionizing particle background
- Bismuth germanium oxide / bismuth germanate ($Bi_4Ge_3O_{12}$) (BGO) crystals (8 sensors): Measures the Bhabha background and serves as luminosity monitor
- Pure Thallium cesium iodide (CsI) crystals and cerium-doped lutetium yttrium orthosilicate (LySo) crystals (6 pure, 6 doped): Measurement of γ rays and X-rays
- He-3-tubes (4 sensors): Measurement of thermal neutron rate
- Micro-time projection chamber (TPC) (4 sensors): Measurement of fast neutron rate and recoil spectrum

Phase 2 (∼ Autumn 2017 until June 2018) For Phase 2, the QCS magnets will be installed and the Belle II detector will be rolled onto the beam line. The VXD is not included in this first attempt of luminosity commissioning using the QCS system with nano beams. Furthermore, the newly constructed DR for the positrons will be put into operation. The goal is to obtain the peak luminosity of $1 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. Further background studies will be performed to assure a safe integration of the VXD later on. A special Phase 2 vertex detector will include the following components:

- CLAWS [112] (16 sensors): Measures the delay between trigger and particles at the IP and the damping time of newly injected bunches
- Front-End I4 (FE-I4) ATLAS Near Gamma Sensors (FANGS) [113] (15 sensors): Composed of radiation-hard silicon pixel detectors to measure the synchrotron X-ray spectrum.
- Pixelated ladder with ultra-low material embedding (PLUME) (2 ladders): Consists of complementary metal-oxide-semiconductor (CMOS) pixels on light support structure to measure the collimator adjustment.
- Diamond sensors (8 sensors): Determination of the total ionizing dose
- PIN diodes (80 sensors): Measurement of X-ray and ionizing particle background
- Two PXD ladders and four SVD ladders: They are similar to the final Belle II vertex detector, installed in the "final" arrangement. They are located at $\phi = 0\,^\circ$ (horizontal plane) for the largest background sensitivity. The radiation tolerance for phase 3 will be investigated.
- He-3-tubes (4 sensors): Measurement of thermal neutron rate
- Micro-TPC (8 sensors): Measurement of fast neutron rate and recoil spectrum

Phase 3 (∼ Autumn 2018) In the third phase the VXD will be installed and put into operation. Furthermore, the beam currents will be increased and the peak luminosity will be further tuned and increased gradually from $1 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ to $80 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. The physics runs are expected to start in early 2019.

3.3 Belle II

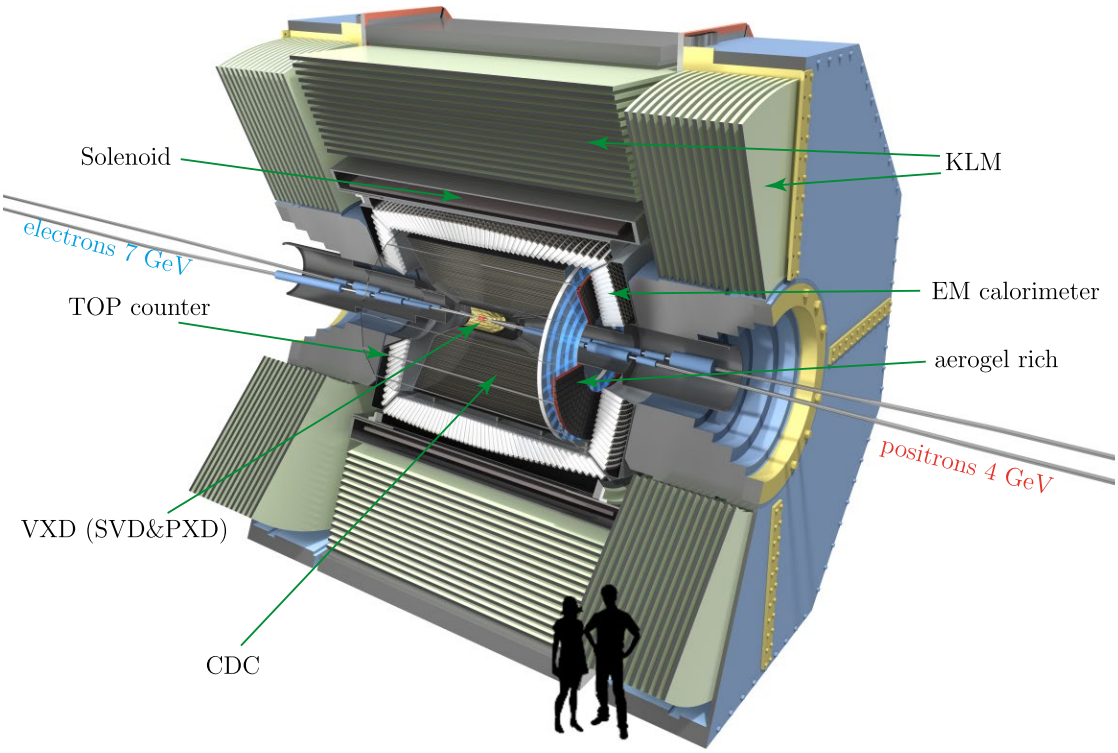


Figure 3.10: Belle II Detector. It consists of several sub-detectors [1].

Various sub-detectors are required with dedicated measurement tasks, such as the determination of the momentum, energy, particle type and charge sign in order to determine the physical behavior (interactions and decays) of the produced particles. The Belle II detector consists of many sub-detectors which are described in this section. They are arranged in an onion-like shell structure, i.e., one layer is placed above the other in a cylindrical way in order to cover an almost 2π solid angle. Each sub-detector has a well-defined task. Using all of the combined information provided by each one allows the study of the physics of the particle collisions. Detailed information about the sub-detectors can be found in [85]. Here, only a short overview of the various components of Belle II is given, starting from the outside and moving towards the interaction region (see Fig. 3.10). The Belle II detector can be subdivided into an outer and inner part. The outer part consists of the KLM, the solenoid and the ECL. They are reused from the predecessor Belle experiment. The inner part containing the ARICH, TOP, CDC and VXD are replaced by newly developed sub-detectors.

3.3.1 KLM

The KLM (identifies K_L^0 and muons) is the outermost detector of Belle II. It is divided into three parts: the forward endcap, the backward endcap and the barrel, which covers the area in between. The detector consists of 14 iron plates with a thickness of 4.7 cm and 14 (in endcaps, 15) active detector elements based on glass-electrode resistive plate chambers (RPCs) in between. The innermost layers of RPCs were replaced by polystyrene scintillator strips with wave-length shifting (WLS) fibers combined with silicon photomultiplier (SiPM) detectors [114]. They can tolerate high radiation doses, which are approximately 100 times larger compared to the previous Belle experiment. In addition, the SiPMs can work in a strong magnetic field without significant degradation of the operational functionality. The strips are 40 mm wide, which is a compromise between the spatial resolution and the number of readout channels. A sketch is shown in Fig. 3.11. When a particle traverses the strip scintillator light is created, which is collected by the WLS fibre. It propagates to the SiPM, which is installed at the near end of the fiber. In order to increase the total light yield, a mirror is assembled at the far end of the fiber.
The coverage of the polar angle range is $20° < \Theta < 155°$ for the endcaps and $45° < \Theta < 125°$ for the barrel. If a K_L^0 passes the iron plates, hadronic showers are created and detected. Muons (and hadrons which do no create any showers) above the momentum of $\sim 0.6\,\mathrm{GeV}/c$ are detected by depositing EM energy.

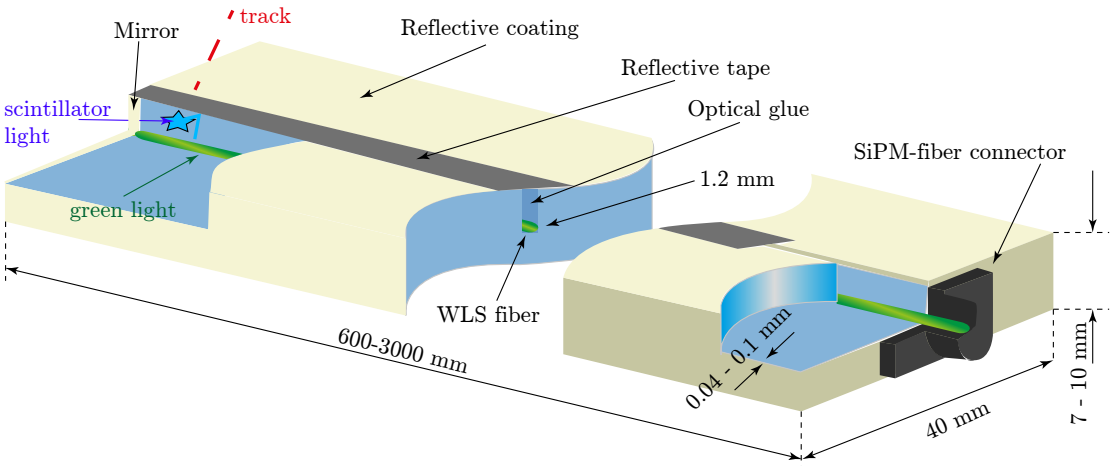


Figure 3.11: Schematic view of the scintillator strip [114].

3.3.2 Solenoid

A superconducting solenoid is installed within Belle II, creating a 1.5 T magnetic field [115]. Its diameter is 3.4 m, its length is 4.4 m. The charged particles are deflected by the magnetic field, which allows the reconstruction of the particles' momenta using the tracking information from the sub-detectors (CDC).

3.3.3 ECL

The electromagnetic calorimeter (ECL) is composed of 6624 scintillation crystals which consist of thallium-doped cesium iodide (CsI(TI)) to fulfill the physics requirements in terms of high light output, short radiation length, X_0, and good mechanical properties. Each has a truncated pyramidal shape of $6 \times 6\,\mathrm{cm}^2$ and a length of 30 cm.
The ECL detects photons (in the energy range beyond 20 MeV) of the decay products of neutral particle (such as neutral pions, π^0) with a high efficiency. Furthermore, it determines the angular coordinates and photon energy. In addition to this, the ECL identifies electrons and hadrons, measures the luminosity on- and offline, detects the K_L^0 in cooperation with the KLM and generates signals for triggering [116].

3.3.4 ARICH

The aerogel ring-imaging cherenkov detector (ARICH) is used for particle identification (PID) in the forward endcap region. A proximity-focusing ring imaging detector has been developed due to space constraints. It consists of aerogel[2] radiator, a high position resolution Hybrid Avalanche Photo-Detector (HAPD) and readout electronics [118]. It separates pions from kaons up to a maximum momentum of $4\,\mathrm{GeV}/c$ [119]. Particles passing the detector create Cherenkov light, which is emitted in a cone-like structure and hits the photo detector. Depending on the angle, the mass is calculated by $m = p/c\sqrt{n^2\cos^2(\Theta_\mathrm{o}) - 1}$, where p denotes the particle momentum, c is the speed of light, n is the refractive angle of aerogel and Θ_o is the opening angle of the Cherenkov cone.

3.3.5 TOP

The time of propagation (TOP) detector consists of 16 modules. Each module has two quartz radiator bars of total $\sim 2.5\,\mathrm{m}$ length [120]. The TOP has around 8200 channels in total.
The task of the sub-detector is to separate charged kaons ($K^\pm$) from charged pions ($\pi^\pm$). It is the primary device for the PID in the barrel region of Belle II. Particles hitting the detector emit Cherenkov light in the quartz bars. The opening angle (Θ_o) of the cone depends on the particle's velocity. The emitted photons travel to the photon detector at the end by total reflection in the quartz bars. A sketch is shown in Fig. 3.12. Depending on Θ_o, the path of the photons to the detector vary, which results in a different propagation time. This propagation time of light (from the incident position of the charged particle until the arrival at the detector) is measured. Thus, one can distinguish charged kaons from charged pions; the propagation time difference being in the range of $\sim 100\,\mathrm{ps}$ for particles with momenta of $2\,\mathrm{GeV}/c$ [121].

[2] A gel which consists of a microporous solid in which the dispersed phase is a gas [117].

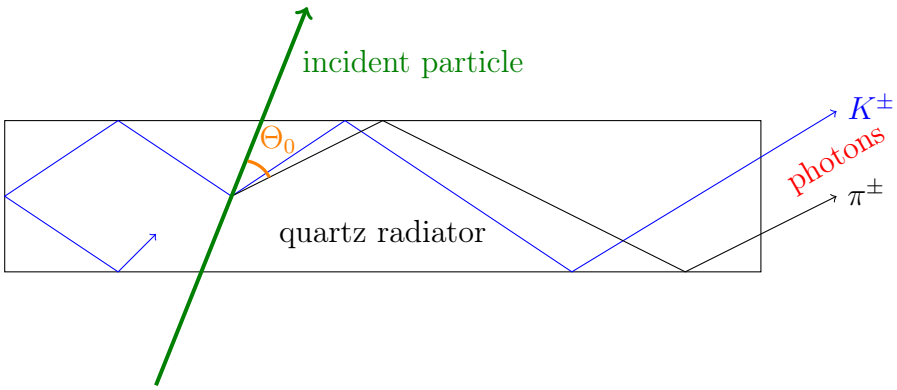


Figure 3.12: Working principle of the TOP detector.

3.3.6 CDC

The central drift chamber (CDC) is a cylindrical chamber equipped with 14336 sense wires (made of 30 µm gold-plated tungsten) and 42240 field wires (126 µm aluminum wires). The field wires and sense wires are biased with opposite voltages. They are arranged alternatingly parallel to the beam pipe and at an angle, called axial and stereo layers. The chamber is filled with a helium (50 %) and ethane (50 %) gas mixture.
The CDC measures the momenta and reconstructs the tracks of charged particles. Moreover, the energy loss $\mathrm{d}E/\mathrm{d}x$ within the gas volume is measured to provide information for the particle identification [85, 122]. In addition to this, it provides reliable and efficient trigger signals. If charged particles pass the CDC, electrons are created from collisions with the gas atoms. Those electrons drift to the sense wires, while creating more electrons on their path by further collisions. The created current pulse is measured by the readout electronics. The drift time, measured by the current pulses, gives information about the position of the tracks of the charged particles. The spatial point resolution is approximately 100 µm.

3.3.7 VXD

The vertex detector (VXD) consists of two sub-detectors, the silicon vertex detector (SVD) and pixel detector (PXD). The VXD is composed of six detector layers. They are described in more detail the following sections.
One purpose of the VXD is the measurement of particle tracks combined with the CDC in order to reconstruct the origin or decay vertices of the created particles, such as B mesons. The VXD should be as close as possible to the IP to minimize errors in the extrapolations. The other aim is the reconstruction of the particles' momenta using the curved trajectories of charged particles caused by the solenoid field. Moreover, the VXD is able to reconstruct tracks with low transverse momentum (low p_t tracks) in the order of around 30 MeV/c. (The low p_t tracks do not reach the CDC). The combined SVD and PXD will provide an impact parameter resolution in the direction of the beam pipe of around $\sigma(d_z) \approx 20$ µm.
The SVD and PXD layers are arranged cylindrically around the beam pipe, as shown in Fig. 3.13 and Fig. 3.14.

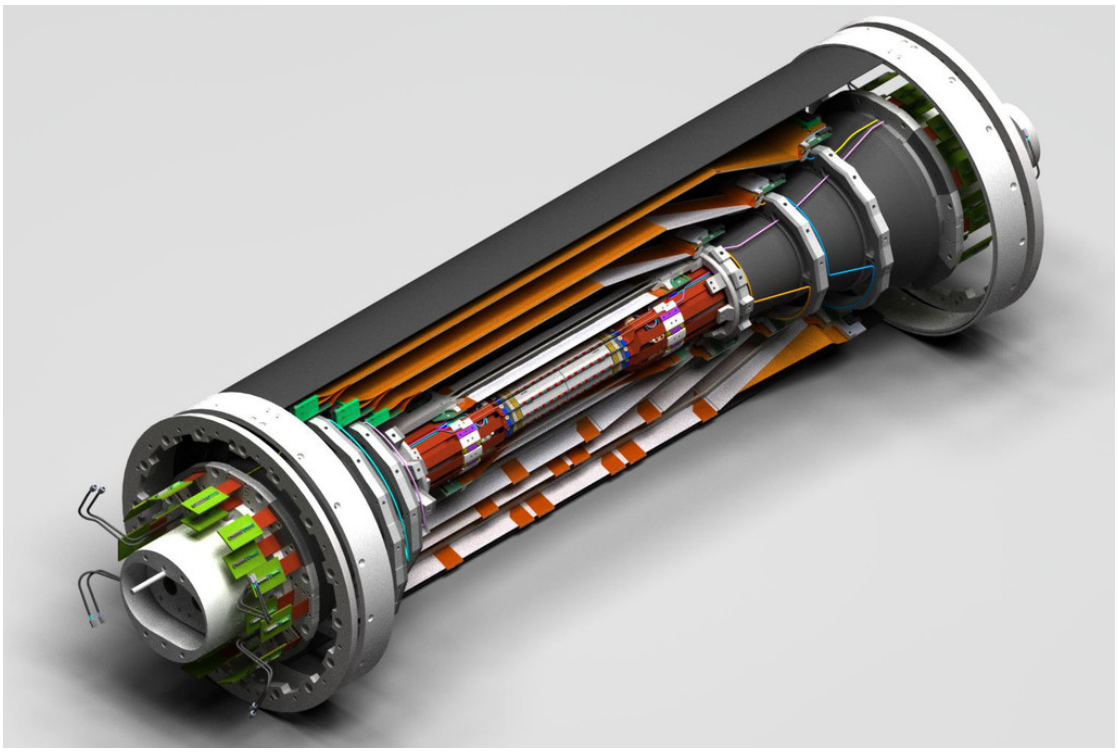


Figure 3.13: Belle II VXD. The sub detector is composed of four layers of silicon strip detectors and two layers of pixel detectors [123].

SVD

The nomenclature of the silicon vertex detector (SVD) is (a bit) confusing. This is due to historical reasons. In the former Belle experiment, the vertex detector only consisted of a silicon strip detector. The SVD of Belle II consists of four layers of double-sided silicon detectors (DSSDs). They are located at 38 mm, 80 mm, 104 mm and 135 mm around the center of the beam pipe [85]. The strips on the top and bottom side of a single layer are (mostly) arranged orthogonally. Particles passing a layer of the SVD create electron-hole pairs in the silicon bulk. The electrons drift to the n-side strips, whereas the holes drift to the p-side strips. Reading out the strips, the particle track can be determined in two dimensions, as shown in Fig. 3.15.

The major task of the SVD is to reconstruct the tracks of the passing particles and determine their momenta. Moreover, the SVD is able to reconstruct secondary, long-lived particles which decay outside of the PXD. The SVD, like all other sub-detectorrs of Belle II, must cover the full acceptance, i.e., $17° < \Theta < 150°$. The detector must provide precise spatial resolution, have a very low material budget (to avoid multiple scattering) and must be radiation-tolerant for the entire Belle II operation time. The occupancy should be below 1 %. Since the peak luminosity will be a factor of 40 higher compared to KEKB, the background will also increase. In addition, the number of background hits roughly decreases with the inverse square of the radius, i.e., the closer the detector is located to the IP, the more background hits are detected, resulting in higher occupancy. Since the DSSD

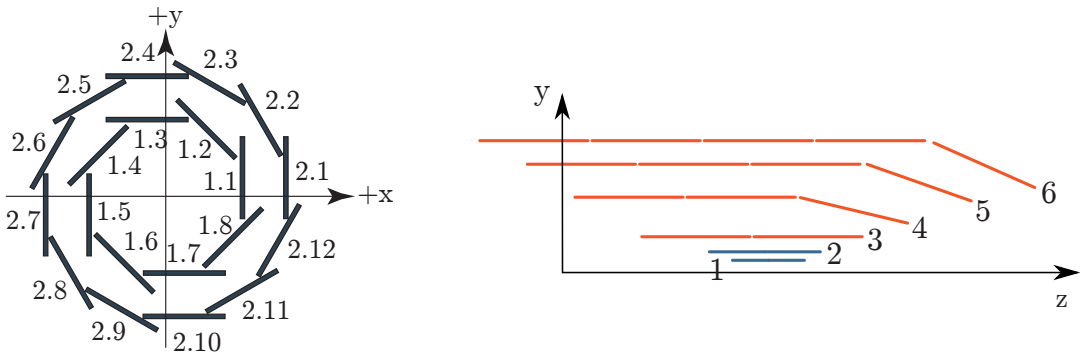


Figure 3.14: **Left**: Arrangement of the PXD layers around the beam pipe. **Right**: Alignment of the SVD and PXD layers around the beam pipe and their corresponding numbering [124].

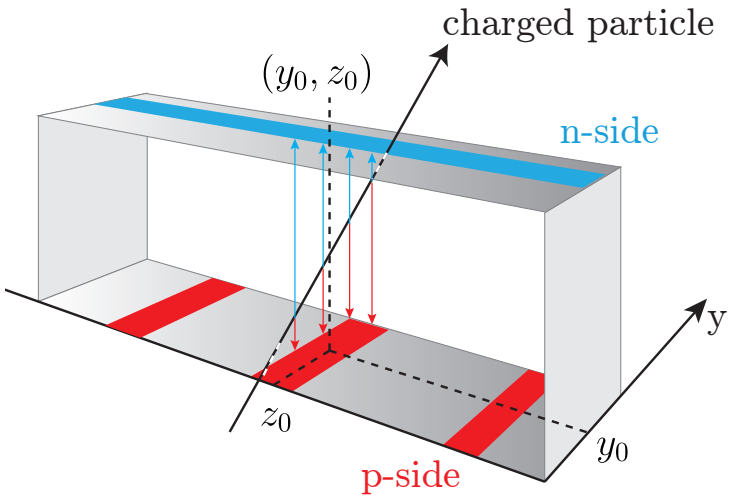


Figure 3.15: A particle passing the SVD creates electron-hole pairs. The electrons drift to the n-side while the holes drift to the p-side. Reading out the strips on both sides of a SVD layer, the position of the incident particle can be determined.

cannot cope with the tremendously high background, the innermost layers have to be equipped with occupancy-tolerant pixel sensors.

PXD

The pixel detector (PXD) is only briefly touched in this section. It is the main work of this thesis, and more details can be found in chapter 4. The PXD has two layers located at radii of 14 mm and 22 mm around the IP, forming the innermost detector of Belle II. The inner layer consists of eight sensors while the outer layer is equipped with twelve sensors. It is comprised of approximately eight megapixels which are read out continuously every 20 µs.
Its main task is the precise position measurement of passing particles in order to reconstruct the origin ("vertex") of the produced particles. It is able to detect particles with very low transverse momentum (p_t) in the range of 40 MeV to 75 MeV.

3.4 Interaction Region

The 7 GeV electron beam stored in the HER and the 4 GeV positron beam from the LER collide at the interaction point. The nano-beam scheme, described in Sect. 3.2.2, requires focusing magnets close to the IP. The final focusing quadrupole magnets, called QCS, are installed within the interaction region (IR), which is approximately 4 m long. The interaction region includes superconducting quadrupole magnets and permanent quadrupole magnets, providing the beam focus and reducing the betatron oscillations at the IP. A picture of the QCS system is shown in Fig. 3.16. A technical drawing is shown in Fig. 3.17.

Figure 3.16: Picture of the superconducting quadrupole magnet system at the installation (February 2017) [125].

The beam pipe at the IP has an inner radius of 10 mm. The inner surface is coated with 10 µm gold in order to reduce the synchrotron radiation, which hits the VXD. On the one hand, multiple scattering and the deflections of the created particles (and their corresponding decay products) should be avoided. Therefore, the beam pipe should be as thin as possible. On the other hand, the SR is tremendously high, which would damage the innermost VXD. The optimal thickness of the gold foil, taking multiple scattering and the protection of the PXD into account, was calculated to 10 µm [126]. It shields the PXD from the SR.
The beam pipe at the interaction region consists of double-walled beryllium. It is composed of low-Z material, resulting in low multiple scattering, but provides mechanical stiffness and resistance to corrosion. Furthermore, the melting point is relatively high. The high thermal conductivity is advantageous for the heat dissipation. Both need to be cooled by the heating of synchrotron radiation and wall current. Therefore, paraffin flows between the two walls of the beam pipe and water is circulated at the bellows to assure a proper heat conduction and thus cooling. Beam optics and control instruments are also installed within the IR, such as beam position monitors (BPMs), in order to control the beam trajectories and luminosity measurement instruments.

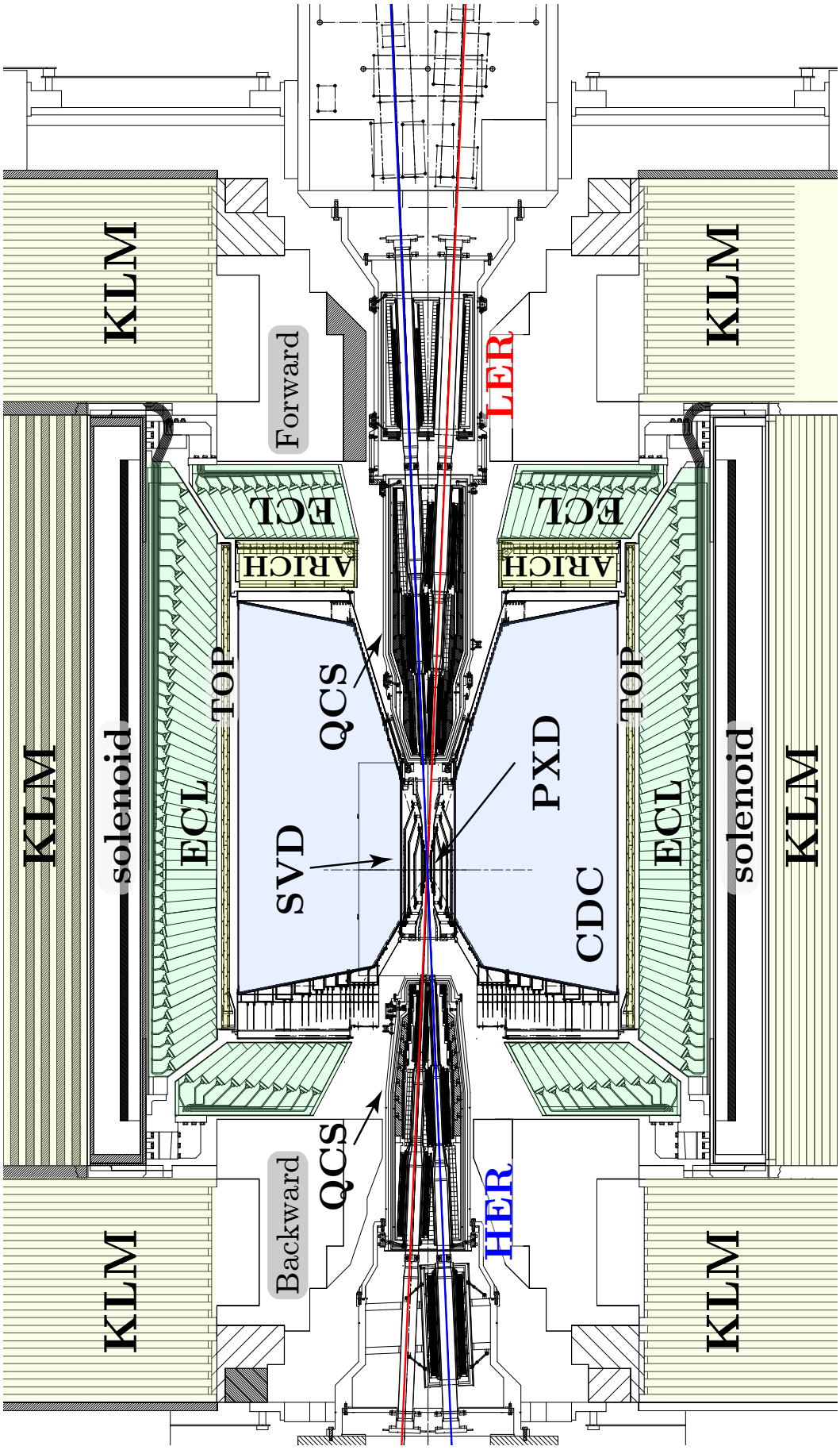


Figure 3.17: Interaction region with the surrounding Belle II detector [127].

Chapter 4

Pixel Vertex Detector

4.1 Requirements for Belle II PXD

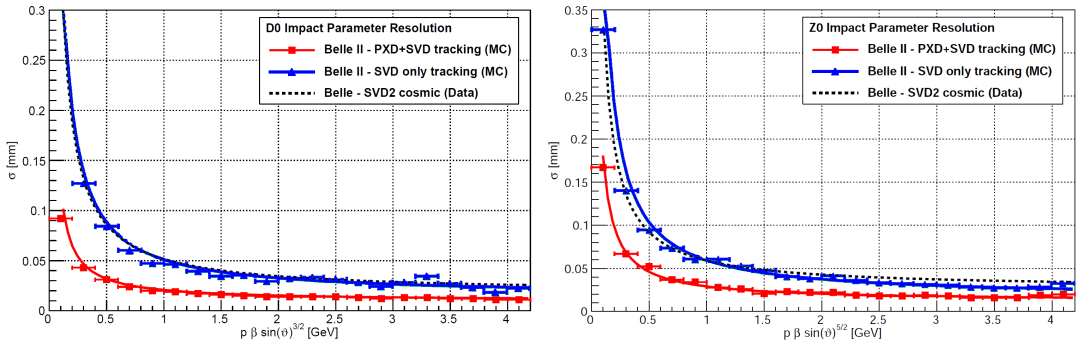
The increased luminosity of SuperKEKB and the accompanying increased background, caused by the nano beam scheme and the decreased beam pipe diameter, gives rise to new and challenging requirements of the VXD, which are explained in this section.

The expected high occupancy prevents the usage of a "traditional" silicon vertex detector with double-sided strips (SVD) as was used in Belle. The occupancy is defined as the ratio of strips above the threshold divided by the number of total strips per sensor side per event. The SVD cannot cope with the expected occupancies on the order of 10 % and is therefore not suited as the innermost detector in Belle II.

For this reason, a pixel detector is required to detect the secondary (or tertiary) particles and to reconstruct the decay vertices of the B mesons. The readout mechanism for the pixels needs to be fast enough in order to avoid pile-up, i.e., if particles from different events create signals in the same pixel. The estimated occupancy is approximately 1.3 % for the inner layer and approximately 0.5 % for the outer layer [93]. The PXD must also withstand the huge radiation doses, particularly since the background increases with the inverse square of the radius. The close proximity to the beam pipe requires a radiation hardness of up to 20 kGy/smy[1] [93]. Furthermore, the pixel sensor is required to provide precise spatial resolution in order to allow precise vertex reconstruction. The boost in SuperKEKB is reduced from 0.42 to 0.28 resulting in an average decay length of approximately 125 µm. The PXD must be able to resolve these small position resolutions. The quality of the vertex reconstruction is expressed by the *impact parameter resolution*. It is defined as the distance from the point of closest approach of a charged track to the true vertex. The two impact parameters $d0$ and $z0$ are the transverse (xy plane) and longitudinal (Rz plane) projections of the point of closest approach. The impact parameter is primarily affected by the multiple scattering (see below) of traversing particles within the detector (and beam pipe) and by the intrinsic resolution of the PXD. Figure 4.1b and Fig. 4.1b show the impact parameter resolution of the Belle II VXD compared to the Belle SVD.

In order to reduce multiple scattering and to minimize gamma conversion, the detector must be thin. Furthermore, the control and readout electronics should

[1] A smy corresponds to 10^7 s.



(a) $d0$ impact parameter resolution. (b) $z0$ impact parameter resolution.

Figure 4.1: Impact parameter resolution of Belle II compared to Belle, where p denotes the momentum of the traversing particle and Θ is the polar angle with respect to the beam axis [26].

contribute as little as possible to the overall material budget. In the ideal case, they are not mounted in the acceptance region.

Charged particles traversing a medium are deflected by multiple scattering. There are many small deflections mostly caused by Coulomb scattering. The distribution of the scattering angles has a width of [32]:

$$\sqrt{\langle \Theta_0 \rangle} = \frac{13.6\,\text{MeV}}{\beta c p} z \sqrt{x/X_0}\left[1 + 0.038 \ln(x/X_0)\right] \tag{4.1.1}$$

where $\beta c = v$ is the velocity, p and z denote the momentum and charge in units of elementary charge of the incident particle, respectively, x is the thickness and X_0 is the radiation length of the scattering medium. If a charged particle passes the sensitive volume of a single PXD layer (75 µm thick), eq. (4.1.1) simplifies to:

$$\langle \Theta_0 \rangle = \frac{2.81 \cdot 10^5\,\text{eV}}{\beta c p} z \tag{4.1.2}$$

The momentum distribution of particles expected from B decays produced at the $\Upsilon(4S)$ resonance is shown in Fig. 4.2. As it can be clearly seen, most of the particles have a low momentum $< 500\,\text{MeV}$. The smaller the momentum, the wider the distribution of the scattering angles. A 75 µm thick silicon detector is thin enough that multiple scattering effects are rather small. The scattering angles for different particle momenta and incident angles are shown in Tab. 4.1. Furthermore, the power dissipation, in particular, the heat dissipation should be as low as possible to avoid bulky cooling systems (such as cooling pipes) contributing to the material budget.

4.2 Available technologies and detectors

In this section, the available technologies and detectors and their properties are briefly discussed regarding their suitability for a pixel detector at Belle II. The

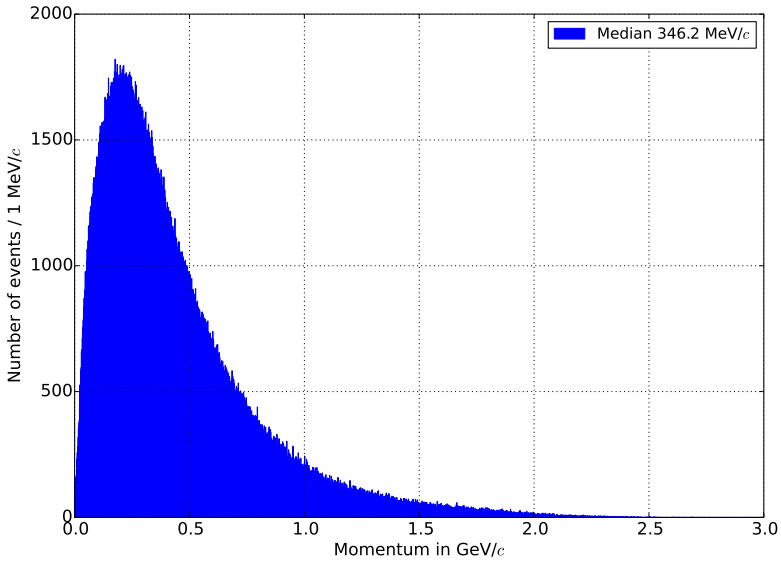


Figure 4.2: The transverse momentum distribution of particles passing the two layers of the pixel detector. The median is 347 MeV.

Table 4.1: Deflection angle by multiple scattering for different particle momenta (smallest and very large momenta of the shown distribution in Fig. 4.2) and incident angles (rectangular and diagonal incidences).

	median mom.		mean mom.		small mom.		large mom.	
p [GeV/c]	0.347	0.347	0.440	0.440	0.023	0.023	2.438	2.438
E [GeV]	0.412	0.412	0.470	0.470	0.024	0.024	2.526	2.526
incident angle [°]	90	45	90	45	90	45	90	45
material [µm]	75	106	75	106	75	106	75	106
Θ_0 defl. angle [°]	0.06	0.07	0.04	0.05	0.71	0.86	0.01	0.01

detector must be fast (few tens of microseconds), thin (below 100 µm) and have a low power consumption (to avoid bulky cooling systems).

- The ATLAS hybrid pixel sensors [128] cannot be used for Belle II because they are too thick, about 256 ± 3 µm. In addition to this, the readout electronics (which could be thinned down to 90 µm [129]) are mounted on top of the pixels resulting in even thicker devices, hence further material budget.
- Charge coupled devices (CCDs) are not appropriate for the Belle II PXD since they have a very slow readout with low noise in the range of few milliseconds[2]. In addition to this, the CCDs are always sensitive during the readout. Thus, the position of a particle passing the detector cannot be determined during the readout process unless the exact time of the incidence is known. Furthermore, moving charges in the silicon bulk can be trapped,

[2]This could be partially solved by reading out multiple columns in parallel. However, the noise increases with decreasing the readout time.

which reduces the signal amplitude. This could be improved by cooling, which in turn increases the material budget, thus the multiple scattering.

- Monolithic active pixel sensors (MAPSs) are based on standard CMOS technology in a p-type epitaxial-layer mounted on a low resistivity p-type substrate [130]. Although they provide high signal-to-noise ratio (due to the low intrinsic capacitance) in the order of 30 : 1 [131], the charge collection time is relatively long, approximately 100 ns. This would result in long integration times for the entire PXD. Further development is required to use this technology for the construction of pixel detectors in future experiments. Recent publications have shown that the CMOS-based pixel detectors could be thinned down to 50 µm and achieve a total readout time of 5 µs for a 64×64 pixel matrix [132]. Scaling this to 192 rows would result in ~ 20 µs.
- The monolithic active DEPFET structures offer a combined signal detection and integrated amplification [133]. They can be thinned to 50 µm [134], provide a high signal-to-noise-ratio, excellent spatial resolution and have a low power consumption, i.e., do not require active cooling. Moreover, they can withstand the high radiation doses of the background levels close to the IP. The DEPFET is the detector technology of choice for the Belle II PXD. It will be discussed in more detail in this chapter.

4.3 Overview of the Pixel Vertex Detector

The pixel detector (PXD) of the Belle II experiment (shown in Fig. 4.3) consists of two layers of self-supporting ladders, each composed of monolithic active pixel sensors in DEPFET technology (DEPleted p-channel Field Effect Transistor). The two layers of ladders are installed in a roughly cylindrical shape resembling a windmill structure around the beam pipe at radii of 14 mm and 22 mm. The angular acceptance of the azimuth angle is 2π while the polar angle is between 17 ° in the forward direction and 150 ° in the backward direction, as required by the overall Belle II acceptance.
The inner layer (layer 1) includes eight ladders while the outer layer (layer 2) includes twelve ladders. Each ladder is composed of two modules that are glued together at the short edge in order to cover the required polar angle range in Belle II[3]. Each module is equipped with 14 ASICs that have been developed to control and to read out the DEPFETs. Six *Switchers* control the pixels, four *Drain current digitizers (DCDs)* read out the signals and four *data handling processors (DHPs)* filter the data and transfer them to the off-module data acquisition system. The PXD incorporates in total 7,680,000 pixels that are read out in the *rolling shutter mode* with a maximum trigger rate of 30 kHz.

In the following section, the detector will be explained in detail. The discussion starts with a single DEPFET pixel cell, its working principle and the operation parameters, followed by the pixel design used in the PXD of Belle II. The DEPFET

[3]Due to mechanical space limitations in terms of wafer sizes, the production of a single module with the foreseen dimensions is technically not feasible.

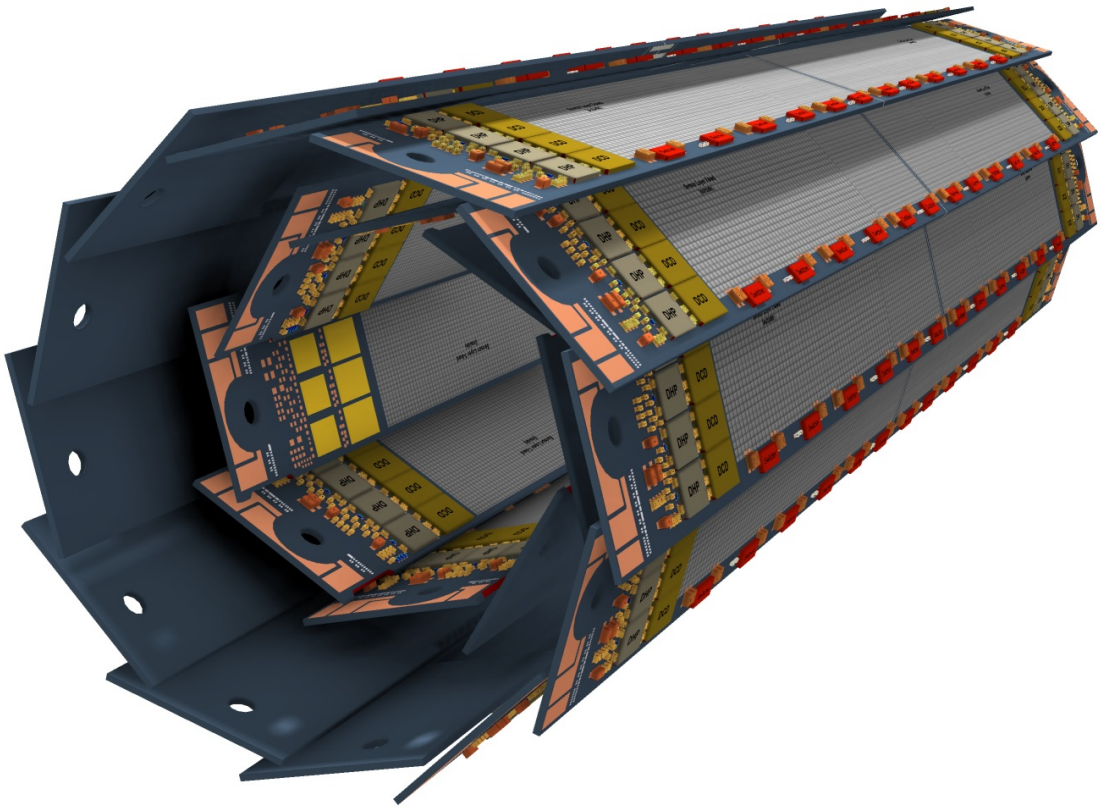


Figure 4.3: The PXD for Belle II. It consists of 40 modules arranged in two layers around the beam pipe. Each module is equipped with 14 ASICs, approximately 100 decoupling capacitors and termination resistors [1].

cells are arranged to form a large array, called the *DEPFET matrix*. After the required operation voltages for the matrix are presented, the module consisting of the DEPFET matrix and the surrounding support structure is introduced. The required control and readout electronics, their tasks, operation principles and control are explained. Next, the ladder composed of two modules is discussed. Finally, the arrangement of the ladders forming the pixel detector and the accompanied required cooling is presented.

4.4 DEPFET

The DEPFET concept was proposed by Kemmer and Lutz in 1987 [133]. It is a monolithic active structure that offers a combined signal detection and integrated in-pixel amplification. A p-channel Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is integrated into a fully sideward-depleted silicon bulk which serves as the detector substrate. The cross-section of this device is illustrated in Fig. 4.4. The intrinsic advantages of the DEPFET device are the very small input capacitance providing low noise and low power consumption. Furthermore, the DEPFET has an internal signal amplification and a non-destructive readout, i.e., there is no charge loss during the readout mechanism. In addition to this, it offers

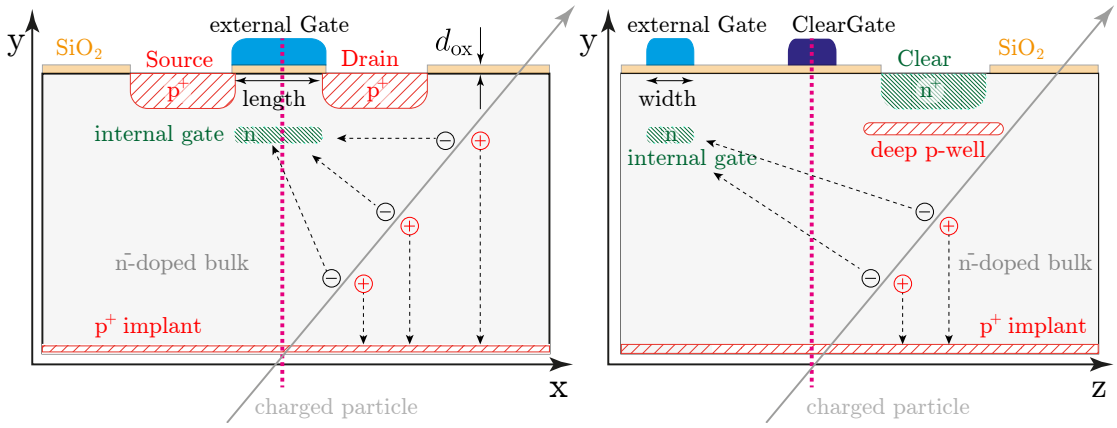


Figure 4.4: Cross-section of a DEPFET pixel cell (xy and zy planes along the purple axis). It consists of a MOSFET (*Source*, *Drain* p^+ implants, an external Gate and a *ClearGate* of polysilicon) onto a sideward-depleted n^- doped silicon bulk, where plus indicates a highly doped implant and minus indicates a lightly doped implant. An additional n-doping below the *external Gate* forms the *internal Gate*. If electron-hole pairs are created, the electrons accumulate in the *internal Gate* and modulate the Source-Drain current while the holes drift to the p^+ backside. A n^+ doped *Clear implant* is located in each pixel to reset the detector (i.e., to empty the *internal Gate*).

a high position resolution and a non-structured backside, which provides a large, uncovered and clear entrance window [135].

4.4.1 Working Principle of a DEPFET Pixel Cell

This section briefly describes the working principle of the DEPFET pixel cell (see Fig. 4.4). The current of the DEPFET is controlled by two gates, the *external* and the *internal Gate*. The *external Gate* corresponds to the Gate of the transistor. The amount of current is adjusted by the applied voltage. In addition, a potential minimum (*internal Gate*) is located less than one micrometer below the *external Gate* in the silicon substrate. Charged particles hitting the DEPFET create electron-hole pairs in the sideward-depleted n^- doped silicon bulk. The holes drift to the backside contact while the electrons accumulate in the *internal Gate*. Due to the capacitive coupling of the stored electrons and the conductive channel of the MOSFET, the Source-Drain current increases depending on the number of electrons in the *internal Gate*. The current can be read out non-destructively, i.e., multiple readouts neither distort nor destruct the signal, which scales with the number of accumulated electrons in the *internal Gate*. The DEPFET pixel is reset by the Clear mechanism: the electrons drift from the *internal Gate* to the *Clear region* by applying a positive voltage to the *Clear implant*. The different voltages and mechanisms in the DEPFET device is explained in the following.

4.4.2 Operating voltages for a DEPFET pixel (cell)

In the following, the *p*- and *n*- implants the operation of a single DEPFET pixel cell are explained.

External Gate Each DEPFET pixel has a "classical" MOS transistor gate, which is called the *external Gate*. The amount of current between the *Source implant* and the *Drain implant* (see Fig. 4.4) is adjusted by the Gate voltage V_{G}. Applying a sufficiently negative Gate voltage (relative to the Source voltage) forms a conductive channel (with holes) between the *Source implant* and the *Drain implant* below the *external Gate*. This allows charge carriers moving from the *Source implant* to the *Drain implant*. Applying an appropriate positive voltage at the *external Gate* (relative to the Source voltage) switches the *p*-channel MOSFET off, i.e., no current flows between the *Source* and *Drain implants*. The voltage that switches between enabling and disabling the transistor is denoted by the *threshold voltage* V_{T}.

Depletion To create a drift field in the DEPFET pixel (cell) and to separate the created electron-hole pairs the silicon bulk needs to be depleted. The voltage that defines the entire depletion of the silicon bulk is called the *Depletion voltage*. The voltage that is applied to the depletion is called *Backside voltage*. The process is described in detail later, since the depletion is performed for multiple DEPFET pixels simultaneously.

Internal Gate The Source-Drain current I_{ds} of a DEPFET is controlled by the voltage applied at the *external Gate* of the transistor and by the *internal Gate*. The fully depleted bulk and an additional *n* implant below the *external Gate* structure form a floating potential minimum, the *internal Gate*. It is located close to the transistor channel, less than 1 µm below the surface [136] and behaves like an additional Gate of the transistor.
A charged particle traversing the DEPFET pixel cell creates electron-hole pairs. The holes drift to the p^+ contact on the backside, while the generated electrons are attracted by the *internal Gate*. These electrons modulate the Drain current. Thus, the Source-Drain current is modulated by the Gate voltage and by the amount of electrons stored in the *internal Gate*.

Clear The *Clear region* is an n^+ implant near the MOSFET pixel cell structure. Its purpose is to remove the accumulated charge from the *internal Gate*. In that case, a conductive path has to be created (formed by a punch-through) between the *internal Gate* and the *Clear implant*. In order to increase the voltage between these nodes, the MOSFET is enabled (a negative voltage, relative to the Source voltage, needs to be applied at the *external Gate*) which switches off the capacitive coupling between the *external* and the *internal Gate*. The *Clear region* becomes the most attractive for the electrons and its potential is large enough to be able to remove all electrons from the *internal Gate* (see Fig. 4.5a).
If a sufficiently positive voltage ($\sim +15\,\mathrm{V}$ relative to the Source voltage) is applied at the *Clear implant*, a punch-through will be established to the *internal Gate*.

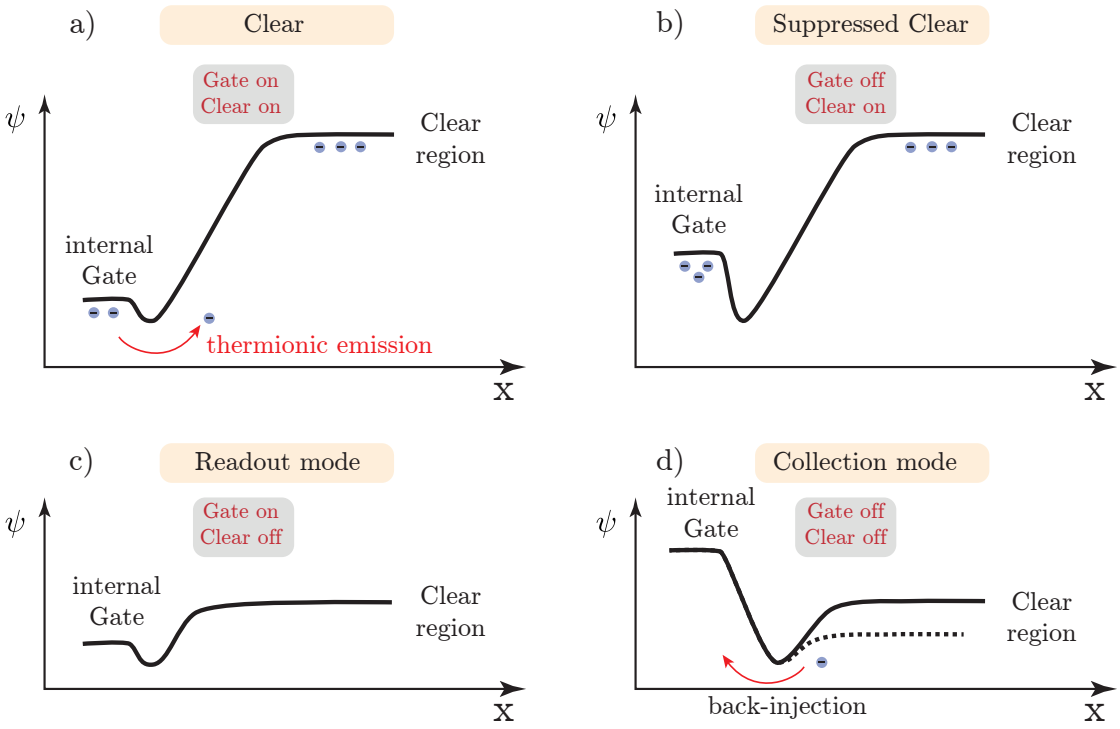


Figure 4.5: Sketches of the potential distribution between *internal Gate* and *Clear region*. a) Real Clear: The electrons are attracted to the positive potential at the *Clear implant*. b) Suppressed Clear: The potential barrier between the *internal Gate* and the *Clear region* is too large, such that the electrons remain in the *internal Gate*. c) Readout mode: The DEPFET pixel cell is enabled while the Clear mechanism is disabled to sample the Drain current. d) Collection mode: The DEPFET and the Clear mechanism are both disabled. The dashed lines represents a very low Clear voltage which could result in back-injection.

Since the electrons move to the most positive potential, they drift from the *internal Gate* to the *Clear region*. The Clear mechanism is only performed when the DEPFET pixel cell is reset, i.e., to empty the *internal Gate*. During the charge collection mode a small positive voltage is applied at the *Clear implant*. The resulting potential distribution is shown in Fig. 4.5d.
In addition, a p well (deep p implant) is located beneath the *Clear implant* to prevent *back-injection*, i.e., to prevent electrons injecting from the *Clear region* (back) into the *internal Gate*. The p implant is shown in Fig. 4.6. It is a negative space charge that shields the *Clear region*. Otherwise, the *Clear region* would be more attractive for the signal electrons than the *internal Gate*.
This additional p implant causes an inflection point of the potential distribution across the bulk, which is shown for optimal Clear and Backside voltages in Fig. 4.6a. The local potential minimum for the signal electrons is indicated by the dashed yellow line, which defines the path of drifting electrons from this region (local minimum) to the *internal Gate*. Increasing the Clear voltage (Fig. 4.6b) results in a decreased barrier between the potential minimum and the *Clear region*. A fraction of the electrons drifting within the bulk to the potential minimum could overcome this barrier and further move to the *Clear implant*. This charge is

"lost" and does not contribute to the overall signal. Decreasing the Backside voltage (to more negative values) shifts the potential minimum upwards (Fig. 4.6c). In addition, it lowers the potential well. As a consequence, some electrons could overcome the barrier (between potential minimum and *Clear region*) and drift to the *Clear implant*. Optimal Clear and Backside voltages must be found in order to collect all of the electrons that are created within the silicon bulk (the measurements will be presented in Sect. 6.11). The Clear voltage should not be too low (back-injection occurs, supported by the measurements shown in Sect. 6.11) nor too large (decreased charge collection efficiency).

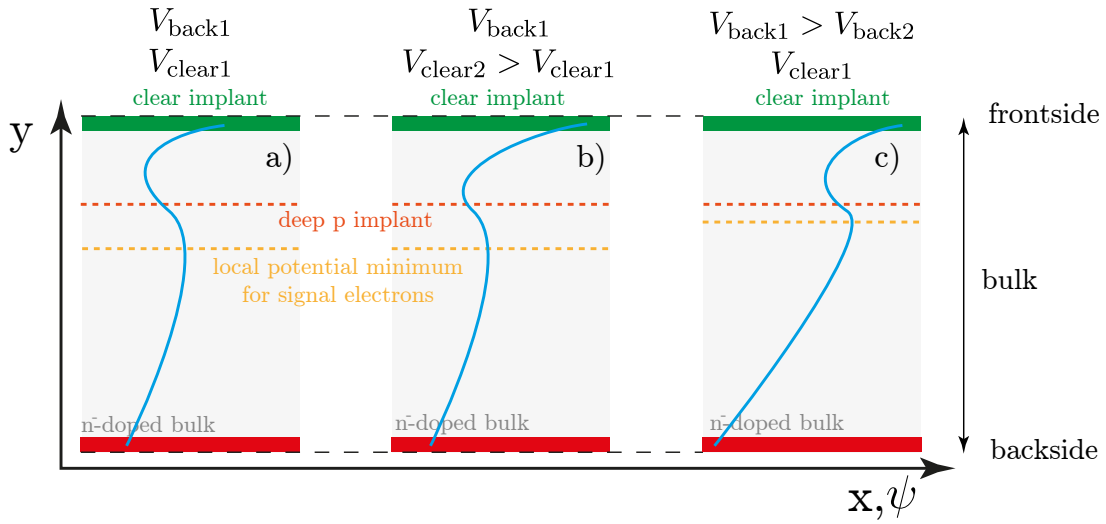


Figure 4.6: Cross-section of a DEPFET pixel cell below the *Clear implant*. a) Potential distribution within the silicon bulk for optimal voltages (V_{back1}, V_{clear1}). b) Increasing the Clear voltage decreases the potential barrier above the deep p implant ($V_{\text{clear2}} > V_{\text{clear1}}$). c) Decreasing the Backside voltage (more negatively) also decreases the potential minimum below the deep p implant ($V_{\text{back2}} < V_{\text{back1}}$).

ClearGate The *ClearGate* is a polysilicon structure separating the DEPFET MOS transistor and the *Clear region* (see Fig. 4.4). In order to understand the task of the *ClearGate structure*, the charge collection/integration must be distinguished from the Clear mechanism.
In the charge collection mode, the *ClearGate* forms a potential barrier between the *internal Gate* and the *Clear region*, as illustrated in Fig. 4.5d. During the Clear process this barrier should be low enough so that the electrons can drift easily to the *Clear implant* (Fig. 4.5a). There are two possibilities to vary the voltage applied at the *ClearGate* and thus change the height of the barrier. The first possibility is that the ClearGate voltage could be controlled directly. Therefore, an additional control circuitry is mandatory. The space required for these control lines is not available in the pixel design for the PXD. The second possibility, which is used for the PXD, is to introduce a capacitive coupling, which is discussed in detail in [137, section 12]. Applying the Clear voltage affects the ClearGate potential (capacitively coupling). Thus, the ClearGate potential becomes more positive and the potential barrier between the *internal Gate* and the *Clear region* decreases.

These methods support the Clear process. The electrons can traverse the potential barrier by thermionic emission and can drift to the n^+ implant. After having removed all electrons from the *internal Gate*, the DEPFET pixel cell is ready for the next measurement.

Figure 4.5 shows sketches of the potential distribution between the *internal Gate* and the *Clear region* for different scenarios.

- **Real Clear mechanism** (Fig. 4.5a)**:** The MOSFET is enabled. The conductive channel shields the *internal Gate* from the *external Gate*. The potential of the *internal Gate* becomes negative while the potential at the *Clear region* becomes positive. The electrons in the *internal Gate* can overcome the small potential barrier (created by the *ClearGate*) by thermionic emission and drift to the *Clear implant*. Due to the capacitive coupling of the *ClearGate* to the *Clear*, the barrier decreases.
- **Suppressed Clear** (Fig. 4.5b)**:** The potential of the *internal Gate* is shifted by applying positive Clear voltage since there is no shielding to the *external Gate*. The potential barrier (between the *internal Gate* and the *Clear region*) is too large for electrons to drift to the *Clear implant*.
- **Readout mode** (Fig. 4.5c)**:** The potential of the *Clear region* is much lower (compared to the Clear process) since a smaller positive Clear voltage is applied at the *Clear implant*.
- **Collection mode** (Fig. 4.5d)**:** The potential barrier is larger (due to the non-existing shielding from the *external Gate*). If this Clear voltage is too low, the potential distribution changes such that the *internal Gate* is more attractive for the electron in the *Clear region* than the *Clear implant*. This is shown by the dashed line. In this case, electrons could move from the *Clear region* to the *internal Gate*. This is called *back-injection*. As a result, the signal is distorted.

Circuit Diagram

A circuit diagram representing the DEPFET is shown in Fig. 4.7. The current of the MOSFET is modulated by the *external Gate* and the *internal Gate*. The charge stored in the *internal Gate* can be removed by applying a sufficiently high Clear voltage. The *Clear* is capacitively coupled to the *ClearGate structure*, which controls the potential barrier between the *internal Gate* and the *Clear implant*.

4.4.3 Pixel layout

The working principle and operation voltage of a single DEPFET pixel (cell) has been introduced in the previous section. In order to form a larger sensitive area, the individual DEPFET pixel cells are arranged in a two-dimensional grid. This results in a large *DEPFET matrix*. The economic and compact layout to place many DEPFET pixel cells in close environment are described in this section.

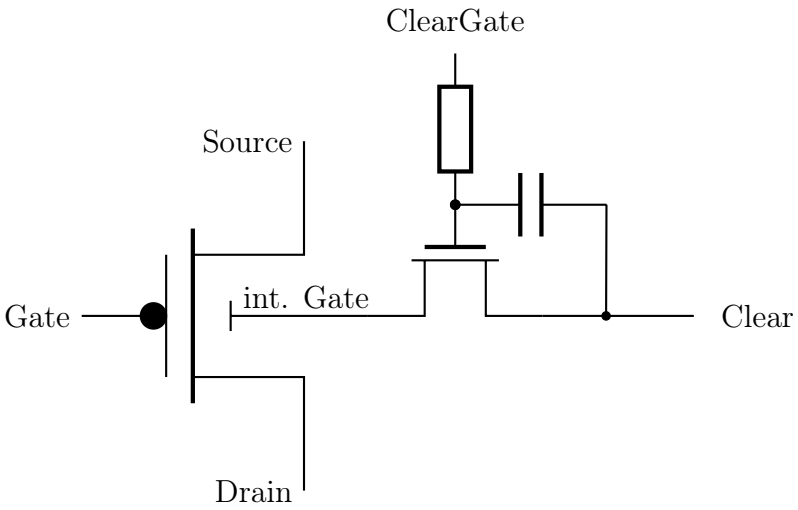


Figure 4.7: Circuit (diagram) of the DEPFET. The Drain current is modulated by the voltage at the *external Gate* and by the amount of charge stored in the *internal Gate*. The *internal Gate* is reset by applying a sufficiently high voltage at the *Clear*. The *ClearGate*, creating a potential barrier between the *internal Gate* and the *Clear region*, is capacitively coupled to the *Clear*.

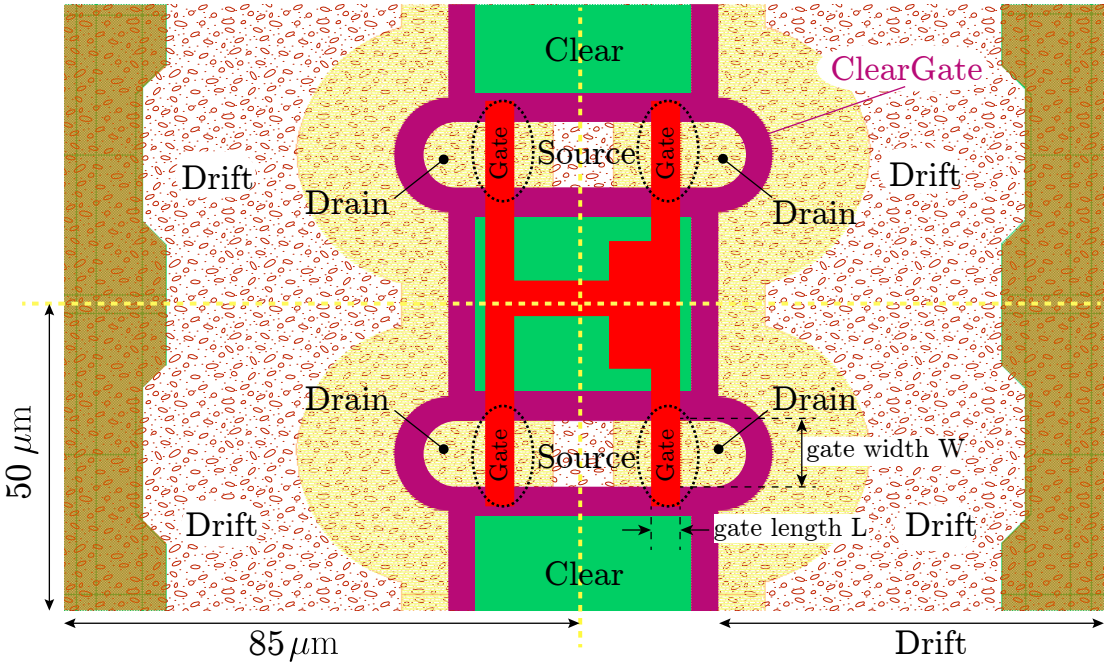


Figure 4.8: Layout of PXD9 DEPFET pixel sensor module. Two pixels share a common *Source implant* and a common *Clear implant* [136]. Color code: purple: polysilicon 1 (*ClearGate*), red: polysilicon 2 (*external Gate*), green: n^+ implant (*Clear implant*), light yellow: n implant (also *internal Gate*), red pattern: p implant (drift), orange: additional drift implants.

Various different designs have been simulated, produced and tested to arrive at the final Belle II design. The analysis and characterizations of the different designs

and layouts can be found in [137–140]. Different DEPFET prototype sensors with various pixel designs and different thicknesses have been produced, for instance, PXD5 with 450 µm thick active area and PXD6 with a thinned sensitive area of 50 µm. The current design is called PXD9 where the active area has a thickness of 75 µm.
The DEPFET pixel layout for Belle II is shown in Fig. 4.8. The pixel cell structure consists of two layers of polysilicon and various p and n implants. Figure 4.8 shows two double cells, i.e., four DEPFET pixels which are separated by the yellow dotted lines. The purple ellipses which are connected by vertical straight lines denote a polysilicon layer, called *poly1*. This layer forms the *ClearGate* structure. It separates the MOSFETs (*Source implant*, *external Gate structure*, *Drain implant*), the *Clear implant* and the surrounding drift region. The red rectangles in the middle depict another polysilicon layer, called *poly2*. This layer forms the *external Gate*, i.e., the Gate of the MOSFET between the *Source implant* and the *Drain implant*. An n^+ implant is located in the green squares, bounded by the *poly1*, between the individual pixels. Those are the *Clear regions*. These implants are above and below a pixel pair, i.e., at both sides of the *internal Gate*, providing a fast and rigorous Clear mechanism. The orange/brown regions at the boundaries of the pixels in Fig. 4.8 are additional p implants, decreasing the drift time for electrons to the *internal Gate*. Around the *poly1* structure n implants (yellow pattern) are arranged as large ellipses to pull the electrons in the direction of the *internal Gate*, i.e., they increase the drift fields. In addition to this, these ellipsoidal implants serve as barrier for holes which could be emitted from the *Source implant* to the p^+ doped backside.

4.4.4 Operation voltages for a DEPFET matrix

The basic voltages for the operation of a single DEPFET pixel were already described in Sect. 4.4.2. Arranging multiple DEPFETs in a matrix form, additional metallic connections (called *metallization*) and biasing for its operation are needed, which is introduced in this section.

Depletion One way is to create a p^+ implant on the backside of the bulk, which supports the depletion of the entire silicon substrate by applying an appropriate negative Backside voltage (relative to the Source voltage). Therefore, a wire-bond has to be connected to the thin sensitive part making the backside processing more complicated. Another approach is the *punch-through mechanism*, which is described in detail in [138]. In this case, an electrode is connected to a p^+ implant on the front side (*punch-through contact*). Applying a sufficiently negative Backside voltage, the entire silicon bulk becomes depleted. The depletion process can be divided into five phases (compare to Fig. 4.9) (for 75 µm thick silicon):

1. Applying a negative Backside voltage at the punch-through contact, the depletion of the area around the p^+ implant expands ($\sim -35\,\mathrm{V} < V_{\mathrm{backside}} < 0\,\mathrm{V}$).
2. At approximately $-35\,\mathrm{V}$ the backside is reached and a bulk current is flowing.

3. The depletion expands from the backside and the bulk gets depleted ($\sim -70\,\mathrm{V} < V_{\mathrm{backside}} < -35\,\mathrm{V}$).
4. At approximately $-70\,\mathrm{V}$ the entire bulk is depleted. This defines the Depletion voltage. Interface, surface and bulk currents appear.
5. Further decreasing the Backside voltage results in a saturation of the current. Furthermore, the minimum potential within the bulk is shifted.

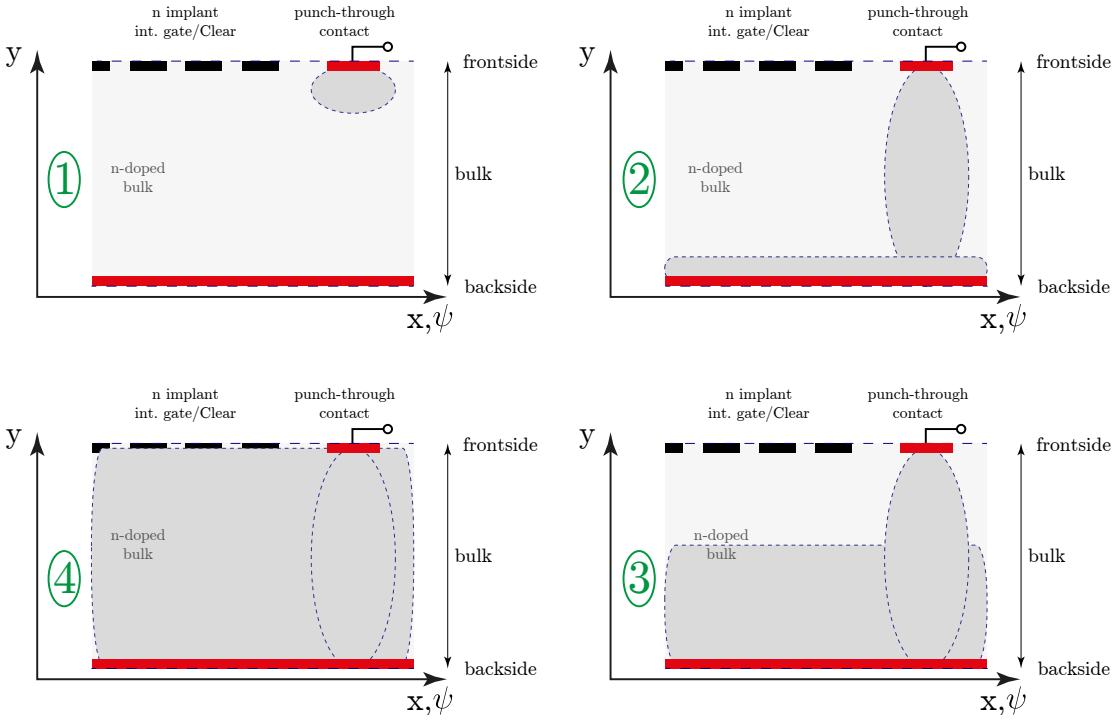


Figure 4.9: The depletion of the silicon bulk is performed in four phases. *Phase 1:* Applying a negative voltage at the *punch-through contact* starts to deplete the area around the implant. *Phase 2:* At $\sim -35\,\mathrm{V}$ the backside is reached (for 75 µm silicon). *Phase 3:* The bulk starts getting depleted. *Phase 4:* The entire silicon bulk is completely depleted.

When the entire silicon bulk is fully depleted, the holes, which mainly originate from leakage currents (at the surface) and from the bulk (due to thermally created electron-hole pairs), drift through the n^- bulk to the p^+ layer at the backside. They further move along the backside in the direction to the *punch-through contact* while they overcome a small potential barrier. Those holes are responsible for the punch-through current. A sketch of the punch-through effect and the potential distribution between the pixel and the backside are illustrated in Fig. 4.10. For a detector consisting of multiple DEPFETs, a single implant for the entire active region is sufficient.

Drift The distribution of the potentials within the silicon bulk for the integration time are shown in Fig. 4.11. The movement of the electrons in the silicon bulk is mainly due to two drift fields, the vertical and the lateral ones. The process of

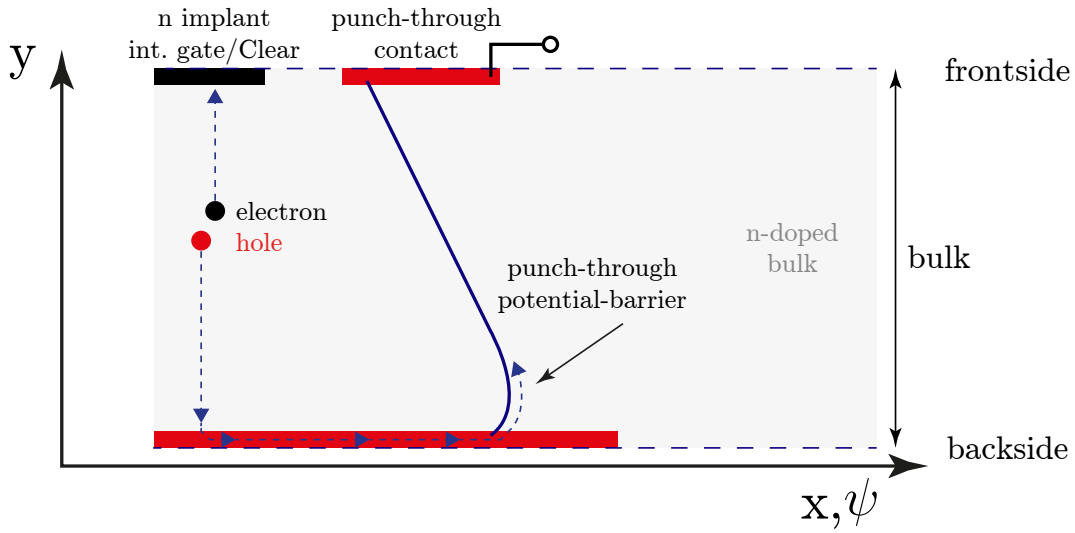


Figure 4.10: Sketch of the punch-through mechanism [138]. Applying a sufficiently negative Backside voltage makes the holes drift to the p^+ backside. They move along the implant on the backside. Afterwards, they overcome a small potential barrier and cross the bulk to the punch-through contact.

the charge collection to the *internal Gate* is simplified as follows. First, electrons created in the bulk drift within in a few nanoseconds to the vertical local potential minimum. Afterwards, they are further horizontally shifted into the *internal Gate* (see Fig. 4.12) in a slower process because the lateral drift fields are much weaker compared to the vertical ones. The drift structure, realized by a non-structured p implant (see Fig. 4.8), is biased with a negative potential of approximately $-5\,\mathrm{V}$ (relative to the Source voltage), which would result in an iso-potential plane near the surface and a weaker lateral field in the depth.
In Fig. 4.11b, two potential steps are visible near the surface. These steps are caused by additional deeper implants to increase the lateral drift fields. The p implants at the boundaries (orange/brown) regions in Fig. 4.8 push the electrons into the direction of the MOS structure, causing the potential step 1 in Fig. 4.11. The yellow ellipsoidal n implants in Fig. 4.8 around the *Clear Gate structure* attract the electrons into the direction of the *internal Gate* causing the potential step 2 in Fig. 4.11. Electron trajectories for the charge collection processes are plotted in Fig. 4.12.

Bulk and Guard Special arrangements were made to ensure that electrons created outside of the pixel structure (for instance, from the surrounding support structure) do not enter the sensitive area and distort the signal. To prevent this the entire matrix is enclosed in a ring-like n^+ implant. Applying a Bulk voltage of approximately $+10\,\mathrm{V}$ relative to the Source voltage is sufficient to collect the electrons generated outside the sensitive area and simultaneously deplete the *Bulk* between this implant and the pixels at the border. In addition, a p^+ guard ring implant is situated between the active pixel area and the n^+ doped area. The potential is fixed to $-5\,\mathrm{V}$ (relative to Source voltage). This geometry prevents electrons from outside the sensitive area to drift into the sensitive area.

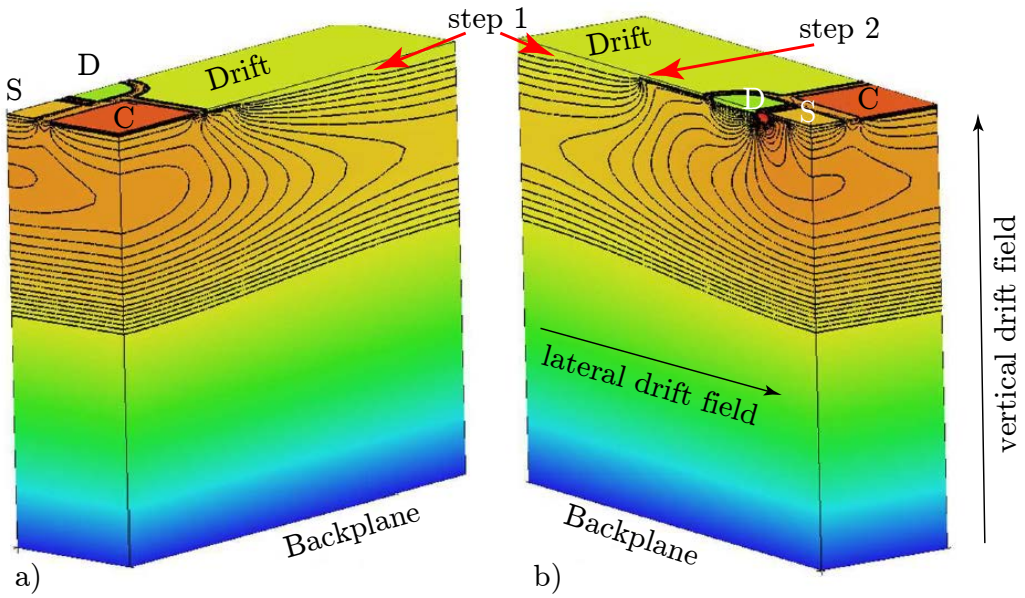


Figure 4.11: Potential distribution within the DEPFET during the charge collection process [136, 141, 142]. **S** denotes the p^+ source implant, **D** is the p^+ Drain implant and **C** is the n^+ *Clear implant*. The two drift fields (vertical and lateral) are marked.

4.5 Electrical connections of DEPFET pixel cells

The individual DEPFET pixels, shown in the layout in Fig. 4.8, must be electrically connected in order to apply the operation voltages. Furthermore, the signal of each individual DEPFET pixel cell must be measured, i.e., the Source-Drain current must be read out from each pixel cell individually. Therefore, two aluminum metal layers are placed on top of the DEPFET structure. Due to space limitations, an ingenious metal routing is required. For example, two pixels share a common *Source implant* and four pixels share the same *Clear implant*. Figure 4.13 shows the pixel structure and the metallization for the electrical interconnections placed on top. The light blue vertical lines are the first aluminum layer, called *alu1*. The Clear, Gate and Drift and Source nets are connected by traces in this metal layer. The second aluminum layer (*alu2*) is placed on top, illustrated by the horizontal dark blue lines. The *Source*, *Gate* and the individual *Drain contacts* are connected to the metal traces of the second aluminum layer. Connections between the two aluminum layers are shown as the small turquoise rectangles, for instance, the connection of the *Drift*, *Gate* and *Drain contacts*. The connections between *alu1* and the silicon bulk are shown as small black rectangles, for instance, *alu1* of the Source net is connected to the silicon bulk in the middle of a two-pixel cell.

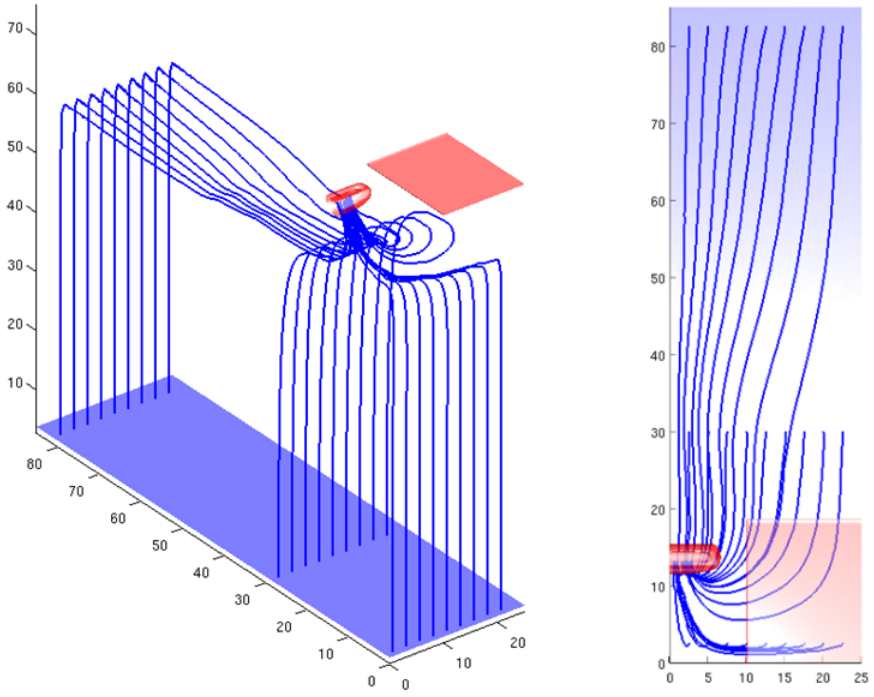


Figure 4.12: The electron trajectories are shown for the charge collection process of a single DEPFET pixel cell. First, the created electrons are shifted upwards, and then drift sidewards to the *internal Gate*, denoted by the small red rectangle [136, 141, 142].

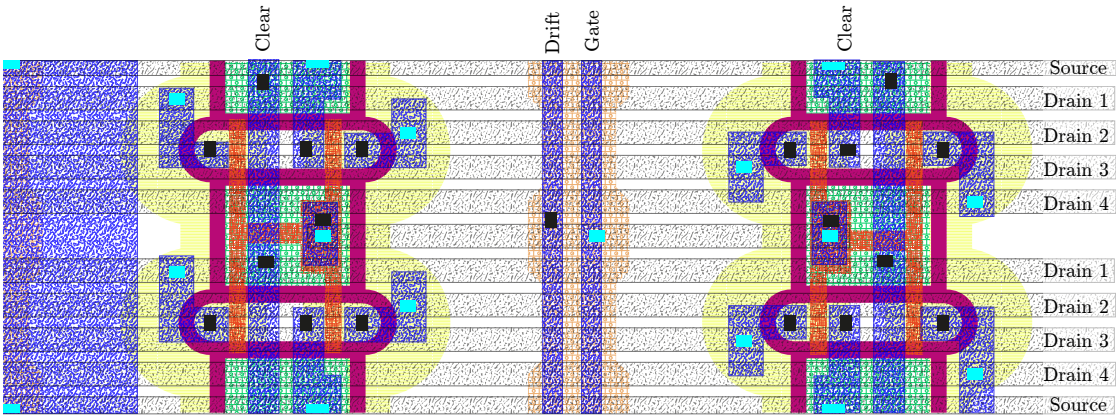


Figure 4.13: Pixel layout and metallization (two layers of aluminum). Same color code as in Fig. 4.8, dark blue: aluminum metal layer 1 (*alu1*), gray: aluminum metal layer 2 (*alu2*), turquoise rectangles: contacts between *alu1* and *alu2*, black rectangles: contacts between *alu1* and silicon.

4.5.1 Amplification

The mathematical treatment of the DEPFET is fully discussed in the app. B.3. The most important equations describing the Drain current (I_{ds}), the external (g_{m}) and internal (g_{q}) amplifications are given in [143]:

$$I_{\mathrm{ds}} = -\frac{W}{L}\mu_{\mathrm{h}}C_{\mathrm{ox}}\frac{1}{2}\left[f\frac{Q_{\mathrm{sig}}}{WLC_{\mathrm{ox}}} + V_{\mathrm{G}} - V_{\mathrm{T}}\right]^2 \tag{4.5.1}$$

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{G}}} = -\frac{W}{L}\mu_{\mathrm{h}}C_{\mathrm{ox}}\left[V_{\mathrm{G}} - V_{\mathrm{T}} + f\frac{Q_{\mathrm{sig}}}{WLC_{\mathrm{ox}}}\right] = \sqrt{\frac{2W\mu_{\mathrm{h}}C_{\mathrm{ox}}}{L}}\sqrt{I_{\mathrm{ds_{sat}}}} \tag{4.5.2}$$

$$g_{\mathrm{q}} = \frac{\partial I_{\mathrm{ds}}}{\partial Q_{\mathrm{sig}}} = -\frac{f\mu_{\mathrm{h}}}{L^2}\left[V_{\mathrm{G}} - V_{\mathrm{T}} + f\frac{Q_{\mathrm{sig}}}{WLC_{\mathrm{ox}}}\right] = f\sqrt{\frac{2\mu_{\mathrm{h}}}{WL^3C_{\mathrm{ox}}}}\sqrt{I_{\mathrm{ds}}} \tag{4.5.3}$$

$$g_{\mathrm{q}} = g_{\mathrm{m}}\frac{f}{WLC_{\mathrm{ox}}} \tag{4.5.4}$$

where W and L denote the width and length of the transistor (see Fig. 4.8), μ_{h} is the mobility of the holes, $C_{\mathrm{ox}} = \frac{\varepsilon_{\mathrm{ox}}\varepsilon_0}{d_{\mathrm{ox}}}$ is the oxide capacitance per unit area with ε_0 being the vacuum permittivity, $\varepsilon_{\mathrm{ox}}$ the dielectric constant of the oxide and d_{ox} the width of the oxide layer (see Fig. 4.4). V_{G} and V_{T} are the Gate and threshold voltages, Q_{sig} is the signal charge stored in the *internal Gate* and $f \in (0, 1]$ is the coupling factor describing how much of the charge in the *internal Gate* will be induced into the channel.

4.5.2 Effects influencing the signal

Two effects may distort the signal (drain currents) of the DEPFET pixels. *Leakage current* originates from *thermal generation* of charge carriers within the silicon bulk. It increases exponentially with temperature ($I_{\mathrm{leakage}} \propto T^2 e^{-1/T}$) [144]. *Surface current* is generated at the depleted interface between the semiconductor and the oxide. The electrons drift into the *internal Gate* resulting in a Source-Drain current modulation while the holes contribute to the Source-Drain current. The impact of these effects is negligible for non-irradiated DEPFETs.
In addition, shot noise, (channel) thermal noise, flicker noise, electronic noise from the readout electronics and common mode noise may distort the signal. The effects are discussed in Sect. 4.14.

4.6 Readout mechanisms

Different readout mechanisms for the DEPFETs are possible. The advantages and disadvantages of each method are discussed in the following. The DEPFET pixel cell is switched on by applying a sufficient low Gate voltage relative to the Source voltage and the signal is measured. Afterwards, the pixel is reset by applying the Clear pulse.

Source Follower

In the source follower mode, the Source-Drain current is constant and the Drain voltage is fixed. Assuming a constant voltage applied at the *external Gate*, the Source voltage depends on the charge stored in the *internal Gate*. This readout mechanism cannot be used for the PXD at Belle II because of the large setting times, which depends on the capacitance of the amplifier and the DEPFET capacitance [137]. Therefore, another readout mechanism is used, called the *drain follower*. The method and the settling time of the source follower are discussed in [145].

Drain Follower

In contrast to the source follower method, the Source, Drain and Gate potentials are set to constant voltages in the Drain follower mode. In this case, the Drain current of the DEPFET depends on the charge stored in the *internal Gate*. Measuring the current is done with a low input resistance and consequently the rise time is sufficiently small, in the order of a few nano-seconds (for small test matrices with low parasitic capacitance) [137]. A disadvantage is the increased sensitivity to bulk damage [145]. Nevertheless, this mechanism has been chosen for the PXD at Belle II.

Correlated double sampling

In the correlated double sampling readout, the current is measured twice, once before and once after applying the Clear pulse (see Fig. 4.14a). Taking the first sample before the Clear pulse, the modulated current is measured consisting of the sum of the signal & *pedestal current*, where the *pedestals* are defined as readout current without any signal. Having applied the Clear pulse in order to remove the electrons stored in the *internal Gate* it is sampled again to obtain the pedestal value. The signal is the difference between the pedestal after the Clear pulse and the sample before the Clear pulse, i.e., the charge stored in the *internal Gate* can be calculated. In this case the $1/f$ noise is mostly eliminated (due to fast sampling). However, the thermal noise (see Sect. 4.14) is increased by a factor of $\sqrt{2}$ because the samples of the signal & pedestal and pedestal are uncorrelated and the white noise is recorded twice. Furthermore, at least two sampling points are needed resulting in a longer readout time compared to the single sampling introduced in the next paragraph. The readout time T_{readout} and the signal current I_{signal} are given as:

$$\begin{aligned} T_{\text{readout}} &= T_{1^{\text{st}}\text{ sample}} + T_{\text{Clear pulse}} + T_{2^{\text{nd}}\text{ sample}} \\ I_{\text{signal}} &= I_{\text{pedestal \& signal}} - I_{\text{ped}}, \end{aligned}$$

where $T_{i^{\text{th}}\text{ sample}}$ denotes the time period for the i^{th} sampling, $T_{\text{Clear pulse}}$ is the time period for the applied Clear pulse, $I_{\text{pedestal \& signal}}$ is the current of the pedestal & signal and I_{ped} is the pedestal current.

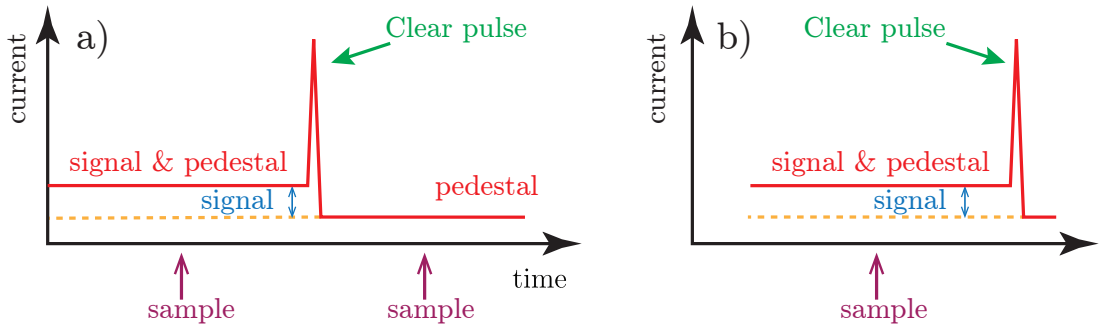


Figure 4.14: a) Correlated double sampling; two sampling points before and after the Clear pulse are measured. The difference yields the DEPFET signal. b) Single sampling; one sampling point is measured before the Clear pulse. One obtains the DEPFET signal by subtracting the average of the pedestals. The Drain current shows a spike during the Clear procedure since the large positive voltage change the transconductance of the MOSFET.

Single sampling

The method chosen for the PXD is the single sampling readout (see Fig. 4.14b). The current is measured only once, and the main advantage is the reduction of the readout time. However, pedestals are needed to obtain an average pedestal current $\langle I_{\text{ped}} \rangle$. Using this information, the signal is obtained by calculating and subtracting the average of the pedestals. Using this method, analog-to-digital converters (ADCs) are required with a large dynamic range (see Sect. 4.8.2) to resolve the signal and the pedestal current. In contrast, for the correlated double sampling method, ADCs with a smaller dynamic range are sufficient since the pedestal current is subtracted from the signal & pedestal currents in the readout electronics before the current is digitized by the ADC. Using this method requires stable pedestals, i.e., they must not vary over time. The readout time T_{readout} and the signal current I_{signal} are given by:

$$T_{\text{readout}} = T_{1^{\text{st}}\text{ sample}} + T_{\text{Clear pulse}}$$
$$I_{\text{signal}} = I_{\text{pedestal \& signal}} - \langle I_{\text{ped}} \rangle$$

4.7 Control and Readout Scheme

The matrix operates in the *rolling shutter mode*, i.e., row-wise readout. In order to speed up the readout process, a four-fold readout scheme is applied. The *Clear contacts* and *Gate contacts* of four consecutive DEPFET pixel rows are connected to a single *Clear electrode* and a single *Gate electrode*, respectively. The connection of the *four-fold* readout scheme is shown in Fig. 4.15.
The number of controlled Gate (and Clear) rows is reduced by a factor of four, i.e., only 192 Gates and Clears output drivers are required instead of 768. Since every pixel should be read out individually, the number of Drain lines is increased four times. Thus, 1000 Drain lines must be measured for a single Gate electrode.

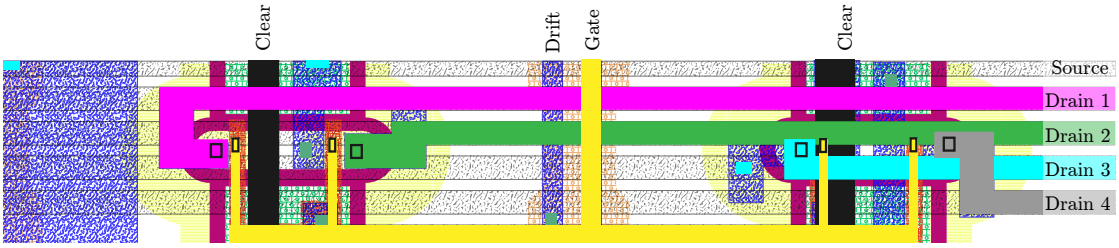


Figure 4.15: Metalization of the DEPFET pixels; the *four-fold* readout scheme is highlighted. Common *Gate* and *Clear lines* control four pixels in a row; therefore four Drains lines are required to measure the Drain currents of all individual pixels.

Therefore, the Gate output $i \in [1, 192] \cap \mathbb{N}$ is switched on by applying a negative voltage relative to the Source voltage. Hence, all DEPFETs connected to this Gate output are enabled and the Drain currents are measured. After the measurements the Clear pulse is applied and the transistors are switched off. In the next step, the Gate output $i + 1$ is switched on. A sketch of the rolling shutter readout is shown in Fig. 4.16.

In order to distinguish between electrical rows (corresponding to Gate and Clear electrical connections) and geometrical rows (i.e., geometrical arrangement of the pixels) the nomenclature of Tab. 4.2 is used. The conversion is as follows (start to

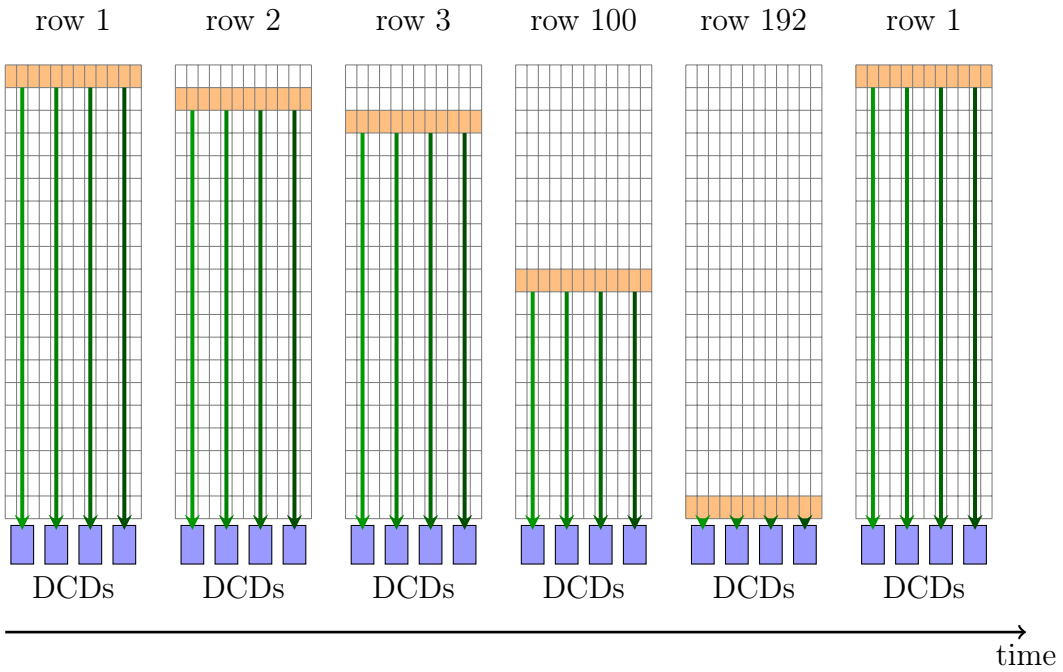


Figure 4.16: Sketch of the *rolling shutter readout* mechanism. The DEPFET pixels are enabled row-wise and their Drain currents are read out consecutively (from left to right). The orange row depicts the active Gate row. The green arrows represent the direction of the Drain currents flowing into the DCDs.

Table 4.2: Nomenclature of geometrical and electrical rows and columns.

Format	Name	Abbreviation
geometrical	geometrical row	$\mathrm{row}_{\mathrm{geo}}$
	geometrical column	$\mathrm{col}_{\mathrm{geo}}$
electrical	electrical row (gate)	$\mathrm{row}_{\mathrm{gate}}$
	electrical column (drain)	$\mathrm{col}_{\mathrm{drain}}$

count with row 0 and column 0) [124]:

$$\mathrm{row}_{\mathrm{geo}} = 4 \cdot \mathrm{row}_{\mathrm{gate}} + \mathrm{col}_{\mathrm{drain}} \mathrm{mod} 4 \tag{4.7.1}$$

$$\mathrm{col}_{\mathrm{geo}} = \left\lfloor \frac{\mathrm{col}_{\mathrm{drain}}}{4} \right\rfloor \tag{4.7.2}$$

$$\mathrm{row}_{\mathrm{gate}} = \left\lfloor \frac{\mathrm{row}_{\mathrm{geo}}}{4} \right\rfloor \tag{4.7.3}$$

$$\mathrm{col}_{\mathrm{drain}} = 4 \cdot \mathrm{col}_{\mathrm{geo}} + \mathrm{row}_{\mathrm{gate}} \mathrm{mod} 4 + \cdot \mathrm{ID}_{\mathrm{DHP}} \tag{4.7.4}$$

where ID denotes the number of the DHP and $\lfloor \ldots \rfloor$ is the floor function.

4.8 ASICs

Control and readout electronics are required for a proper operation of the modules. For the rolling shutter mode, the Gate and Clear voltages must be changed within a few nanoseconds. The Drain currents must be digitized and filtered for the relevant data above a certain threshold (zero-suppression) and finally transferred to the data acquisition (DAQ) system. Since no commercial devices are available, custom-made ASICs are demanded. A schematic overview is shown in Fig. 4.17. The various ASICs are introduced here. Their detailed functionalities and features are explained in this section. The *Switchers* perform the control of the Clear and Gate lines. The DCDs are installed for the digitization of the Drain currents[4]. The digital signal from the DCD is transmitted to the DHP, which extracts real signals from pedestals (zero-suppressing). This serves as data reduction. Furthermore, the DHP transmits its data through a Kapton cable through the data handling hub (DHH) to the PXD DAQ system. All ASICs are configured via a Joint Test Action Group (JTAG) chain. The JTAG master interface is the DHH.

4.8.1 Switcher

The Gate and Clear channels are controlled by the *Switcher* ASICs [146]. Each Switcher has 32 channels, hence six Switchers are mounted on a module for 192 Gate and Clear lines. They are able to switch Clear voltages ($\Delta U_{\mathrm{clear}} = 28\,\mathrm{V}$)

[4] Although the DCD has 256 channels only 250 are connected to the Drain lines of the matrix.

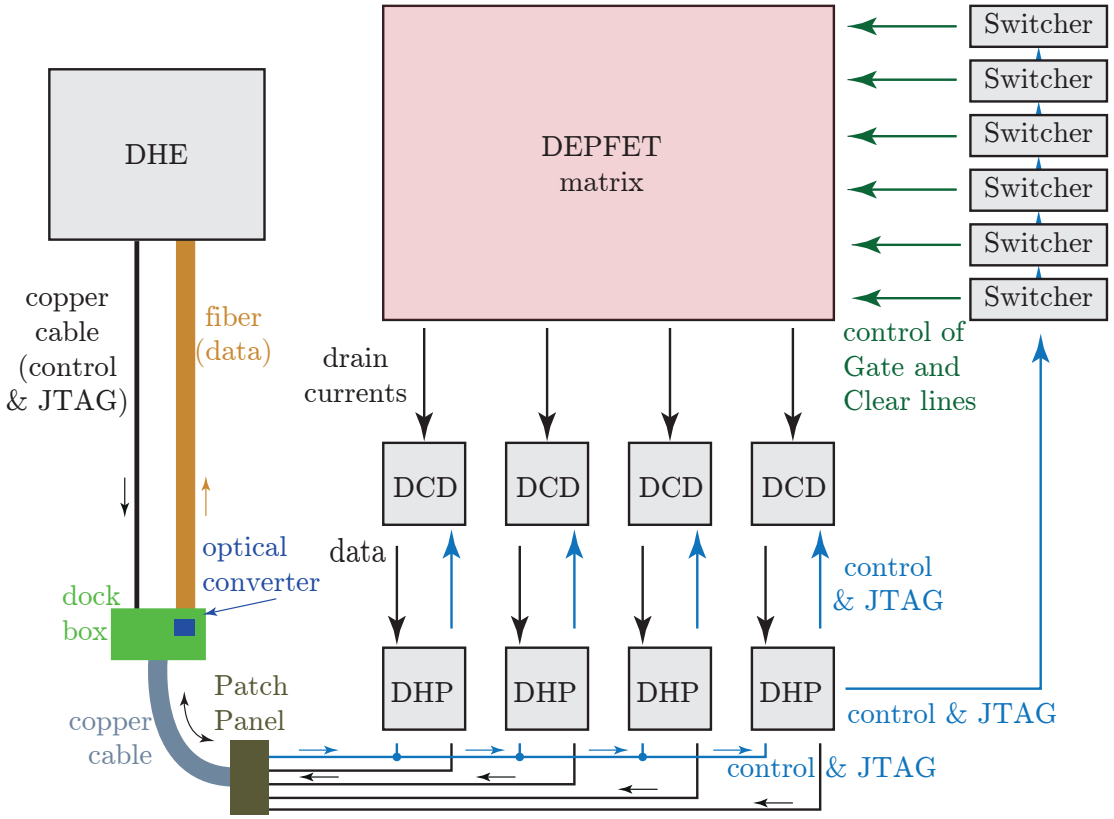


Figure 4.17: Sketch of the various ASICs and their functions. The DHPs are connected to the DHH off-module control.

and Gate voltages ($\Delta U_{\text{gate}} = 18\,\text{V}$) within 20 ns for a capacitive DEPFET load of 130 nF [147]. The Switchers must withstand the harsh radiation of SuperKEKB. Moreover, the power consumption must be quite low since they cannot be cooled actively. They are controlled by four different differential control signals: `SerIn`, `Strobe Clear` (`StrC`), `Strobe Gate` (`StrG`) and `Clock`. Moreover, several registers can be set, such as the termination (sets a 100 Ω resistor at the four control nets). The different versions that have been produced and tested are listed in Tab. 4.3. The latest Switcher version (SwitcherB18v2.1) has been tested at the beginning of 2017. In this iteration, the termination resistors for the four control signals can be set individually, in contrast to the previous versions. They are all produced by the semiconductor manufacturer, formerly known as Austria Micro Systems (AMS).

Switcher sequence

The Switcher allows different operation modes, listed below:

- **Non-overlapping Gates:** The electrical rows are switched on consecutively, i.e., when the electrical row i is switched off, the electrical row $i + 1$ is switched on.
- **Overlapping Gates:** Two electrical rows are switched on simultaneously for a few nanoseconds. If two DEPFETs sharing the same Drain line are in the

Table 4.3: Switcher versions and properties. The output voltage is referenced to ground. The latest version has termination resistors for each control net [147–149]. The Gated Mode is explained in Sect. 6.12

Name	SwitcherB33	SwitcherB18v1.0	SwitcherB18v2.0
Technology	AMS 350 nm	AMS 180 nm	AMS 180 nm
Chip size	2030 × 3600 µm^2	1470 × 3600 µm^2	1470 × 3627 µm^2
Supply voltage	3.3 V	1.8 V	1.8 V
Output voltage	≤ 50 V	≤ 20 V	≤ 50 V (20 V swing)
Gated Mode	no	no	yes

on-state, the currents add up, distorting the signal. Therefore, the overlap has to be short and should not interfere with two consecutive measurements.

- **Skip mode:** Certain Gate outputs can be skipped, i.e., they are not enabled.

A sketch of the control signals and the output drivers for the normal Switcher operation (non-overlapping gates) is shown in Fig. 4.18.
The data handling processor from TSMC (DHPT) contains a Switcher sequence memory for two times 512 128-bit memory words. Each 128-bit word is composed of four 32-bit sub-blocks for each Switcher control signal. Each sub-block encodes the control of one Gate and one Clear output driver of the Switcher. The 128-bit word is divided as shown in Tab. 4.4. This encoding allows a flexible and user-defined control sequence for the Switcher.

Table 4.4: The sequence of the four Switcher control signals are encoded into a 128-bit memory word.

bits	function
$[0, \ldots, 31]$	`SerIn` memory
$[32, \ldots, 63]$	`Strobe Clear` memory
$[64, \ldots, 95]$	`Strobe Gate` memory
$[96, \ldots, 127]$	`Clock` memory

Signal Timing:
One of the 32 bits, also called a *tick* in the following, is applied at a rate of 305 MHz. This results in a readout time of approximately 105 ns for the control of a Gate (Clear) signal for a single electrical DEPFET matrix row. For lab measurements, another clock operation frequency, corresponding to 250 MHz for the DCD, is available. The clock distribution is explained in detail in app. C.1.
The Switcher sequence must be implemented carefully, taking the requirement for proper operation into account:
A negative voltage, relative to the Source voltage, must be applied at the *external Gate contact*[5] of the MOSFET to obtain a conductive channel below the *external*

[5]since the DEPFET is a PMOS transistor

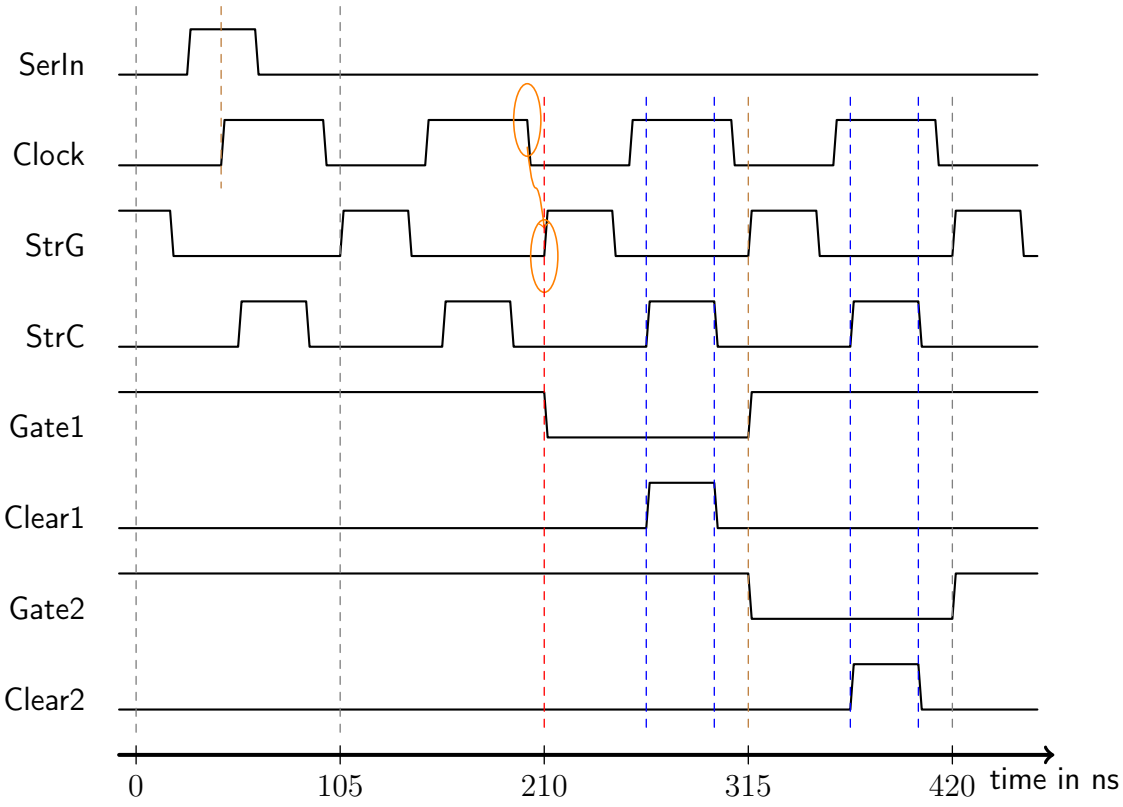


Figure 4.18: Normal Switcher sequence. The wave forms of the control signals and the output drivers are shown schematically [147]. The vertical black and red line indicate that the first Gate row is enabled after two clock cycles of the `SerIn` signal. In addition, the rising edge of `Strobe Gate` must be after the falling edge of the `Clock`, marked with the orange ellipses. The blue lines indicate the lengths of the Clear pulses, corresponding to the lengths of the `Strobe Clear`. The Gates rows are enabled successively, i.e., the next Gate row is activated when the previous one is disabled. This is controlled by the rising edge of `Strobe Gate` (brown line).

Gate (see Fig. 4.18). Therefore, the GateOn voltage is lower compared to GateOff. For the Clear behavior it is the other way around. The ClearOn voltage is higher compared to the ClearOff voltage. Within the DEPFET project the following nomenclature is also used:

GateOn	=	GateLow		GateOff	=	GateHigh
ClearOn	=	ClearHigh		ClearOff	=	ClearLow

The Switcher control signals and their timing are explained in the following:

• **SerIn:** The `SerIn` signal is applied once (in the Switcher sequence) for the entire readout cycle of the matrix. The `Clock` must be *high* when the `SerIn` signal is applied (see Fig. 4.18). It defines the active Switcher channel, i.e., it defines the channel within the Switcher for which the applied `Strobe Clear` and `Strobe Gate` signals are processed. Hence, the control for the output drivers is only granted for this particular channel. The other outputs are not active, i.e., ClearOff and GateOff voltages are applied. The `SerIn` signal is clocked (by the Switcher clock) through a 32-bit deep shift register. The active channel is delayed by two clock cycles. The sketch of the Switcher shift register and the switching of the active channel is shown in Fig. 4.19.

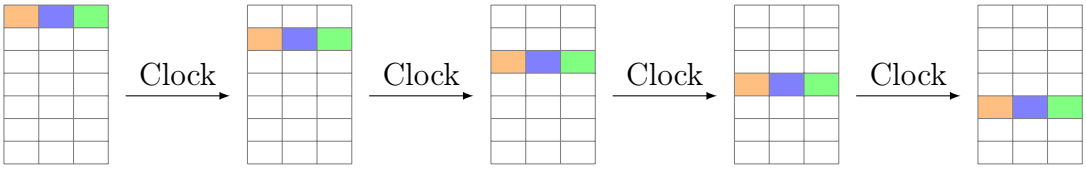


Figure 4.19: Sketch of the active Switcher output drivers. The 32 rows correspond to the 32 Switcher output drivers (Gate and Clear). The orange cell denotes the active channel. The blue cell depicts the active Gate output and the green cell is the active Clear output. They are shifted with each Switcher clock cycle. Only the active channel responds to the control signals `Strobe Clear` and `Strobe Gate`.

The Switcher also has a `SerOut` signal, which actually forwards the `SerIn` signal to the next Switcher (this `SerOut` of previous Switcher is the `SerIn` of the next Switcher). Hence, it is possible to operate several Switchers in series. While the `SerIn` signal is connected in series, `Strobe Gate`, `Strobe Clear` and `Clock` are connected in parallel as shown in Fig. 4.20.

• **StrG:** When the `Strobe Gate` is *high* (the `Clock` must be *low* during the rising edge) the Gate of the active channel is enabled, i.e., the GateLow voltage is applied. The next channel is switched on when the `Clock` shifts the `SerIn` to the next entry in the shift register and and the `Strobe Gate` signal is applied again. Consequently, the readout time could be extended for a specific row i by skipping the `Strobe Gate` signal in the Switcher memory[6] for row $i + 1$.

[6]The entire readout cycle must be extended by additional 32 ticks to have only a single `SerIn` signal in the entire Switcher chain.

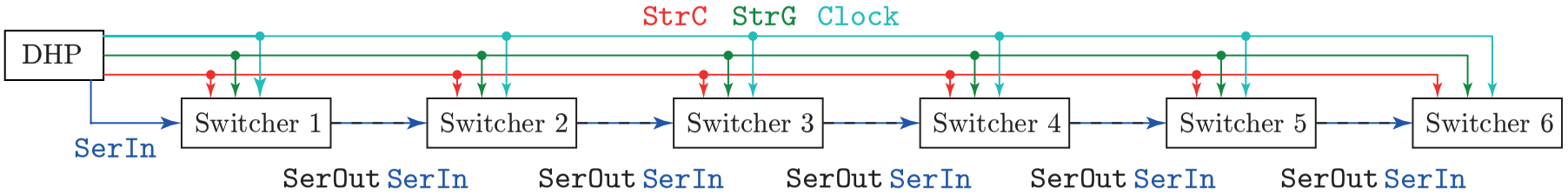


Figure 4.20: Connection between DHP and the Switchers. The `Strobe Clear`, `Strobe Gate` and `Clock` are connected in parallel, whereas the `SerIn` is connected in series. The `SerOut` of the Switcher i serves as `SerIn` for the next one $(i + 1)$.

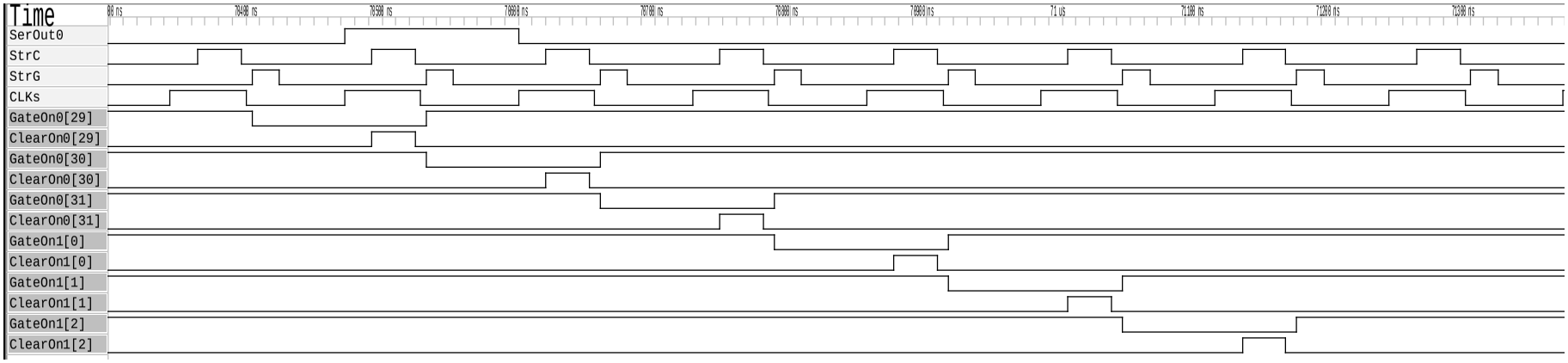


Figure 4.21: Verilog simulation of Switcher output driver for six consecutive gates. The three last outputs of Switcher 1 and the three first outputs of Switcher 2 are shown.

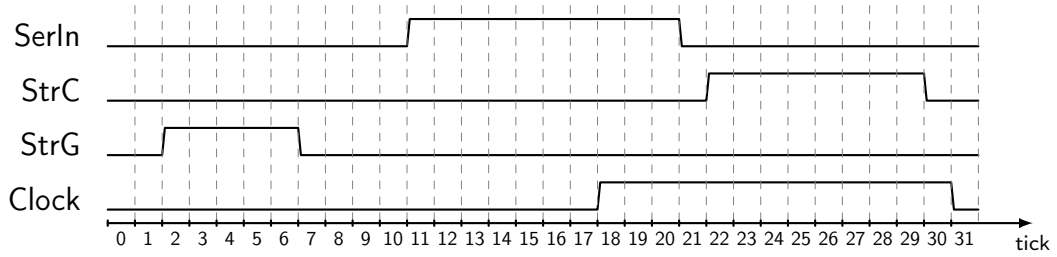


Figure 4.22: The Switcher control sequence for 32 bits. The `SerIn` signal is only applied once per frame. This illustration corresponds to the 128-bit word, which encodes the `SerIn` pulse.

• **StrC:** The `Strobe Clear` signal is applied only when the Gate is enabled and the `Clock` is *high*. As long as the `Strobe Clear` signal is applied as logical 1, the ClearOn voltage is applied at the active channel. It can be set in $1/32 \cdot T_{\text{period}}$ steps, i.e., tick-wise. Due to the parasitic capacitance of the Clear lines on the PXD modules, the `Strobe Clear` should be applied at least for four ticks.

• **Clock:** The `Clock` is applied at the Switcher to synchronize the circuits. A duty cycle of 50 % is not required as shown in Fig. 4.22.

The same Switcher control sequence for a single channel (`Strobe Clear`, `Strobe Gate` and `Clock`) is repeated for all 192 128-bit words. The only difference is the `SerIn` signal, which will be described in detail in Sect. 4.8.4. The optimal sequence for non-overlapping gates has been developed and is shown in Fig. 4.22.
A simulator of the Switcher ASIC in Verilog has been set up [150] using the Switcher logic [147]. The simulation of non-overlapping gates in shown for six consecutive gates in Fig. 4.21.

4.8.2 Drain Current Digitizer (DCD)

The Drain current digitizer (DCD) measures the Drain currents of all DEPFETs pixels [146, 151, 152]. With 8-bit precision and a sampling rate of 100 ns, the ADCs convert the currents into a digital signal [153]. The pedestal current is in the range of 100–120 µA [154]. The stored electrons in the *internal Gate* contribute only

Table 4.5: DCD versions and properties [153, 155, 156].

Name	DCDB(v2)	DCDBv4pp
Technology	UMC 180 nm	UMC 180 nm
Chip size	$3240 \times 4969\,\mu m^2$	$3240 \times 4969\,\mu m^2$
Supply voltage	1.8 V	1.8 V
ADC	two cyclic	pipeline ADCs
max. clock	400 MHz	400 MHz

approximately 10–15 % to the Drain current [136]. Therefore, a pre-defined amount of current is subtracted from the Drain current. This leaves a smaller current in the dynamic range to be digitized. Besides this, a compensation current can be added to each DEPFET individually, resulting in an even narrower pedestal distribution. The ASIC is configured via JTAG. The different versions of the DCDs are listed in Tab. 4.5. They are produced by United Microelectronics Corporation (UMC). The concept of the DCD, the electronic circuits and optimization parameters are explained in detail in [153, 157–159]. A short description of the basic functionality is presented in this section.

DCD working principle

The basic circuit of the DCD is shown in Fig. 4.23. A detailed schematic of the current receiver is shown in Fig. 4.24.

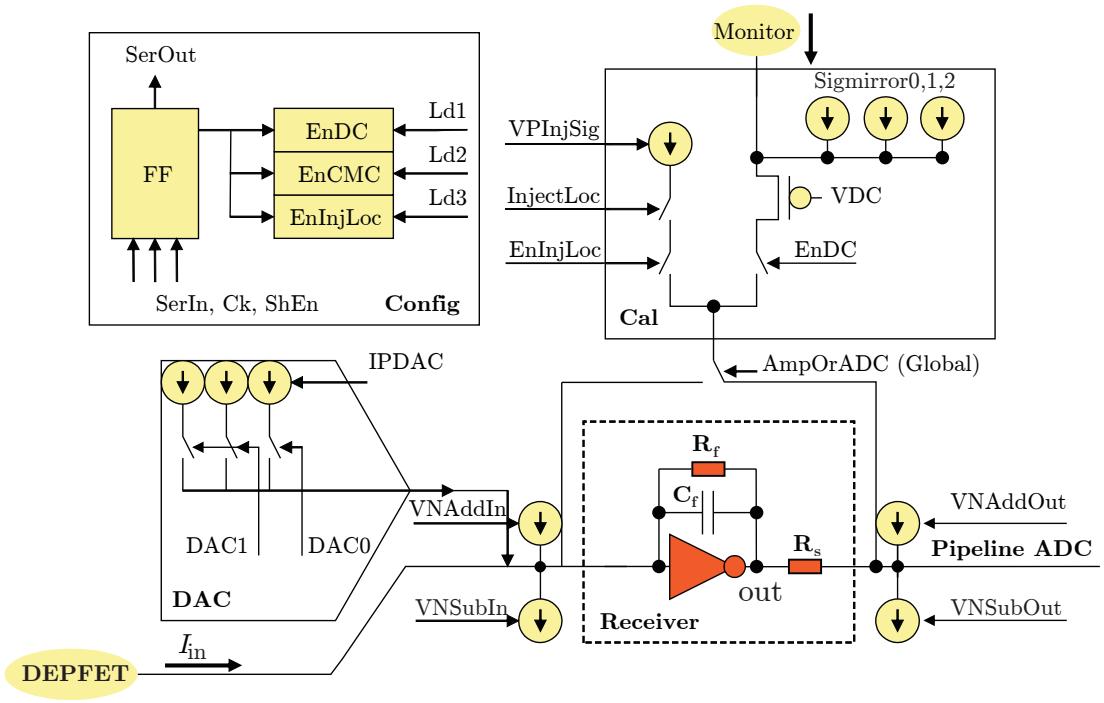


Figure 4.23: The basic analog circuit of the DCD [153]. The DEPFET Drain current is labeled as I_{in}.

The DCD receives the DEPFET Drain current as input current (I_{in}) with a certain voltage V_{in}. An individual current can be added for each DEPFET pixel with the amount of $I_{\text{DAC-glo}}$=`IPDAC` $\times z$, $z \in \{0, 1, 2, 3\}$ (see Sect. 6.9). In addition, current can be added (`VNAddIn`) and subtracted (`VNSubIn`) globally, i.e., the same amount of current for all 256 input channels, before it flows into the receiver (see Fig. 4.23). Alternatively, an analog common mode correction is enabled, which controls the amount of current flowing into the receiver (see Sect. 4.14.3). The current receiver is composed of a transimpedance amplifier and an output resistor. It keeps the input potential (i.e., the DEPFET Drain voltage) constant and amplifies the signal. Different combinations of capacitors and resistors can be added to the feedback path via JTAG, like the capacitor C_f and resistor, R_f, to adjust the timing constant

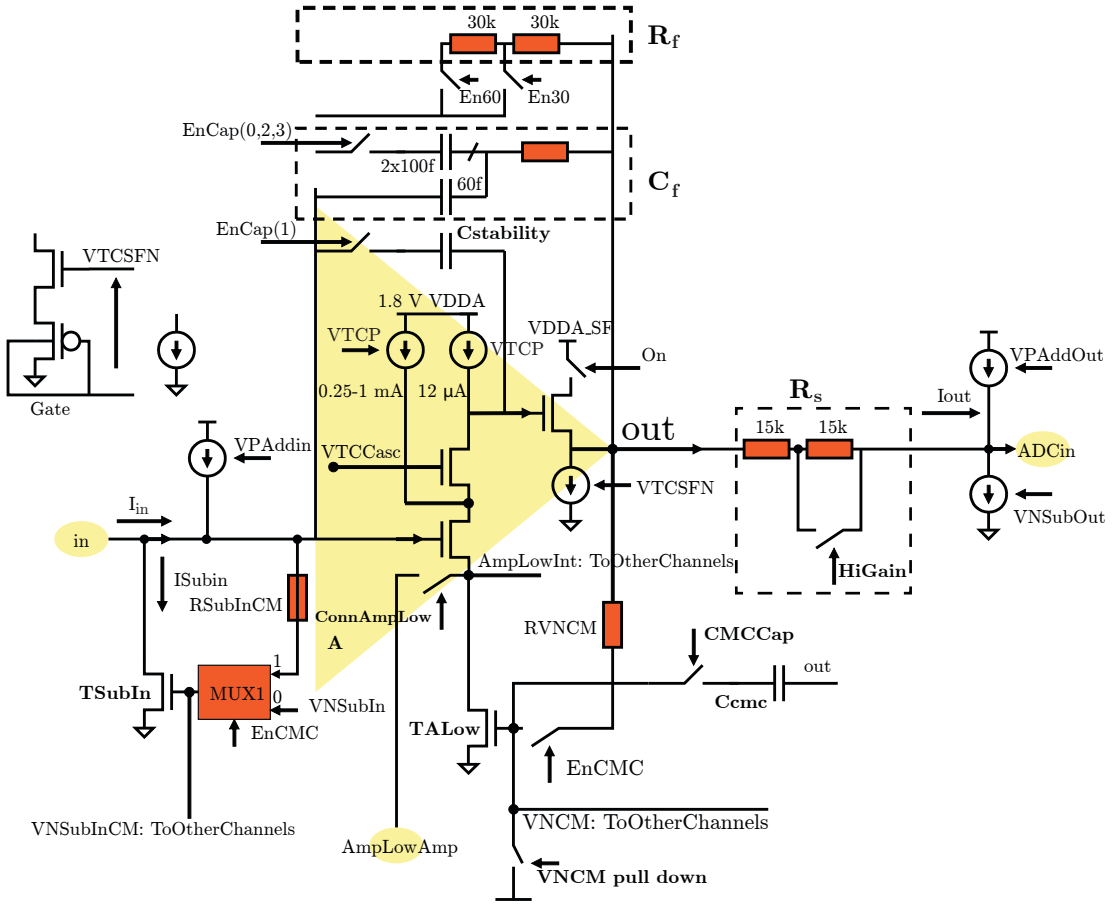


Figure 4.24: The DCD current receiver [153]. Additional current sources (and sinks) can be set to adjust the dynamic range and gain of the ASIC.

$\tau \sim C_f R_f$. The advantages of using a transimpedance (compared to a regulated cascode) amplifier are the signal-independent time constant and variable gains (see below). The current is converted to a voltage $V_{out} = V_{in} - I_{in} R_f$ by the amplifier, which is applied at the output node (`out`). An additional current source (`VNAddOut`) and sink (`VNSubOut`) allow adding (and removing) globally a specific amount of current to all input channels. An additional resistor R_s converts the voltage into a current (in order to keep the input voltage at the ADC at a constant potential [159]), which flows into the ADCs, given as

$$I_{out} = I_{offset} - \frac{R_f}{R_s} I_{in} \tag{4.8.1}$$

where $I_{offset} = (V_{in} - V_{ADCin})/R_s$ can be compensated by the current sources (and sinks) `VNAddIn`, `VNSubIn`, `VNAddOut`, `VNSubOut`. The value $R_f/R_s =: G$ is defined as the *gain*, which adjusts the granularity of the ADC and consequently the dynamic range (i.e., the maximal current that the DCD can measure). Four different combinations can be chosen in the version DCDBv4pp, where two are the same denoted by 2 and $\tilde{2}$, by setting the switches `En30`, `En60` and `HiGain`, which are listed in Tab. 4.6. The maximum dynamic range is stated with 16 µA in [153].

Table 4.6: Different combinations of R_f (`En30`, `En60`) and R_s (`HiGain`) adjusting the gain of the transimpedance amplifier. The check marks represent closed switches and the dashes represent open switches (see Fig. 4.24). Rough values for the measured gains in [nA/ADU] and the measured dynamic ranges are given. The dynamic ranges are smaller compared to the theoretical values due to the non-linearity behavior at the lower and upper boundaries.

Gain	R_f	R_s	`En30`	`En60`	`HiGain`	amplification	dyn. range
1	30 kΩ	30 kΩ	✓	-	-	139 nA/ADU	31 µA
2	30 kΩ	15 kΩ	✓	-	✓	87 nA/ADU	19 µA
$\tilde{2}$	60 kΩ	30 kΩ	-	✓	-		
4	60 kΩ	15 kΩ	-	✓	✓	57 nA/ADU	12 µA

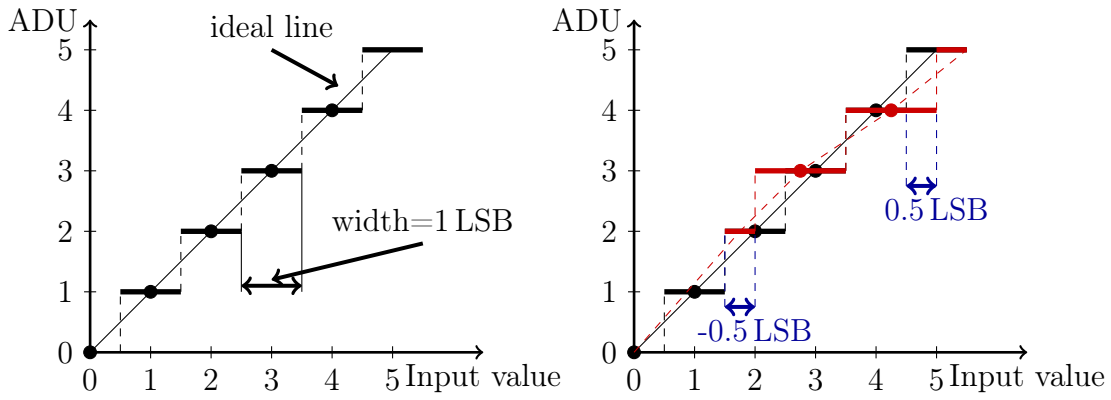
Dedicated measurements regarding the dynamic range are presented in Sect. 6.4.

Calibration of ADCs

A *monitor pin* has been designed for calibration purposes, which is connected to a dedicated contact of the DCD. An external current source can be attached to this pin (referenced to analog ground (AGND)). In this way, a well-known current can be injected directly into the ADCs, which then can be optimized in terms of integral non-linearity (INL), differential non-linearity (DNL) and *missing codes*, which will be explained in this section. The DCD can be configured via the JTAG and the ADC(s) can be selected to which the monitor pin is connected. In this way, the current can be "guided" from the external current source into a dedicated ADC. This has the following disadvantages:

- To calibrate all ADCs, each receiver must be connected to the monitor pin in sequence.
- The monitor pins of all four DCDs mounted on a module are connected in parallel on the metal system of the module. The parallel connection reduces the number of wire-bond pads and metal routing lines on the modules and also the number of traces in the Kapton cable. As a result, the calibration cannot be performed for all four DCDs in parallel.
- The DCD current is limited to roughly 40 µA. In contrast, the DEPFET Drain current is approximately $100 - 120$ µA. Thus, only the gain for the low currents can be calibrated. Using this method, it is assumed that the gain does not change for larger currents.

A precise calibration of all ADCs revealed that the gain is the same for all receivers of a single DCD. Consequently, to obtain the conversion factor (for each DCD channel) from analog-to-digital unit (ADU) to nano Ampere, it is sufficient to characterize a few ADCs of each DCD. Six out of 256 input channels are not connected to the DEPFET sensor on the modules. They are suited for calibration purposes with the external current source.



(a) Ideal ADC transfer curve. The ideal line crosses the steps at the center.

(b) DNL error: The ideal step width is shown as black line, the problematic (non equal) step widths are indicated in red. There can be both positive and negative errors.

Figure 4.25: Sketches of ADC transfer curves. An ideal curve and another one with DNL errors. See text for details.

Transfer curves

The DCD must be optimized before it can be used for reliable and sophisticated measurements of the DEPFET pixel Drain currents. In order to characterize the proper functionality of the DCD, *ADC transfer curves* are considered.

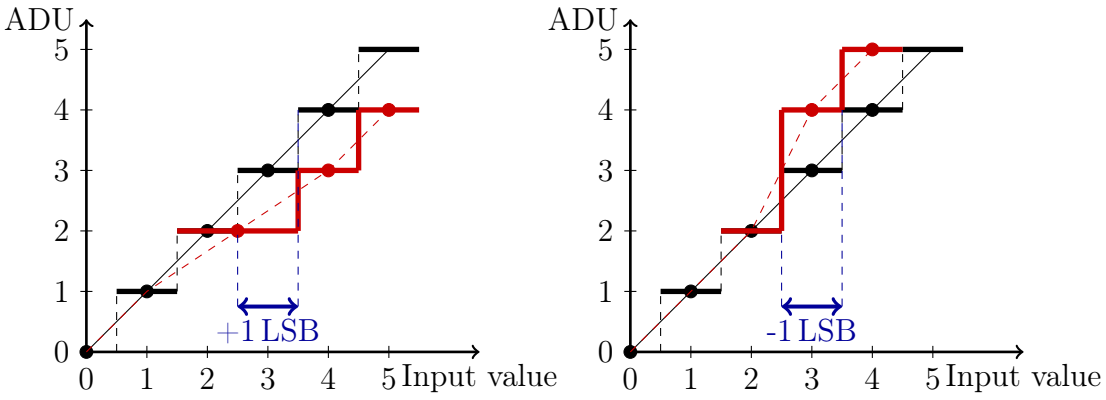
An ADC converts the input voltage (analog signal) into a digital output code. Since an 8-bit ADC is used, the DCD can output a total of 256 digital values (*codes*). The output code as a function of the input signal results in a staircase characteristic due to the discrete output values. An ideal transfer curve function (infinite resolution) is shown in Fig. 4.25a as straight line. The step width is defined as the least significant bit (LSB). Assuming a dynamic range of 16 µA and an 8-bit ADC, the LSB becomes:

$$1\,\mathrm{LSB} = \frac{\text{dyn. range}}{\#\,\text{steps}} = \frac{16\,\mu\mathrm{A}}{2^8 - 1} = 62.5\,\mathrm{nA} \tag{4.8.2}$$

However, a real ADC behaves differently. It could have a specific offset, a different gain, or DNL and INL errors, as explained in the following:

- **Differential non-linearity (DNL):** The differential non-linearity is the deviation of the real step width from the ideal one, as shown in Fig. 4.25b. It can have either a negative value, if the step width is smaller than 1 LSB, or a positive value, if the step width exceeds 1 LSB. Errors of LSB=1 are called *wide codes*, see Fig. 4.26a. (For the ideal ADC the DNL is zero by definition)
- **Missing codes:** *Missing codes* occur if the step width is zero (DNL=−1) for certain input values. Thus, a binary code (ADU) is skipped. An example is shown in Fig. 4.26b.

- **Offset error:** The offset point is defined as the midpoint of the zeroth output code. Figure 4.27a shows two transfer functions with a positive offset (red) and a negative offset (blue) on the x-axis.
- **Gain error:** Assuming no offset error the gain error is defined as the difference on the y-axis between the real transfer function and the ideal one. This results in a difference of the slopes. Figure 4.27b depicts two gain errors with different slopes.
- **Integral non-linearity (INL):** In the first step, a straight line (ideal line in Fig. 4.28) from the two ends of the transfer function is drawn, when the offset and gain errors are compensated. Next, the deviations of the transfer function (i.e., from the midpoints of each output code) to this straight line is calculated. The integral non-linearity error is measured by the difference on the y-axis (see Fig. 4.28).



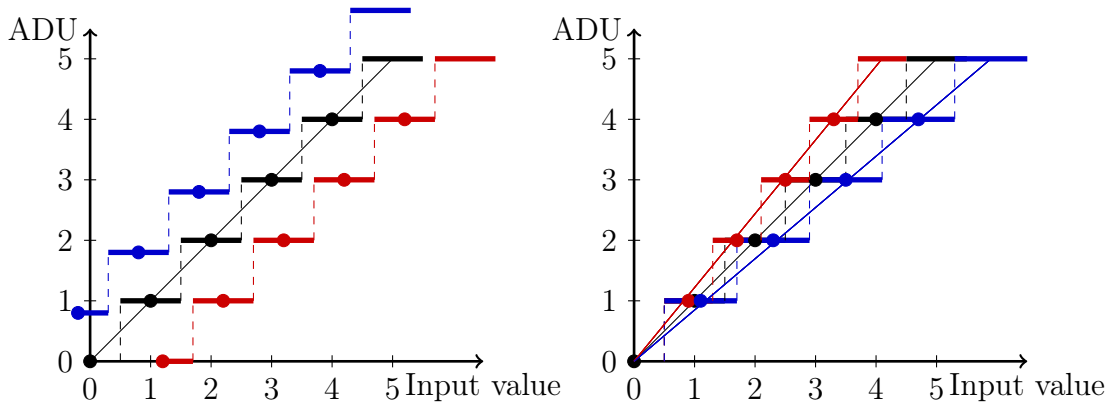
(a) The red curve depicts a *wide code*, i.e., a DNL error of +1.

(b) The red curve depicts a *missing code*, i.e., a DNL error of -1.

Figure 4.26: Sketches of ADC transfer curves with missing codes and wide codes. See text for details.

Impact on the PXD resolution

If the DCD is not optimized, missing codes (DNL=-1) could occur in the worst case. In that case the input signal height is not converted properly to a digital output value. Dedicated studies were performed [160] to estimate the impact of missing codes on the resolution of reconstructed tracks for pixels of $50 \times 55\,\mu m^2$, corresponding to the smaller pixels in the innermost layer close to the beam pipe. Assuming a cluster signal of less than 20 ADUs and missing codes up to 4 ADUs, the vertex position resolution deteriorates by less than 0.2 µm. For the same signal and missing codes of 8 ADUs the resolution deteriorates by less than 0.9 µm. In addition, two extreme cases were analyzed. The position resolution is not affected if the signal is cut above 25 ADUs. Moreover, assuming binary readout, the resolution becomes worse on average by $\sim 2\,\mu m$.



(a) Offset Error: The midpoint of the zeroth output code does not match with the origin. There can either be a positive offset (red curve) or a negative one (blue curve).

(b) Gain error: The deviation of the slopes from the ideal transfer curve corresponds to a gain error. The red and blue curves are examples for gain errors.

Figure 4.27: Sketches of ADC transfer curves with offset errors and gain errors. See text for details.

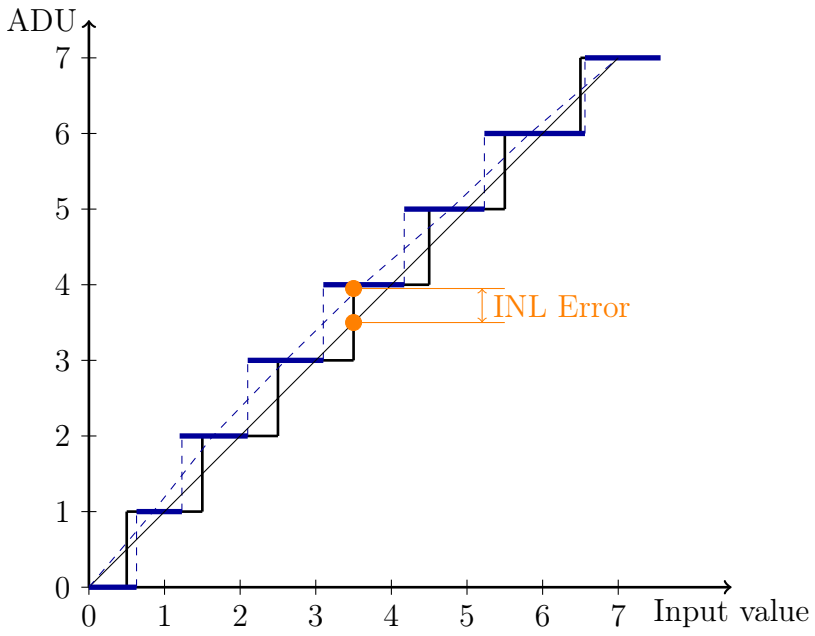


Figure 4.28: The deviations in ADU of the recorded transfer function (blue) to the straight line between the two end points of the transfer function (green) yields the INL error. The green transfer function represents an ideal one.

Recording of Transfer Curves

The measurement of the DCD transfer curves requires a linear current source with low noise. The test current is injected via the monitor pin (see Fig. 4.23). The ADC is connected by enabling the `EnDC` setting (switch) and `pulldown VDC` [153]. There are four different options to calibrate the ADCs with current sources:

1. **DCD internal current source:** Internally the DCD has three global (for all input channels) current sources, `sigmirror 0,1,2`, which are connected to the monitor pin (see Fig. 4.23). Each of them can be adjusted by a 7-bit register (i.e., 128 settings) up to a maximum value of 32.4 µA. The current can be guided via the `EnDC` setting to the input of the selected ADC.
   The internal current sources need to be calibrated in order to know the equivalent amount of current corresponding to one increment of the setting, i.e., one digital-to-analog converter (DAC) value. Therefore, an external Source Measure Unit (SMU) is connected to the monitor pin. The current flows from the DCD to the SMU. All 1024 ADCs (of all four DCDs) are disconnected (disable `EnDC`). The `sigmirror` current sources of each of the four DCDs are scanned from their minimum to their maximum values.
   The advantage of this current source is the integration within the DCD since no external noise can be picked up in the transmission path between the source and the ADC. However, there are also several disadvantages. The granularity of the `sigmirror` current sources is low ($\sim$ 84.5 nA/ADU). It has only 384 DAC settings although the DCD has 256 output codes. Thus, the DNL and INL cannot be studied accurately and missing codes cannot be detected. Another disadvantage is the control, which is quite slow. It is set via the JTAG configuration, which is integrated in the slow control system. Furthermore, the ADCs of the DCD cannot be characterized simultaneously since the monitor pin is connected to all four DCDs.

2. **DHE current source:** The data handling engine (DHE) is equipped with a low noise current source. It provides approximately 190 µA which can be set in increments of 3.82 nA. One core of the DHE has the dedicated task to step the current source through the minimum and maximum values and to send a dedicated trigger to the DHP (to receive data) [161]. The current source allows fine adjustments such that the DNL and INL can be well detected. However, due to the long path from the DHE to the module ($\sim$ on the order of 15 m for the Belle II PXD), additional pickup noise can distort the calibration. Moreover, the ADCs can only be characterized subsequently since the four DCDs share a common monitor net, as already described above.

3. **Source Measure Unit:** One could also use an SMU to calibrate the current receivers in the DCDs. The only difference compared to the DHE current source measurement is the exactly-known current, which flows into the ASICs, and the short cables. Additional low-pass filter must be added to reduce the noise, i.e., the current fluctuation in time.

4. **DEPFET as current source:** To speed up the entire procedure all of the receivers (ADCs) should be characterized at the same time. Therefore, the DEPFETs as current source can be chosen to record the ADC curves. Keeping in mind that the Drain current scales in proportion to the square of the Gate voltage ($I_{\mathrm{ds}} \propto V_{\mathrm{gs}}^2$), the study of the INL is possible only up to a certain extent. However, it is sufficient to calibrate the DCD and optimize it to exclude missing codes and finding parameters for a linear gain [157].

Table 4.7: DHP prototypes and properties [165, 166]. They all have the same size $3280 \times 4200\,\mu m^2$. The latest versions (1.1 and 1.2) include bug fixes of the previous ones. Version 0.2 had a predefined, fixed, non-changeable switcher sequence.

Name	DHP0.2	DHPT1.0	DHPT1.1	DHPT1.2
Technology	IBM 90 nm	TMSC 65 nm	TMSC 65 nm	TMSC 65 nm
individual sw. seq.	no	yes	yes	yes
GatedMode	no	yes	yes	yes

4.8.3 Data Handling Processor (DHP)

The data handling processor (DHP) preprocesses the data from the DCD by discriminating real hits from noise (*zero-suppression*). In addition, it controls and synchronizes the readout and control of the Switchers [162, 163].

For a single frame (i.e., 20 µs) each DCD delivers 49 kB[7]. Since the PXD consists of 40 modules with 4 DCDs each, the total data rate is 7.860 MB per frame, corresponding to 393.000 GB/s. The DHP reduces the data by zero-suppression, i.e., only the data of pixels which have a signal above a pre-defined threshold are sent to the data acquisition system. The others (below the threshold) are not processed further. Moreover, it performs the common mode correction (more details are given in Sect. 4.14.3). Assuming a maximal occupancy of 3 % results in a data rate of approximately 22 GB/s for the entire PXD[8] [164]. The DHP has a 1.6 Gbps high-speed link to send the data to the data acquisition system, which is adequate to transmit all zero-suppressed data at 3 % occupancy with a rate of 30 kHz. The DHP has different memory in order to store the pedestal values, DCD data, the Switcher sequences and the *offset-compensation* values, which will be introduced in Sect. 4.8.7. The DHP0.2 was the first full-sized ASIC, for the data-processing of the Belle II PXD. It was submitted in the middle of 2011. It performed the full data processing, included a Switcher sequencer and a bias generator. Furthermore, the link performance from the DHP to the off-module DAQ system (the DHH) was improved by adding a pre-emphasis to counteract the low-pass filter of the cable. The tests were successful with the exception of minor issues with the maximum speed of the CMOS output clock and the fact that the *Gated Mode* operation (which will be introduced in Sect. 6.12) was not possible. Having changed the technology to 65 nm Taiwan Semiconductor Manufacturing Company (TSMC), two prototypes (DHPT0.1 and DHPT0.2) have been produced and tested in 2011 and 2012. The DHPT1.0 has been developed in mid-2013. It includes improved memory and processing resources, is compatible with the footprint from the previous versions, allows the Gated Mode operation and has two Switcher memories, which can be configured by the user individually. A design error harmed the serializer of DHPT1.0, which resulted in unstable high-speed links between the DHP and the DHH. The problem was fixed with the DHPT1.1

[7] 256 $\text{columns}_{\text{drain}}$ times 192 $\text{rows}_{\text{gate}}$; each pixel has a 8-bit resolution.

[8] Besides the data containing the pixel signal, additional frame headers, pixel positions and common modes value are added to the data stream.

version. An uncontrolled clock phase problem has been encountered and fixed in version 1.2. An overview of the different versions is listed in Tab. 4.7.

High-speed signals between DHP and DHE

The communication between the DHE and the DHPs is realized by JTAG (for the configuration) and by high-speed signal transmission (for the readout of the recorded DCD data). The latter one refers to data rates of 1.6 Gbps using aurora[9] 8b/10b encoding[10] [163]. Each DHP has a separate high-speed data transmission

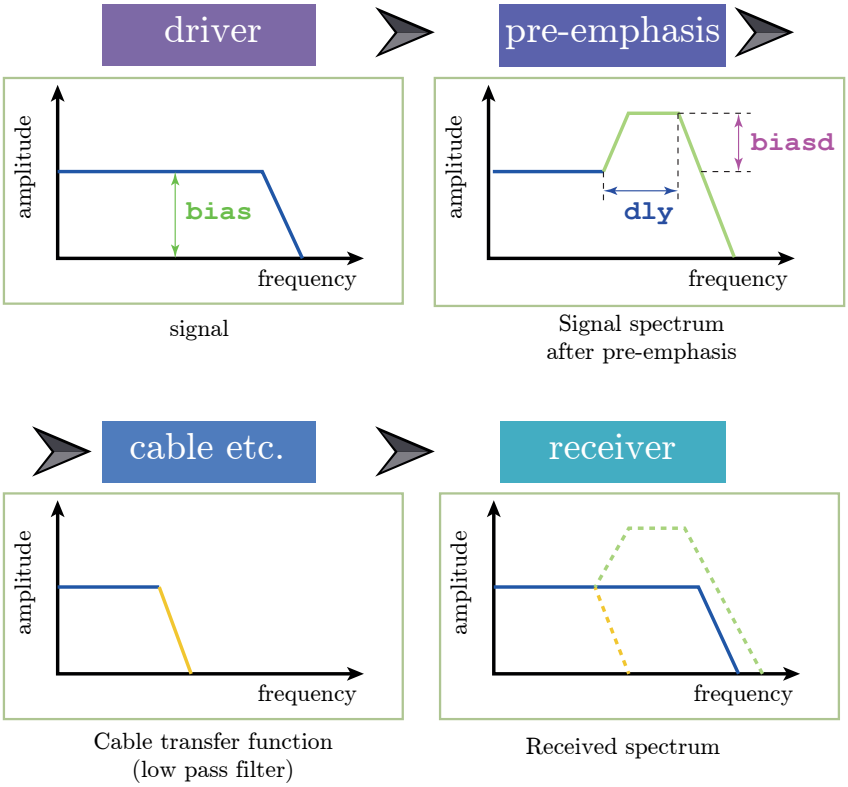


Figure 4.29: Sketch of the signal spectrum of the DHP high-speed link with pre-emphasis [166].

link to the DHE, resulting in four high-speed links for each module. The data is transferred from the ASICs along the silicon module via copper traces to the wire-bond pads. Wire-bonds connect them to the Kapton cable, which is attached to a Patch Panel. From there, the data is transmitted via Infiniband connectors through a shielded cable to a general junction (*dock box*) between the cables coming from the detector and those going to the outside of the Belle II detector (see Fig. 4.17). An optical transmitter converts the electrical signals into optical ones, which are sent by fibers to the DHE.
To correctly send the data along the entire readout chain (routing on silicon module, wire-bonds, Kapton cable and Infiniband), a special Current Mode Logic

[9] The Auroral protocol has been developed by Xilinx for high-speed signal communication.
[10] Symbols of 8-bits are mapped to 10-bit symbols resulting in a reasonable recovery of the clock and providing DC-balance [167].

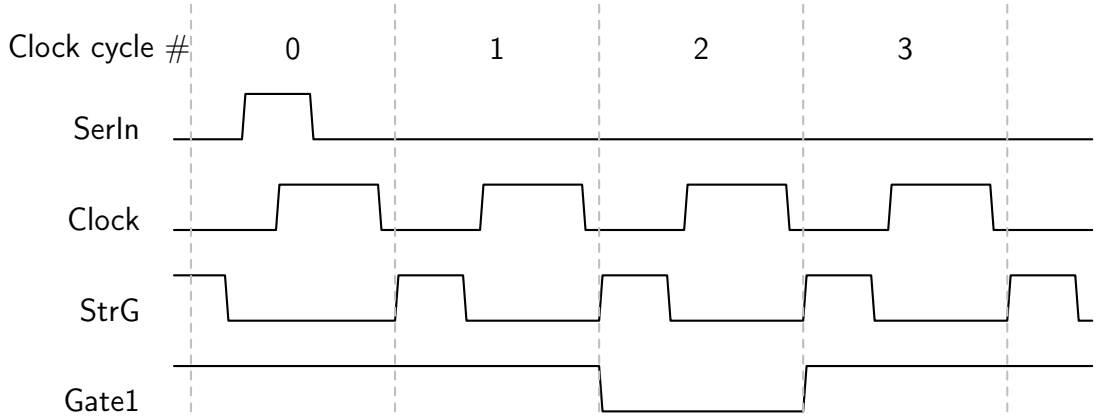


Figure 4.30: Normal Switcher sequence with four clock cycles. The clock cycles are numbered as shown in top of the figure. The wave forms of the control signals and the output drivers are shown schematically [147].

(CML) driver has been developed to compensate the attenuation within the readout chain of the high frequency signal [166] by a pre-emphasis added on the amplitude of the signal. Due to the attenuation, this additional "ripple" vanishes. Hence, the signal at the receiver side is not diminished and can be read properly by the field programmable gate array (FPGA), which is assembled on the DHE. A sketch of the signal spectrum including the pre-emphasis is shown in Fig. 4.29. The output signal can be adjusted by three parameters:

1. `bias`: Amplitude of the signal (8-bit JTAG register `IDAC_CML_TX_BIAS`)
2. `biasd`: Amplitude of the pre-emphasis (8-bit JTAG register `IDAC_CML_TX_BIASD`)
3. `dly`: Width of the pre-emphasis in the time domain (2-bit JTAG register `pll_cml_dly_sel`)

4.8.4 Synchronization between DHP, Switcher and DCD

The signal of a physical pixel ($\mathrm{row_{geo}}$, $\mathrm{col_{geo}}$) must be assigned correctly to the pixel position in the recorded data. Therefore, the synchronization between the Switcher and DHP and the timing between the DCD and the DHP must be correct.

The control of the Switcher has already been discussed in Sect. 4.8.1. The timing diagram of the Switcher is shown in Fig. 4.30. It requires two clock cycles (0 and 1) to process the `SerIn` signal and to enable the first Gate output driver (Gate 1). Thus, if the `SerIn` signal were written in the first data word of the Switcher sequence in the DHP memory, then the entire readout time would be increased by an additional two Gate rows ($2 \cdot \mathrm{row_{gate}}$), corresponding to 209.63 ns at the nominal global reference clock of 76.33 MHz. To overcome this, the `SerIn` signal is applied at the end of the Switcher sequence, in the data word 190, i.e., the `SerIn` is already sent in the previous frame.

Sampling Point Optimization

The Gate rows of the DEPFETs are switched on for 128 ns (using the DHE global clock GCK=62.5 MHz). As already explained in the previous sections, the Switcher sequence for controlling a single Gate and a Clear output driver consists of 32 ticks. One tick corresponds to the DCD clock cycle, 4 ns. The DCD samples the current within 128 ns. This sampling point can be adjusted in 4 ns steps. Thus, the sampling point $t_{\text{sample}} \in [0, 4, \ldots, 124]$ ns can be positioned.
The goal is to find the optimal timing to measure the Drain current, i.e., to find the correct sampling point. To do so, the Drain current is sampled multiple times at all 32 possible sampling points. This allows the measurement of the time evolution of the DEPFET Drain current within the 128 ns. This is done in the following way. As a starting point, the Switcher sequence presented below is written into the DHP Switcher sequence memory and the DEPFET signals are recorded.

net/tick	01 02 03 04 05 06 07 08	09 10 11 12 13 14 15 16	17 18 19 20 21 22 23 24	25 26 27 28 29 30 31 32
SerIn	0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1	1 1 1 1 1 1 0 0	0 0 0 0 0 0 0 0
StrC	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1	1 1 1 1 1 1 1 0
StrG	0 1 1 1 1 1 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Clock	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1	1 1 1 1 1 1 1 1

In the next step, the Switcher sequence is shifted by one tick (illustrated by the red bits) and written into the DHP Switcher sequence memory:

net/tick	01 02 03 04 05 06 07 08	09 10 11 12 13 14 15 16	17 18 19 20 21 22 23 24	25 26 27 28 29 30 31 32
SerIn	0 0 0 0 0 0 0 0	0 0 0 0 0 1 1 1	1 1 1 1 1 1 1 0	0 0 0 0 0 0 0 0
StrC	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1
StrG	0 0 1 1 1 1 1 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Clock	1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 1 1 1 1 1	1 1 1 1 1 1 1 1

The Drain currents are sampled again for the same rows. This procedure of shifting the Switcher sequence by one tick is repeated 31 times. As a result, the current of the DEPFETs is obtained as a function of time.
Since the matrix is read out in the rolling shutter mode, groups of four geometrical DEPFET rows (row_{geo}) are enabled and disabled subsequently. In this way, the current curve of a single pixel corresponds to 128 ns, which will be shown in Sect. 5.8 and Sect. 6.5.

4.8.5 Communication between DCD and DHP (DEPFET data)

In this section the nomenclature of the DCD is briefly introduced. Additionally, the data transmission between the DCD and the DHP is presented. A digital test pattern verifying the correct data transmission between the two ASICs and the proper optimization algorithm for reliable data transfer are discussed.

Overview of nomenclature

Each DCD has 256 input channels for measuring and digitizing the Drain currents of the DEPFET pixels (see Fig. 4.31). The data transmission between a single DCD and a single DHP proceeds via 64 *transfer lines*. The 256 DCD input channels are grouped into eight *column pairs*, each consisting of 32 input channels. The DCD output data of a single column pair, corresponding to the input data of the DHP, are multiplexed in an 8-bit bus. One bus consists of eight transfer lines to transmit 8 bits (1 byte) of data simultaneously from the DCD to the DHP within one DCD clock cycle. Since each DCD has 256 input channels, there are eight such column pairs, corresponding to eight 8-bit buses and 64 transfer lines between the two ASICs.

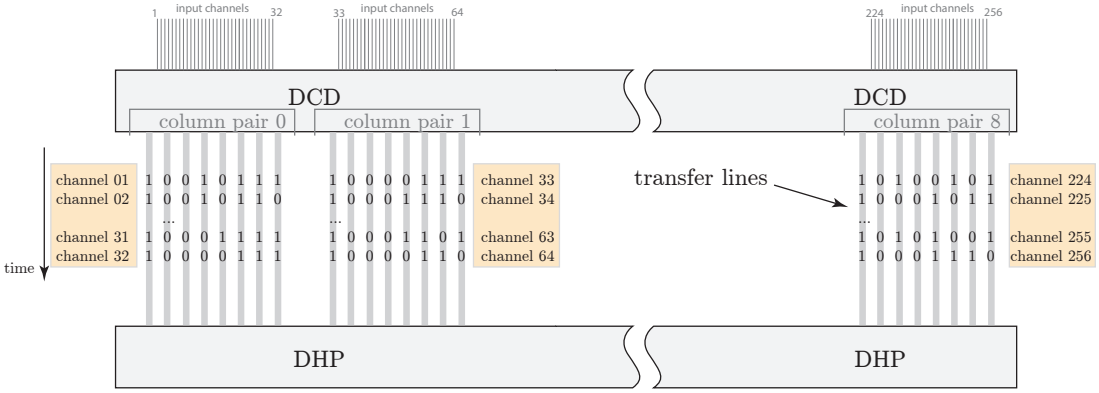


Figure 4.31: Illustration of the data transmission between DCD and DHP. The 8-bit signals of the 32 input channels are sent subsequently within within one DCD clock.

Data transmission and relation to the rolling shutter mode

In the following, the timing of the DCD–DHP data transmission and its relation to the rolling shutter mode is briefly described.
The time to control a single DEPFET Gate (and Clear) output driver corresponds to 32 ticks, as already introduced in Sect. 4.8.1. The frequency of a tick corresponds to the clock of the DCD. During the control of a single Switcher output driver within these 32 ticks, the DCD samples at the same time the currents of 32 input channels. Moreover, the digitized current signals of 32 channels are transferred to the DHP within the 32 DCD clock cycles. In other words, the DCD sends 1 byte within 3.28 ns (at the nominal global reference clock (GCK)=76.33 MHz) on each column pair (8-bit bus) .

InterASIC Communication

Low-voltage differential signaling (LVDS) is favorable for the transmission of these high frequency signals between DCD and DHP. This results in 16 electrical connections for a single 8-bit bus. In conclusion, 128 inter-ASIC connections would be required for the entire data transmission. Due to space constraints on the *module*

value	MSB	bit-6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB
-128	1	0	0	0	0	0	0	0
-127	1	0	0	0	0	0	0	1
-126	1	0	0	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
-1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
126	0	1	1	1	1	1	1	0
127	0	1	1	1	1	1	1	1

Table 4.8: Encoding of the signal transmission of the DCD. MSB is the Most Significant Bit, while LSB means the Least Significant Bit.

(on which the ASICs are mounted; it will be introduced in Sect. 4.9.1) this is not feasible so that only the p line of the differential signal can be connected between the both ASICs. This results in a total of 64 data lines for the DCD-DHP data transmission.
The signal of the 8-bit ADCs are sent via the 8-bit output buses in the data type of `signed int8`. One can represent 256 values with 8 bits. The signal range is from -128 to $+127$. The encoding of the signal is given in Tab. 4.8. In addition, there are also two data lines for the pedestal compression (introduced in Sect. 4.8.7) for each column pair. A sketch of the data transmission between the two ASICs is shown in Fig. 4.32. The layout, i.e., the routing of the data lines between the DCD and DHP is shown in Fig. 4.33. They are divided in two groups:

- **DCD⟶DHP**: The data pins on DCD side are named DO$\langle x \rangle y$ while on DHP side they are called DI$\langle x \rangle y$. The "I" and "O" means "Input" and "Output", respectively. The x represents the bus and y the bit number (LSB, bit-1, ..., bit-6, MSB). The 8-bit data is transmitted via the eight transfer lines. They are shown as the red connections in Fig. 4.33.
- **DHP⟶DCD**: The traces for the signal to transmit the offset compensation is realized by 16 transfer lines. They are illustrated as the blue lines in Fig. 4.33.

DCD test pattern

The DCD has a hard-coded test pattern [153], which can be enabled via the JTAG configuration. When activated, the DCD continuously sends the same pre-defined digital data to the DHP. The data repeats for every 32 channels, i.e., the same data is sent simultaneously on all eight 8-bit buses. (The data sampled by the ADCs is overwritten.) It transmits the pattern represented in Tab. 4.9 and shown in Fig. 4.34:

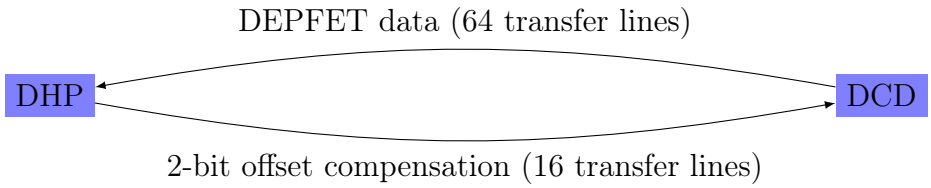


Figure 4.32: Sketch of the data transmission between the two ASICs.

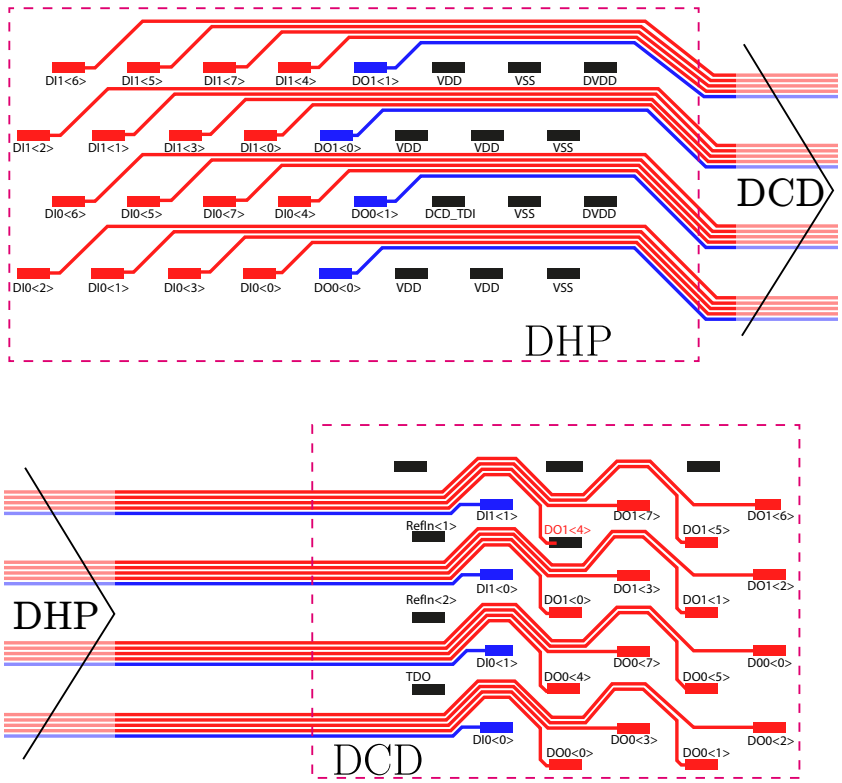


Figure 4.33: Layout of the data transfer lines on the module for two column pairs (out of eight). The red traces transmit the DEPFET data from the DCD to the DHP while the blue traces represent the 2-bit-offset compensation, i.e., data is transferred from the DHP to the DCD.

In order to find the right sampling point of the DCD waveform, the sampling point can be shifted in time by delay settings. The delay registers consist of 4 bits, i.e., 16 values are possible. A schematic of the sampling point shift is shown in Fig. 4.35. Using these delay elements, the sampling time can be controlled precisely. The correct sampling point is shown in Fig. 4.35b. Since the transitions between a logical 1 and logical 0 is not as sharp as shown in the sketch (due to parasitic capacitance and ohmic resistances of the electrical connections and pick-up noise), a wrong interpretation of logical 0 and logical 1 could result. (For instance, a 1 is sampled although a 0 is sent, see Fig. 4.35a and Fig. 4.35c.) The maximum number of wrong readings in the repeating bit stream is four. This could occur in

channel	value	MSB	bit-6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB
0	-127	1	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0
2	127	0	1	1	1	1	1	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
30	127	0	1	1	1	1	1	1	1
31	0	0	0	0	0	0	0	0	0

Table 4.9: The test pattern of 32 DCD channels represented in 8 bits. The MSB is bit 7 and the LSB is bit 0. This pattern is the same for all eight column pairs, i.e., repeats eight times for all 256 channels.

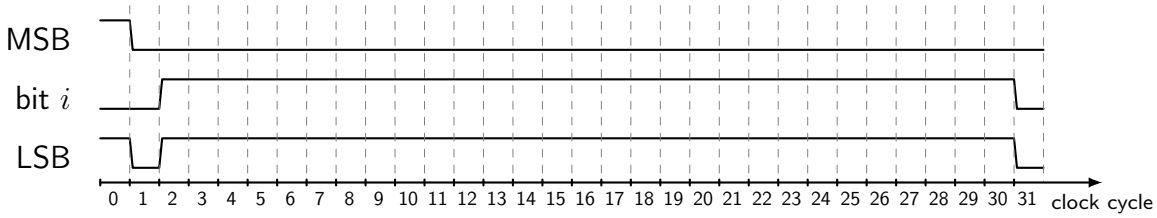


Figure 4.34: Sketch of the waveform of the DCD test pattern for the eight transfer lines (LSB, bit i, $i \in \{2, 3, 4, 5, 6\}$ and MSB)

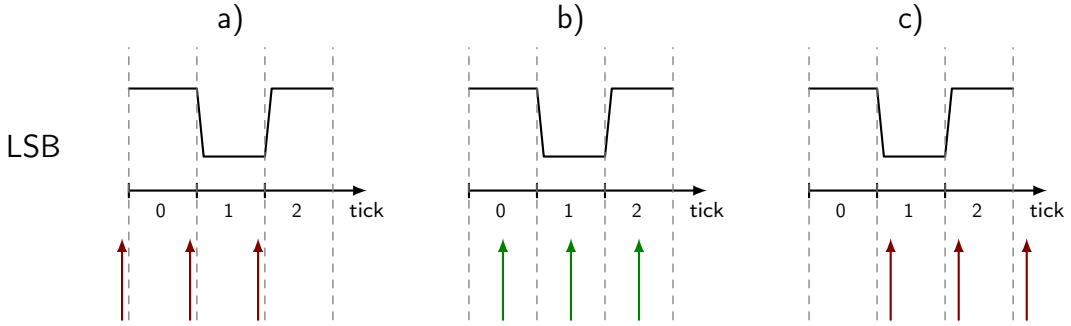


Figure 4.35: The arrows represent the sampling point time. The shift in time (i.e., delays) are shown as the red and green arrows. **a)** too early, wrong tick **b)** ok **c)** too late, wrong tick

the LSB transfer line when the sampling point is shifted. Consequently, the logical 0 in the DCD clock cycle 31 could be read as a logical 1, the logical 1 in DCD clock cycle 0 could be misinterpreted as logical 0 etc.
There are two possibilities of how the sampling point can be shifted by delay elements (the DCD register names are described in app. C.2):

- **Global delay:** The global delay is set for all 64 bus lines simultaneously.
- **Local delay:** The local delay is set for each transfer line individually, i.e., the optimal sampling point for each transfer line can be set.

Optimization algorithm:

In order to optimize the delay for the proper data transmission between the DCD and the DHP, a fixed test pattern is enabled in the DCD and the data is read by the DHP. This is repeated for different combinations of global delay (GD) and local delay (LD) settings. When the delay is properly set, the pattern read in the DHP must match the one which is input into the DCD. The analysis is performed in two steps. In the first step, the global delay is determined. In the second step, the local delay value for each transfer line must be determined.
An example is given to illustrate the optimization algorithm. For the sake of simplicity, the algorithm is explained for a single transfer line and two global delay values. However, this step must be repeated for all possible 16 global delay values and all 64 transfer lines.
For each local delay value, the average number of transmission errors is counted and written into an array (this corresponds to a row in the scatter plot). For instance, for a specific DCD–DHP pair with transfer line 5 and global delay 2, the transmission errors listed in Tab. 4.10 is obtained.

Table 4.10: Average number of incorrect readings for different local delay settings for a fixed global delay of 2 and transfer line 5.

LD	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
⟨errors⟩	1	0	0	0.1	0	0	0	0	0	0.2	1	1.5	2	2.2	2.1	3

The number of consecutive correct readings (*cluster size*) is counted, i.e., the number of consecutive 0. In this example two regions are obtained, two correct readings for local delays 1 and 2 and, in addition, there are five consecutive 0 for local delays 4, 5, 6, 7 and 8. This results in a maximum cluster size of 5. For the same transfer line 5 and global delay 3, the number of transmission errors listed in Tab. 4.11 are measured. The maximum number of consecutive correct readings

Table 4.11: Average number of incorrect readings for different local delays for global delay of 3 and transfer line 5

LD	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
errors	0	0	0.01	0.1	0	0	0	0	0.7	1	1.2	1.3	2	2.6	2.5	3.7

is 4 in this case. This procedure is repeated for every global delay and for every transfer line. The maximum number of correct readings (in this example for global delay 2 it is 5 and for global delay 3 it is 4) are written in arrays. One array is written for each transfer line (i.e., for a 8-bit bus), resulting in the readings for the maximal cluster sizes listed in Tab. 4.12.
The column-wise minima are calculated (the minima are listed in the last row of Tab. 4.12). The maximum of these minima defines the global delay value. In this example, the global delay is set to 2.
Having adjusted the global delay value, the local delay settings for each transfer

Table 4.12: Overview of the largest cluster sizes for all 64 transfer lines with different global delay values. In addition, the minima (along the transfer lines) of the maximal cluster sizes for each global delay setting is determined.

Global Delay	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
transfer line 0	8	8	7	6	5	4	4	3	2	2	1	0	0	0	0	0
...																
transfer line 3	3	4	5	4	4	3	4	3	2	1	1	0	0	0	0	0
...																
transfer line 63	6	5	7	6	5	5	4	2	2	2	1	0	0	0	0	0
Minima	3	4	5	4	4	3	4	3	2	1	1	0	0	0	0	0

line has to be determined as well. In Tab. 4.10, the local delays are set such that they are in the middle of consecutive correct readings. For two transfer lines (5 and 7) the average number of transmission errors are listed in Tab. 4.13.

Table 4.13: Average number of incorrect readings for transfer lines 5 and 7 for different local delays at fixed global delay of 2.

LD	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
TL 5	1	0	0	0.1	0	0	0	0	0	0.2	1	1.5	2	2.2	2.1	3
TL 7	0.9	0	0.2	0.3	0	0	0	0.6	1	2.2	2	2.4	2.7	2.9	3.1	3

Thus, for transfer line 5 the global local delay is set to 6 while for transfer line 7 the local delay is set to 5. All lines have the global delay 2.

4.8.6 Synchronization between DCD and DHP (DEPFET data)

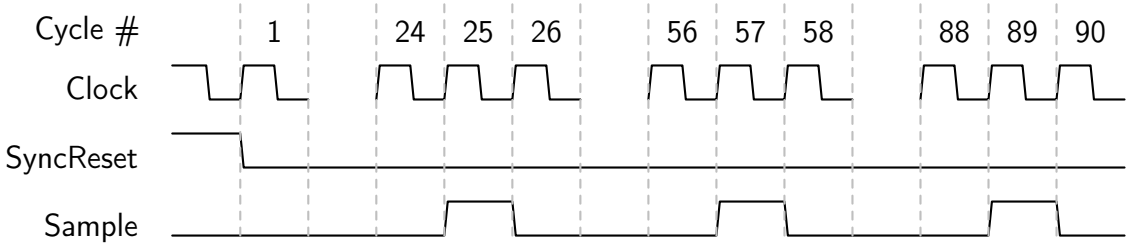


Figure 4.36: Timing diagram of sampling the Drain current referenced to `SyncReset` in clock cycles of the DCD [153].

The sampling and the data processing timing diagrams of the DCD are shown in Fig. 4.36 and Fig. 4.37, respectively. The following process happens for all eight column pairs in parallel. The DCD starts to sample the Drain currents in the time windows 18–25, 50–57, 82–89, ... clock cycles after the falling edge of `SyncReset`,

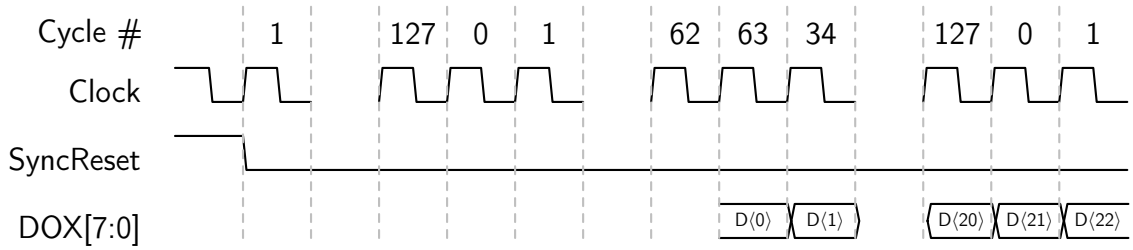


Figure 4.37: Readout scheme of DCD [153]. The first data (of the first channel) is sent 191 clock cycles after the falling edge of `SyncReset`. DOX[7:0] represents the data output of the 8-bit bus.

which is issued (controlled) by the DHP, [153]. Thus, the sampling moments are on clock cycles 25, 57, 89, ... The digitized data of the first channel is sent 191 clocks after the falling edge of `SyncReset`. This delay between sampling and sending the data is a result of the design of the ASIC and cannot be changed by any setting. The DHP has to write these data to the correct internal memory addresses. Therefore, a dedicated delay register can be varied to match the pixel signal with the correct memory position. The measurement and adjustment are explained in Sect. 6.3.3.

4.8.7 Pedestal Compression

In order to decrease the pedestal spread and, therefore, to increase the dynamic range of the 8-bit digitizer of the DCD, a *2-bit offset compensation* can be activated within the DCD by adding a certain amount of current individually to each pixel. The amount of current is set by the DHP and sent to the DCD. Due to limitations in the number of inter-ASIC communication lines on the module, there are only two transfer lines available (corresponding to two bits) for each DCD column pair, i.e., for 32 input channels (see Fig. 4.33)[11]. For that reason only three different current values can be added to each pixel individually.
A global current source (for the added pixel current) is adjusted by a dedicated DCD setting. The individual current $I_{\mathrm{DAC-ind}}$ added to each pixel is a multiple of the global current $I_{\mathrm{DAC-glo}}$, summarized in Tab. 4.14.
The idea is to separate the shifted pedestal distribution into four equally spaced domains (see sketch in Fig. 4.38). All pixels are separated into four groups, depending on their pedestal values, which corresponds to the four colors in the sketch. The current value $k \times I_{\mathrm{DAC-glo}}$, $k \in \{0, 1, 2, 3\}$ is added to the Drain current as shown in Tab. 4.14. In this way the entire pedestal spread is compressed theoretically by a factor of four.
In the first step, the pedestal distribution is shifted to the lower dynamic range of the DCD as illustrated in Fig. 4.38a and Fig. 4.38b. Only about one fourth is visible in the (positive) dynamic range (red part of the distribution). The rest is theoretically below the dynamic range, i.e., they have hypothetical negative ADU

[11] This results in a total of 16 transfer lines for all 256 input channels.

Table 4.14: Bit encoding for pedestal correction [153]. DI means data input, X denotes the column pair $(0, \ldots, 7)$ and $[0:1]$ are the two transfer lines corresponding to the two bits.

DIX[1:0]	$I_{\text{DAC–ind}}$
2'b00	$0 \times I_{\text{DAC–glo}}$
2'b01	$1 \times I_{\text{DAC–glo}}$
2'b10	$2 \times I_{\text{DAC–glo}}$
2'b11	$3 \times I_{\text{DAC–glo}}$

values, illustrated by the blue, green and orange parts of the pedestal distribution. In reality, 75 % of the pixel values are located at the edge of the lower dynamic range at 0 ADU. However, to illustrate and simplify the explanation of the procedure negative ADU values are assumed. In this configuration the pixels, which are part of the blue, green and orange part, do not change their ADU values, if electrons created by a minimum ionizing particle (MIP) accumulate in the *internal Gate*. The DCD cannot resolve the current. The signals can only be detected for a huge signal, which could be created by particles generating a signal which corresponds to several MIPs, e.g. slow pions (see app. B.5).
In the second step, the optimization of the individual pixel current values is performed to reduce the pedestal spread. To do so, for each $I_{\text{DAC–ind}}$ value the offsets $0, 1, 2, 3$ are applied subsequently to all pixels. Using the calibration data, a global $I_{\text{DAC–glo}}$ is calculated (for all pixels of a DCD) and for each pixel either $0, 1, 2$ or $3\times$ $I_{\text{DAC–glo}}$ is applied. The details of the algorithm is described in detail in [168]. Consequently, a narrowed pedestal distribution is obtained, which is located in the lower dynamic range of the DCD (see Fig. 4.38c).

4.8.8 Synchronization between DHP and DCD (Offsets)

The DHP and DCD has to be synchronized to properly apply the offset correction. The synchronization procedure is explained below for a single DCD column pair, but is applied to all eight DCD column pairs.
The DCD needs 22 clock cycles to switch the desired current value to the DEPFET pixel after releasing the `SyncReset` signal, as shown in Fig. 4.39. The values for the pixels within a column pair are sent with decreasing number, i.e., the value of channel 31 (at DCD clock cycle 22) is the first transmitted data while the value for channel 0 (at DCD clock cycle 52) is the last transmitted value. The commands for all 32 DCD input channels are sent within 32 DCD clock cycles. As already mentioned, the PXD is read out in the rolling shutter mode, i.e., the Gates rows (row_{gate}) are switched on subsequently. The offset current value added for pixel (row_{geo}, col_{geo}) must be sent one Gate row (row_{gate}) in advance, corresponding to 32 DCD clock cycles. For instance (see Fig. 4.39), the signal of $\text{row}_{\text{gate}} = 2$, channel 31 is sent in DCD clock cycle 54, i.e., 32 clock cycles after the data was transmitted for $\text{row}_{\text{gate}} = 1$, channel 31 (at DCD clock cycle 22). This procedure

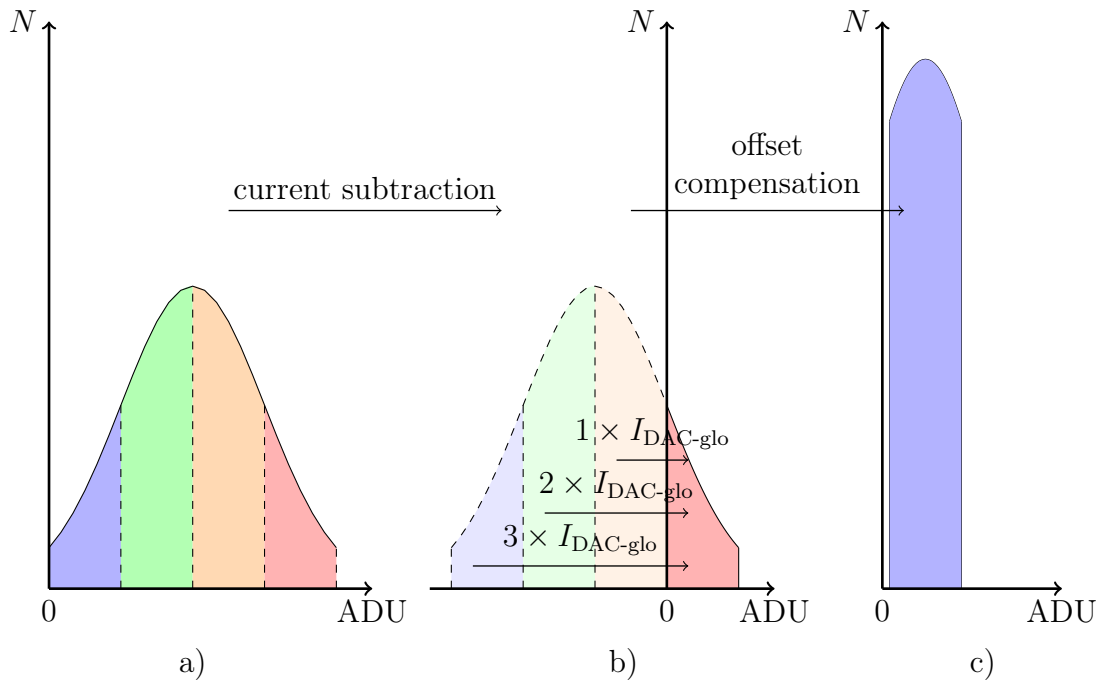


Figure 4.38: Principle of the offset compression (N corresponds to the number of pixels): In the first step, the pedestal distribution (a) is shifted such that three-quarters are theoretically below the dynamic range of the DCD (b). Consequently, they have have hypothetical negative ADU values. In the second step, the optimization is performed resulting in a narrowed pedestal distribution (c), located in the lower dynamic range of the DCD.

is subsequently applied for the entire matrix. In order to shift the transmission of the offset data from the DHP to the DCD in time, a 7-bit register within the DHP must be adjusted. The procedure to find the optimal delay settings and the measurements are presented in Sect. 6.9.1.

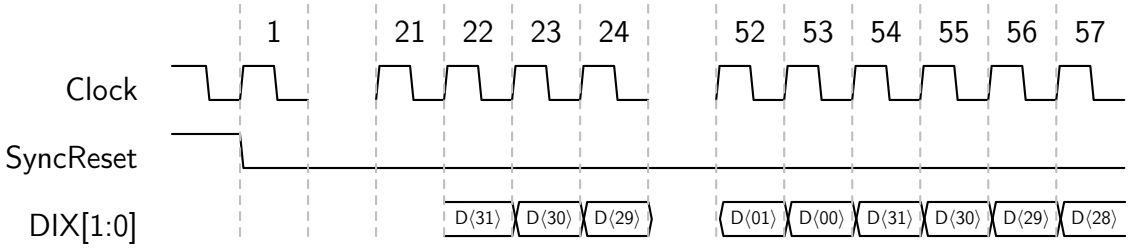
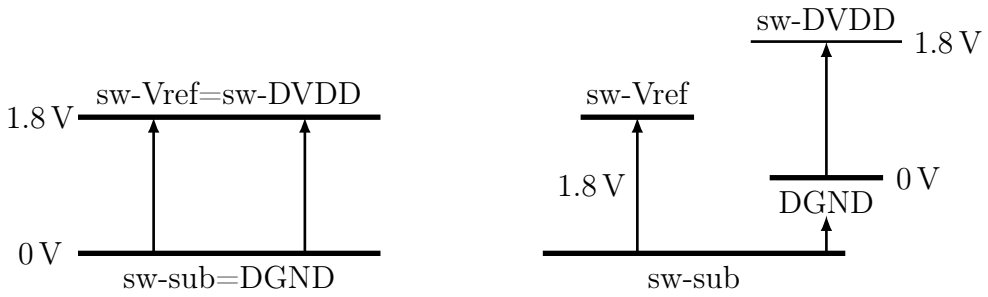


Figure 4.39: Input scheme of offset compression within DCD [153]. DIX[1 : 0] denotes the data input of column pair X with two bits 0 and 1.

4.8.9 Power-up sequence

A sophisticated power up sequence has been developed to power the ASICs properly and avoid possible damages.



(a) Powering of the digital domain that is applied for the lab. The sw-substrate net is shorted to the digital ground and the sw-Vref net is connected to sw-DVDD net.

(b) Powering scheme for the final Belle II experiment. The sw-substrate and the sw-Vref nets are decoupled. The most negative voltage must be applied at the sw-substrate net.

Figure 4.40: Powering of the digital domain of the Switcher.

In the first step the Switchers are biased. The Switcher has three digital power nets: *Switcher-Vref (sw-Vref)*, *Switcher-DVDD (sw-DVDD)* and *Switcher-substrate (sw-sub)*. Additionally, it has four nets from the analog domain: *ClearOn*, *ClearOff*, *GateOn* and *GateOff*. For the lab setup, the Switcher-Vref and Switcher-DVDD nets are shorted. The Switcher-substrate net is connected with the digital ground (DGND) (see Fig. 4.40a). For the operation in Belle II, the powering is slightly changed (see Fig. 4.40b). The Switcher-substrate voltage must always be the most negative voltage applied at the Switcher [147]. Due to the irradiation of the DEPFETs, the threshold for the GateOn voltage shifts such that it becomes more negative compared to ground. Therefore, the Switcher-substrate net has to be biased with a voltage lower than or equal to the GateOn voltage[12].
The difference between the Switcher-substrate voltage and the Switcher-Vref voltage must not exceed 1.8 V due to design reasons [147]. Consequently, the potential applied at the Switcher-substrate must be lowered step-by-step. The flowchart is shown in Fig. 4.41 and an example is illustrated in Tab. 4.15.
When the Switchers are fully powered, the DHPs are biased. Resetting all the registers within the DHP requires that the *DHP-core* voltage is switched on before (or at the same time as) the supply voltage *DHP-DVDD*[13].
Next, the DCD is powered. The DCD has four supply voltages, one for the digital part *DCD-DVDD* and three for the analog domain, *DCD-AVDD, DCD-RefIn* and

[12] A dedicated powering scheme for the lab setup was made since the first generations of the power supply (PS) did not provide enough output channels to connect all power nets as it is foreseen in the Belle II experiment.

[13] The CRESET pins of the DHPs are each connected to a 100 nF capacitor. The capacitors are coupled to ground. The JTAG registers, which are connected to the CRESET signal, are supplied by the core voltage. Hence, to ensure a proper reset, DHP-core must be applied before DHP-DVDD.

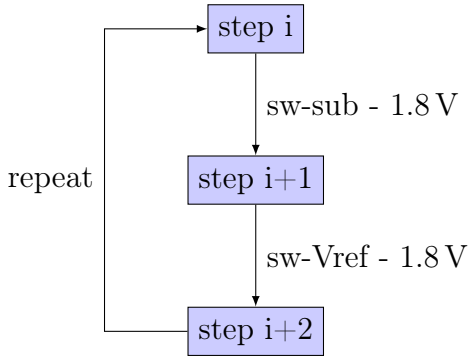


Figure 4.41: Flowchart of lowering Switcher-Vref and Switcher-substrate voltages.

Step	Switcher-Vref	Switcher-sub
1	0 V	0 V
2	0 V	−1.8 V
3	−1.8 V	−1.8 V
4	−1.8 V	−3.6 V
5	−3.6 V	−3.6 V
6	−3.6 V	−5.2 V
7	−5.2 V	−5.2 V
8	−5.2 V	−7.0 V
...	...	...

Table 4.15: Subsequently lowering the Switcher-Vref and Switcher-substrate voltages.

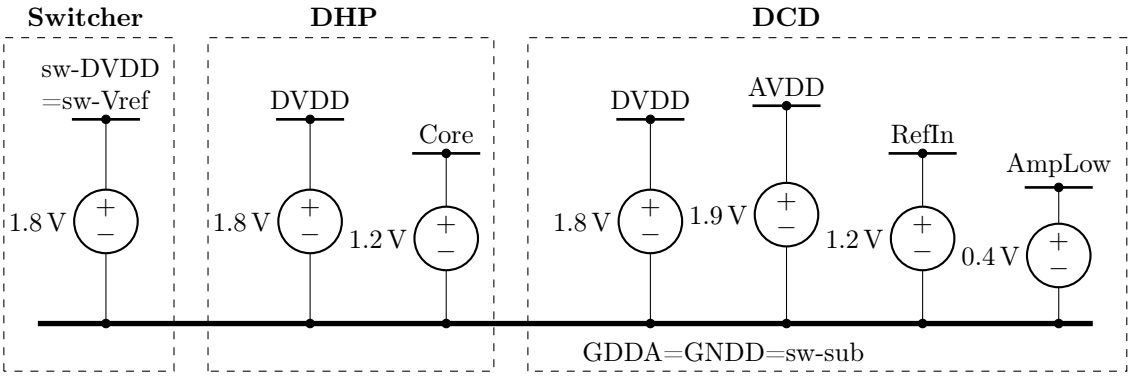


Figure 4.42: Bias scheme of the 14 ASICs for the lab setup.

DCD-AmpLow. The internal registers of the DCDs are random when the ASIC is biased. Hence, they consume a lot of power. In order to avoid damages, the DCDs should be configured shortly after being biased. Current limits are set for the analog nets before having them configured (stage 1) to avoid damages. Since the ASICs are configured using JTAG, the configuration happens step-by-step, not simultaneously. Having written the registers to the DCDs, the current limits are increased to ensure proper functionality (stage 2)[14].
The voltages applied at the ASICs and the current limits for the two stages (before and after having configured the DCDs) are listed for the lab setup in Tab. 4.16. The bias scheme for the ASIC is shown in Fig. 4.42. The flowchart of the power-up sequence in the lab and beam tests is shown in Fig. 4.43.

[14]On a previous prototype, the hybrid 6 setup, three DCDs were assembled on a module. The low current limits (i.e., the separation into two stages) were not applied. Having configured a DCD results in a low power consumption. When the first two were configured, the third one was still in an undefined state, i.e., the current consumption was quite large ($\gtrsim 1.5$ A for AVDD). The bond-wires melted due to the high current. This served also as a kind of fuse. The high currents could harm and damage the DCD.

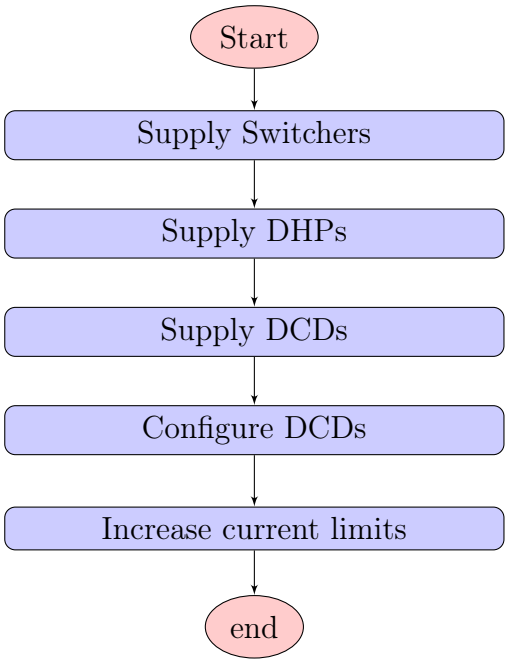


Figure 4.43: Flowchart of the power up sequence for the ASICs. The analog domain for the DCD is split into two stages with different current limits.

Table 4.16: Voltages and current limits for the ASICs in the lab setup configuration.

Voltage	voltage	current stage 1	current stage 2
Switcher-DVDD	1800 mV	30 mA	30 mA
Switcher-Vref	1800 mV	30 mA	30 mA
Switcher-Sub	0 mV	10 mA	10 mA
DHP-core	1200 mV	800 mA	800 mA
DHP-DVDD	1800 mV	550 mA	550 mA
DCD-DVDD	1800 mV	940 mA	940 mA
DCD-AVDD	1900 mV	340 mA	3000 mA
DCD-RefIn	900 mV	180 mA	1000 mA
DCD-AmpLow	400 mV	340 mA	1300 mA

4.9 Module and ladder layout

In this section the layout of a module, which is defined as a DEPFET matrix with the surrounding periphery for the control and readout electronics, is described. In addition, the ladder for the PXD consisting of two modules glued on the short edge is presented.

4.9.1 Module

The DEPFET pixels are arranged in a matrix layout, as already described in Sect. 4.4.3. Monte Carlo (MC) simulations [169] have been carried out in order to find the optimal pixel sizes and thickness for the reconstruction of decay vertices, accurate position resolutions and excellent impact parameters. If detectors are thick they have higher signals and also better resolutions by charge sharing of neighboring pixels. The thicker they are the more multiple scattering occurs. The conclusion is to have a 75 µm thick sensitive area. The position resolution by charge sharing has been found to be more important than the slightly increased multiple scattering.

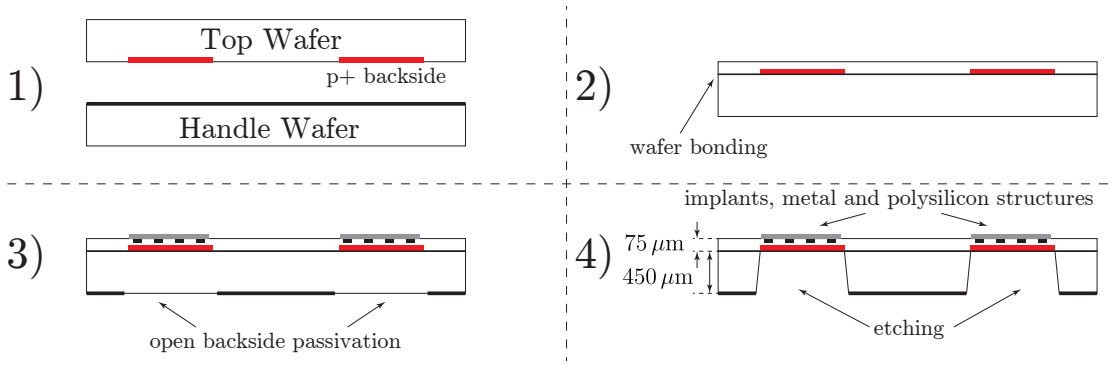


Figure 4.44: The production steps and thinning technology of the modules.

The production of the modules is briefly summarized (see Fig. 4.44) in the following. In the first step, the back side p^+ implants of the top wafer are performed. In step two, the handle wafer (450 µm thick) with silicon on insulator (SOI) on the top side is bonded to the bottom of the top wafer. The top wafer is thinned to the desired 75 µm by wafer grinding and polishing techniques. In the third step, all of the implants for the DEPFET pixels, polysilicon and metal structures are performed. In addition, the backside passivation is partially opened for the edging process. In the last step, the handle wafer is partially edged leaving the support frame to provide mechanical stiffness. To keep the material budget as small as possible, cavities are etched into the support structure. A sketch of those grooves are shown in Fig. 4.45. Thus, the sensitive area is 75 µm thick while the rims have a thickness of 525 µm. More details are found in [135, 170].
Having produced the DEPFET pixels with all implants and metal systems on the wafer, the individual sensors are cut into sections called *modules*.

The sensor matrix is composed of 192,000 DEPFET pixels. For the Belle II PXD, a compromise has been made for the pixel geometry between fast readout and high position resolution resulting in two pixel regions with different pixel sizes. Near the interaction point a small pixel size is chosen. Larger pixels are placed at the outer regions, where particles hit the PXD at a shallow angle. If no charge sharing occurs, i.e., a single pixel is hit, the position resolution is $\sigma_{\text{pos}} = \frac{p}{\sqrt{12}}$, where p denotes the pixel pitch. In the case of charge sharing, a weighting algorithm can be used to reconstruct the incident particle's position with a resolution of

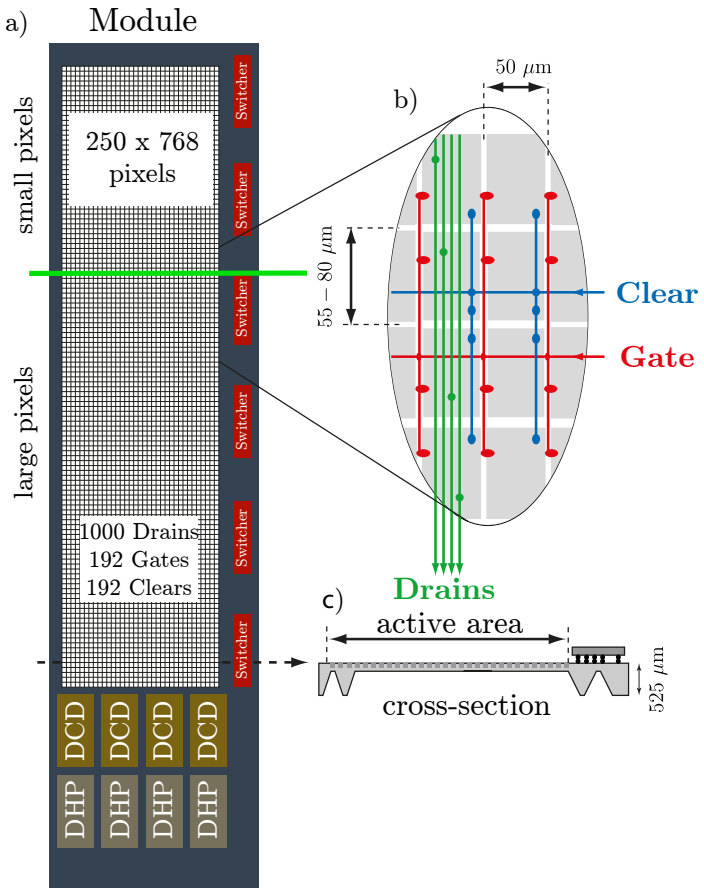


Figure 4.45: a) The PXD modules. The sensitive part, consisting of 192,000 DEPFETs, is surrounded by the support structure and ASICs. b) The four-fold readout scheme is highlighted. A common Gate and Clear line controls four pixel rows at the same time; therefore, four Drain lines are required to measure the Drain current of all pixels in one column. c) Cross-section of a module. Grooves are etched into the support structure to minimize multiple scattering. ASICs are mounted at the *balcony* and at the *end-of-stave* [171].

$\sigma_{\text{pos}} \propto \frac{p}{\text{SNR}}$, where SNR is the signal-to-noise ratio [172] A pixel matrix consists of 256×250 small pixels and an additional 512×250 large pixels. The pixel sizes for the two layers of the PXD are listed in Tab. 4.17.
Signal and power traces are directly routed on the silicon (oxide) in three metal layers (two in aluminum and one in copper) [173].
As shown in Fig. 4.45, the Switchers are mounted on the balcony to control the Gates and Clears of DEPFET rows. The DCDs and DHPs are placed at the end-of-stave (EOS) between the sensitive DEPFET area and the Kapton attachment. Furthermore, decoupling capacitors and resistors are soldered onto the module to ensure stable voltages and proper operation.

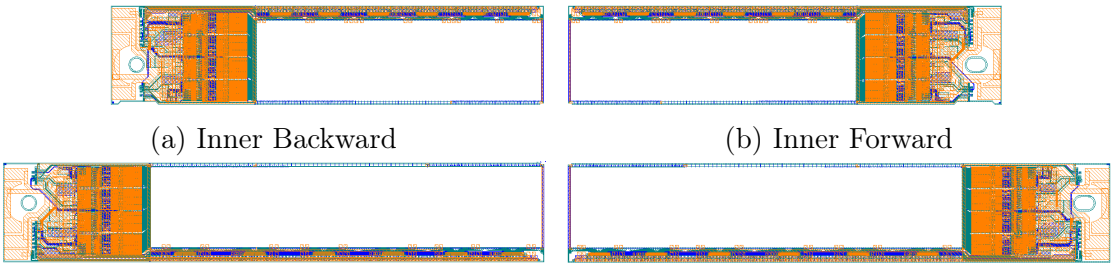
Module types

In total, there are four different designs for the inner (layer 1) backward, inner forward, outer (layer 2) backward and outer forward geometries. The layouts are

Table 4.17: Pixel sizes of the PXD. They are divided in two sections. The large pixels (512 × 250) are located close to the readout electronics (forward and backward regions) while the small pixels (256 × 250) are in the central region (see Fig. 4.45 and Fig. 4.49).

	length	width	small pixel	large pixel	sensitive area
Layer 1	67.975 mm	15.4 mm	$55 \times 50\,\mu m^2$	$60 \times 50\,\mu m^2$	$12.50 \times 44.80\,mm^2$
Layer 2	84.975 mm	15.4 mm	$70 \times 50\,\mu m^2$	$85 \times 50\,\mu m^2$	$12.50 \times 61.44\,mm^2$

shown in Fig. 4.46. Their dimensions are listed in Tab. 4.17, where the forward and backward modules have the same dimensions for each layer.



(a) Inner Backward (b) Inner Forward

(c) Outer Backward (d) Outer Forward

Figure 4.46: Layouts of the pilot run modules. The blue lines depict the first aluminum layer, the green lines represent the second aluminum layer and the orange lines are in the copper layer. The white rectangular areas correspond to the thinned sensitive area.

The layouts of the modules are quite similar. The pixel layouts are all the same (for both pixel sizes). The differences are in the metal routing for the Switcher control (see Fig. 4.47). For the outer backward (OB) and inner forward (IF), DHP 4 controls the Switchers and the readout (rolling shutter mode) starts with the rows close to the DCDs. In contrast, for the outer forward (OF) and inner backward (IB) modules, DHP 1 controls the Switchers. The rolling shutter always reads in v-direction (see Fig. 4.47).
Six modules are produced on a single wafer, one IF, two OF, two OB and one IB (see Fig. 4.48). In order to assign a module to the production runs, the modules are labeled with their wafer number, followed by the device under test (DUT). For instance, *W30-OB1* corresponds to the OB1 module on wafer 30. Around the modules there are test structures, such as small matrices consisting of 16 $\text{rows}_{\text{gates}}$ and 128 $\text{columns}_{\text{drain}}$ (corresponding to 64 × 32 rows_{geo} × $\text{columns}_{\text{geo}}$). They are labeled with the wafer number followed by a combination of a letter and a number, which depends on their position on the wafer, e.g. W30-F00.

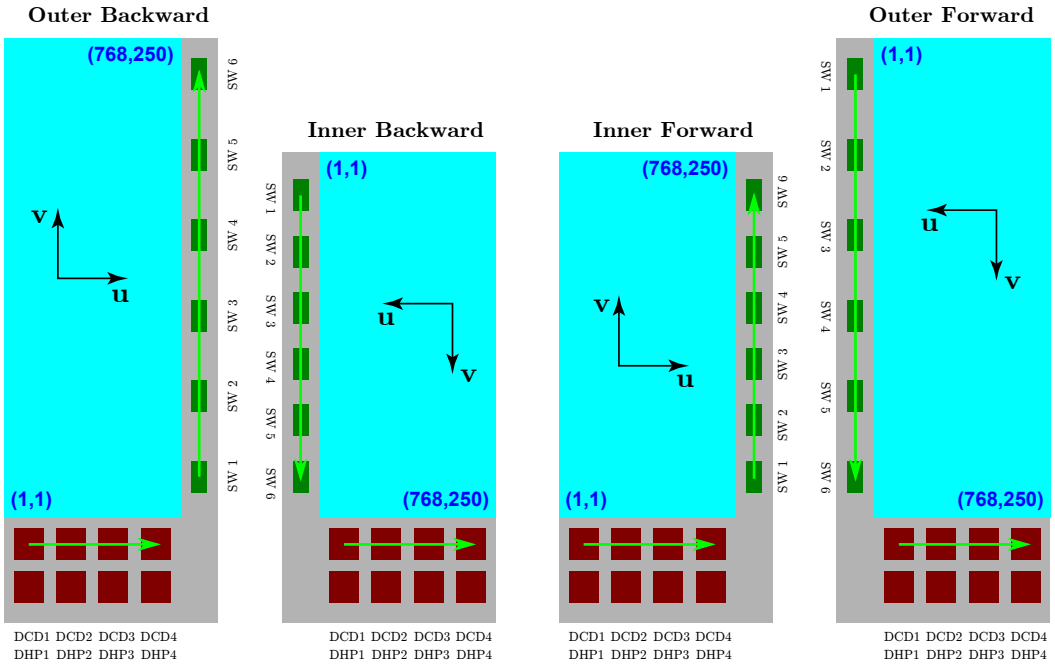


Figure 4.47: Numbering of ASICs and readout direction according to the JTAG chain [124]. The origin $(1, 1)$ of the pixel numbering is either in the lower left or upper left corner, depending on the readout direction.

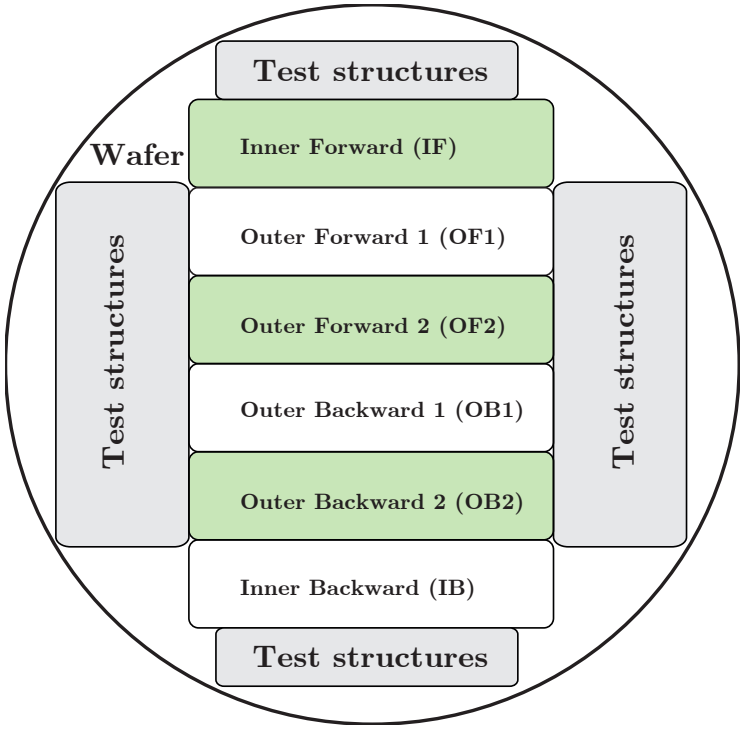


Figure 4.48: Sketch of the wafer layout with six modules [174].

4.9.2 Ladder and PXD

Two modules (backward and forward of the same layer) are glued together at the short edge, forming a DEPFET *ladder* using small ceramic joints (see Fig. 4.49). Thus, enough stiffness for the long ladders is provided and a *self-supporting structure* is ensured. The self-supporting structure of the DEPFET matrix in the active volume is unique in the world of high energy physics experiments. The low material budget avoids additional multiple scattering, which would be caused by any additional mechanical parts.

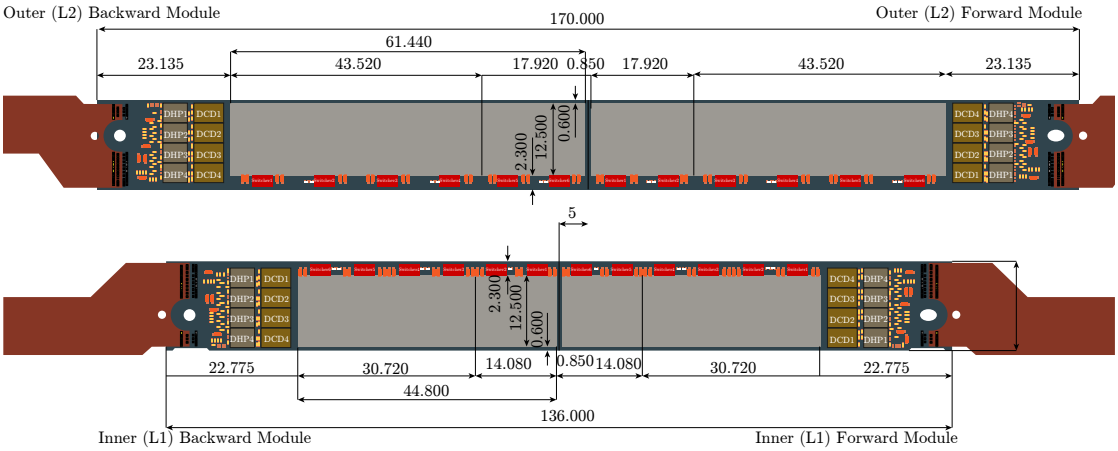


Figure 4.49: Modules of both PXD layers. All dimensions are in mm. Two are glued together resulting in a gap of 0.85 mm between the two sensitive areas [1].

4.10 Data Acquisition

The data from 40 modules is transferred to 40 DHEs. Five DHEs are connected to a data handling concentrator (DHC); thus, there are eight DHCs for the entire PXD. The DHC receives the trigger for the readout and the clock from the global Belle II DAQ system. The data is sent onwards to four online selection nodes (ONSENs). An overview is shown in Fig. 4.50. The aurora data protocol is used for the entire data chain from the modules to the ONSENs.

Data Handling Hub (DHH)

The data handling hub (DHH) consists of the data handling engines (DHEs) and the data handling concentrators (DHCs). The DHE is directly connected to the modules. It receives the data from the four DHPs (each with 1.6 Gbps) assembled on a module, provides the JTAG master interface for the entire ASICs and performs the cluster reconstruction and classification [164].
Five DHEs are connected to a DHC, each with a 6.5 Gbps link. The DHC uses the hit information from the DHEs and builds sub-events, which are characterized by a trigger number. The DHE and DHC modules are based on Xilinx Virtex-6 LX130T FPGA card, which is equipped with up to 4 GB of memory. More details are given in [164, 175].

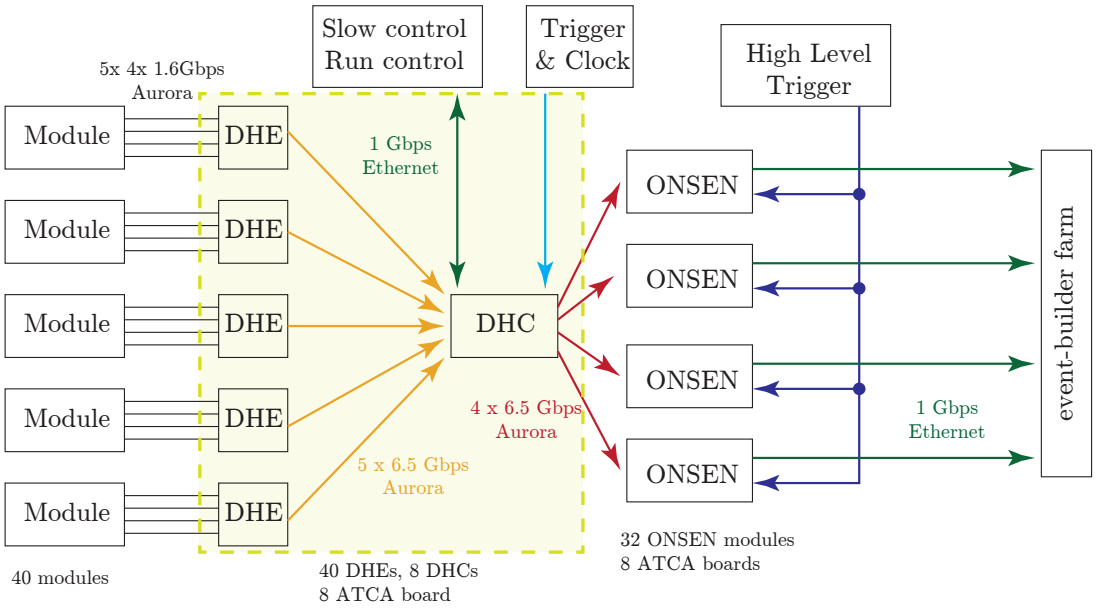


Figure 4.50: Data readout chain from the modules to the Belle II data acquisition system.

Online Selection Node (ONSEN)

The ONSEN system receives the data from the eight DHCs each with 4×6.5 Gbps links) and reduces the data by an adjustable factor of (~ 10) by selecting clusters in regions of interest (ROIs) [176]. The ONSEN buffers the entire PXD (zero suppressed) data for a maximum of 5 s. During that time, the event is reconstructed using the sub-detectors surrounding the PXD, the most important of which is the CDC. The tracks found in the CDC are extrapolated to the PXD layers and define the ROIs on the PXD sensors. The ONSEN discards all of the pixels from the PXD which are not within a ROI. Hence, fake hits (noisy ADCs), background hits etc., are neglected, which yields an adequate[15] data-reduction.
The ONSEN system uses the Virtex 5 FPGA technology for the fast data collection and data reduction. An FPGA and additional 4 GB random-access memory (RAM) are assembled on micro telecommunications computing architecture (MicroTCA) cards. There are in total 33 cards, which are mounted in 9 advanced telecommunications computing architecture (ATCA) carrier boards, called computer nodes (CNs) [177, 178]. The ONSEN system finally sends the PXD data to the global Belle II DAQ system.

4.11 Mechanical arrangement of PXD ladders

The arrangement of the PXD ladders around the beam pipe and the overlapping areas is shown in Fig. 4.51. The sensitive areas overlap for both layers, as shown by the green (inner layer: layer 1) and yellow (outer layer: layer 2) wedges. For

[15]The PXD generates approximately a factor of ten the data of all other sub-detectors.

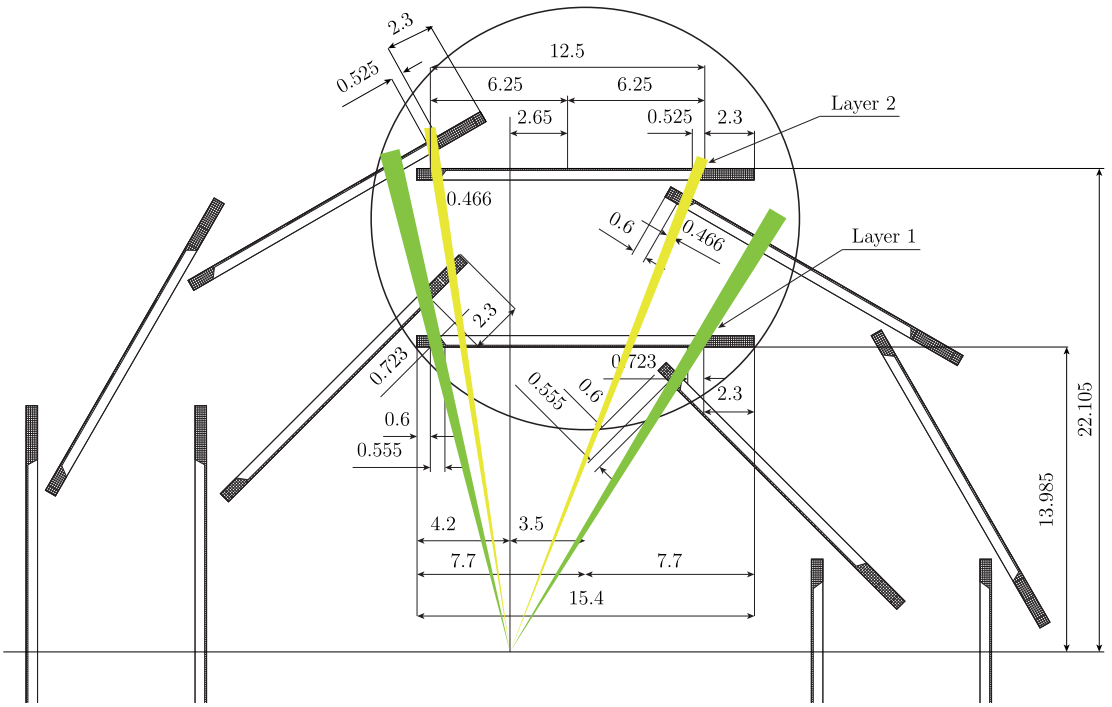


Figure 4.51: Windmill structure of the sensor modules around the beam pipe. The green and yellow wedges represent particles passing the overlap of two sensors. The green ones traverse two modules (one in the active region) of layer 1 and a single sensor of layer 2. The yellow ones cross one active sensor in layer 2. As shown by the left yellow wedge, the particle can also pass four modules.

mechanical stiffness of the self-supporting structure, the border is 525 µm thick, while the sensitive part is only 75 µm thick.

4.12 Power Consumption and Cooling

The power consumption of the DEPFETs within a module is quite low, because of the rolling shutter readout amounting to

$$P_{\text{module}} = \langle I_{\text{drain}} \rangle V_{\text{ds}} N_{\text{pixel}} = 100\,\mu\text{A} \cdot 5\,\text{V} \cdot 1000 = 0.5\,\text{W}$$

where $\langle I_{\text{drain}} \rangle$ denotes the average Drain current, V_{ds} is the Source-Drain voltage and N_{pixel} is the number of simultaneously enabled pixels. However, the power consumption of the readout and control ASICs contribute the major part of the total power of the PXD, which is approximately 9 W per module, with a total of 360 W for all 40 modules [179]. The details are listed in Tab. 4.18.
Active cooling is required to ensure a proper functionality of the detector, minimizing the shot noise and the leakage current of the sensors. The DEPFETs and the Switchers are cooled by forced nitrogen flow guided by carbon tubes (having holes with a diameter of 0.3 mm) in the SCB, shown as the dark-turquoise and violet pipes in Fig. 4.52. The pipes are located in the acceptance area of the PXD. The readout ASICs are cooled by CO_2 as described in the following. The EOS (region

Table 4.18: Expected and measured power consumption of a single module. The measurements were performed with the DHP 1.2, the DCD 4.2 and the Switcher 2.2.

Device	Expected power	Measured power
DHP	} ∼ 8 W	1.1 W
DCD digital		1.6 W
DCD analog		5.6 W
Switcher	∼ 0.5 W	0.2 W
DEPFET Sensor	∼ 0.5 W	0.5 W
Total	∼ 9 W	9 W

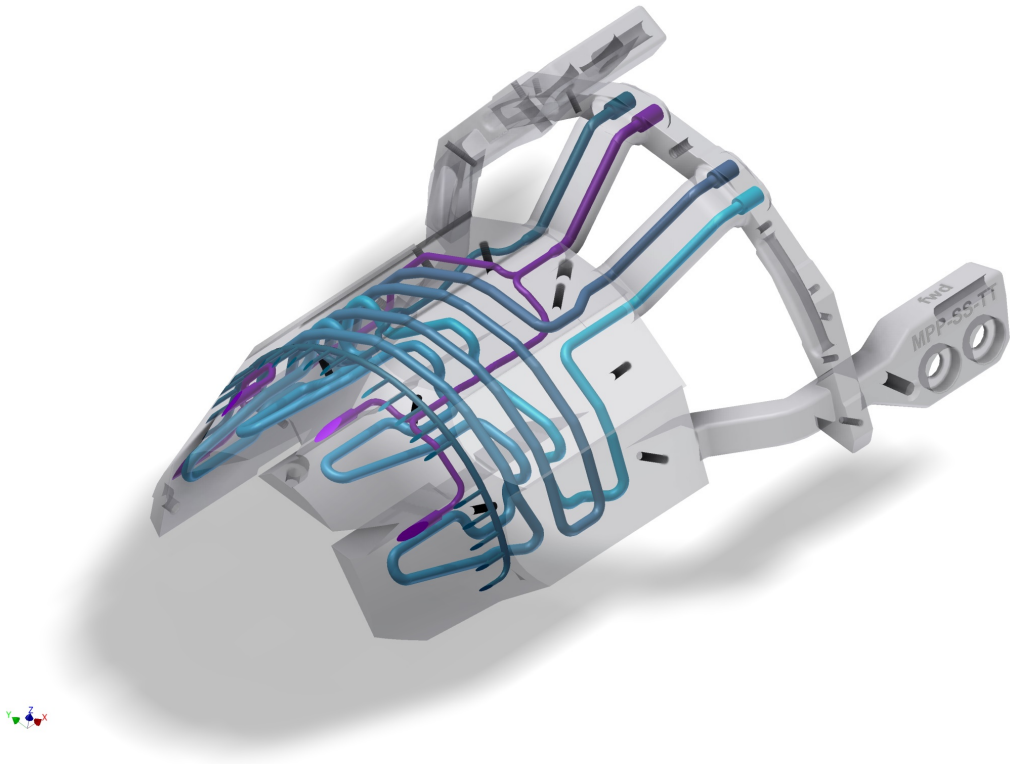


Figure 4.52: SCB of the PXD. The upper two pipes (dark turquoise and violet are nitrogen connections. The lower right connections are the pipes for the CO_2 [1].

where the DCDs and DHPs are placed; see Fig. 4.45) of the module is mounted on the SCB and fixed by M1.2 screws (the torque is 7 mNm). The SCB is produced using metal 3D printing technology [1] and is shown in Fig. 4.52. The SCB is cooled by CO_2, based on the 2-phase accumulator controlled loop (2PACL) method [180]. Using two-phase CO_2 is favorable because the high heat transfer coefficients and the small tubes which are routed within the SCB. The temperature of the cooling medium is approximately −30 °C [181]. The ASIC heat is used to evaporate the liquid CO_2 while keeping the temperature and the pressure constant. Using this cooling concept does not require any additional cooling hardware in the active area

of the sensor and thus does not contribute to the overall material budget. A thermal mock-up has been built to study the temperature distribution, the mechanical and the thermal performance and to optimize the cooling concept [179].

4.13 Signal Transport and Data Acquisition

For the off-module signal transport, a Kapton cable is attached to the module, which has a length of approximately half a meter (see Fig. 4.53). The Kapton is soldered on the module and an additional $\sim$ 90 wire-bonds are placed for the interconnection of the electrical signals between the Kapton and the module. On the other end, it is connected to a printed circuit board (PCB) with a tiny 100 pin connector.

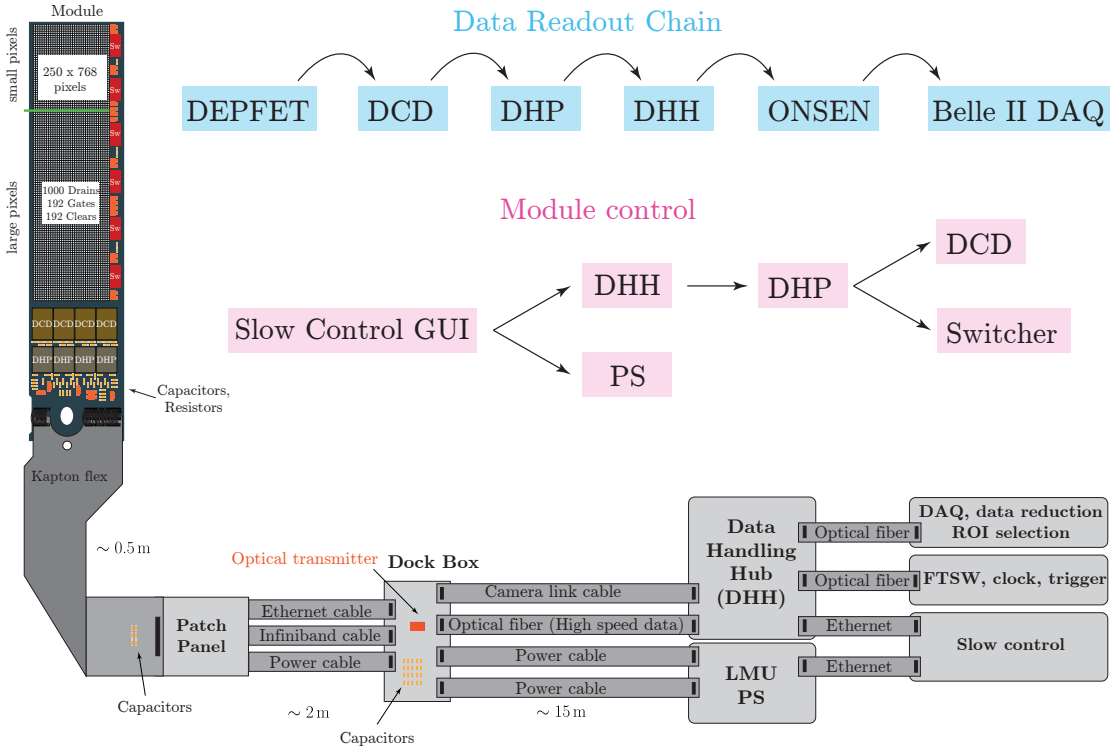


Figure 4.53: Sensor and accompanied readout chain of a module.

In addition, the analog and digital grounds are connected in the Kapton cable. All of the DEPFET data, the control signals and the entire powering is transferred via the Kapton cable. Since there are four different modules (layer 1 forward/backward and layer 2 forward/backward), four different designs are required. Depending on the module type, the Kapton cables have different lengths between 430 mm and 471 mm.

The Kapton cable is plugged into the patch panel[16] (see Fig. 4.53). Two data cables and one power cable are soldered onto the patch panel. Their ends are plugged into the *dock box*. This box is a PCB equipped with decoupling capacitors (for

[16]There are also four different patch panels depending on the module type.

filtering of the common mode noise, see Sect. 4.14.3) and it serves as junction box to interface between different cables. The DEPFET signals are transferred from the module to the dock box by copper wires. An optical transmitter in the dock box converts the electrical input to an optical output, which is further transmitted via fibers to the DHH. The DHH and the dock box are connected by an optical fiber and by a camera link cable to provide the control signals. The DHH receives triggers from the front-end timing switch (FTSW) and transmits the data from the module to the ONSEN and finally to the overall Belle II DAQ system. Two $\sim 15\,\mathrm{m}$ cables provide the power from the PS to the dock box. The box and the DHH are controlled by the Experimental Physics and Industrial Control System (EPICS) based slow control.

4.14 Noise Contributions

This section is split into three parts. First, the noise contributions regarding the detector are presented: The shot noise, the thermal noise (in the channel and the polygate) and the Flicker noise. Second, other noise sources contributing to the signal and the readout electronics are discussed. In the last part, the common mode noise is introduced. The Fano noise gives information about the fluctuations of generated electron-hole pairs in silicon by absorbed photons, which is discussed in app. B.4.
As discussed in the previous sections, the current of the DEPFET is analyzed by the DCD. The current measuring hardware in the DCD is composed of an operational amplifier with a feedback network, consisting of a resistor and a capacitor. A simplified schematic of the typical noise sources is shown in Fig. 4.54.

4.14.1 Detector Noise

In this section, the noise originating from the DEPFET matrix and from the ASICs is discussed.

Shot Noise

Shot noise occurs from the leakage current of the bulk and from interface traps at the surface. Charge carriers crossing the *pn* junction is a random process and dominated by statistical fluctuation. The shot noise current (mean square) is given by [133, 182]:

$$\langle I_{\mathrm{sh}}^2 \rangle = 2eI_{\mathrm{f}}\Delta f \tag{4.14.1}$$

where Δf denotes the frequency bandwidth of the system, e is the elementary charge and I_{f} is the forward junction current.
For MOSFETs, the shot noise is rather negligible. It is in the order of 10–100 fA, which is much smaller compared to the Drain current ($\sim 100\,\mu\mathrm{A}$) [183, chapter 11]. Shot noise is more present in short channel MOSFETs ($d_{\mathrm{ox}} < 20\,\mathrm{nm}$, where d_{ox} denotes the thickness of the oxide) due to the Gate tunnel current of the leaky oxide. For long channel MOSFETs, the charge entering the depletion region is due to thermal vibrations in the resistance of the channel [184, chapter 8].

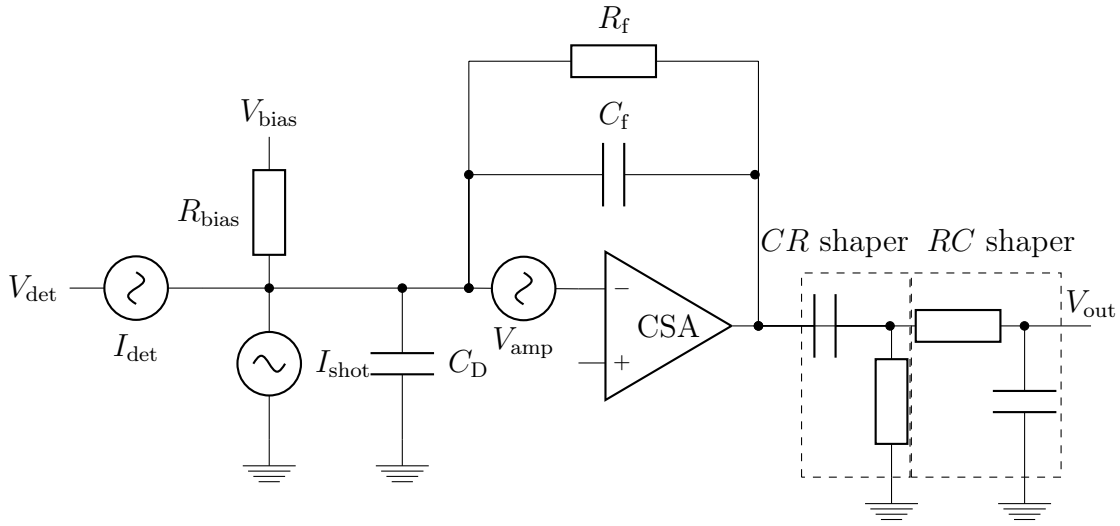


Figure 4.54: Simplified schematics of the DCD amplifier with typical noise sources. V_det and I_det denote the noise sources from the detector, i.e., thermal channel noise and Flicker noise. I_shot is the noise spectrum caused by the leakage current and the bias network. C_D represents the capacitance of the detector. V_amp is the power spectrum of noise at the input of the CSA. R_f and C_f are the feedback resistor and capacitance. R_bias denotes the bias resistor. The CR shaper corresponds to an differentiator while the RC circuit corresponds to an integrator.

Thermal Noise

Thermal noise is created by random thermal excitations of charge carriers in (semi)-conductors, independent of the applied voltage. It is theoretically well understood and can be described mathematically by thermodynamics. For the voltage fluctuations $\langle V_\mathrm{n}\rangle$ of an ohmic resistor R without any applied voltage, the spectral density is [133]:

$$\frac{\mathrm{d}\langle V_\mathrm{n}^2\rangle}{\mathrm{d}f} = 4k_\mathrm{B}TR \quad \Leftrightarrow \quad \frac{\mathrm{d}\langle I_\mathrm{n}^2\rangle}{\mathrm{d}f} = \frac{4k_\mathrm{B}T}{R} \tag{4.14.2}$$

where k_B represents the Boltzmann constant, T is the absolute temperature and f is the frequency. Since the thermal noise is independent from the frequency, it is sometimes also called *white noise*.

Channel Thermal Noise

For a MOSFET, the resistance of the conducting channel below the *external Gate* is not constant. Therefore, another approximation is required, which is derived in [143, 185]. One can distinguish three cases:

- **Linear region**: The MOSFET operates in the linear region ($V_\mathrm{ds} \ll V_\mathrm{gs} - V_\mathrm{T}$), where V_ds denotes the Source-Drain voltage, V_gs is the Gate-Source voltage

and V_{T} the threshold voltage. The Drain current noise is:

$$\frac{\mathrm{d}\langle I_{\mathrm{d}}^2\rangle}{\mathrm{d}f} = 4k_{\mathrm{B}}Tg_0 \tag{4.14.3}$$

where g_0 is the channel conductance at zero Drain-Source voltage.

- **Saturation point**: Operating at the saturation point ($V_{\mathrm{ds}} = V_{\mathrm{gs}} - V_{\mathrm{T}}$), the thermal noise for the channel is:

$$\frac{\mathrm{d}\langle I_{\mathrm{d}}^2\rangle}{\mathrm{d}f} = \frac{8}{3}k_{\mathrm{B}}Tg_{\mathrm{m}} \tag{4.14.4}$$

where g_{m} is the transconductance of the Gate (see eq. (4.5.2)).

- **Saturation region**: Applying a voltage $V_{\mathrm{ds}} > V_{\mathrm{gs}} - V_{\mathrm{T}}$ the thermal noise in the channel is mathematically written as

$$\frac{\mathrm{d}\langle I_{\mathrm{d}}^2\rangle}{\mathrm{d}f} = 4k_{\mathrm{B}}T\gamma g_{\mathrm{m}} \tag{4.14.5}$$

where γ is a complex function of biasing and MOSFET parameters [185].

Other Sources for Thermal Noise

The statistical fluctuations of the charge carriers (in the conductive channel below the *external Gate*) affect the Gate-channel capacitance. Due to the capacitive coupling, the Gate current noise is approximated by [185]:

$$\frac{\mathrm{d}\langle I_{\mathrm{g}}^2\rangle}{\mathrm{d}f} \approx 4k_{\mathrm{B}}T\frac{g_{\mathrm{m}}}{5}\left(\frac{f}{f_{\mathrm{T}}}\right)^2 \tag{4.14.6}$$

where $f_{\mathrm{T}} \approx \frac{g_{\mathrm{m}}}{2\pi C_{\mathrm{GS}}}$ is the cut off frequency of the MOSFET and C_{GS} is the Gate-Source capacitance. Moreover, thermal Drain current noise is also caused by statistical fluctuations of electrons in the *internal Gate*, which modulate the Drain current by the capacitive coupling.

Polygate Thermal Noise The total spectrum of the Drain noise for n Gates (*polygates*) can be approximated by [185]:

$$\frac{\mathrm{d}\langle I_{\mathrm{d}}^2\rangle}{\mathrm{d}f} = 4k_{\mathrm{B}}Tn\frac{R_{\mathrm{i}}}{12}g_{\mathrm{m}}^2 \tag{4.14.7}$$

where R_{i} denotes the resistance of Gate i. The noise decreases for increasing number of Gates. More details are given in [185].

Substrate Thermal Noise The resistance of the substrate also contributes to the thermal noise of the Drain current. The noise can be reduced by an appropriate bias of the bulk substrate [185].

Flicker noise

Flicker noise, also known as $1/f$ noise, is observed in all kinds of electronic devices. It is described by the *number fluctuation model* [186, 187]. It assumes that free charge carriers are randomly trapped and detrapped some time later within the Gate oxide, at the boundary of the silicon and silicon oxide region [185, 188]. When the charge carrier is temporarily trapped, the Drain current of the MOSFET is modulated. The current noise is interpreted as a superposition of charge carriers, which are trapped and released. The modulation of the Drain current is expressed as:

$$\frac{\mathrm{d}\langle I_\mathrm{d}^2\rangle}{\mathrm{d}f} = \frac{K_\mathrm{F} I_\mathrm{ds}}{C_\mathrm{ox} L^2 f}, \tag{4.14.8}$$

where K_F is a device-specific constant The number of charge carriers being trapped per unit time depends on the temperature, the electron capture cross-section and on the depth of trap [143].

4.14.2 Noise in the Readout Electronics

The total spectrum of the noise at the output of the charge sensitive amplifier (CSA) (see Fig. 4.54) is given as [189]:

$$\langle V_\mathrm{CSA}^2(f)\rangle = \underbrace{\left|\frac{C_\mathrm{D}+C_\mathrm{f}+C_\mathrm{gs}+C_\mathrm{gd}}{C_\mathrm{f}}\right|^2 \langle V_\mathrm{amp}^2\rangle}_{\text{amplifier noise}} + \underbrace{\left|\frac{1}{2\pi \mathrm{i} f C_\mathrm{f}}\right|^2 \langle I_\mathrm{shot}^2\rangle}_{\text{leakage and bias network}}, \tag{4.14.9}$$

where C_D denotes the detector capacitance, C_f is the capacitor in the feedback path of the CSA, C_gs is the Gate-Source capacitance and C_gd is the Gate-Drain capacitance. The entire input capacitance at the CSA is abbreviated by:

$$C_\mathrm{tot} = C_\mathrm{D} + C_\mathrm{f} + C_\mathrm{gs} + C_\mathrm{gd}. \tag{4.14.10}$$

The noise of the output of the CSA is weighted by the response function of the shaping amplifier to obtain the total noise spectrum at the output of the shapers. A response function of a simple CR-RC[17] shaper [185, 189] is assumed:

$$H_\text{CR-RC}(f) = \left(\frac{\mathrm{i}2\pi f\tau}{1+\mathrm{i}2\pi f\tau}\right)\left(\frac{A}{1+\mathrm{i}2\pi f\tau}\right), \tag{4.14.11}$$

where τ describes the time constant of the RC integrator and the CR differentiator and A is the DC gain of the integrators.
This results in the total integrated RMS noise after the CR-RC shaper, given as:

$$\langle V(f)_\mathrm{out}^2\rangle = \int_0^\infty |V(2\pi\mathrm{i}f)|^2 |H_\text{CR-RC}(2\pi\mathrm{i}f)|^2 \mathrm{d}f. \tag{4.14.12}$$

[17] This consists of a CR (capacitor-resistor) circuit, which is followed by a RC (resistor-capacitor) circuit. Using this arrangement, the pulse passes the CR shaper first (differentiator), afterwards the RC shaper (integrator).

The equivalent noise charge (ENC) is calculated by dividing the total integrated RMS noise by the signal amplitude for a single electron charge q, i.e.,

$$ENC^2 = \frac{\langle V_{\text{out}}^2 \rangle}{V_{\text{max}}^2} \qquad \text{with } V_{\text{max}} = \frac{qA}{C_{\text{f}}\,\text{e}}. \tag{4.14.13}$$

Thus, one obtains (e denotes the Euler's number) [185]:

$$\begin{aligned} ENC_{\text{Thermal}}^2 &= \frac{8}{3}\frac{k_{\text{B}}T}{g_{\text{m}}} C_{\text{tot}}^2 \frac{1.57e^2}{4\pi\tau q^2} \\ ENC_{\text{Flicker}}^2 &= \frac{K_{\text{f}}}{C_{\text{ox}}^2 WL}\frac{C_{\text{tot}}^2 e^2}{2q^2} \\ ENC_{\text{Leakage}}^2 &= qI_{\text{leak}}\frac{1.57e^2\tau}{2\pi q^2} \\ ENC &= \sqrt{ENC_{\text{thermal}}^2 + ENC_{\text{Flickr}}^2 + ENC_{\text{shot}}^2} \end{aligned}$$

$$ENC = \sqrt{\underbrace{\frac{2}{3}k_{\text{B}}T\frac{1}{g_{\text{m}}}1.57\frac{C_{\text{tot}}^2 e^2}{\pi q^2\tau}}_{\text{thermal noise}} + \underbrace{\frac{K_{\text{f}}}{C_{\text{ox}}^2 WL}\frac{C_{\text{tot}}^2 e^2}{2q^2}}_{\text{Flicker noise}} + \underbrace{I_{\text{leak}}1.57\frac{e^2\tau}{2\pi q}}_{\text{shot noise}}} \tag{4.14.14}$$

For the DEPFET the total ENC is given as [130]:

$$ENC = \sqrt{\underbrace{\alpha\frac{8k_{\text{B}}Tg_{\text{m}}}{3g_{\text{q}}^2}\frac{1}{\tau}}_{\text{thermal noise}} + \underbrace{2\pi a_{\text{f}}C_{\text{tot}}^2}_{\text{Flickr noise}} + \underbrace{qI_{\text{leak}}t_{\text{frame}}}_{\text{shot noise}}} \tag{4.14.15}$$

where $\alpha \approx 1$, depending on the shaping of the amplifier, a_{f} is a process dependent normalization factor and t_{frame} is the frame time of the PXD.
In order to minimize the ENC the following issues should be considered:

- Cooling of the device to lower the thermal noise and the leakage current.
- Keeping the overall capacitance at minimum.
- Find an optimal time constant τ of the shaper (thermal noise decreases with large τ in contrast to the shot noise, which increases for large τ).
- On the one hand, for minimizing the Flicker noise the length L and the width W of the *external Gate* should be as small as possible. On the other hand, W and L also influence the external (g_{m}) and internal (g_{q}) amplifications. The g_{m} should be large and the g_{q} should be low to minimize the ENC.

The ATHENA experiment performed DEPFET thermal noise measurements. The thermal noise is 3.3 electrons for a readout time of 5 µs [190]. Scaling this to the readout time in Belle II, which is approximately 50 ns (105 ns for enabling a row_{gate} in which the Clear pulse is applied for 32 ns and additional 20 ns for enabling and disabling the DEPFET) according to eq. (4.14.2) the thermal noise contribution is estimated to be approximately 25 electrons.

The leakage current noise, i.e., the shot noise (see eq. (4.14.1)), can be divided into the *bulk generated leakage current* and the *surface generated current*: When SuperKEKB reaches an integrated luminosity of $50\,\mathrm{ab}^{-1}$, corresponding to neutron fluences of $\Phi_{\mathrm{neq}} \approx 2 \cdot 10^{13}\,\mathrm{neq/cm}^2$, the bulk leakage current noise due to radiation damage corresponds to approximately 47–49 electrons [138, 191].
Furthermore, the surface generated leakage current noise is calculated to approximately 50 electrons [191] after irradiation (when SuperKEKB reaches the integrated luminosity of $40\,\mathrm{ab}^{-1}$, corresponding to a dose of $\sim 105\,\mathrm{kGy}$).

The maximal noise in the DCD is expected to be approximately 120 nA, corresponding to 240 electrons (assuming a $g_{\mathrm{q}} = 500\,\mathrm{pA}/e^-$), which is below one LSB of 160 nA. Thus, the noise contribution from the readout electronics clearly dominates the noise contributions. The overall noise of the DEPFET and the DCD is estimated by:

$$\Delta_{\mathrm{Noise}} \approx \sqrt{\underbrace{(33\,e^-)^2}_{\text{thermal noise}} + \underbrace{(43\,e^-)^2}_{\substack{\text{bulk}\\ \text{shot noise}}} + \underbrace{(50\,e^-)^2}_{\substack{\text{surface}\\ \text{shot noise}}} + \underbrace{(240\,e^-)^2}_{\text{DCD noise}}} = 251\,e^- \qquad (4.14.16)$$

The signal of a MIP corresponds to approximately 2.7 µA, corresponding to ($\sim$ 5000 electrons) [153]. Thus the signal-to-noise ratio is more than 20. However, due to the power lines, unshielded cable serving as an antenna for pick up noise, the overall noise of the module with the required system components is studied in Sect. 6.7.

4.14.3 Common Mode Noise

In addition to the noise from the detector and electronics, additional noise could occur in the power supply lines, which leads to common mode noise, resulting in undesired and random behavior of the electronic circuit. The common mode noise originates from coupling a power line to an external conductor, such as a chassis, earthing or another conductive material. Typically, DC-DC converters, mounted in the power supply, produce most of the common mode noise due to the capacitive coupling between the output voltages (for the module) and the chassis ground[18].
In normal operation, the current should flow along a wire from the power supply to the load, i.e., the PXD module. Due to possible ground loops and the capacitive coupling of the system, a fraction of the current returns via the chassis and not in the dedicated wire. A sketch is shown in Fig. 4.55.
The finite output impedance of the power supply and the current consumption of the PXD module variable in time are susceptible to inductive and capacitive couplings.
In addition, the long cables ($\sim 15\,\mathrm{m}$) between the PS and the module can pick up noise, i.e., serve as antennas. Another reason for common mode noise is the ground instabilities of the power supply. Common mode noise does not only affect a single net but also neighboring channels. For those reasons, it should be lowered to a

[18] Dedicated measurements have been performed in [192].

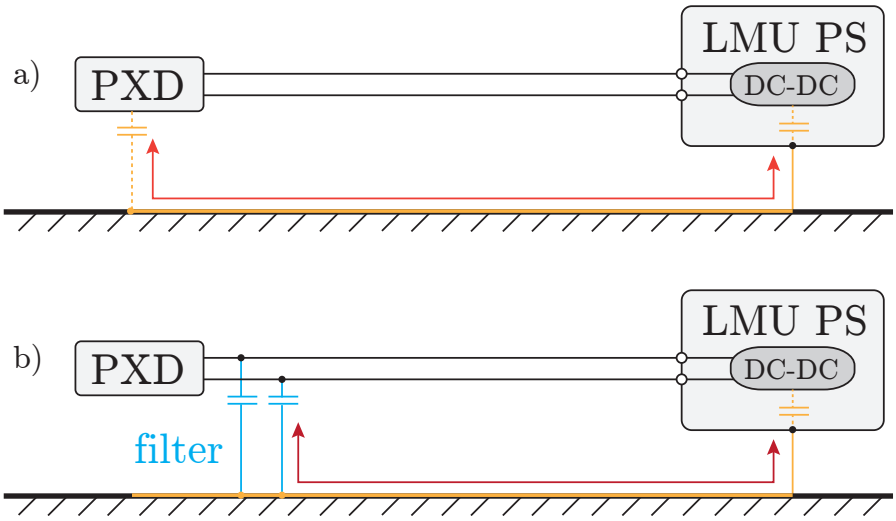


Figure 4.55: a) Common Mode Noise by capacitive coupling to chassis (ground). The current path is shown as the red arrow causing common mode noise. b) Capacitors, which couple to chassis (ground) are used to suppress the common mode noise.

minimum. In order to counteract this effect, decoupling capacitors (referenced to chassis), serving as filters should be assembled between the PS and the PXD. The common mode correction can be applied at different stages of the signal processing:

- The DCD has an internal analog common mode correction network. Using this feature, the mean of all connected pixels (250 out of 256 for each DCD) is subtracted from each Drain channel, mathematically expressed by:
  $\widetilde{\text{sig}}_{i,j} = \text{sig}_{i,j} - \sum_j p_{i,j}/250$ with $j \in \{\text{connected channels}\}$
  The realization in the DCD is explained in detail in [153].
- The DHP allows the correction of the signals by digital operation for zero suppressed data, as described below
- Offline common mode calculation and correction of the recorded data according to the same algorithm as used in the DHP. For this case, all pixels, which are connected to the same Gate, must be read out.

The signals in the DHP are corrected by the common mode correction as follows [166]. Since the readout of the 1000 DEPFET Drain currents is split into four DCDs and DHPs, the common mode correction procedures, performed by the readout ASICs, are performed for each DCD individually, i.e., DCD 1–DHP 1 have no exchange of information with the other three ASIC pairs.

1. Frames ($\sim$ 100–1000) are recorded without digital[19] common mode correction. Consequently, the signal of each individual DEPFET pixel is known, which corresponds to the median of the recorded data. The pedestal value for the pixel in row i and column j is denoted by $ped_{i,j}$ and the measured current value is $sig_{i,j}$.

[19]Digital is referred to DHP or a computer, in contrast to the analog common mode correction performed in the analog part of the DCD.

2. The average of the signals $\widetilde{CM}$ for all pixels[20] connected to a single Gate is calculated according to:

$$\widetilde{CM} = \frac{\sum_j sig_{i,j}}{N} = \frac{\sum_j sig_{i,j}}{250} \tag{4.14.17}$$

where N corresponds to the number of pixels in a row connected to the DHP, i.e., 250.

3. The common mode for the active Gate row is calculated, depending on the pixel signal, according to (DEPFET pixels with unusually large Drain currents are excluded):

$$CM = \frac{1}{N} \sum_j \left(sig_{i,j} \cdot \mathbb{1}(sig_{i,j} < \widetilde{CM} + th) + \widetilde{CM} \cdot \mathbb{1}(sig_{i,j} \geq \widetilde{CM} + th) \right) \tag{4.14.18}$$

where $\mathbb{1}$ is the indicator function:

$$\mathbb{1} = \begin{cases} 1 & \text{for } x \in \{\text{connected channels}\} \\ 0 & \text{for } x \notin \{\text{connected channels}\} \end{cases} \tag{4.14.19}$$

'th' denotes a certain threshold (in units of ADU). The calculated common mode value 'CM' is subtracted from all pixels of the active row to obtain the common mode corrected signal $\widetilde{sig}_{i,j}$:

$$\widetilde{sig}_{i,j} = sig_{i,j} - CM \quad \forall j \in \{\text{connected channels}\} \tag{4.14.20}$$

The contribution of the common mode noise is studied in detail in Sect. 6.7.

4.15 Outline of Measurements

The measurements are divided into three chapters.
Chapter 5 is dedicated to the Electrical Multi-Chip Module (EMCM). It serves for the verification of the proposed metal system on the module, i.e., the metal connections between the DEPFET pixels, ASICs and the end-of-stave [193]. The metal system of the outer backward module is placed on a piece of silicon with the same dimensions as an outer module of the pixel vertex detector. All 14 ASICs are flip-chipped on the module and the passive components are added. Finally, a prototype of the Kapton cable is attached to the module. Detailed characterizations of the entire control and readout procedures are then performed. The functionality of the Switchers are verified and the proper data readout of the DCDs. Furthermore, possible problems are deduced resulting in a change of the final metal system to be placed on the final modules. Having approved the layout (and additional design changes) the first prototype DEPFET matrix fully equipped with the metal system, all 14 ASICs, passive components and the Kapton cable were produced.
In chapter 6 the functionality of the DEPFET modules, the communication and

[20] one excludes the 6 non-connected channels of the DCD

synchronization between the 14 ASICs is optimized, the controlling of the individual control and readout electronics, the proper data transmission until the data acquisition system and the supply distribution on the module are studied. Various measurements are performed for detailed characterizations in terms of operation voltages, ASIC settings, noise, signal-to-noise ratios and control sequences. In addition to the system behavior, the measurements must be disentangled to distinguish between ASIC-related, DEPFET-related and module-related problems. Special attention is paid to the Gated Mode operation. This mode is essential during the damping time of the continuous top-up injection. Of particular interest are the system behavior and its response. The large parasitic capacitances and ohmic traces along the module could harm the operation. Dedicated software has been developed to operate the module in this mode and to analyze the measurements.

Chapter 7 presents the first operation of pilot run module in a beam test campaign. Having successfully developed the software to control, to read out and to analyze the modules, they are operated in a magnetic field of 1 T at the DESY facility with an incident electron beam of up to 6 GeV. The cluster charge distribution, intrinsic position resolution and hit efficiencies of the prototype modules are studied.

Chapter 5

Electrical Multi-Chip Module

5.1 Introduction

The layout of the electrical multi-chip module (EMCM) is shown in Fig. 5.1. It resembles the OB module, introduced in Sect. 4.9.1. The silicon support provides all of the electrical interconnections between the Kapton cable, the ASICs and DEPFETs. The silicon support structure acts like a PCB. The EMCM is meant to study the optimized metal system of the modules. It is equipped with all of the metal routings, passive surface-mount device (SMD) components and ASICs but without the DEPFET matrix. It has been developed for several reasons:

- Verification of circuit design. Investigation of the space requirements for routing and passive components (decoupling capacitors and LVDS termination resistors).
- Measurements of the signal integrity. The EMCM includes testpads to probe signals (like Switcher output drivers or voltages), measure cross-talk between neighboring signals, ground bounces, etc.
- Verification of the power distribution, voltage drops along the module, parasitic capacitances and resistances.
- Confirmation of the technological feasibility of the three metal layers (two aluminum, one copper).
- Practicing the flip-chipping of the ASICs on the module, assembly of the passive components and attachment of the Kapton cable (off-module interconnection) to the silicon module.
- Verification of the requirement of copper in the sensitive region (i.e., area above or below the DEPFETs).
- Noise measurements of all DCD channels at the full clock rate of 305 MHz required for the operation of the PXD at Belle II.
- JTAG programming and boundary scan of all 14 ASICs on a module.
- Optimization of timing and synchronization (DCD, Switcher and DHP).
- Stable operation of all data-links between the DHP and the DHE simultaneously.
- Optional: operation of a small DEPFET matrix on top of the EMCM.

These reasons mainly focus upon the three metallization layers and the test of the technological feasibility. In addition, it is important to perform module tests to ensure proper functionality of the ASICs and the inter-chip communication, i.e., the data transmission between the ASICs. The layout of the EMCM is shown in Fig. 5.1. An additional small DEPFET matrix (16 $\text{rows}_{\text{gate}}$ and 128 $\text{columns}_{\text{drain}}$ corresponding to 64 rows_{geo} and 32 $\text{columns}_{\text{geo}}$ due to the four-fold readout) is optionally mounted on top of the EMCM and connected via wire-bonds to the silicon support structure. The first 16 channels of the last Switcher are connected to the DEPFET matrix. The Drain lines are approximately 45 mm long to emulate the long Drain lines of the final Belle II PXD sensors. DHP 4 is connected to the Switchers and Switcher 6 controls the small matrix.

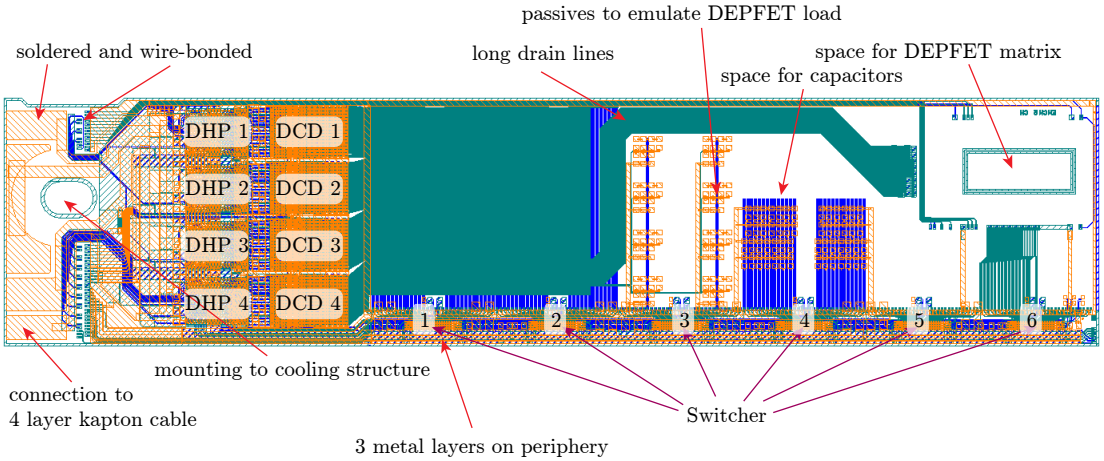


Figure 5.1: Layout of the EMCM. The blue lines show the first aluminum layer, the green routings represent the second aluminum layer and the orange traces are in the copper layer.

Seven EMCMs are produced on a single wafer (see Fig. 5.2). In order to assign each EMCM to the production runs, the modules are labeled with their wafer number followed by the DUT number. For instance, EMCM W17-3 corresponds to the EMCM on wafer 17 DUT 3.

First, electrical tests of the EMCM at the production site are performed by a "flying needle" system to test all of the different electrical nets for shorts and opens. After a successful quality check, pretested ASICs (on needle card setups) are mounted by flip-chipping (ASICs are soldered) on the EMCM. Afterwards, the passive components are attached. Subsequently, the Kapton cable is soldered and wire-bonded. In the next step, the fully-equipped module is mounted on an aluminum jig to fix it mechanically and to cool it properly. Finally, a PCB is installed close to the EMCM where some of the Switcher outputs are connected via wire-bonds in order to monitor the Gate and Clear outputs of the Switchers, e.g., the Clear pulses can be measured with an oscilloscope. A picture of the fully-installed module is shown in Fig. 5.3.

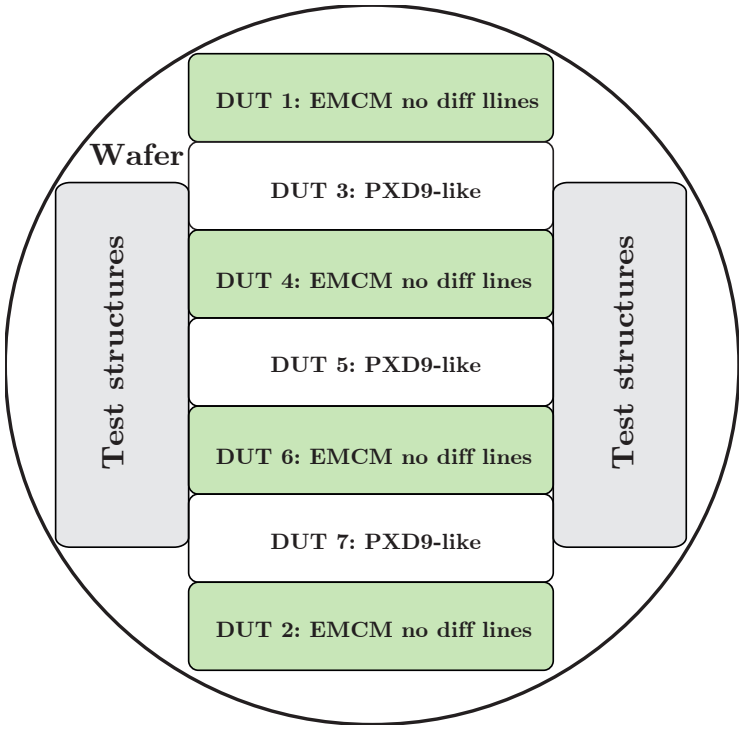


Figure 5.2: Sketch of the wafer layout with seven EMCM modules (DUT 1 to 7) on top [174]. For this particular wafer, four EMCMs with a non-LVDS clock between DCD and DHP are produced, as well as three EMCMs with a differential clock between the two ASICs.

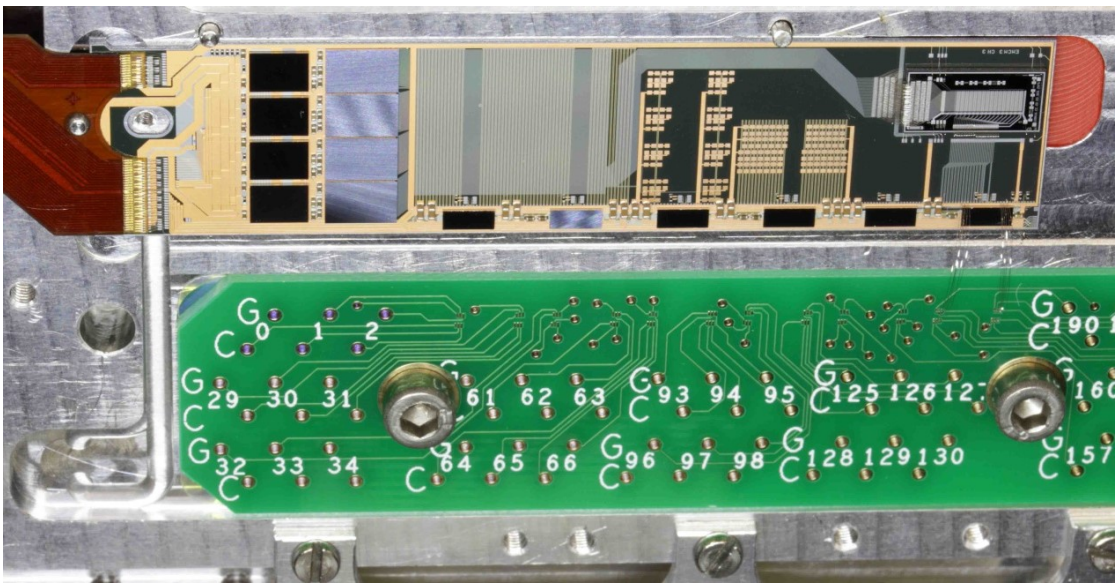


Figure 5.3: Fully-equipped EMCM with all ASICs (six Switchers, four DCDs and four DHPs), passives and attached Kapton cable. An active DEPFET sensor is placed on top and electrically connected via wire-bonds to the control and readout ASIC. Additional wire-bonds are connected to the PCB to verify approximately 20 Switcher outputs.

5.2 Lab Setup

A simplified setup, compared to the entire PXD DAQ system in Belle II, is used to perform the lab measurements. A diagram of the DAQ system is shown in Fig. 5.4.

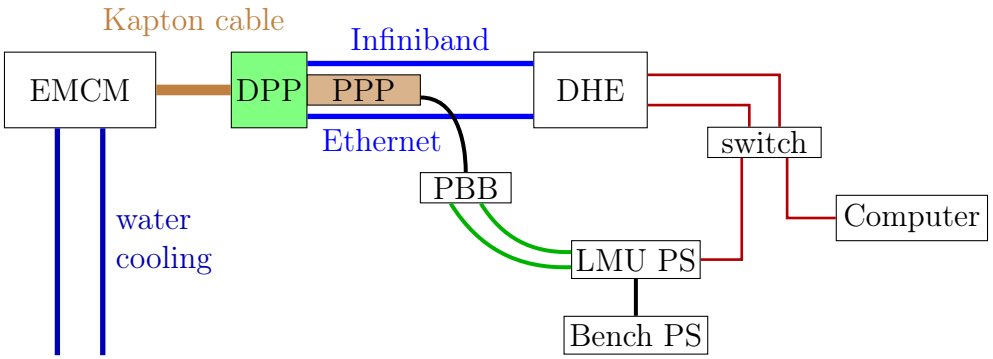


Figure 5.4: Diagram of the EMCM lab setup. The end of the Kapton cable is connected to two patch panels, the DPP and PPP. One Infiniband cable and one ethernet cable are connected to the DHE. The PPP is connected to the PBB, where the interconnection between Glenair connector and Mixed-D-Sub connector is established. Two bulky (12 mm diameter) green cables are connected to the power supply. The PS and DHE control and data-acquisition is done by a computer.

The Kapton cable is connected to two patch panels, the data patch panel (DPP) and the power patch panel (PPP). A *Glenair cable*[1] connects the PPP with the power breakout board (PBB), which in turn is connected to the power supply.
Power chain: A custom-made PS is biased by 24 V from an external, commercial bench power supply. Two bulky green cables (for the analog and digital domains, see Fig. 5.4) with a diameter of 12 mm are plugged between the PS and the PBB [194]. The PBB serves as conversion board between Mixed-D-Sub connectors (of the two green cables) and the Glenair connector. The Glenair cable connects the PBB and the PPP. The PPP is attached to the Kapton cable of the EMCM and the Glenair cable.
Data chain: A four-layer PCB, the DPP, is mounted at the end of the Kapton cable. Two cables (two Infiniband cables – later one Infiniband cable was replaced by a category 7 (CAT7) ethernet cable) establish electrical connections between the EMCM and the DHE. The DHE has two network connections, one for the slow-control and another one for the data output. Since the PS is also controlled via network, the three network cables (from the DHE and the PS) are plugged into a switch. A computer is also included in this network, which acquires the data from the EMCM and controls the PS and the DHE.
Cooling: The EMCM is mounted on an aluminum jig into which a cooling chamber is integrated. Circulating tap water keeps the jig and the EMCM at a low temperature ($\sim 16\,^{\circ}$C).

[1] The manufacturer is the company “Glenair”. For that reason the cable is called the “Glenair cable”.

5.3 Switcher measurements

On the EMCM each of the Switcher outputs has an aluminum pad ($50 \times 100\,\mu m^2$) that allows the measurement of the Gate and Clear output signals of the Switchers using a needle contact. Due to space constraints (the Clear and Gate pad of a single row have a spacing of only 30 µm), two needles probing simultaneously is not possible. Therefore, the measurements of Gate and Clear must be performed sequentially. An appropriate trigger signal for the oscilloscope is required in order to align the rising and falling edges of the Gate and Clear. The `SerIn` signal (see Sect. 4.8.1) could be a candidate. Unfortunately, the signal is LVDS, which cannot be probed with a single-ended probe. Furthermore, a special probe equipped with an active amplifier is needed to measure these fast pulses. Only one of these special probes is available in the lab.

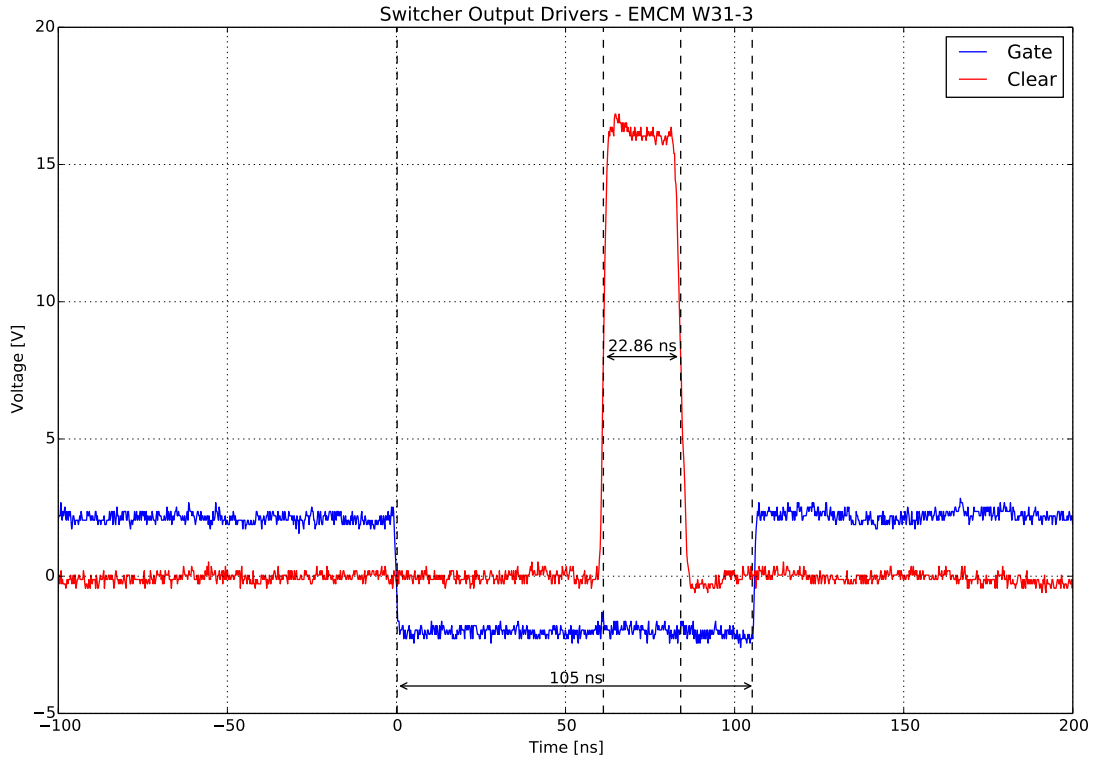


Figure 5.5: EMCM-W31-3: Switcher output drivers of Gate and Clear for a total total integration time of 20.15 µs, corresponding to a GCK of 76.33 MHz (nominal readout speed). The widths are measured at half-maximum.

Due to the problems described above, an appropriate electrical signal cannot be found to serve as a trigger for the oscilloscope. Therefore, the rising and falling edges of the Gate and Clear need to be aligned manually; as an indicator of the Clear pulse, the cross-talk effect between Clear and Gate is used. When the ClearOn voltage is applied, a small ripple appears in the Gate voltage. This indicates the rising edge of the ClearOn. The measurement of a Switcher output driver is shown in Fig. 5.5. The Gate is active for 105 ns. In addition, the Clear

pulse is only applied for 22.86 ns, although a pulse of 26.23 ns is expected. Parasitic capacitance, bad electrical contacts of the active probe and high ohmic resistance of the Switcher-substrate net (which will be explained in detail in chapter 6) cause these uncertainties. However, as it will be shown in chapter 6, the short Clear pulse is sufficient to empty the *internal Gate* completely.

5.4 Communication between DCD and DHP (DEPFET data) on the EMCM

In order to test the proper communication between the DCD and the DHP on the EMCM, the test pattern in the DCD (see Sect. 4.8.5) is enabled and the global and local delay parameters are varied. For each setting, the test pattern is transferred around 2000 times and the number of reading errors in the transmitted bit stream is plotted as a function of the local and global delay elements (the DCD registers are described in app. C.2).

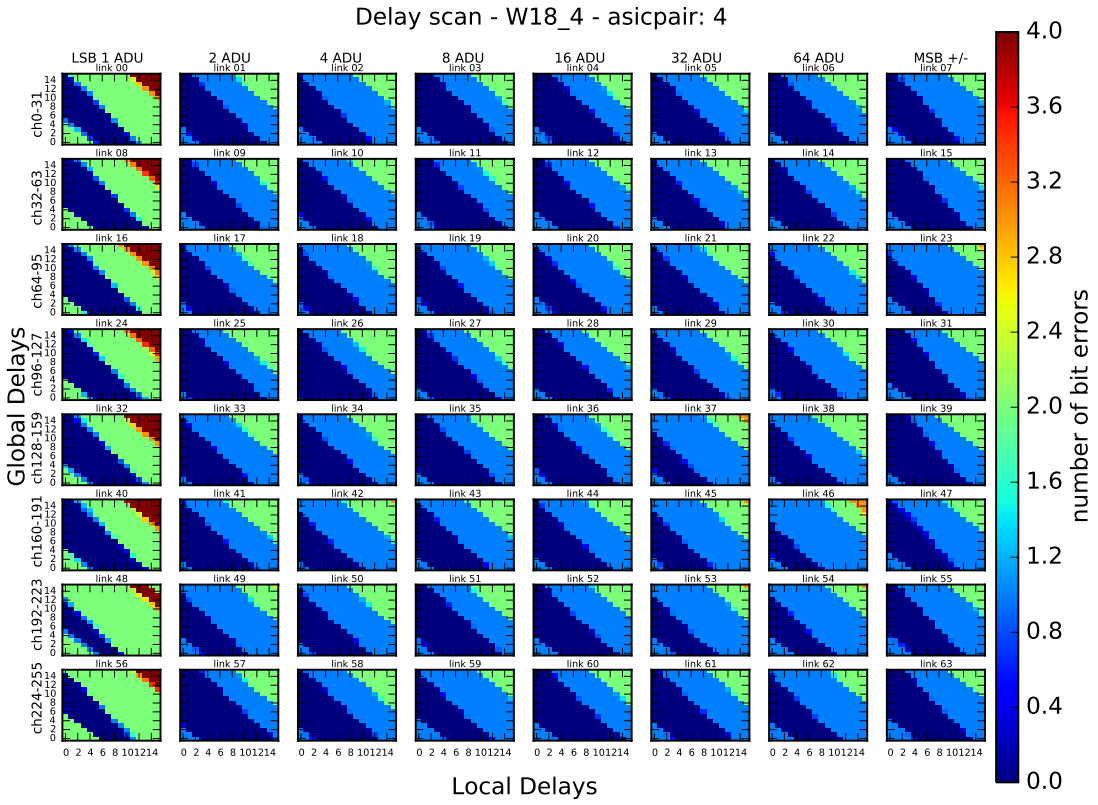


Figure 5.6: Scan of delay elements for all 64 transfer lines (bits) for DCD–DHP communication. The GCK is 62.5 MHz, corresponding to a 250 MHz DCD clock. The dark blue region represents delay settings without communication errors.

The measurements are performed for different global clocks (250 MHz and 305 MHz for the DCD) to see the difference of the data transmission errors. The number of transmission errors in terms of the global and local delays are shown in Fig. 5.6 and Fig. 5.7, respectively. It can be clearly seen that for the fast clock (i.e.,

GCK=76.33 MHz, Fig. 5.7), there are some transfer lines which do not transmit the test pattern correctly for any delay settings. Due to this reason, it has been decided to perform most of the measurements with the reduced speed of GCK=62.5 MHz, corresponding to an approximately 20 % slower data transmission compared to the nominal readout speed in the Belle II experiment.
However, the measurements shown in Fig. 5.6 and Fig. 5.7 are for a single ASIC-pair, i.e., one out of the four DCD–DHP combinations on an EMCM. For other pairs, no transmission errors have been observed for the appropriate delay settings. The test pattern is rather weak in terms of verifying the data transmission between the two ASICs. This is because of the low number of rising and falling edges of the bit stream (see Fig. 4.34). It would be favorable to have a more complex test pattern in terms of the mixture of logical 0 and 1. This has been developed in the latest DCD version [195].

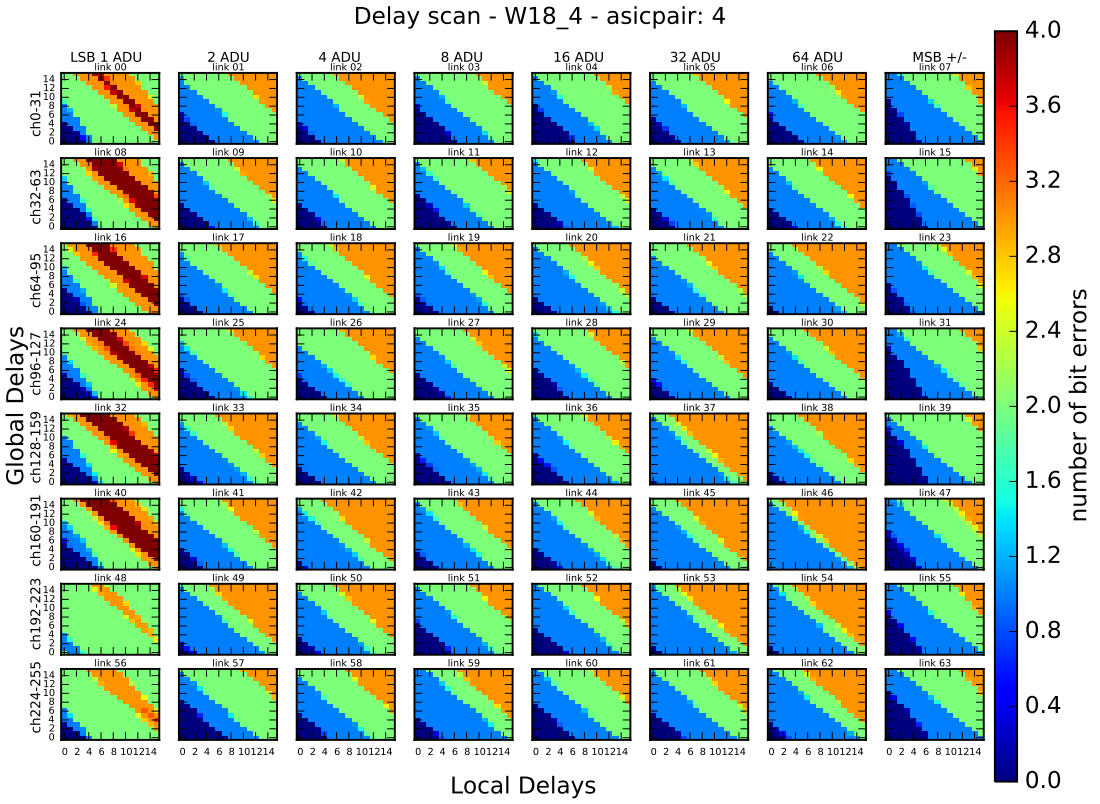


Figure 5.7: Scan of delay elements for all 64 transfer lines (bits) for DCD–DHP communication. The GCK is 76.33 MHz, corresponding to a 305 MHz DCD clock. The dark blue region represents delay settings without communication errors. Some of the transmission lines show transmission errors for all combinations of delay settings (no dark blue regions).

5.5 Communication between DHP and DCD (Offsets) on the EMCM

This section focuses on the influence of the transmission from the DCD to the DHP while sending data to the other direction. The layout, i.e., the routing of the data lines between the two ASICs, was already shown in Fig. 4.33.
The cross-talk studies of the bidirectional data transmission is done in the following way for the different DCD clocks (250 MHz and 305 MHz):

1. The test pattern is enabled while the 2-bit offset compensation is disabled. The best delay elements are determined ensuring proper data transmission from the DCD to the DHP, as explained in the last section.
2. The offset compensation is enabled. The measured data is analyzed bit-wise and deviations from the nominal test pattern are determined.

The lab measurements revealed that the cross-talk for a larger readout speed (DCD clock of 305 MHz) is larger compared to a slower readout (DCD clock of 250 MHz). In the following measurement, the faster clock speed is used since the impact of the cross-talk should be studied at the nominal Belle II readout speed[2]:
The measurements of interest are the bit errors of the digital DCD test pattern, which are received by the DHP when the 2-bit offset compensation is enabled. For this reason, random bits are sent from the DHP to the DCD simulating the active offset compensation for the DEPFET pixels, and the continuously read test pattern by the DHP is analyzed bit-wise. The ADU values of the problematic transmission lines, i.e., where errors in the data transmission from the DCD to the DHP occur, are plotted as a function of the readout cycle in Fig. 5.8. The problematic transfer lines, i.e., with bit errors in the transmission are denoted by DO$\langle x \rangle y$.

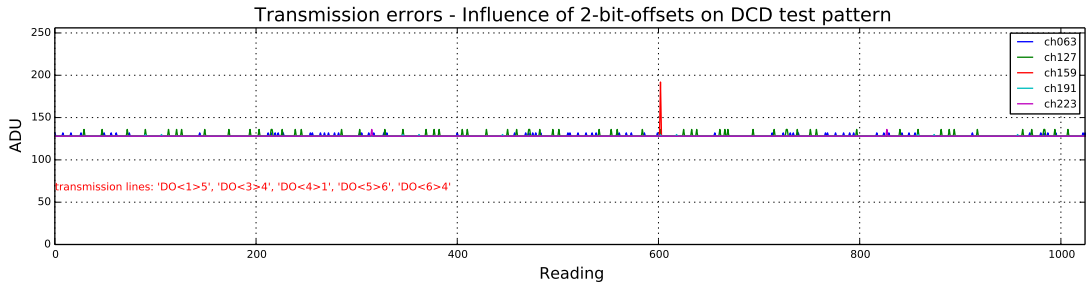


Figure 5.8: The measured ADU values of transfer lines with transmission errors for the inter-ASIC communication between DCD and DHP are shown as a function of the readout cycle.

Five out of eight column pairs (i.e., 32 DCD input channels as mentioned in the previous chapter, see Sect. 4.8.5) are affected by improper transmission of the DCD test pattern. In addition, the test pattern is very weak in terms of communication

[2]Correct delay values for the proper data transmission from DCD to DHP have been successfully found for all 64 transfer lines.

tests, since the number of falling and rising edges for the bits is rather low, as already stated in the previous section.
As a consequence, the spacing between the transfer lines on the module has been increased from 4 µm to 21 µm for the future designs, the parasitic capacitance on the DHP receiver side has been reduced in version 1.1 and the strength of the output drivers of the DCD has been increased for the next submissions (version 4.2) from 1.2 mA to 1.84 mA [153, 195].

5.6 Measurements of High-speed Signals

Two different measurements are performed in order to test the link stability and signal integrity, which are presented in the following subsections.

5.6.1 Eye diagram

The waveform of a digital signal is triggered on the rising and falling edges, corresponding to the transitions of logical 0 to logical 1 and vice versa. The edges for multiple transitions are sampled and stored. These are overlayed in a single plot as a synchronized superposition of all signal transitions. The obtained pattern

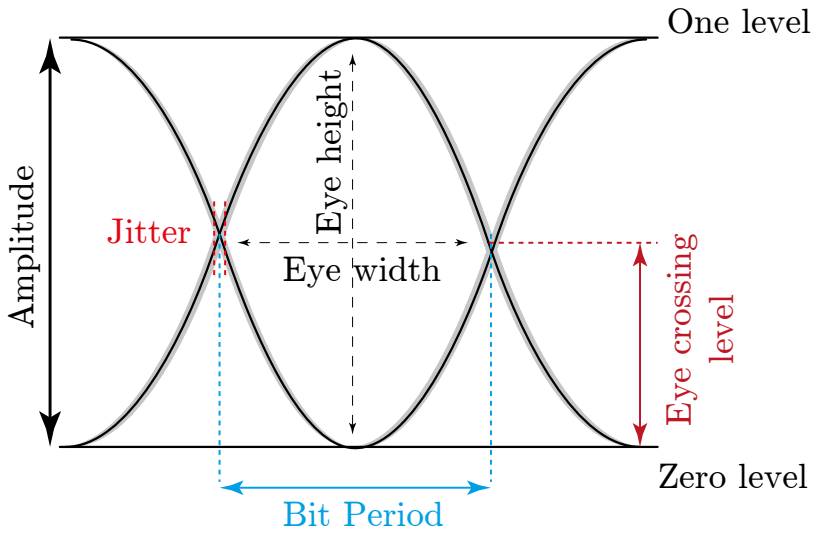


Figure 5.9: Sketch of an eye diagram and typical measurements.

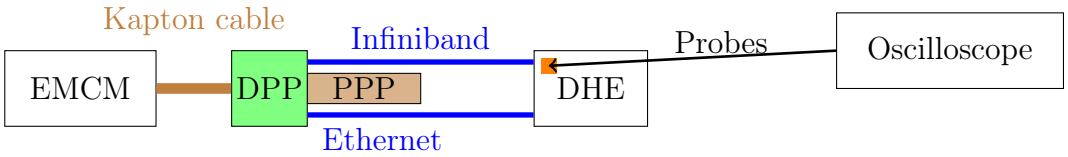


Figure 5.10: Diagram of high-speed signal measurement. The probes connected to the oscilloscope are soldered on the coupling capacitors of the DHE (orange rectangle).

resembles an eye (see Fig. 5.9). An oscilloscope with a high bandwidth is required for this measurement. For the measurements presented in this chapter, an oscilloscope with a bandwidth of 16 GHz has been used. The probes have been soldered directly on the input coupling capacitors, which are mounted in the DHE (see Fig. 5.10). In this way, the electrical quality of the digital signal can be visualized. The data eye diagram reveals the following information about the signal integrity (see Fig. 5.9):

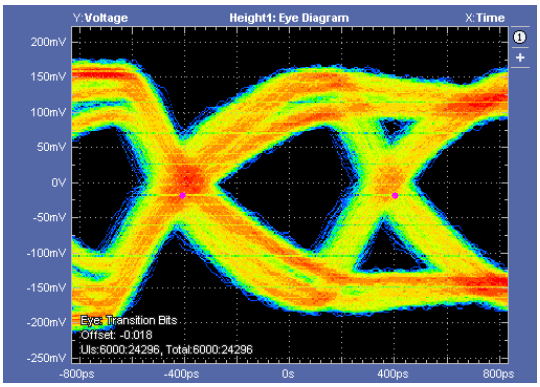
- One level: The voltage level that corresponds to the P signal level (for single-ended signals this corresponds to a logical 1).
- Zero level: The voltage level that corresponds to the N signal level (for single-ended signals this corresponds to a logical 0).
- Amplitude: The difference between the P and N level (for single-ended data, it is the difference between the 0 and 1 level). The received data will be interpreted as a 0 or 1 depending on its voltage level at the sampling point.
- Jitter: The jitter is the time deviation of the ideal period for a transferred bit, i.e., $t_{\text{jitter}} = |t_{\text{measured bit event}} - t_{\text{ideal bit event}}|$.
- Eye-crossing percentage: The eye-crossing percentage is defined by: $ec = \frac{\text{crossing level - zero level}}{\text{one level - zero level}} \cdot 100$.
- Bit period: The bit period is the time difference between two consecutive crossing points (T). The data transmission frequency is $f = 1/T$.
- Eye height: The vertical eye opening corresponds to the amplitude in the optimal case. Due to noise, attenuation and jitter the height is decreased.

The high-speed data between DHP and DHE is transmitted using LVDS. Therefore, the upper and lower levels correspond to the P and N levels (in the literature, the voltage levels are also defined as $V+$ and $V-$). The amplitude corresponds to the voltage difference of the two signals. The minimum peak-to-peak voltage corresponding to the height of the eye diagram must be at least 125 mV[196].
Measurements of the EMCM feature only the DHP0.2 and its successor, the data handling processor from TSMC (DHPT1.0). The high-speed link performance of later submissions of the ASICs have only been measured on a prototype consisting of one Switcher, one DCD, one DHP and one small (32×64 pixel) matrix (*hybrid 5*). Due to a design bug of the CML driver of the DHPT1.0, the core voltage must be raised from the nominal value of 1.2 V to higher voltages (1.4–1.6 V) in order to ensure stable high-speed links[3].
The measurements of the eye diagram for different clock frequencies and different cable lengths[4] of the DHPT1.0 on EMCM W17-3 are shown in Fig. 5.11. The parameters are listed in Tab. 5.1 (see Sect. 4.8.3).
The most stable link is established for GCK= 62.5 MHz and 3 m Infiniband cables. For the nominal readout speed of GCK= 76.33 MHz, some of the links could be established but they are not stable. The small eye height of 80 mV causes the problem.

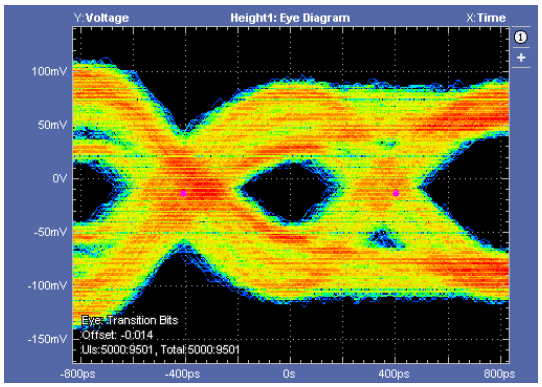
[3]The higher core voltage does not only influence the link stabilities but also the delay elements of the entire ASIC. Thus, changing the core voltage requires a new scan of the delay elements for the transfer lines between DCD and DHP.
[4]Ininiband cables of different lengths were used between the Data Patch Panel and the DHE.

Table 5.1: Overview of the parameters for different cable length, clock frequencies and core voltages.

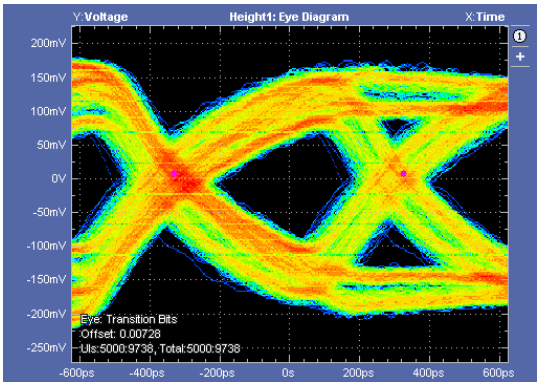
Signaling rate	bias	biasd	dly	$V_{DHP\ core}$	length	eye height	figure
1.250 GHz	127	48	2	1.45 V	3 m	∼ 165 mV	5.11a
1.250 GHz	15	150	2	1.60 V	15 m	∼ 150 mV	5.11b
1.525 GHz	127	48	2	1.60 V	3 m	∼ 80 mV	5.11c
1.525 GHz	7	150	2	1.64 V	15 m		5.11d



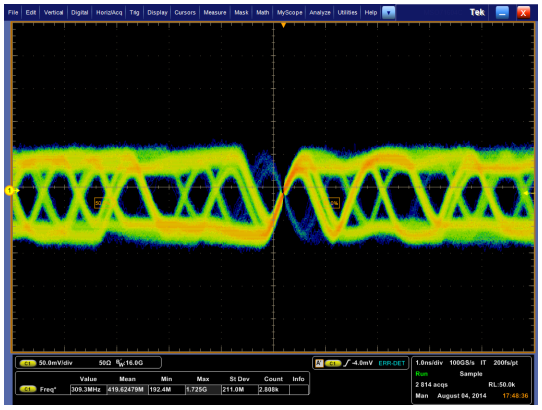
(a) GCK=62.5 MHz, VDD_{core} = 1.45 V, cable length 3 m, eye height=165 mV



(b) GCK=62.5 MHz, VDD_{core} = 1.60 V, cable length 15 m, eye height=150 mV



(c) GCK=76.33 MHz, VDD_{core} = 1.60 V, cable length 3 m, eye height=80 mV



(d) GCK=76.33 MHz, VDD_{core} = 1.64 V, cable length 15 m. An eye diagram cannot be measured.

Figure 5.11: Eye diagrams for different cable lengths and DHP-core voltages.

5.6.2 Link optimization with the DHE

The links between DHP and DHE are optimized by varying the three parameters `bias`, `biasd` and `dly`, which adjusts the amplitude, pre-emphasis and length of the pre-emphasis, as already shown in Fig. 4.29. For each step, an attempt is being made to establish the high-speed link, i.e., a synchronization between the DHP and DHE is initiated. In addition to this, the quality of the link is studied.

Internal diagnostic tools within the FPGA evaluate the eye opening. Figure 5.12 shows the results for a two-dimensional sweep of `bias` and `biasd` for four DHPs while the maximum length of the pre-emphasis is fixed.

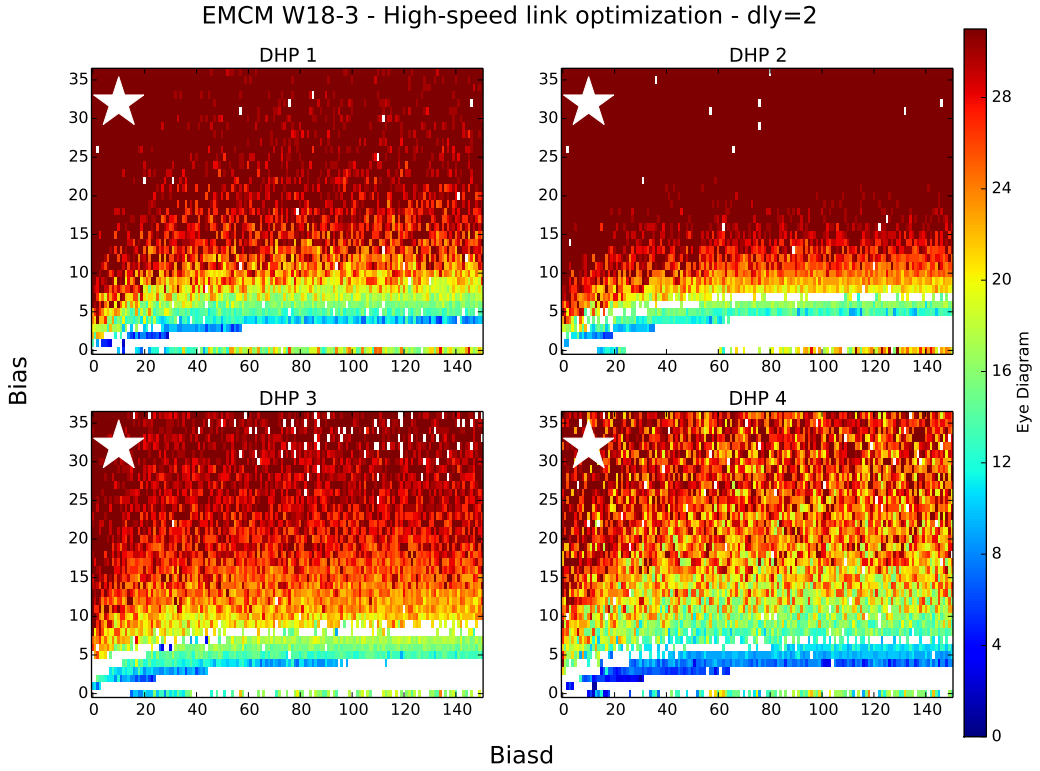


Figure 5.12: Sweep of the link optimization parameters `bias` and `biasd`. The maximum length for the pre-emphasis is fixed to dly=2. The white asterisks are proposals for the settings ensuring optimal link stability.

The color denotes the quality of the established link, where a high value corresponds to a data eye with a large opening, i.e., the link quality improves towards the red color. The blue color correspond to a data eye with a small eye opening (for details see [196]). Parameters with a large eye opening and a large border to the white gaps should be chosen. The proposed values are shown by the white asterisks, e.g., `bias`=32 and `biasd`=10. The white gaps show parameter combinations where no link could be established. Some dots are in parameter ranges where the links could be established well into the surrounding area. These are artifacts, which should not be taken seriously. If these parameters are set manually (after the measurement has been finished), the link could be established successfully. Hence, the data can be transmitted from the DHP to the DHE and can be sent further to the computer, the DAQ system in the lab. If a link cannot be established, no data from the DCDs can be transferred from the EMCM to the computer.

5.7 Matrix operation

A small DEPFET sensor with final Belle II layout, 75 µm thick (PXD9) matrix, called W30-F00 (see Sect. 4.9.1 for naming convention) has been placed on top of

another EMCM, called EMCM-W18-4. The first 16 outputs (Gate and Clear) of the last Switcher are connected via wire-bonds to the DEPFET device. For the readout of the small matrix, 128 Drain lines are wire-bonded to the input channels of DCD4.

The chosen Switcher sequence sends the `SerIn` control signal to the entire Switcher group once within 192 $\text{rows}_{\text{gate}}$. This results in enabling the matrix for 2.05 µs within a readout cycle of 24.58 µs.

The powering scheme of the matrix with the applied operation voltages is shown in Fig. 5.13.

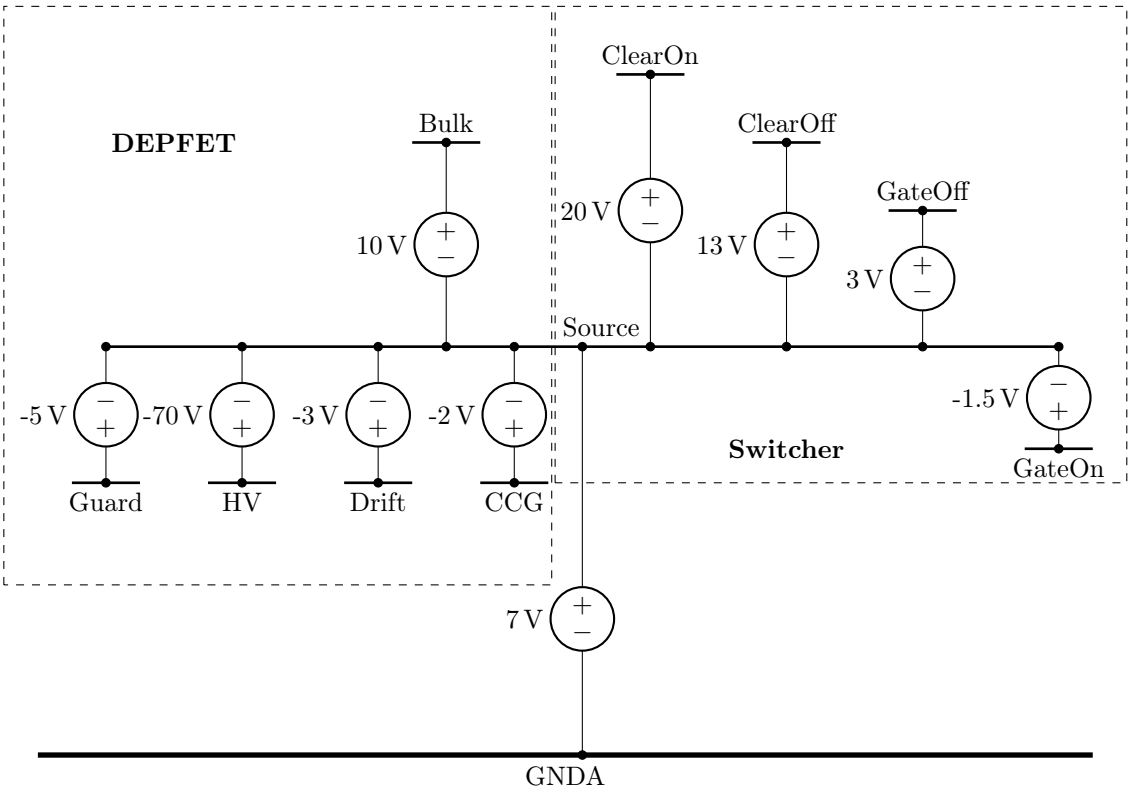


Figure 5.13: Biasing of the DEPFET matrix (assembled on the EMCM).

In order to verify the light sensitivity of the small DEPFET matrix on the EMCM, a laser spot ($\lambda_{\text{Laser}} = 660\,\text{nm}$) shoots at the matrix. The raw data is shown in Fig. 5.14. The laser spot is clearly visible as the large red spot. A pedestal gradient from left to right can clearly be seen along the Gate lines. In addition, some single pixels in the lower region (around rows 665–666) are visible. This is due to the saturation time of the ADCs within the DCD. The detailed characterizations of the PXD9 matrices to be used for the Belle II PXD will be presented in chapter 6. Additionally, the sampling point curve is recorded, which is introduced in the following section.

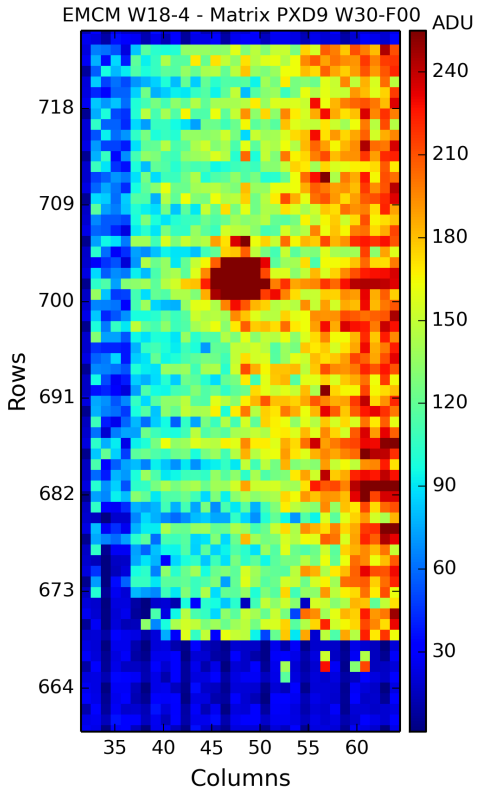


Figure 5.14: A red laser shoots at the small matrix of the EMCM. The spot is clearly visible as the round dark red dot in the center of the small matrix.

5.8 Sampling Point Optimization

Figure 5.15 illustrates the current curve of the matrix attached to the EMCM. The dashed red lines indicate the sampling point for a certain pre-defined Switcher sequence, with a spacing of 128 ns. The $\text{rows}_{\text{gate}}$ are switched on subsequently. For this reason, the Drain current of a $\text{column}_{\text{drain}}$ for multiple $\text{rows}_{\text{gate}}$, i.e., for the entire small DEPFET matrix with its 16 $\text{rows}_{\text{gate}}$[5] is visible. To understand the shape of the Drain current curve (as function of time), a zoom into two consecutive pixels is shown in Fig. 5.16. The dashed gray lines are arranged in 4 ns steps, corresponding to the shifts of the Switcher sequence. The mean value is plotted as the blue curve, the standard deviation is shown as the red area around the mean value. The row_{gate} i is enabled at 56 ns. Due to the long Drain lines (≈ 45 mm) on the EMCM, the signal rise time is quite long, at 20 ns. When the Drain current reaches a plateau, it can be sampled (between 86 ns and 150 ns). The sampling point is indicated by the red dashed line. Afterwards, the Clear pulse is applied to reset the pixel. Applying the large Clear voltage changes the transconductance in the transistor, which is visible as a drop of the Drain current. The next pixel row is enabled 8 ns after having stopped the Clear process. The different signal heights (in ADU) represent the individual pedestal currents of the DEPFET pixels. The pedestal spread is caused by variations in the production of the prototype matrices.

[5] Only 14 are visible due to the settling time of the ADCs within the DCD as mentioned above.

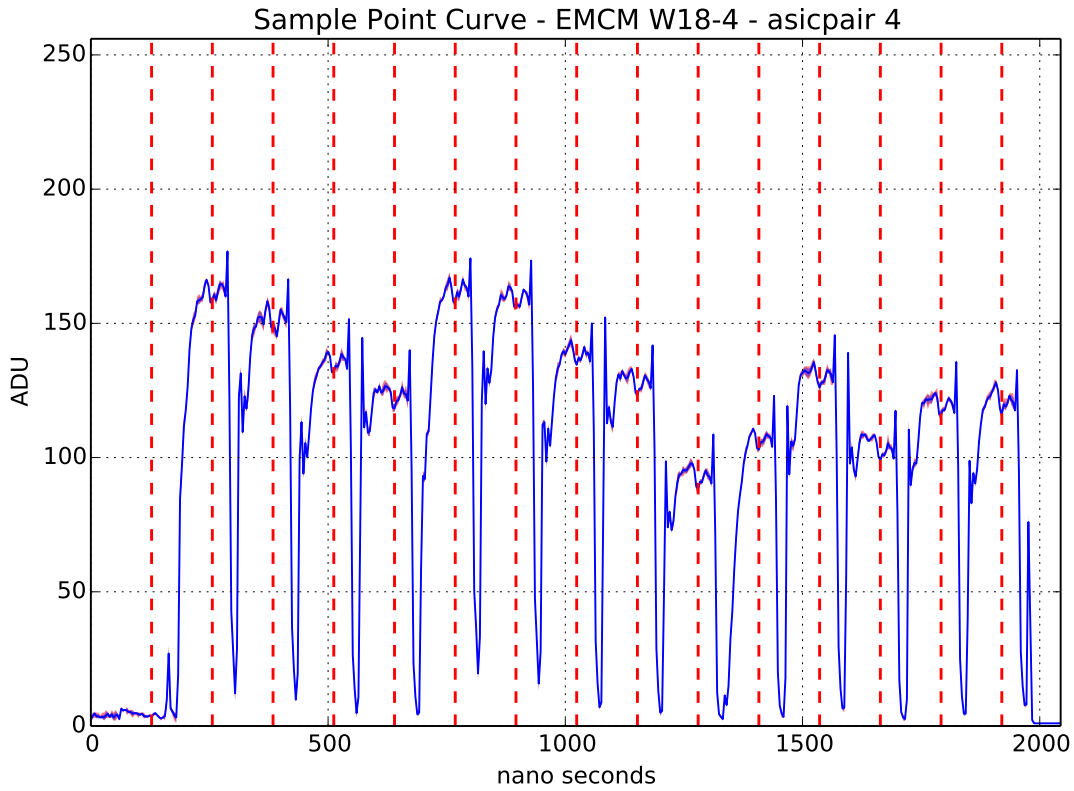


Figure 5.15: Drain current as function of time of the DEPFET matrix, which is assembled on top of the EMCM. The sampling points (red dashed lines) are located in 128 ns steps.

5.9 Summary of EMCM tests

The inter-ASIC communication between the DCD and the DHP was studied in both directions (DCD → DHP and DHP → DCD): The digital test pattern within the DCD was enabled and received by the DHP. Running at the nominal speed, the transmission can be faulty due to cross-talk between the transfer lines, the parasitic capacitance on the receiver side and insufficient output drivers on the sender side. The induced cross-talk of the 2-bit offset compensation may further harm a proper transmission.
In addition, the bug of the CML driver in the DHP results in unstable links for the full readout speed of GCK= 76.33 MHz. Due to the bit errors in the data transmission from the DCD to the DHP and the unstable high-speed links from the DHP to the DHE, most of the measurements have been performed with GCK=62.5 MHz.
A Switcher sequence has been generated, uploaded in the memory of the DHP and some of the 192 Switcher output drivers are measured. The matrix attached to the EMCM is biased. Laser tests proved the light sensitivity of the DEPFET matrix. The first optimization step is to record the Drain current as function of time to find the optimal timing for measuring the Drain current of the DEPFET pixels.

Based on the measurements performed on the EMCM, the following changes are applied to the final layout design:

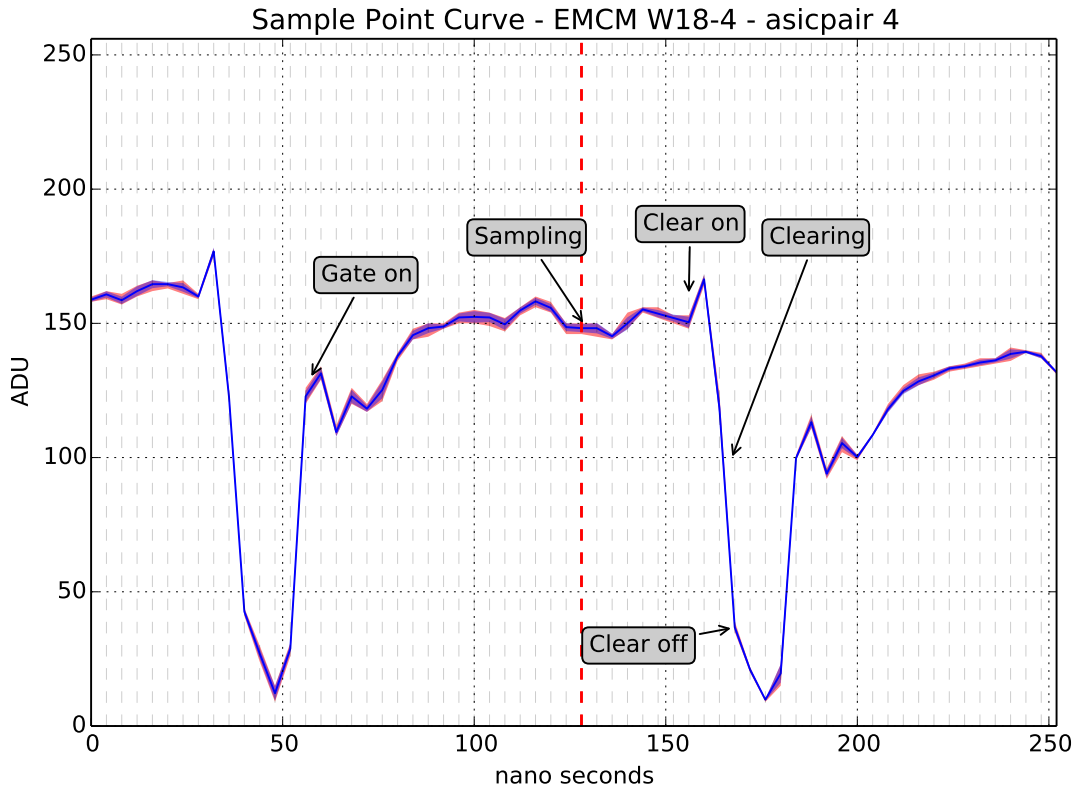


Figure 5.16: Sampling point curve of the DEPFET matrix, which is assembled on top of the EMCM. The sampling point (red dashed line) is located at 128 ns. The gray lines are spaced by 4 ns.

- The clock between DCD and DHP has been changed from a single-ended CMOS signal to LVDS.
- The routing of the high-speed signal lines from the DHP to the DHE has been changed on the EMCM. After discussions and detailed simulations have been performed [197], the signal traces have been routed in copper instead of the first aluminum layer. In addition, the trace width has been widened from 14 µm to 30 µm.
- The spacing of decoupling capacitors and termination resistors on the module has been increased to 200 µm to prevent shorts during soldering of the passives.
- As it has been observed during operation, the DHP-core current was roughly 680 mA[6]. Initially a single wire-bond was designed that is capable of constantly conducting a few hundreds of milliamperes without melting. Currents above the foreseen limit could destroy the connection. Therefore, a few wire-bond pads have been enlarged to allow the placement of multiple wire-bonds.

[6]The increased current was a result of the increased core voltage. The higher voltage was required to establish the high-speed links between DHP and DHE due to a bug in the DHP.

- The strengths of the output drivers of the DCD has been increased from 1.2 mA to 1.84 mA [153, 195]; an additional boost can be enabled in the latest version DCDB4.2.
- The capacitances of the input drivers on the DHP side have been decreased.
- The spacing of the transmission lines for the inter-ASIC communication (i.e., DCD-DHP) has been widened from 4 µm to 21 µm.

Chapter 6

PXD9 Pilot Run

6.1 Introduction

The so-called PXD9 pilot run modules are the first fully functional prototypes of the Belle II PXD, including all 14 ASICs and 192,000 DEPFET pixels. A photograph of the fully assembled IB module without Kapton cable is shown in Fig. 6.1.

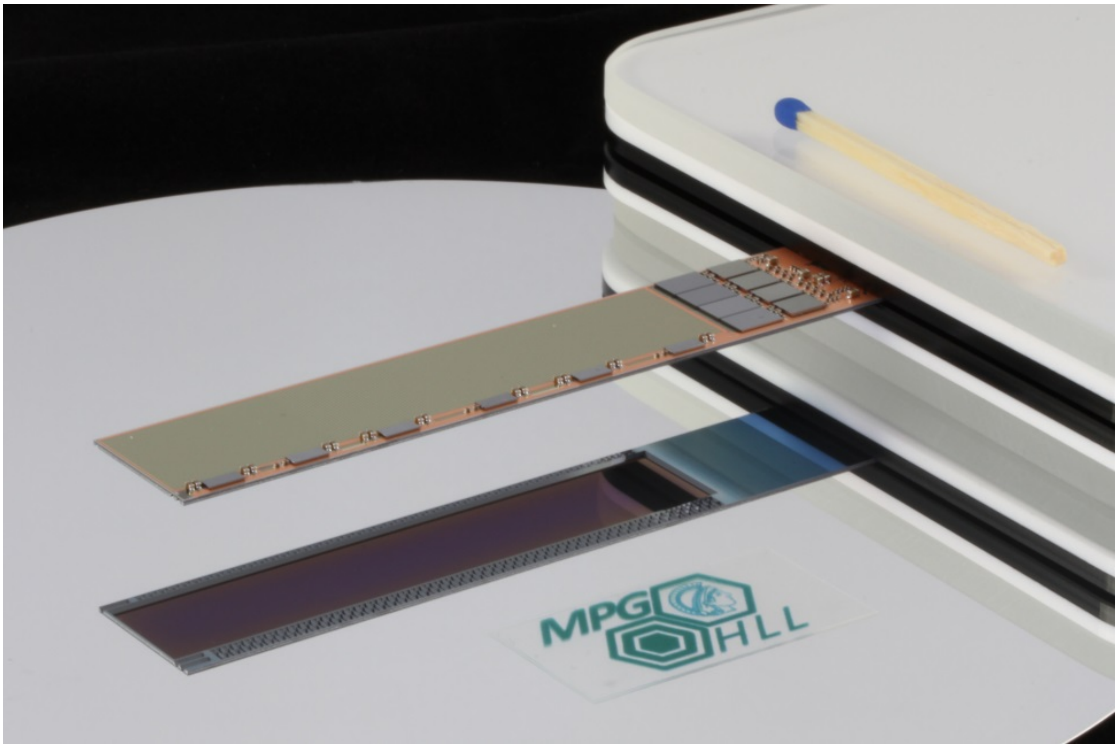


Figure 6.1: Pilot run module (IB) after the assembly of the ASICs and passive components. The thinned area (75 µm) is visible in the mirror image [171].

In this chapter, the pilot run module W30-OB1 (see Sect. 4.9.1 for the naming convention) is characterized in detail. Additionally, the Switcher responses on the module W31-OF1 are studied, which led to a change of the metal system layout (from the old layout *PXD-6* to the new layout *PXD9-7*). An overview of the assembled ASIC versions for the modules, which are presented in this chapter and in chapter 7, is given in Tab. 6.1.

Table 6.1: Overview of the characterized modules in this chapter and chapter 7.

Module	Metal system	DHP	DCD	Switcher	Purpose
W30-IB	PXD9-6	DHPT1.1	DCDB4	SwitcherBv2.0	Beam test
W30-OB1	PXD9-6	DHPT1.0	DCDB4	SwitcherBv2.0	Lab
W31-OF1	PXD9-7	DHPT1.1	DCDB4.2	SwitcherBv2.0	Lab
W35-OB1	PXD9-6	DHPT1.0	DCDB4	SwitcherBv2.0	Beam test

The module specifications are almost the same as for the EMCM, which resembles the outer backward module layout. The differences in the layout and the properties of the module, which were not mentioned in chapter 5, are briefly explained in the following.
In contrast to the EMCM setup, a single patch panel (PP) connects the Kapton cable, the power cable and the data cables. A sketch of the setup is shown in Fig. 6.2. The long Kapton cable ($\sim$ 0.5 m) is bent (in the same way as in the Belle II experiment) and connected to a PP.

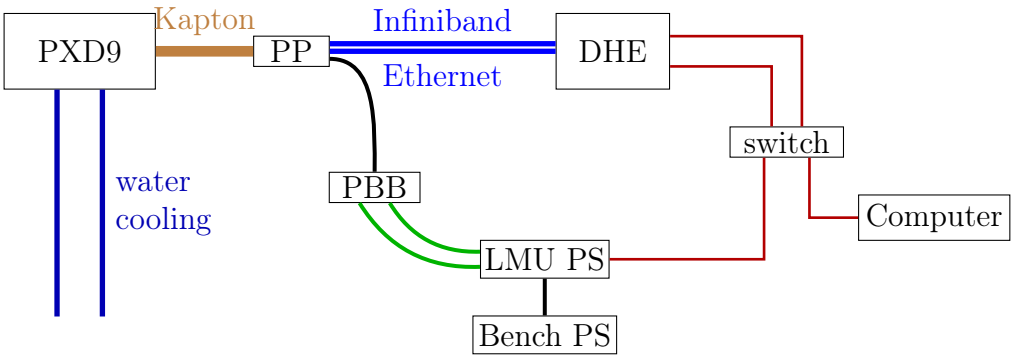


Figure 6.2: Sketch of the pilot run module in the lab setup. The end of the Kapton cable is connected to a single patch panel (PP). One Infiniband and one ethernet (CAT7) cable are connected to the DHE. The PP is also connected to the PBB where the conversion between Glenair connector and Mixed-D-Sub connector is performed. Two bulky green cables are connected to the PS. The PS and DHE control and data-acquisition is done by a computer.

A photograph of the lab setup is shown in Fig. 6.3. The fully equipped module is mounted on an aluminum jig. The mounting jig is assembled on a cooling block, where tap water ($\sim$ 16° C) serves as cooling medium.
The irradiation of the modules close to the interaction point (region with smaller pixel sizes) is stronger than for the rest of the sensitive area. The irradiation leads to shifts of the operating voltages due to the radiation damage (see [191] for more details). In order to ensure a proper functionality of the detector (and decrease the pedestal spread along the beam axis), there are three domains[1] for which different ClearGate and GateOn voltages can be applied.

[1]First domain: Switcher 1 and 2, second domain: Switcher 3 and 4, third domain: Switcher 5 and 6

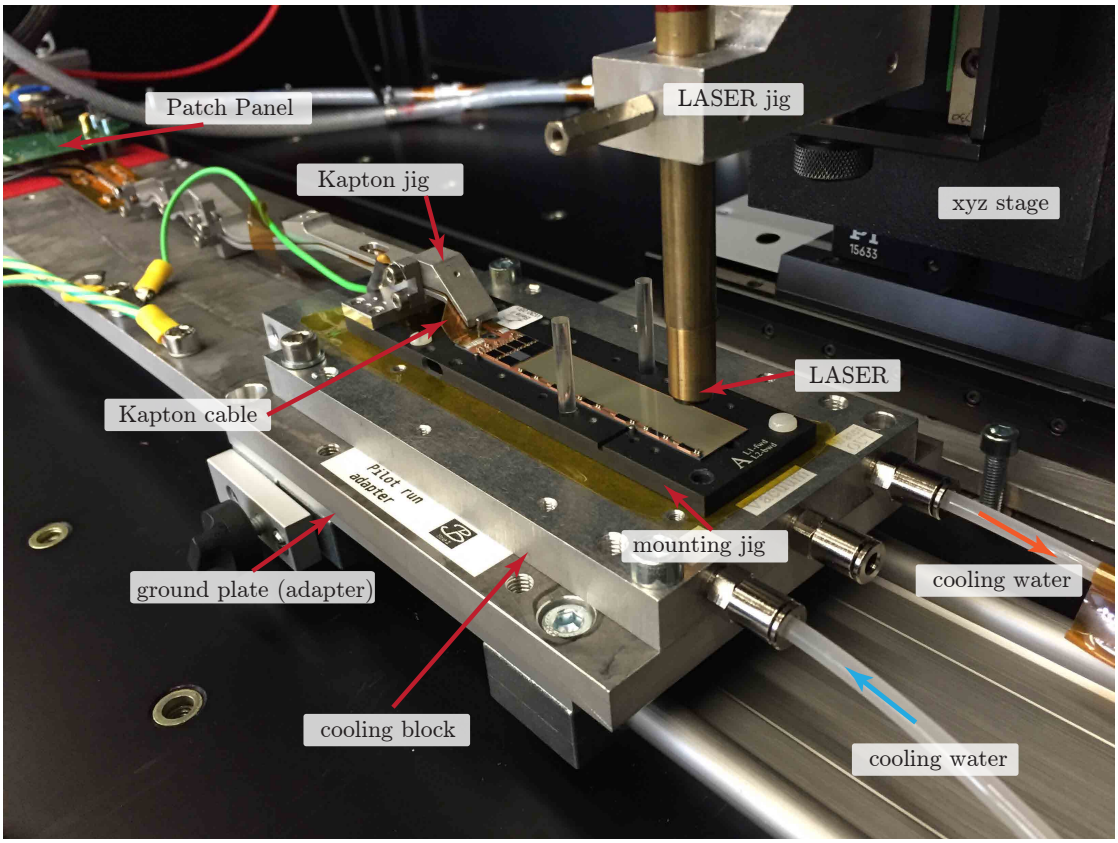


Figure 6.3: Setup of the module. It is placed on a mounting jig, which is electrically insulated against the cooling block. The Kapton cable is bent and guided by an aluminum jig to the patch panel. A laser shoots from the top side.

Additional Information

Some additional information is presented in the following. It is not important with respect to the measurements that are presented in this chapter, but it is beneficial to understand the entire system.

Termination resistors In contrast to the EMCM, the pilot run modules (and also the final modules) do not have any SMD termination resistors for the control signals of the Switcher (`SerIn`, `Strobe Clear`, `Strobe Gate` and `Clock`). Termination resistors of 100 Ω are required at the end of differential signal routing to avoid reflections of the signals, which could cause distortions that result in unexpected behavior of the ASIC. The Switcher can be controlled to enable (or disable) the internal termination resistors. Each Switcher requires a termination resistor for the `SerIn` signal since this is connected in series from one Switcher to the other. In contrast, the `Clock`, `Strobe Clear` and `Strobe Gate` are routed in parallel (see Fig. 4.20). A termination resistor is required only at the very last Switcher of the control data chain, i.e., at the Switcher that has the largest distance to the DCDs. The SwitchersB18v2.0 [147] are assembled on the module W30-OB1, which is characterized in this chapter. For this Switcher version, it is only possible

to simultaneously enable or disable the termination resistors for all nets (`SerIn`, `Strobe Clear`, `Strobe Gate` and `Clock`)[2]. After dedicated measurements, it was shown that the best configuration is to enable the termination resistors in the very last Switcher of the chain (in the v-direction, see Fig. 4.47) and to disable the termination resistors in all the other Switchers for the OB modules.

Major differences to EMCM The major difference compared to the EMCM is the large DEPFET matrix and the long Kapton cable that is attached. This has a direct influence on the power consumption, noise, voltage drops and parasitic capacitances etc., which is discussed in detail in this chapter.

6.2 Powering

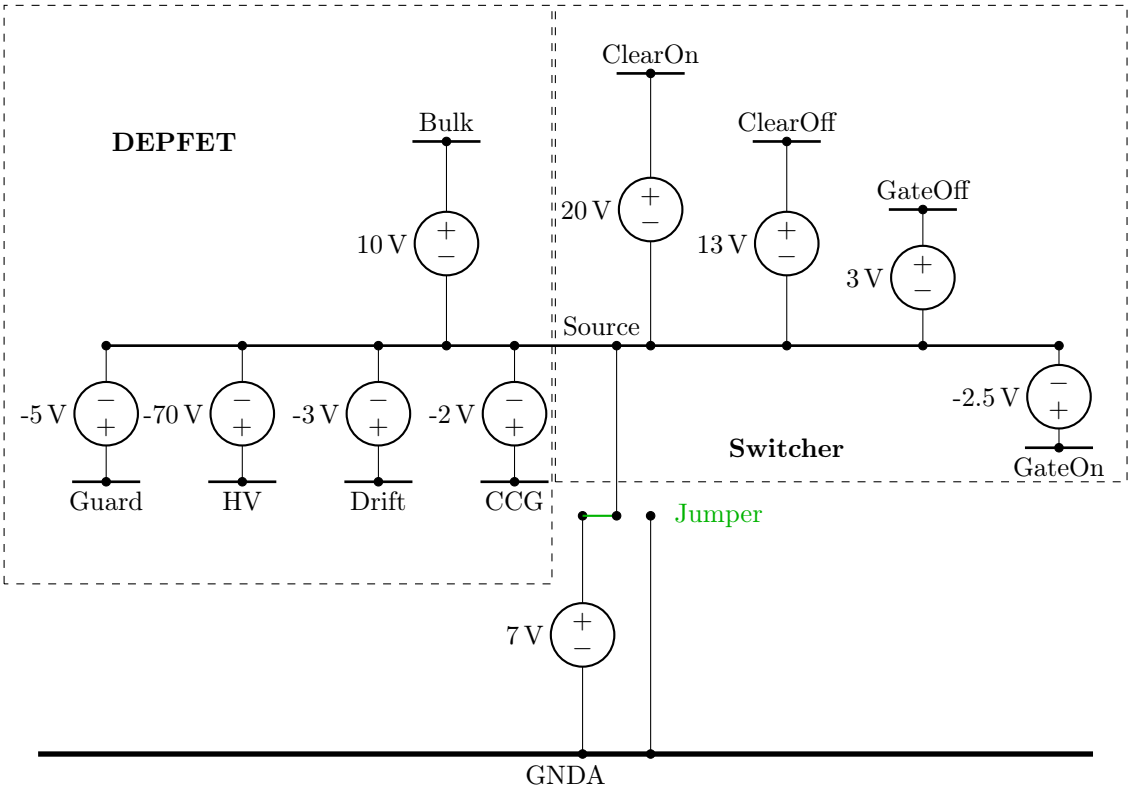


Figure 6.4: Bias scheme of the DEPFET matrix of the pilot run. A solder jumper (green) connects either the source or the analog ground as reference potential of the DEPFET voltages.

A single module is biased with 19 voltages, nine for the ASICs and ten for the DEPFET matrix. The voltages are all provided by a custom-made power supply [194]. The voltage and current limits can be set individually for each bias

[2]This behavior changed in SwitcherB18v2.1. The termination resistors for `SerIn` and the other three can be set individually.

Table 6.2: Power up sequence of the pilot run module.

Step	Net	voltage	current	reason
		Bias ASICs (step 1–11)		
1)	Switcher DVDD	1.8 V	30 mA	
2)	DHP-Core	1.2 V	730 mA	reset JTAG registers
3)	DHP DVDD	1.8 V	550 mA	
4)	DCD DVDD	1.8 V	940 mA	
5)	DCD AVDD	1.9 V	340 mA	restrict current consumption
6)	DCD RefIn	0.9 V	180 mA	restrict current consumption
7)	DCD AmpLow	0.4 V	340 mA	restrict current consumption
8)		Configure DCDs		
9)	DCD RefIn	0.9 V	1000 mA	ensure proper operation
10)	DCD AVDD	1.9 V	3000 mA	ensure proper operation
11)	DCD AmpLow	0.4 V	1300 mA	ensure proper operation
12)	Enable analog DCD part & upload Switcher sequence and bias DEPFET matrix			
13)	Bulk	10 V	10 mA	
14)	ClearOn	12 V	30 mA	Switcher limitation (20 V)
15)	ClearOff	5 V	30 mA	
16)	ClearOn	20 V	30 mA	
17)	GateOff	3 V	30 mA	keep DEPFETs off
18)	GateOn	3 V	30 mA	
19)	Source	6 V	150 mA	
20)	ClearGate	-1 V	10 mA	
21)	HighVoltage	-70 V	10 mA	
22)	Drift	-5 V	10 mA	
23)	Guard	-5 V	10 mA	
24)	GateOn	-2.5 V	30 mA	

channel. The biasing for the ASICs was already described in detail in Sect. 4.8.9. The power up sequence of the DEPFET matrix is discussed here.

The biasing schemes for the ASICs and the DEPFET are shown in Fig. 4.42 and in Fig. 6.4. A defined power up sequence must be kept to ensure proper operation and prevent damage. The steps are listed in Tab. 6.2 (1–7 correspond to current stage 1 while 8–11 correspond to stage 2 in Sect. 4.8.9.).

First, the ASICs are biased, starting with the Switchers. Next, the DHP is biased, followed by the DCD. Having configured all 14 ASICs, the analog components of the DCD are enabled. Finally, the DEPFET matrix is powered (see Tab. 6.2 for the sequence). The order of the power down sequence is inverted (step 24 to step 1; see Tab. 6.2), i.e., in the first step the GateOn voltage is raised and in the last step the Switcher DVDD voltage is switched off.

In the case that the current consumption of certain nets (such as DCD supply voltages or ClearOn) suddenly increases, decoupling capacitors are implemented

to stabilize the voltages. These are mounted on the Kapton cable and on the silicon module close to the ASIC.

6.3 Data transfer issues

In this section, the inter-ASIC communication and the transfer from the module to the DHE (for lab measurements) are described. These are implemented in a way similar to the implementations on the EMCM but the final version of the long Kapton cable ($\sim 0.5\,\mathrm{m}$) and a combined patch panel (for data and power) are used.

6.3.1 High-speed signals between DHP and DHE

The data are transferred from the DHPs (transmitter) to the DHE (receiver) by four 1.6 Gbps high-speed data lines, using Aurora 8b/10b encoding, as already described in Sect. 4.8.3. The signal integrity decreases due to various electrical connections between the transmitter and the receiver. The different components for the data transfer, which are in between, are listed below. The setup is described for the configuration in the lab. The colored stars correspond to the components of the sketch in Fig. 6.5.

1. Bump Bonds: Connection between ASIC and the silicon module.
2. ★ Metal traces on the silicon module: Contact between the bump bonds and the wire-bond pads. The traces are not impedance controlled, which could lead to signal reflections and thus distort the signal.
3. ★ Bond wires (Ø 25 µm): Interconnection between silicon module and Kapton cable.
4. ★ Kapton cable: Wiring between module and patch panel.
5. ★ Connector between Kapton cable and patch panel.
6. ★ Patch Panel: A PCB, which links the connector from the Kapton cable to the Infiniband connector.
7. ★ Infiniband connector: Attached on the PCB. For the real Belle II PXD, the Infiniband cable is soldered on a patch panel together with the wires for the power supply.
8. ★ Infiniband cable to the DHE. In the Belle II PXD, there will be an additional dock box with optical fibres connected to the DHE and a camera link cable as described in Sect. 4.13.

The settings for the signal amplitude, pre-emphasis and the width of the pre-emphasis are swept to find the optimal link parameters (as already described in Sect. 5.6.2). The link quality is recorded by using the internal data eye monitor of the FPGA (within the DHE), which measures the height of the data eye. The scan was performed for a global clock of 62.5 MHz, corresponding to a DCD clock of 250 MHz. The Infiniband cable between the PP and the DHE had a length of 3 m.

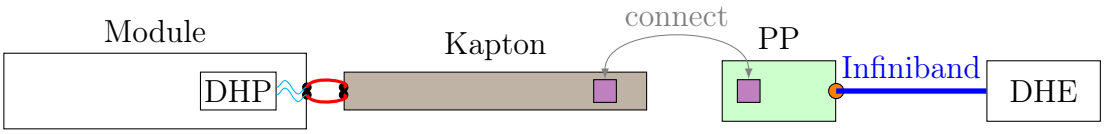


Figure 6.5: Sketch of the data transmission from the DHP to the DHE in the lab setup.

The results of the scan of all four DHPs are shown for the maximal width of the applied pre-emphasis (in the time domain) in Fig. 6.6. The white area represent settings for which no link could be established between the ASIC and the DHE. The height of the data eye is represented in 32 steps. The optimal parameters are extracted and applied to the four DHPs to ensure stable links and proper data transmission from the DHPs on the module to the DHE. The following settings should be chosen: `bias`> 15, `biasd`> 30 and `dly`= 3. An example for optimal parameters (`bias`= 37, `biasd`> 83 and `dly`= 3) are shown in Fig. 6.6 by the white stars.

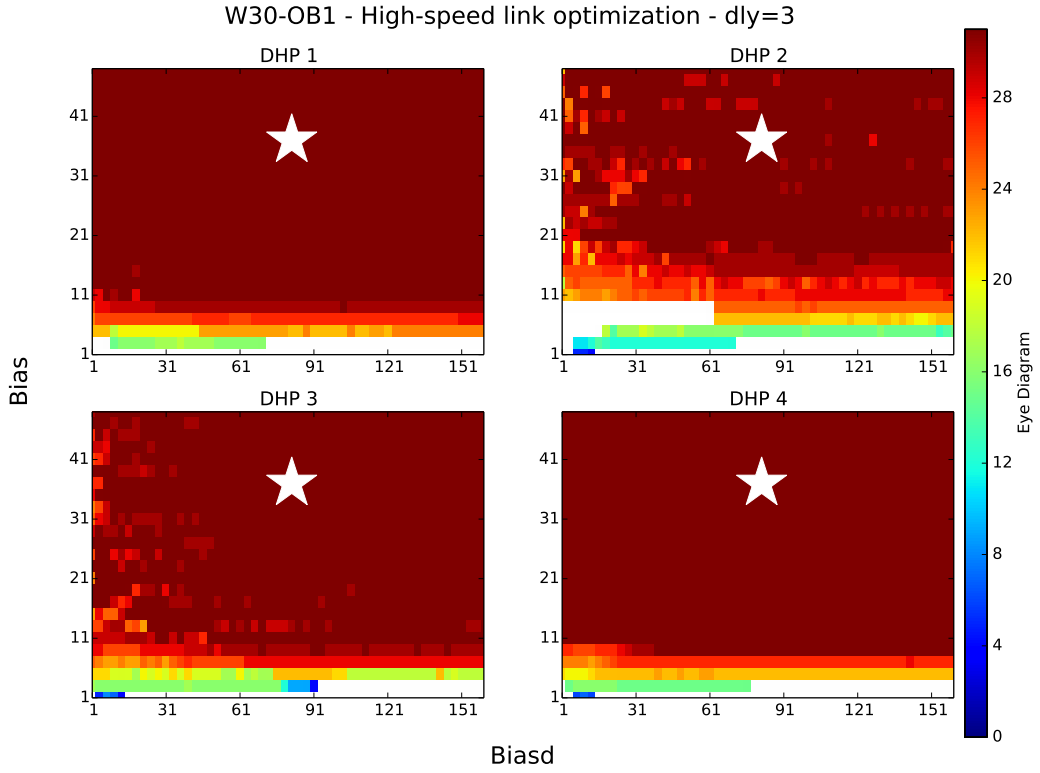


Figure 6.6: Sweep of the parameters to optimize the high-speed link. The plots show the quality of the signal integrity (data eye) for all four DHPs on the module. The maximum width for pre-emphasis is set. The white stars are proposals for settings assuring optimal link stability.

6.3.2 Inter-ASIC Communication

The transmission errors are studied and eliminated to ensure proper data transmission from the DCD to the DHP. For example, the errors are shown for ASIC-pair 4, which behaves quite similarly to the other three ASIC-pairs. Figure 6.7 shows the number of bit errors in the received data for DCD–DHP 4 running at the global reference clock rate of 62.5 MHz.

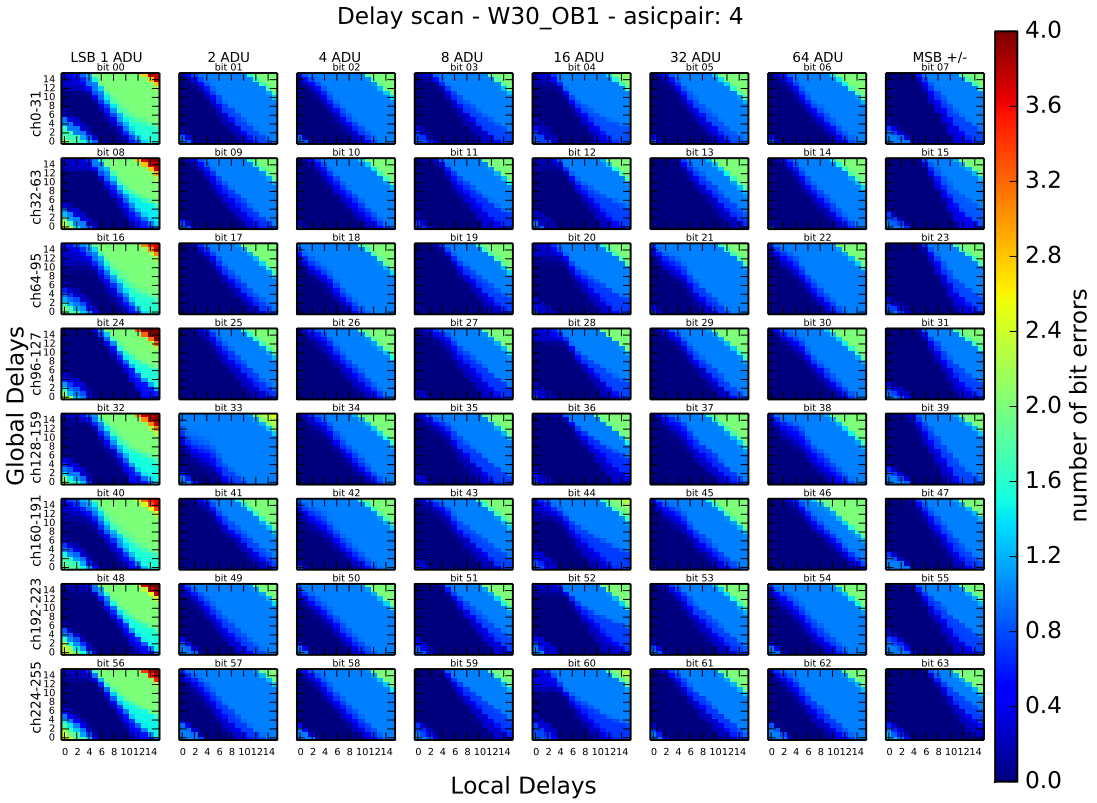


Figure 6.7: Transmission errors on bit level between DCD–DHP 4 using a reference clock rate of 62.5 MHz. The dark blue regions indicate no transmission errors.

Figure 6.8 depicts the number of bit errors for the nominal clock of 76.33 MHz. The delay settings are chosen for correct data transmission from the DCD to the DHP. The range of delay settings for proper transmission is quite small for the nominal global clock of 76.33 MHz compared to the slower one of 62.5 MHz. For instance, the receiver of the transfer line 33 (see Sect. 4.8.5) does not acquire the signal correctly for any combination of local and global delay settings due to deficiencies in the ASICs, which is fixed in the later iteration (as explained in Sect. 5.9). To ensure proper communication and significant results, most of the measurements are performed with the $\sim$ 20 % slower GCK (62.5 MHz), unless otherwise mentioned.

As already described in the EMCM section, the gaps between the metal routings for the interconnection between the two ASICs are widened for future generations of the final PXD modules to reduce cross-talk, which could cause additional trans-

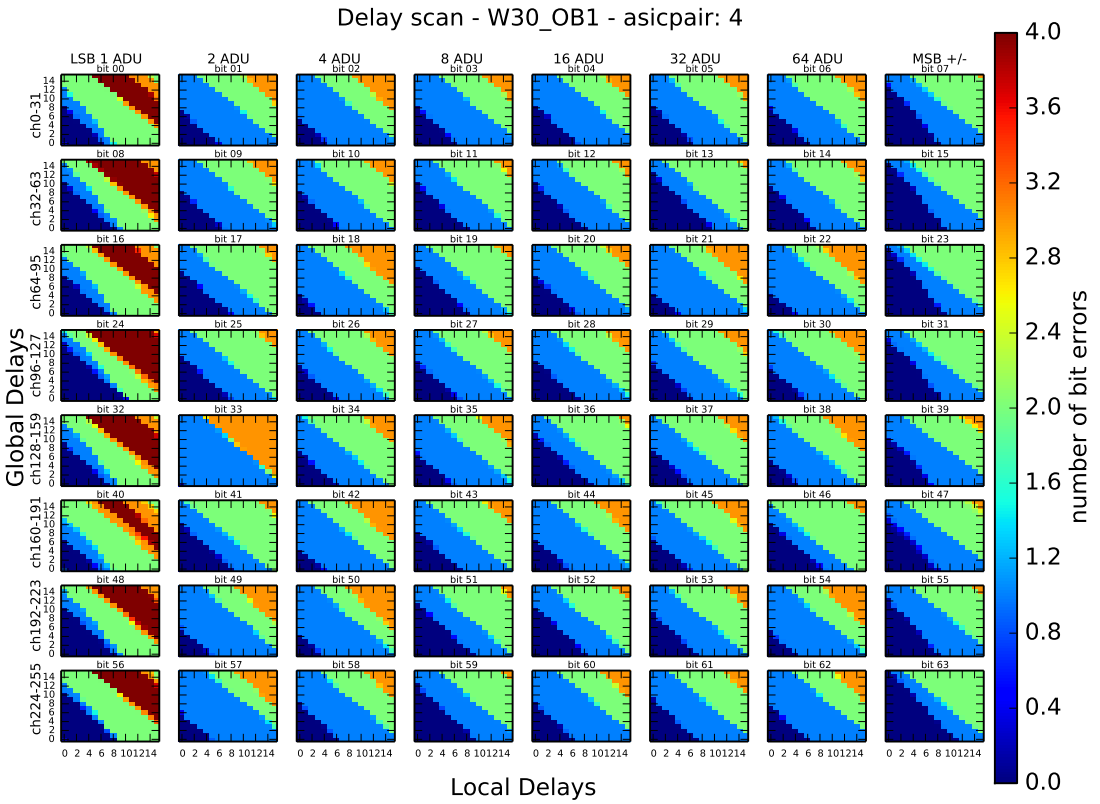


Figure 6.8: Transmission errors on bit level between DCD–DHP 4 using a reference clock rate of 76.33 MHz.

mission errors. However, the design change did not apply for the early module(s) characterized in this chapter.

6.3.3 Synchronization between DCD and DHP (DEPFET data)

As already described in Sect. 4.8.6, the Switcher sequence, the sampling of the DEPFET Drain currents by the DCD, its corresponding data output and the correct memory access of the DHP must be synchronized. In the following, two methods are presented in order to determine the correct starting point in the memory of the DHP into which the data is written as function of time.

1. The GateOn and ClearGate voltages can be adjusted for groups of two Switchers individually, i.e., there are three domains for all six Switchers. The lower the GateOn voltage (relative to the Source voltage), the higher the Drain current ($I_{\mathrm{ds}} \propto V_{\mathrm{gs}}^2 = V_{\mathrm{GateOn}}^2$) becomes. Decreasing the GateOn voltage for one of the three domains results in a local signal increase. This is clearly visible in the pedestals (see Fig. 6.9). In this way, it is known exactly in which rows increased pedestals values are expected ($\mathrm{rows}_{\mathrm{geo}}$ 512–768). The delays are adjusted properly in a way such that exactly those rows show increased pedestal values.

2. Another method is to disable the Clear pulse in a certain row (row_{gate}) (for instance in i, $i \in [1, 192] \cap \mathbb{N}$, i.e., $\text{row}_{\text{geo}} = [i, i+3]$, $i \in [1, 768] \cap \mathbb{N}$). Due to the missing Clear pulse, the *internal Gates* of the DEPFETs (connected to the Clear Switcher output driver) are filled with electrons, which results in increased Drain currents. Thus, the DEPFET rows that are not cleared show higher pedestal values. Using this information, the timing can be adjusted.

The first method is used to determine the correct starting point of the memory pointer as function of time since it is much simpler to change the Gate voltage than to implement a new Switcher firmware, verify it by simulations and finally, write it into the DHP memory. The second method is only mentioned as an alternative for the pilot run modules, which must be used for the EMCM since the Gate voltage of the small matrix is not split into multiple parts. The measurements revealed that different settings for the delay setting (called `frame_sync_proc_dly` in the DHP register [166]) are required for different global reference clocks. For a GCK=62.5 MHz, the settings 65 is recommended, for the nominal clock of 76.33 MHz, the value 57 should be used.

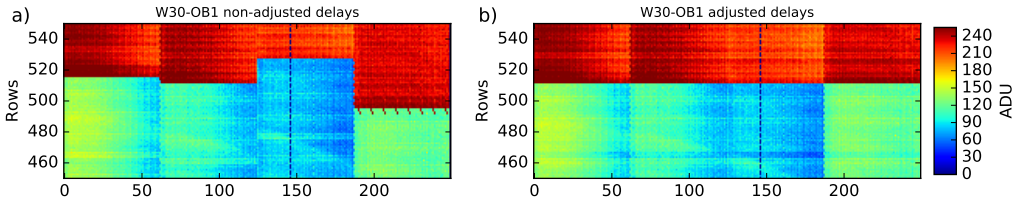


Figure 6.9: Pedestals values for different settings of the `frame_sync_proc_dly` setting.
a) Delay settings are not correct. The increased pedestal values are not at the correct positions. b) Correct adjustment of the delay settings. The increased pedestals are only visible in the expected region controlled by Switchers 5 and 6.

6.4 ADC transfer curves measurements

The optimization of the DCD in terms of ADC transfer curves was already described in Sect. 4.8.2. In this section, the characterizations of the different current sources (DHE and DCD internal current source) and the recording of ADC transfer curves with these current sources are presented. ADC transfer curves with different gains for different `VnSubin` settings are shown and discussed. The slopes and dynamic ranges of the ADCs within the DCDs are analyzed.

Calibration of DHE current source

The calibration of the DHE current source was performed with an external SMU. Figure 6.10 shows the current, the noise and the INL as functions of the DAC value. The linear range of the current source starts at $\sim$ 500 DACs. The noise and INL are quite low[3], below 4 pA. In addition, the DHE current source has a

[3] A MIP generates a signal in the DEPFET pixel corresponding to an increase of approximately 2.7 µA of the Drain current.

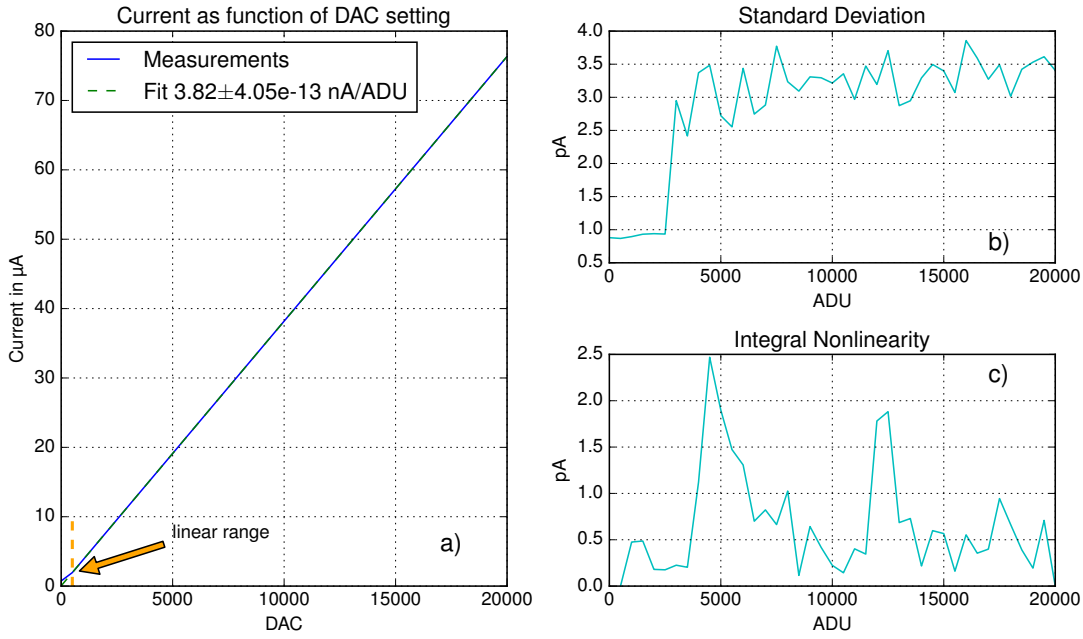


Figure 6.10: Calibration of the DHE current source with an SMU. a) The current as function of the DAC setting. The linear range starts at approximately 500 DAC, indicated by the orange arrow. b) The standard deviation as function of the DAC setting. c) The INL as function of the DAC setting.

very high granularity; 1 DAC corresponds to $\simeq$ 3.82 nA. For these reasons, it is well suited to analyze the ADCs of the DCDs in terms of INL, DNL and missing codes.

ACD transfer curves using the DHE current source

The ADC transfer curves are recorded with different DCD settings in order to determine the optimal parameters for obtaining linear ADC behavior and to avoid missing codes (see Sect. 4.8.2).
The transfer curves for all four DCDs (on module W30-OB1) with all four possible gains (1, 2, $\tilde{2}$, 4; see Sect. 4.8.2) are measured. They are shown[4] for DCD 1 and different gain settings in Fig. 6.11. The dashed lines represent linear fits. The dynamic range, i.e., the current interval that can be resolved by the DCD, varies depending on the gain setting. Due to the non-linear behavior at the lower and upper boundaries, the LSB is up to 10 % smaller than the theoretical value in eq. (4.8.2).
The curves can be shifted along the x-axis by changing the settings for the `VnSubin`, i.e., the amount of subtracted current (see Fig. 4.23) at the input node of the DCD. The measurements of the transfer curves are repeated for different `VnSubin` settings - the curves are shown in Fig. 6.12. The slopes and the dynamic ranges are calculated for each setting. More details are explained in app. C.3. In addition, the amount of current subtracted by one DAC of `VnSubin` can be calculated by

[4]The transfer curves for all four DCDs are shown in the app. C.3.

Table 6.3: Overview of the four DCDs of the pilot run module W30-OB1. The gains, the averaged subtraction of current by one `VnSubin` DAC and the dynamic range as function of the DCD gain settings (1, 2, $\tilde{2}$, 4) are summarized.

		gain in nA/ADU	`VnSubin` in µA/DAC	dyn.r. in µA
DCD 1	Gain 1	138.4 ± 0.8	2.65	30.6
	Gain 2	85.3 ± 0.4	2.69	18.7
	Gain $\tilde{2}$	91.7 ± 0.5	2.69	20.4
	Gain 4	57.2 ± 0.6	2.74	12.2
DCD 2	Gain 1	131.0 ± 2.8	2.52	29.0
	Gain 2	81.0 ± 1.6	2.57	18.4
	Gain $\tilde{2}$	88.1 ± 2.5	2.59	17.6
	Gain 4	55.8 ± 1.8	2.66	12.0
DCD 3	Gain 1	135.4 ± 0.9	2.89	31.1
	Gain 2	84.1 ± 0.6	2.83	18.9
	Gain $\tilde{2}$	89.9 ± 0.4	2.81	20.3
	Gain 4	56.1 ± 0.3	2.81	12.3
DCD4	Gain 1	139.9 ± 1.1	2.79	30.6
	Gain 2	86.3 ± 0.5	2.73	18.9
	Gain $\tilde{2}$	92.4 ± 1.1	2.73	19.4
	Gain 4	57.3 ± 0.6	2.74	12.5

comparing the current values for the same ADU value for different settings of `VnSubin`. As shown in Fig. 6.12, the amount of current between the different transfer curves (each recorded with a `VnSubin` setting difference of four) varies. Thus, due to the inhomogeneity of `VnSubin`, the calculated values for the amount of subtracted current per ADU can be only seen as rough estimates. An overview of the four DCD parameters is listed in Tab. 6.3.
Most of the measurements regarding the characterization of the pilot run W30-OB1 were performed for gain setting 1, corresponding to a gain of approximately 136 nA/ADU and a dynamic range of ~ 30.3 µA, which is equivalent to roughly 12 MIPs.

Calibration of DCD current source

The DCD internal current source (see Fig. 4.23), which could be used to record ADCs transfer curves, needs to be calibrated. The internal current source consists of three individual current sources (`sigmirror` $0, 1, 2$), which are connected in parallel. Since each of these three is controlled by a 7-bit register, corresponding to 128 settings, there are a total of 384 DAC settings. The values are set by the slow control system, which requires approximately 90 s to sweep all 384 values.
In order to measure the current of the DCD internal current source, the common monitor pin of the four DCDs is connected to an SMU (and the ground pin of

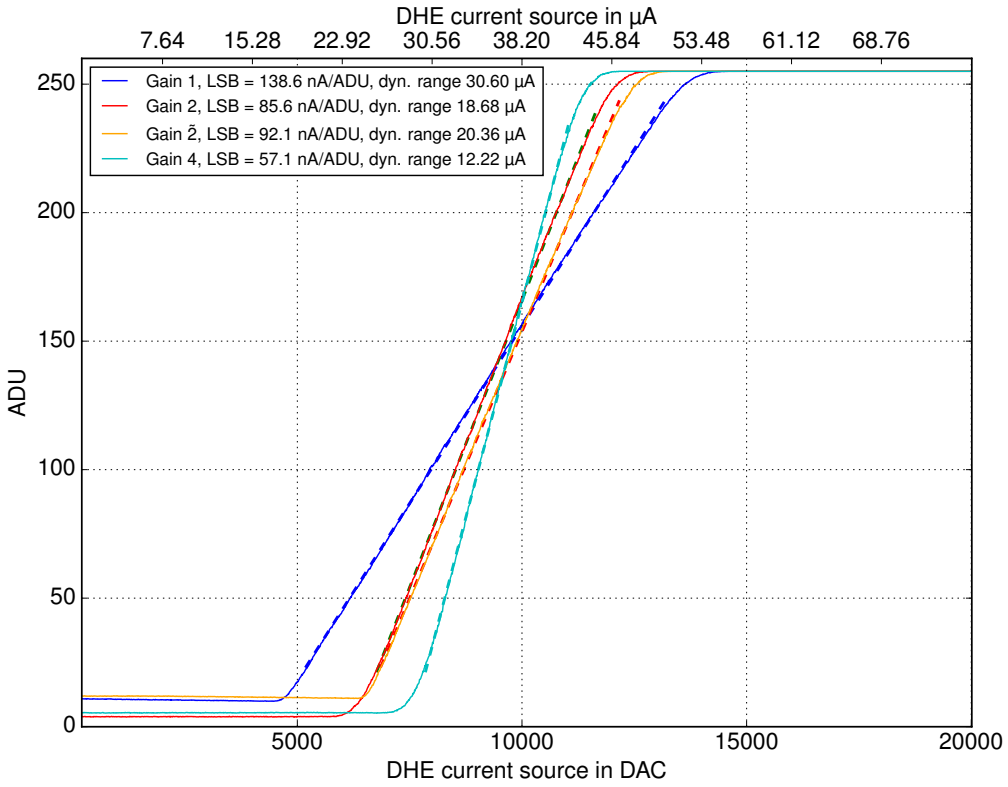


Figure 6.11: ADC transfer curves for four different gain settings of DCD 1 using the DHE current source. The dashed lines represent linear fits. At the lower and upper boundaries a non-linear behavior of the ADC is observed.

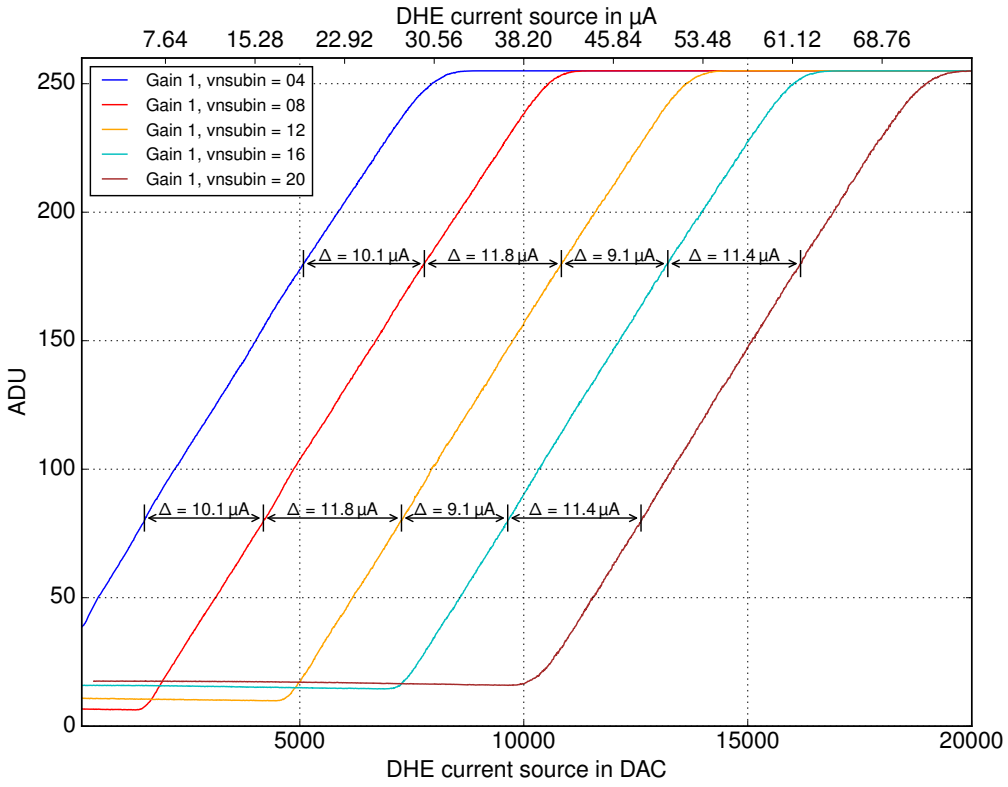


Figure 6.12: Transfer curves for different `VnSubin` settings using the DHE current source.

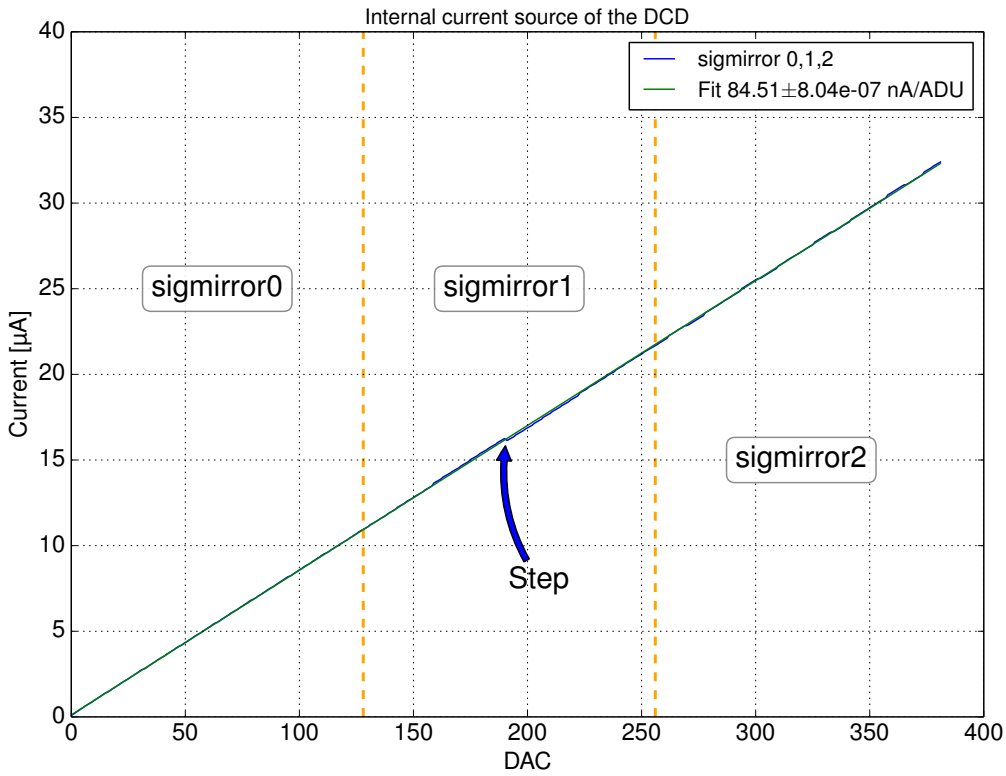


Figure 6.13: Calibration of the internal current source of the DCD.

the SMU to the analog ground)[5]. The patch panel serves as junction box. The measured current as function of the DAC setting is shown in Fig. 6.13. The step size is approximately 84.51 nA/ADU. For this particular DCD, it shows a non-linear behavior at DAC 190.

DCD Transfer curves with DCD current source

Four transfer curves with different DCD gains (1, 2, $\tilde{2}$, 4; see Sect. 4.8.2) are recorded in order to determine the optimal settings to obtain a linear ADC behavior and to avoid missing codes, using the internal current source `sigmirror`. The transfer curves are shown in Fig. 6.14. As it can clearly be seen, the entire dynamic range for gain 1 cannot be covered, since the total output current of the three current sources is less than the dynamic range. If they were stronger, i.e., providing more current, the step size would increase.
The internal current source, `sigmirror`, is too coarse to recognize differential and integral non-linearity. For this reason and because of the limited strength and the long acquisition time for sweeping all 384 DAC parameters to record an ADC curve, the internal current source is not suited for optimizing the ADCs.

DCD Transfer curves with DEPFET current source

The Drain current of the DEPFET depends on the GateOn voltage, see Sect. 4.5.1 ($I_{\mathrm{ds}} \propto V_{\mathrm{gs}}^2 = V_{\mathrm{GateOn}}^2$). The more negative the GateOn voltage, the larger the Drain

[5]Due to the parallel connection of the four monitor nets, only one DCD can be characterized.

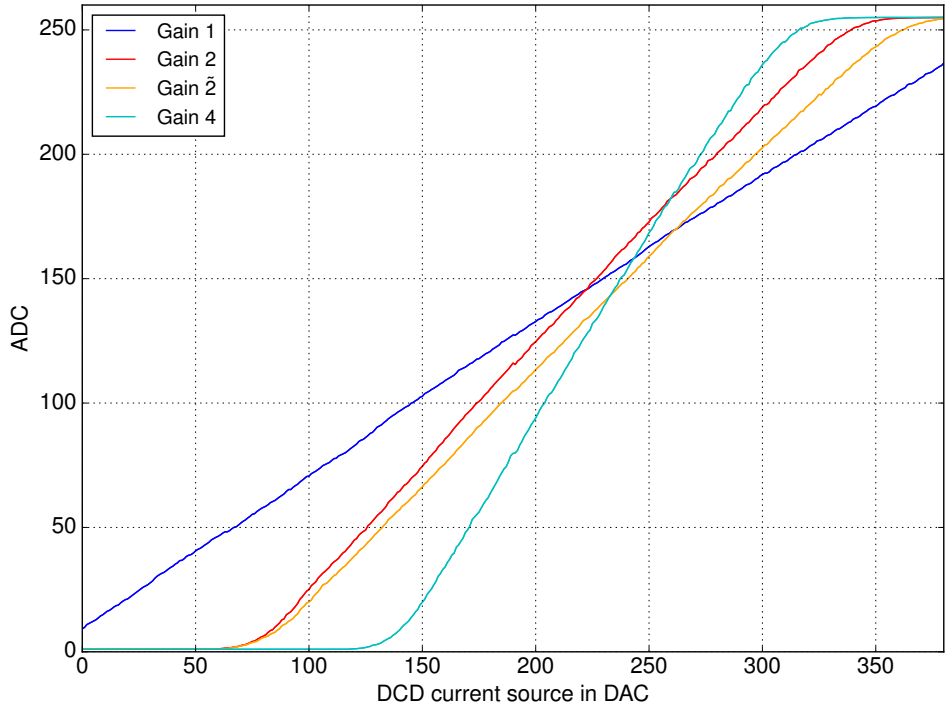


Figure 6.14: ADC Transfer curves for four different gain settings using the internal DCD current source.

current becomes. Therefore, it can be also used for recording ADC transfer curves. However, a possible non-linear behavior has to be taken into account. The GateOn voltage can be swept in steps of 1 mV. The DEPFETs provide a very accurate and fine current source to characterize the ADCs. If a GateOn voltage that is more negative than the threshold voltage ($V_{\mathrm{GateOn}} \ll V_{\mathrm{threshold}}$) is used, the curvature of the quadratic curve could be relatively minimized. The transfer curves of some randomly chosen recorded channels ($\mathrm{col}_{\mathrm{drain}} = 4$, 8, 40 and 40) are shown in Fig. 6.15. The advantage of using the DEPFET as a current source is the parallel characterization of the ADCs resulting in very short time for the entire optimization procedure.

Conclusion of current sources

The different procedures of the ADC characterization can be grouped into two categories:

1) **Monitor pin:** The optimization can be performed by injecting a known current through the monitor pin (shown in Fig. 4.23), which can come either from the dedicated internal current source of the DCD (`sigmirror`) or from an external one (DHE, SMU). However, the input current is limited by the DCD to roughly 40 µA (see Sect. 4.8.2). This is approximately one third of the DEPFET Drain current, i.e., the optimization procedure is performed for an input current, which is far below the nominal values from the sensor. The

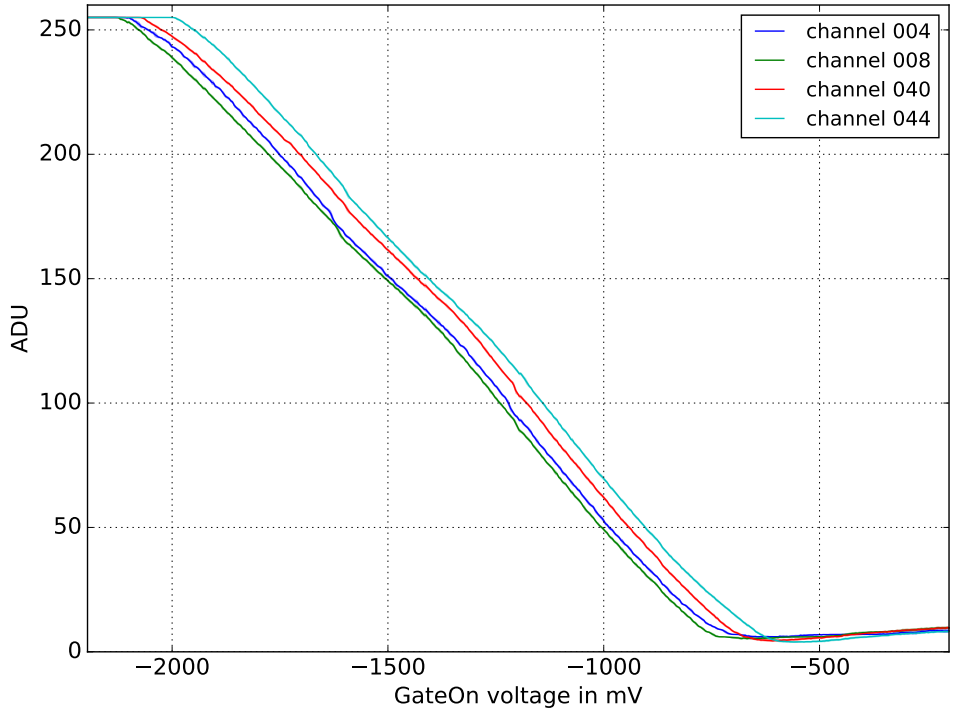


Figure 6.15: Transfer curves for gain=1 using the DEPFETs with variable GateOn voltage as current source.

internal current source of the DCD is too poor to resolve INL and DNL errors. In addition, the output strength is too low to cover the entire dynamic range for the lowest gain. The DHE current source is very fine and provides low noise. However, due to the long distance between DHE and the DCD ($\sim$ 4 m), the current picks up noise along the transmission path. The four monitor pins of all DCDs are connected together on a module. Hence, the ADCs can only be characterized sequentially. The entire procedure takes approximately 300 hours, dominated by the slow control system, for a detailed characterization and optimization.

2) **DEPFET:** The Drain current shows a quadratic behavior as function of the GateOn voltage. However, the performance and optimization procedure can be done in parallel for all ADCs (connected to the DEPFET matrix). This method requires approximately 30 minutes. Therefore, this method is chosen to serve as a current source to characterize the DCDs. The optimized settings and characterization algorithms are explained in [157].

6.5 Sampling Point Curve

The sampling point curve gives information about the Drain current as function of time (see Sect. 5.6). The purpose of this is to find the optimal time of the sampling point for the DEPFET pixel, i.e., at a plateau before the Clear pulse is applied to

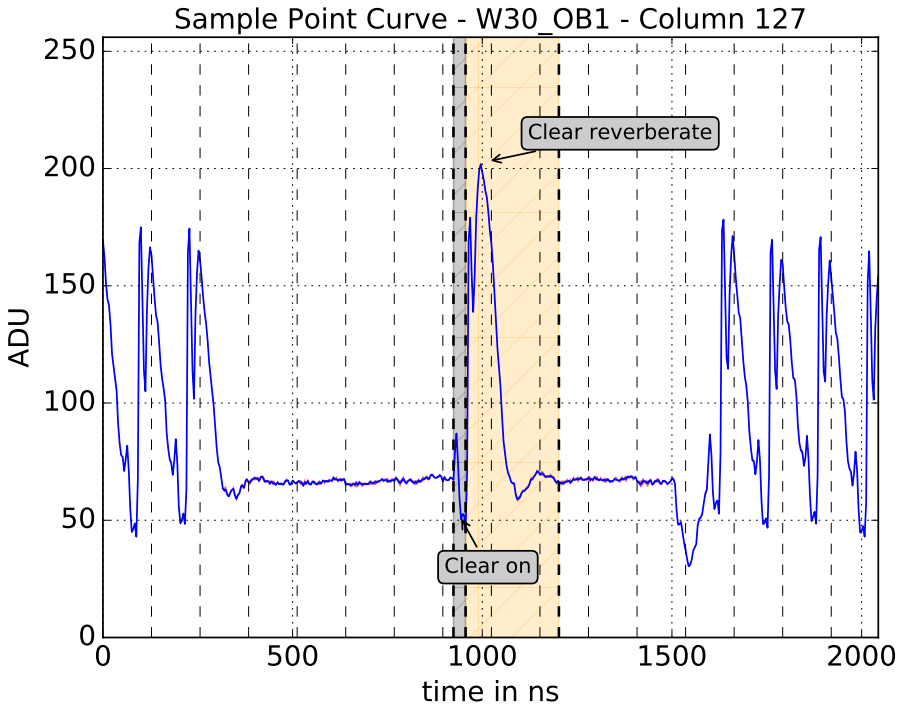
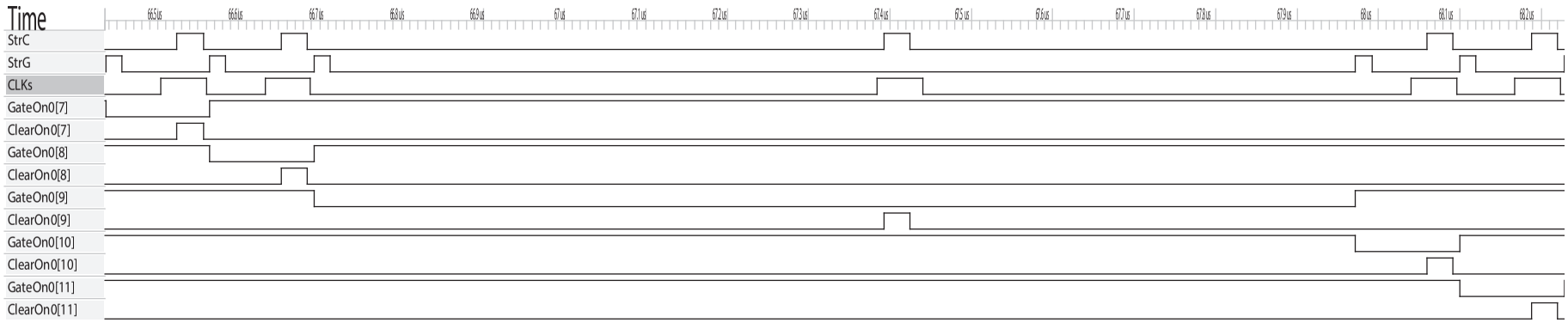


Figure 6.16: Sampling point curve of DCD 1, column 127 of the W30-OB1 module. The Clear pulse is applied for 32 ns (marked by the gray rectangle). Reverberate oscillations occur after switching back to the ClearOff voltage (indicated by the orange rectangle).

reset the pixels. The sampling the Drain current takes the same amount of time for all pixels, since the Clear pulse is applied every 128 ns (for GCK=62.5 MHz). The plots of the sampling point curve presented in this section show the current signal of a specific DCD input channel, i.e., of a single Drain column ($\text{col}_{\text{drain}}$), as a function of time. The Gate rows (row_{gate}) are switched on sequentially and the Drain currents of consecutive pixels are measured. The sampling point curves for different Switcher sequences with variable lengths of enabled $\text{rows}_{\text{gate}}$ (128 ns and 1280 ns) are presented in the following:
The Drain current is changed either by switching to the next row_{gate}, i.e., enabling the next $\text{row}_{\text{gate}} + 1$ or by applying the Clear pulse, since the high voltage (applied at the *Clear implant*) changes the transconductance of the MOSFET. To decouple the two effects, special Switcher sequences are used.
In the following paragraph, the effect of the Clear pulse are presented. Dedicated Switcher sequences have been developed and simulated and are presented in this section. In contrast to the counting scheme in this thesis (starting with 1), the Switcher output driver starts with 0 in the simulations. Gate $x[y]$, $x \in [0,5] \cap \mathbb{N}_0$, $y \in [0,31] \cap \mathbb{N}_0$ corresponds to Switcher x and to the Gate output driver y (row_{gate}).

Effect of the Clear pulse

The $\text{rows}_{\text{gate}}$ are switched on consecutively for 128 ns with the exception, e.g., of $\text{row}_{\text{gate}} = 9$. This row_{gate} is enabled for 1280 ns to study the impact of the



(a) The output drivers for five consecutive $\text{rows}_{\text{gate}}$ are shown. One Switcher row_{gate} is enabled ten times longer than the other $\text{rows}_{\text{gate}}$. The Clear pulse has the same width for all rows.

(b) Three consecutive rows $\text{rows}_{\text{gate}}$ are enabled longer (by a factor 10) compared to the other $\text{rows}_{\text{gate}}$.

Figure 6.17: Verilog simulation of the Switcher logic for $\text{rows}_{\text{gate}}$ that are enabled longer by a factor of ten.

Clear pulse on the Drain current. The Drain current of $\text{col}_{\text{drain}} = 127$ (DCD 1) is shown in Fig. 6.16. The Clear pulse is applied for 32 ns, as indicated by the gray rectangle. It is applied 92 ns after enabling the row_{gate}. The Drain current increases for 8 ns, and then it decreases for 24 ns. Switching back to the normal state, i.e., lowering the voltage at the Clear contact by 15 V, causes recurring oscillations for approximately 246 ns (indicated by the orange rectangle). The time for enabling a row_{gate} is only 128 ns (for GCK= 62.5 MHz) or even shorter ($\sim$ 105 ns), running at the nominal global clock frequency of 76.33 MHz. However, the row_{gate} is disabled (switching to GateOff) 4 ns later after releasing the Clear pulse. As a consequence, the oscillations should not affect the Drain current as much as is measured for this (long-enabled) row_{gate}.
Th simulation of the sequence is shown in Fig. 6.17a. (Without any restrictions, three consecutive rows can also be enabled for 1280 ns, as shown in Fig. 6.17b.)

Effect of switching Gate rows

Switching from one Gate row (row_{gate}) to the subsequent one has an additional impact on the Drain current. As can be seen in the Switcher simulations (Fig. 6.17a

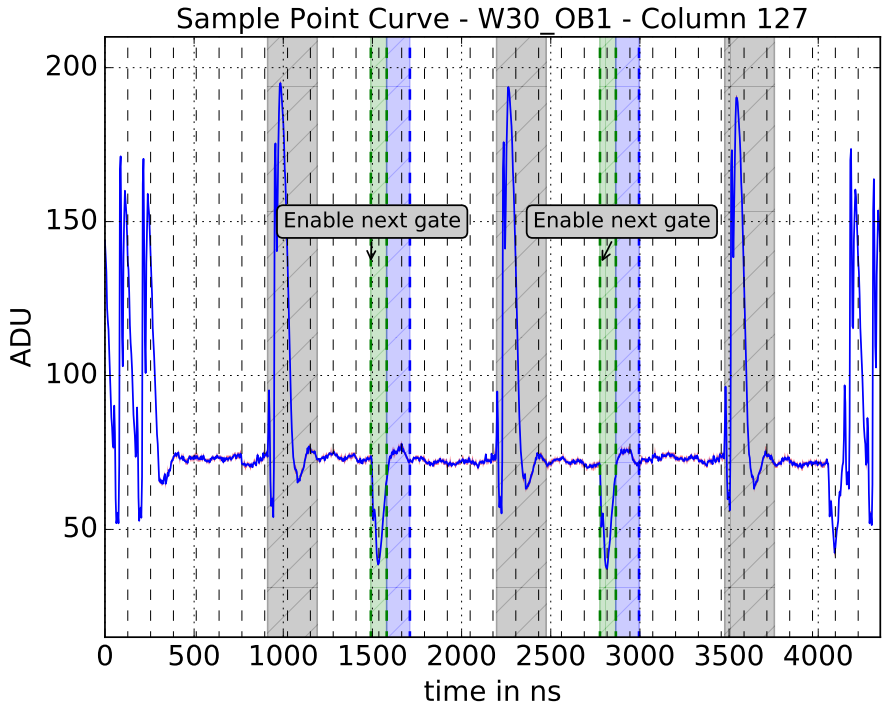


Figure 6.18: Sampling point curve. Three consecutive $\text{rows}_{\text{gate}}$ are enabled for 1280 ns. The impact of the row_{gate} switching is indicated by the green (current drop) and blue (transient oscillation) domains. The impact of the Clear pulse is marked by the gray rectangles.

and Fig. 6.17b), the current $\text{row}_{\text{gate}} = i$ is enabled at the same time when the previous $\text{row}_{\text{gate}} = i - 1$ is disabled. When $\text{row}_{\text{gate}} = i - 1$ is disabled, the Drain current decreases and the Drain current of the consecutive $\text{row}_{\text{gate}} = i$ increases simultaneously. Three consecutive $\text{rows}_{\text{gate}}$ $(10, 11, 12)$ are enabled for 1280 ns in order to study the impact of the row_{gate} switching on the Drain current (decoupled

from the impact of the Clear pulse). The pixels connected to $\text{row}_{\text{gate}} = i - 1$ are already switched off while those that are connected to the subsequent $\text{row}_{\text{gate}} = i$ do not have a conductive channel yet. As a consequence, the Drain current decreases during the process of changing the active row_{gate} (marked as the green domains in Fig. 6.18). In addition, a transient oscillation is clearly visible (marked as the blue domain, the impact of the Clear pulse is marked as the gray areas). These oscillations influence the Drain currents. As a consequence, the DEPFET signals of the next enabled row_{gate} are the sum of the amplified Source-Drain current and this oscillation. Although the oscillation dominates the Drain current, it is observed that signals of the DEPFETs can nevertheless be detected clearly.

Overlapping Gate rows

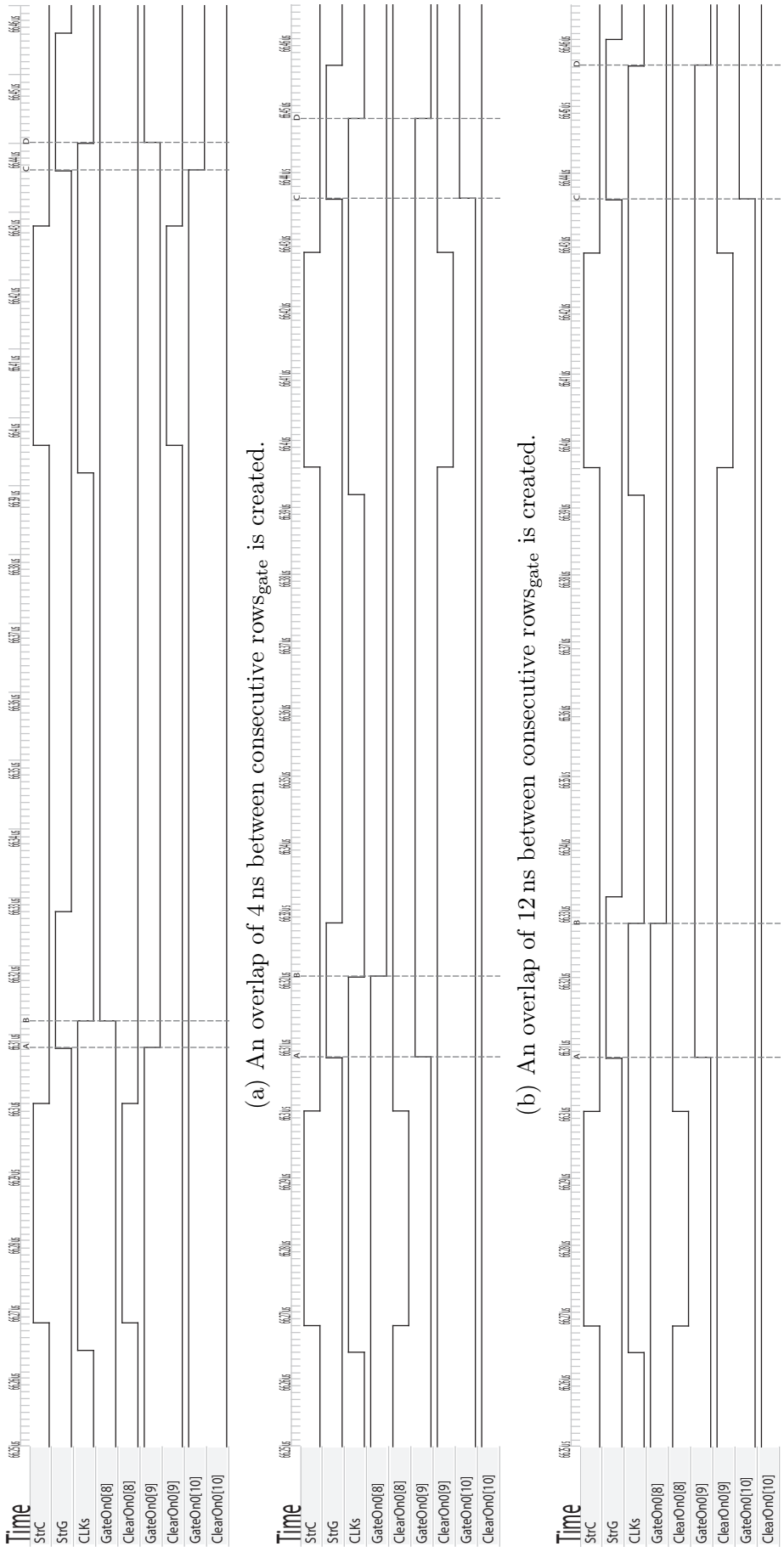
To overcome the problem of the sudden current drop while switching to the subsequent row_{gate}, the Switcher allows overlapping the row_{gate} for a certain time $t_{\text{overlap}} \in [0,\ 1 \cdot t_{\text{tick}},\ 2 \cdot t_{\text{tick}},\ \ldots]$, where t_{tick} denotes the time for one tick of the Switcher sequence, i.e., 4 ns for GCK=62.5 MHz. In that way, the two rows $\text{row}_{\text{gate}} i - 1$ and $\text{row}_{\text{gate}} i$ are enabled simultaneously for a few nanoseconds. The simulations of the Switcher logic for different overlaps (4 ns, 12 ns and 20 ns) are shown in Figs. 6.19a to 6.19c. The time for enabling three consecutive $\text{rows}_{\text{gate}}$ is extended to 1280 ns to study the switching behavior, decoupled from the impact of the Clear pulse on the Drain current.

Measurements for different overlaps of the $\text{rows}_{\text{gate}}$ are plotted in Fig. 6.20. Figure 6.21 shows a zoomed-in version of the transition time between consecutive $\text{rows}_{\text{gate}}$ for the extended Gate time of 1280 ns. It is clearly visible how the Drain current is modulated as function of the row_{gate} overlap time, t_{overlap}. For an overlap of 4 ns, the Drain current is modulated less compared to the other cases. The red curve corresponds to a non-existing overlap ($t_{\text{overlap}} = 0$ ns). For the nominal readout using 32 ticks, i.e., 128 ns for GCK=62.5 MHz, the sampling point curve is shown in Fig. 6.22. The effects of the oscillations caused by row switching and applying the Clear pulse mix. However, a narrow plateau indicated by the dashed line can be seen. This point is chosen as the sampling point.

Conclusion

To find the optimal sampling point, the impact of the Clear pulse and row_{gate} switching must be both taken into account. The sampling point curves of three different setups are compared:

- **Hybrid 5:** The hybrid 5 setup consists of one set of the entire ASIC chain, i.e., one Switcher, one DCD and one DHP. A small matrix (consisting of 16 $\text{rows}_{\text{gate}}$ and 128 $\text{cols}_{\text{drain}}$) is connected via wire-bonds to the control and readout electronics. The electrical connections are as short as possible, in the order of a few millimeters.
- **EMCM:** The EMCM can also be equipped with the same type of small matrix, as already described in Sect. 5.1. The Gate routings are longer ($\sim$



(a) An overlap of 4 ns between consecutive $\text{rows}_{\text{gate}}$ is created.

(b) An overlap of 12 ns between consecutive $\text{rows}_{\text{gate}}$ is created.

(c) An overlap of 20 ns between consecutive $\text{rows}_{\text{gate}}$ is created.

Figure 6.19: Verilog simulations of the Switcher logic for different lengths of overlapping gates.

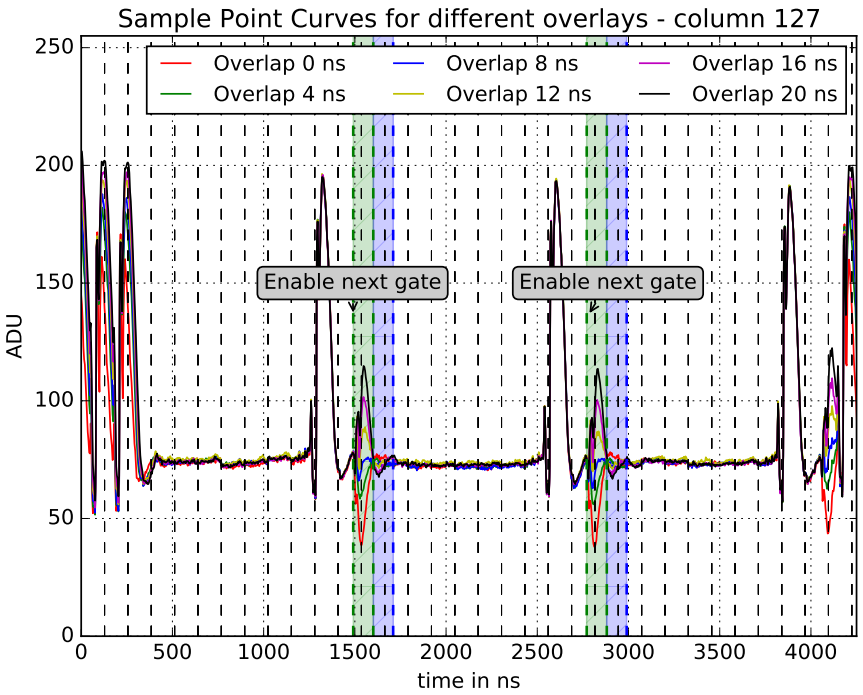


Figure 6.20: Sampling point curves with different overlap lengths for the $\text{rows}_{\text{gate}}$. Three consecutive Gates are enabled for 1280 ns. The impact of the Clear pulse is the same for all overlap lengths.

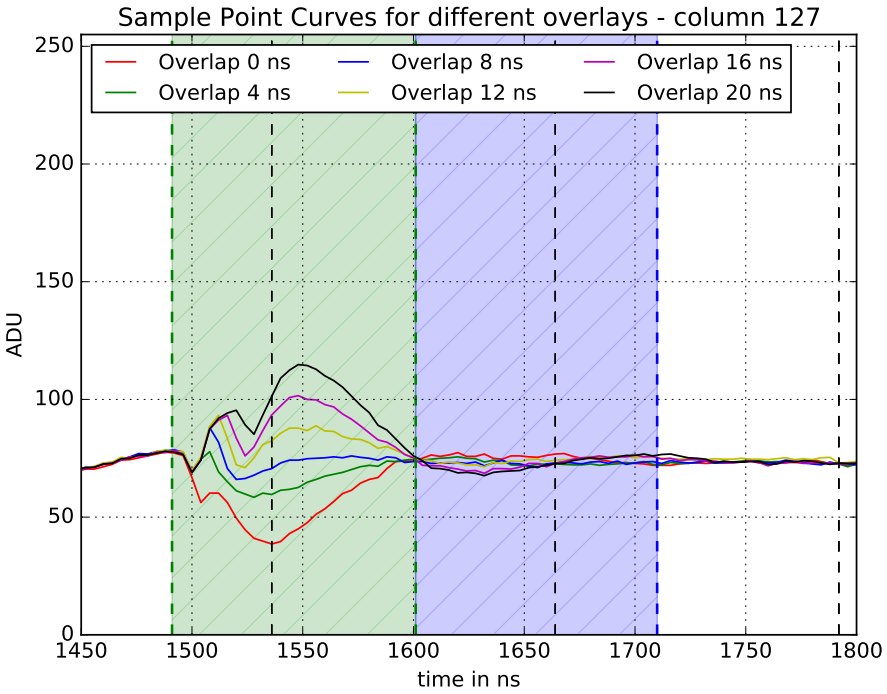


Figure 6.21: Sampling point curves with different overlap lengths for the $\text{rows}_{\text{gate}}$. The Gates are enabled for 1280 ns to avoid the oscillations caused by the Clear pulse. An overlap of 4 ns (green) results in the smallest variation of the Drain current during the process of switching the active $\text{rows}_{\text{gate}}$.

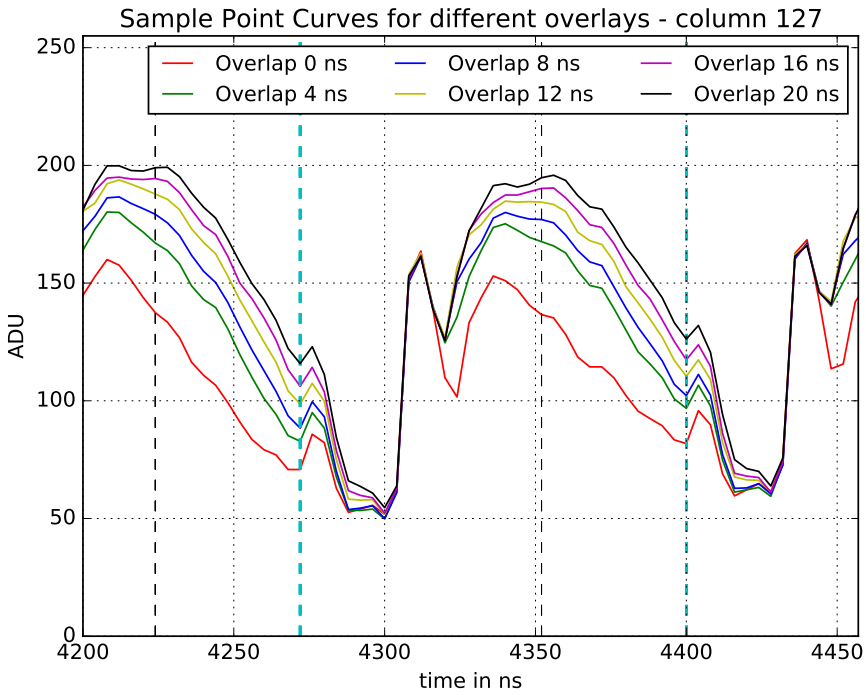


Figure 6.22: Sampling point curves with different overlap lengths for the $\text{rows}_{\text{gate}}$. The Gates are enabled for 128 ns. The impact of the Clear pulse and the switching between consecutive $\text{rows}_{\text{gate}}$ cannot be separated. The drop of the Drain current during the process of changing the active row_{gate} compensates up to a certain fraction with the effect of the applied Clear pulse and the reverberate oscillations.

7 mm) in contrast to the hybrid 5 setup. The Drain lines have approximately the same length as the pilot run module ($\sim$ 45 mm).

- **Pilot Run:** The pilot run module consists of a large sensor, 192 $\text{rows}_{\text{gate}}$ and 1000 $\text{cols}_{\text{drain}}$. The number of $\text{rows}_{\text{gate}}$ is a factor of twelve larger compared to the small matrices and the number of $\text{cols}_{\text{drain}}$ is roughly a factor of eight larger. This results in more parasitic capacitance, which has a direct influence on the Drain currents.

The sampling point curves of these three different test setups are shown in Fig. 6.23. For the pilot run module, the impact of the Clear pulse dominates the Drain current as function of time; a narrow plateau is nevertheless visible. This is chosen as the sampling point, marked with the turquoise dashed lines. The Drain currents of the DEPFETs of the pilot run module behave quite differently compared to the test systems equipped with small matrices. The dominating effect is the impact of the Clear pulse.

Problems

The large parasitic capacitances of the Clear, Gate and Drain lines influence the Drain currents. Almost no plateau in the Drain current as a function of time is reached suited as sampling point. A sort of plateau is visible before applying the Clear pulse, as shown in Fig. 6.22. The Switcher sequence without overlap is chosen because the impact of the Clear pulse (increased Drain current) and

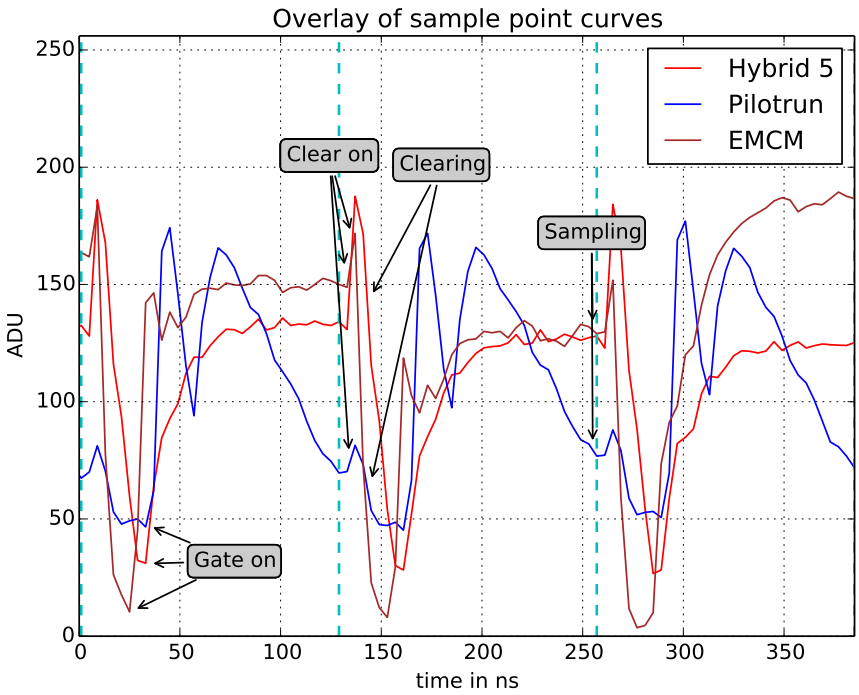


Figure 6.23: Sampling point curves of three different setups, the hybrid 5, the EMCM and the pilot run. A plateau is clearly visible for hybrid 5 and the EMCM. The pilot run only shows a very narrow plateau.

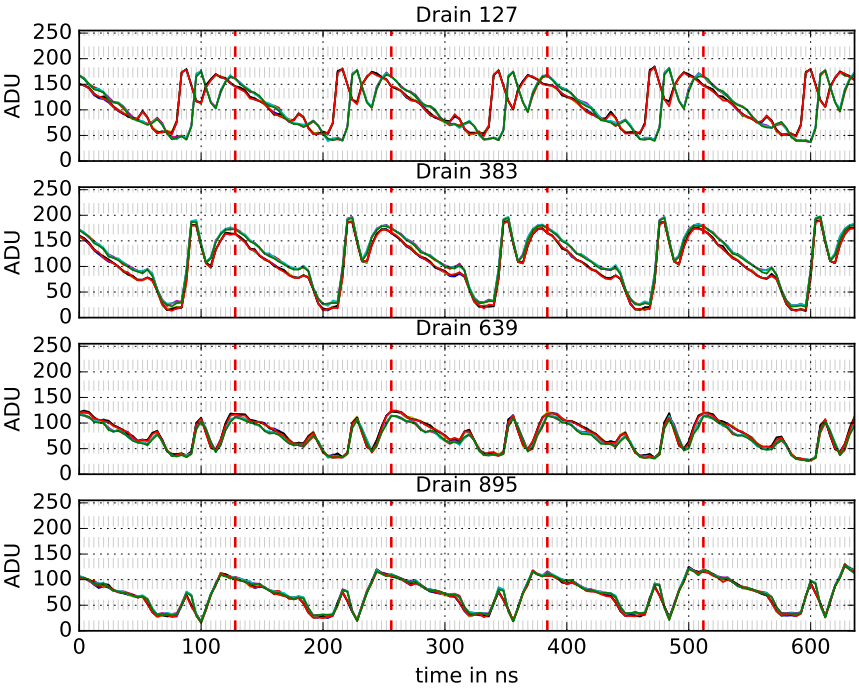


Figure 6.24: Sampling point curves of four different DCDs of the pilot run module W30-OB1. Power cycles are performed between the different measurements. A phase shift of the DHP results in a shift of sampling point in time. The dashed have a distance of 128 ns. The different colors indicate different power-cycles.

the row_{gate} switching process (decrease of the Drain current) compensate up to a certain degree.
A bug in the DHP (up to version DHPT1.1) used in in the pilot run modules causes a phase shift between the synchronous global clock and the outgoing DCD and Switcher clocks. However, the phase shift does not affect the sampling point of the DCD, which is connected to the same DHP as the Switchers (for the module W30-OB1 it is DCD 4). The other three DCDs may shift their sampling point. To study this behavior, various power cycles[6] are performed and the scan of the sampling point curve is repeated. One $\text{col}_{\text{drain}}$ of each of the four DCDs is shown in Fig. 6.24. As it is clearly visible, the phase shifts result in shifted sampling point curves in time. The maximum shift is 12 ns.

Measurements show (see Sect. 6.11 and chapter 7) that a plateau is not strictly required to detect and measure a signal. On the rising and falling edges the Drain current can be sampled and the signals can be measured, which are stable in time as it will be shown by the noise measurements in Sect. 6.7.

6.6 Pedestals

The pedestal value of a DEPFET pixel is defined as the Drain current when the GateOn voltage is applied and the *internal Gate* is empty. A conductive channel with holes is created between the *Source* and the *Drain* p^+ implants. Every pixel behaves slightly differently compared to the neighboring ones. This is primarily due to variations in the production, such as polishing the silicon wafer, inhomogeneous doping, etc.
The pedestals of the entire module for a GateOn voltage of -1 V is shown in Fig. 6.25. Three Drain columns ($\text{col}_{\text{drain}}$) are defective in the area of DCD 3. As a result, those pixels show no signals. They are visible in Fig. 6.25 as the dark blue line along the rows around column 150. There are variations between the DCDs due to different individual DCD specific settings for the ADCs (to reduce INL, DNL and missing codes). A gradient from left to right is visible in DCD 1 and DCD 2. The left geometrical columns (col_{geo}) show increased pedestal values compared to those which are connected on the right. It is not an artifact of the matrix, it is most likely due to cooling issues of the DCDs and voltage drops across the module[7]. In addition to the left-right variation, a narrow ring-like structure (around row_{geo} 100–200 and row_{geo} 400–500) can be seen. This is due to variations in the bulk doping, which could occur in the etching, polishing or other rotating procedures [198].
When the GateOn voltage is decreased, the pedestal spread increases (see Sect. 6.8). The *pedestal compression method*, introduced in Sect. 6.9, allows this spread to be reduced. To verify whether the sensor responds to light, a mask of silicon is put on top of the sensitive part, as shown in Fig. 6.26. The signal of the DEPFETs are recorded and shown in Fig. 6.27, confirming the sensitivity to light. In addition, the correct pixel mapping can be easily verified.

[6] The entire system is powered off and on.
[7] The behavior of different cooling procedures is shown in app. C.4.

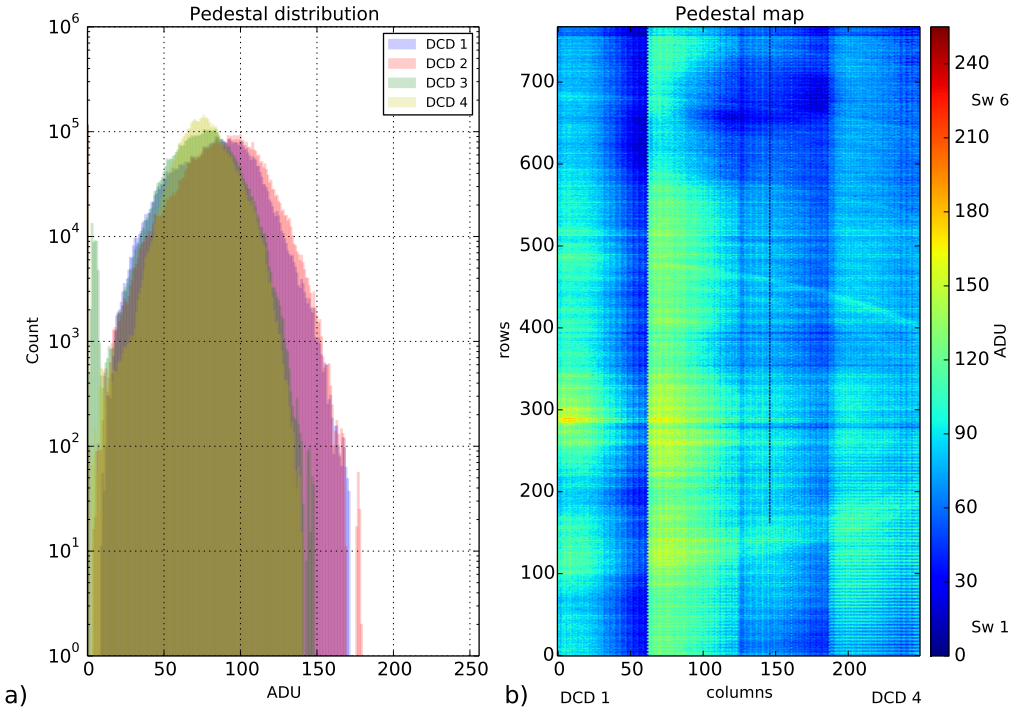


Figure 6.25: Pedestals of the W30-OB1 module at $V_{\mathrm{GateOn}} = -1\,\mathrm{V}$. a) shows the distribution as function of the ADU. b) shows the pedestal map. The pixel values in ADU are color-coded. One Drain line connected to DCD 3 is disconnected around $\mathrm{row}_{\mathrm{geo}}$ 160. This corresponds to the dark blue column $\mathrm{col}_{\mathrm{geo}}$ 146.

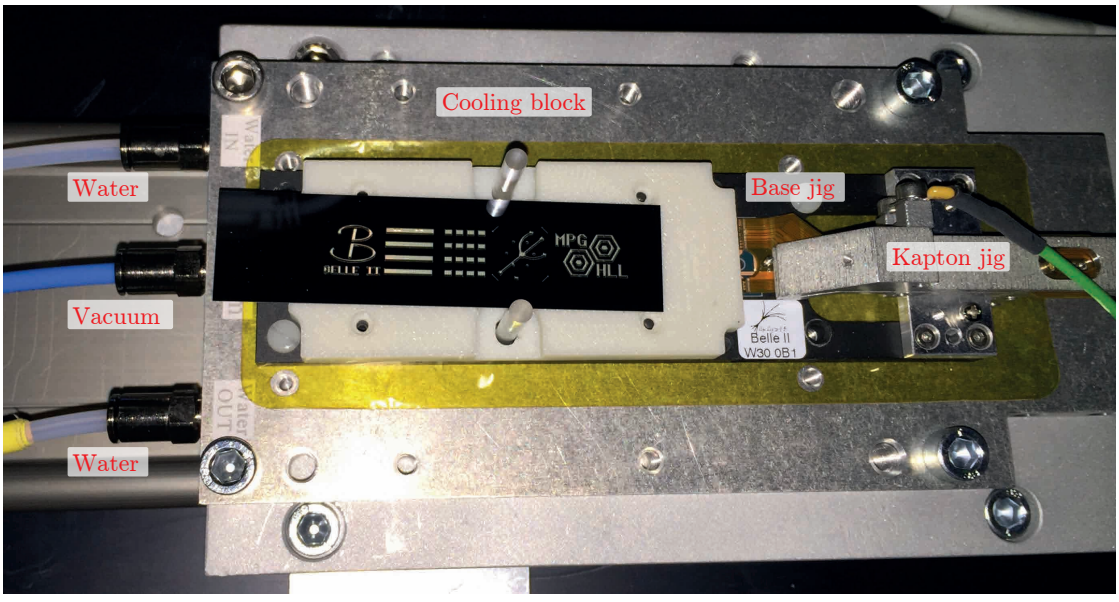


Figure 6.26: A silicon light mask is placed on top of the sensitive part of the detector.

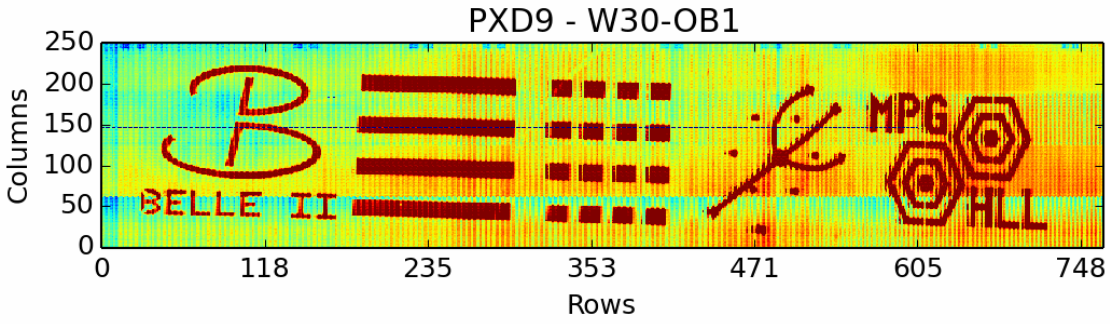


Figure 6.27: A silicon light mask is placed on top of the pilot run module. The larger pixels are on the left (row_{geo} =1–512) while the small pixels are on the right (row_{geo} =513–768).

6.7 Noise

The theoretical treatment of the noise is discussed in detail in Sect. 4.14. The noise of the DEPFET pixels is studied experimentally in this section, in particular, the common mode noise, which dominates all other noise sources (see discussions in Sect. 4.14.3). To disentangle the effect of the decoupling capacitors and the common mode correction (CMC) of the DCD, only the digital common mode correction is applied. For this reason, the analog common mode correction (see Sect. 4.14.3) of the DCD is disabled.
To study the effect of the common mode on the overall noise of the module, 100 frames are recorded with DCD gain 1. The measurements are performed for two different breakout boards, one of which is equipped with decoupling capacitors and the other is not. Each power supply net (of the ASICs and the DEPFET) is decoupled from the chassis ground. The overall noise and the common mode distributions are shown in Figs. 6.28 to 6.30. The common mode correction is calculated as presented in eq. (4.14.18) in Sect. 4.14.3. The mean noise value is 2.27 ADU for the breakout board without capacitors (see Fig. 6.28a). The common mode distribution is quite large as shown in Fig. 6.28b. The values range from -9 ADU to +9 ADU. In contrast, the mean value of the noise is reduced to 0.67 ADU by using the breakout board equipped with decoupling capacitors. The common mode noise mostly disappears in the case of the board with decoupling capacitors (see Fig. 6.30).
For both scenarios, noise values up to 5 ADU are included in the fit of the noise distribution. Pixels with higher noise are not included in the fit. The digital common mode correction cannot completely "filter" the common mode, as can be seen by comparing Fig. 6.29 and Fig. 6.28. Noisy pixels (with higher noise values) can also be caused by transmission errors in the inter-ASIC communication, i.e., between DCD and DHP. The remaining noise originates from the effects discussed in Sect. 4.14: shot noise, thermal noise, leakage current, $1/f$ noise and noise sources from the electronic readout circuits.

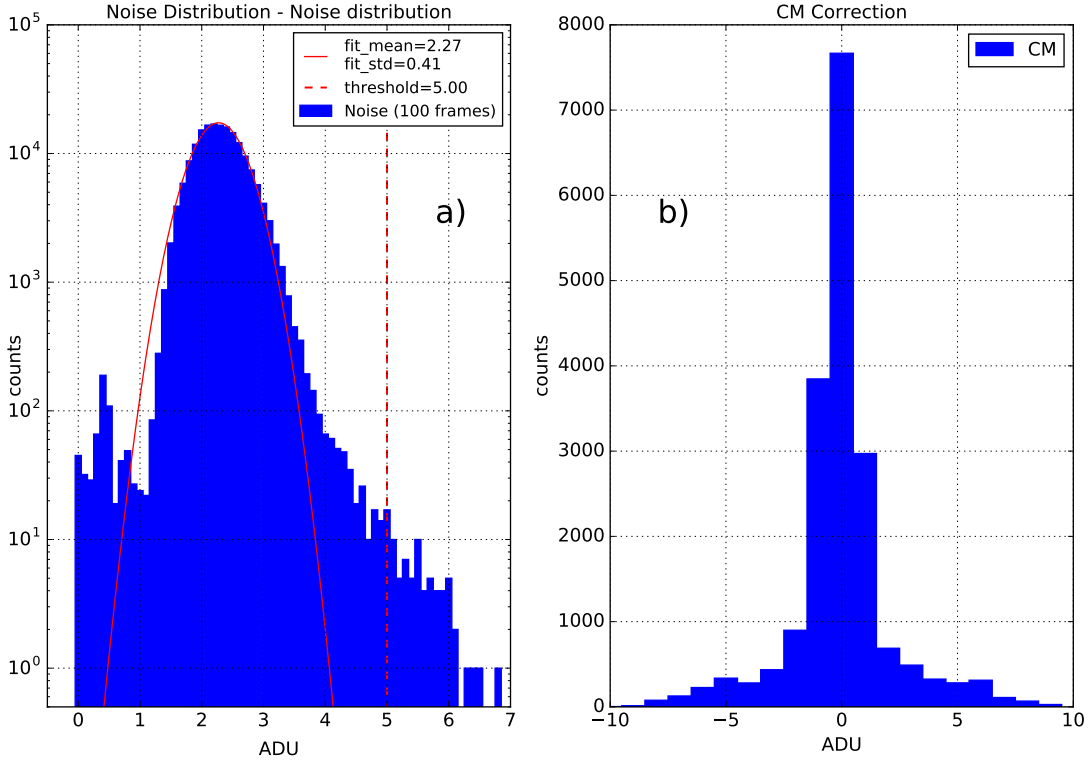


Figure 6.28: a) Noise distribution of all DEPFET pixels using the breakout board without decoupling capacitors and without digital common mode correction. The DCD gain of 1 is selected. b) Common mode noise distribution.

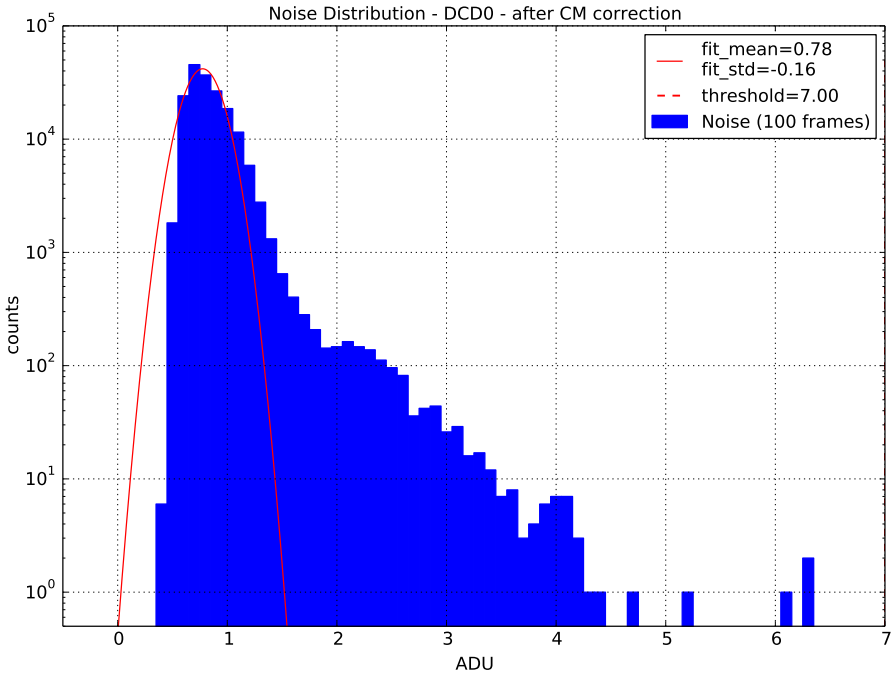


Figure 6.29: Noise distribution (using the breakout board without decoupling capacitors) after digital correction of common mode according to eq. (4.14.20). The DCD gain of 1 is selected. The threshold of 7 ADU is only chosen for the values that are included in the fit.

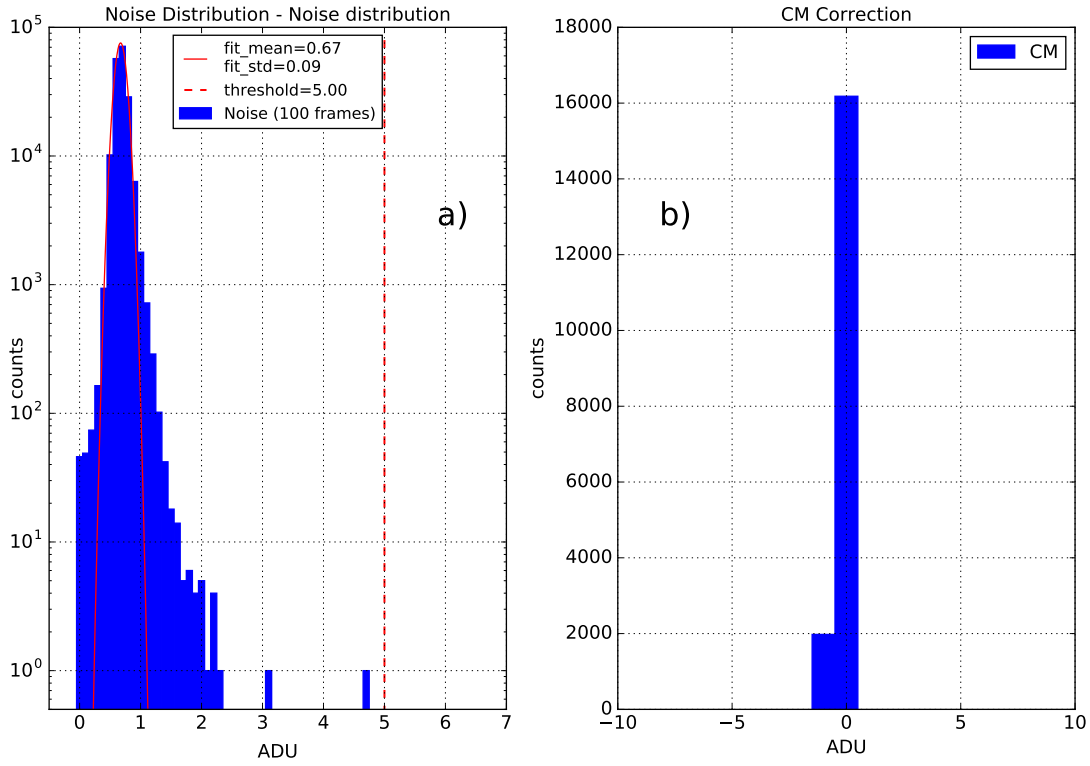


Figure 6.30: a) Noise distribution of all DEPFET pixels using the breakout board with decoupling capacitors. The DCD gain of 1 is selected. b) Common mode noise distribution. There is no value below -1.5 ADU nor above 0.5 ADU.

6.8 I-V Curve

The Drain current of the one-dimensional transistor, I_{ds}, is mathematically described in Sect. 4.5.1. Assuming an empty *internal Gate* ($Q_{\mathrm{sig}} = 0$), eq. (4.5.1) simplifies to:

$$I_{\mathrm{ds}} = -\frac{W}{2L}\mu_{\mathrm{h}} C_{\mathrm{ox}} (V_{\mathrm{gs}} - V_{\mathrm{T}})^2 \tag{6.8.1}$$

The characteristic current-voltage (I-V) curves, for which the Drain current is measured as function of the Gate voltage, will become important to calibrate the irradiated DEPFET pixels and to find the optimal operation settings and voltages. The threshold voltage decreases (to more negative values) due to oxide damages. Consequently, the necessary GateOn voltage needs to become more negative with increasing radiation doses. More details are explained in [191].

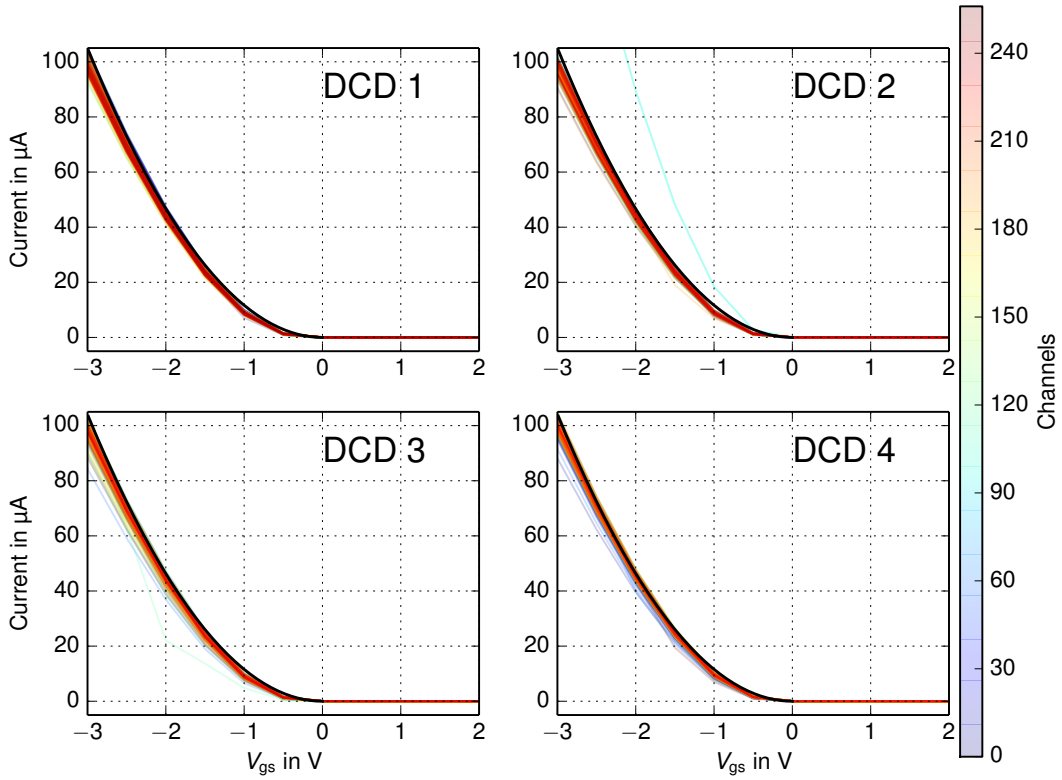


Figure 6.31: Drain current, I_{ds}, measured as function of the Gate voltage, $V_{\mathrm{gs}}(=V_{\mathrm{GateOn}})$. The 1000 Drain lines are split into groups of 250, corresponding to input channels of a single DCD.

I-V Curve using the Source Measure Unit For the unirradiated pilot run module, the I-V curves are measured using an external SMU, before the assembly of the ASICs and passive components[8]. The measurement is performed [154] for GateOn voltages ranging from −3 V to 2 V in steps of 500 mV. The raw data set is

[8] A needle card is used to contact the Drain line pads and the Gate pads.

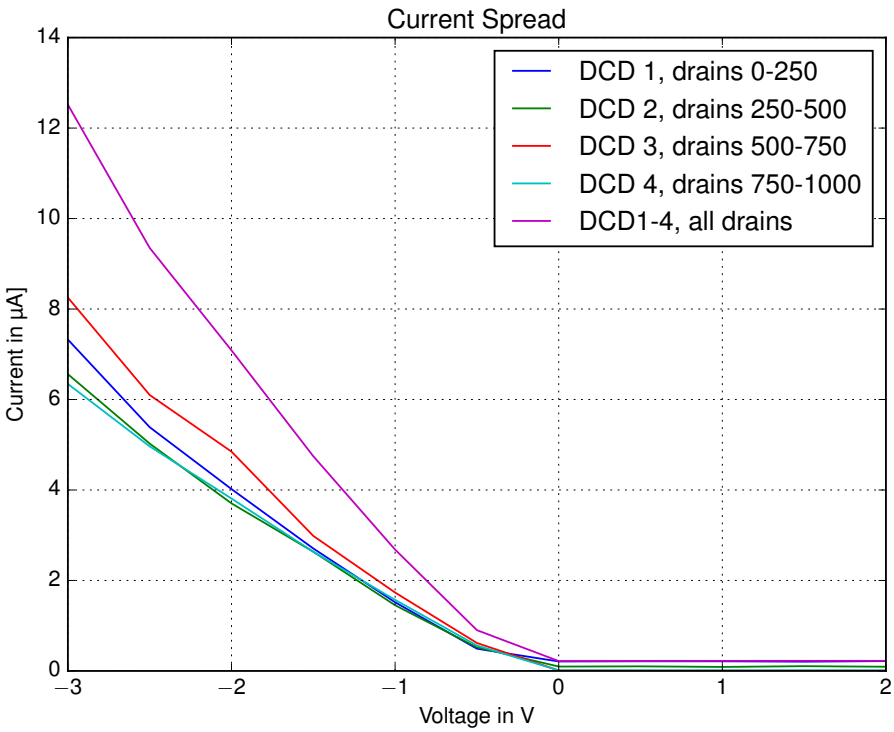


Figure 6.32: The pedestal spread of the Drain lines split in groups of 250 channels and the entire spread across all 1000 Drain lines. The entire spread is around 12.5 µA.

analyzed and shown in Fig. 6.31. The 1000 Drain lines are split into four groups, each with 250 Drain lines, corresponding to the input channels of the four DCDs. The median values are used as fit parameters for a quadratic curve of:

$$f_{\text{fit}} = a(x - b)^2 \tag{6.8.2}$$

The parameters in eq. (6.8.2) are listed in Tab. 6.4:

Table 6.4: Fit parameters for the I-V curve according to eq. (6.8.2).

DCD	DCD 1	DCD 2	DCD 3	DCD 4
$[a]$ in µA/V^2	11.67 ± 0.13	11.67 ± 0.13	11.56 ± 0.12	11.57 ± 0.13
$[b]$ in V	0.07 ± 0.001	0.07 ± 0.001	0.07 ± 0.001	0.05 ± 0.001

The values of b for the threshold voltage are close to zero. Using the extracted parameters (a and b) the hole mobility, μ_{h}, could be calculated with a given capacitance per unit area, C_{ox}, according to eq. (6.8.1). However, this would require a two-dimensional model to describe accurately the transistor. In addition, the hole mobility is not a constant but depends on the GateOn voltage due to scattering processes, which increase at the oxide for more negative GateOn voltages. One Drain line in group DCD 2 shows an increased Drain current (see Fig. 6.31). A short between two Drain lines causes this behavior. The module has been successfully repaired after carrying out this measurement.

The pedestal current spread across the Drain lines is shown in Fig. 6.32. The more negative the GateOn voltage, the larger the current spread becomes. The current spread for each group is between 6–8 µA. The spread[9] across all 1000 Drain lines is approximately 12.5 µA for a GateOn voltage of −2.5 V. The current spread is directly related to the pedestal spread. Only one row_{gate} is contacted and the Drain currents of this particular row_{gate} are measured.

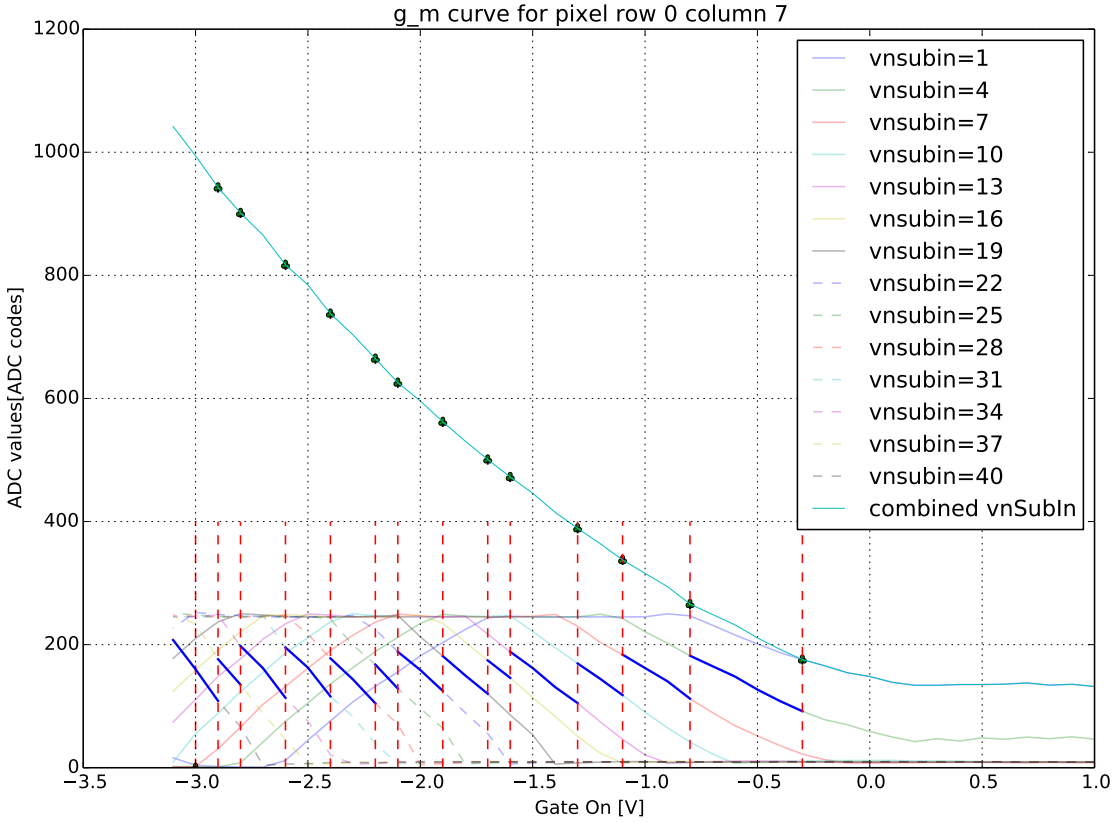


Figure 6.33: I-V curve recorded with the DCD for different `VnSubin` settings and GateOn voltages. The curve between a lower and upper thresholds is added to a global I-V curve.

I-V Curve using DCDs External SMUs cannot be used when the PXD is installed in Belle II. Therefore, another method is required. It is necessary to record I-V curves of the existing module without the requirement of additional devices and without the need to disassemble the detector. The ADC transfer curves are recorded by decreasing the GateOn voltage and measuring the Drain current with the DCD, as explained in Sect. 6.4. The expected Drain currents can grow larger than the dynamic range of the DCD. Consequently, these I-V curves are recorded for different settings of `VnSubin`, the internal current sink of the DCD at the input node (see Fig. 4.23). Doing so, one can shift the Drain currents into the dynamic range of the DCD. This corresponds to a vertical shift of the ADC transfer curves (see app. C.3).

[9] The spread could also increase if the matrix is completely biased.

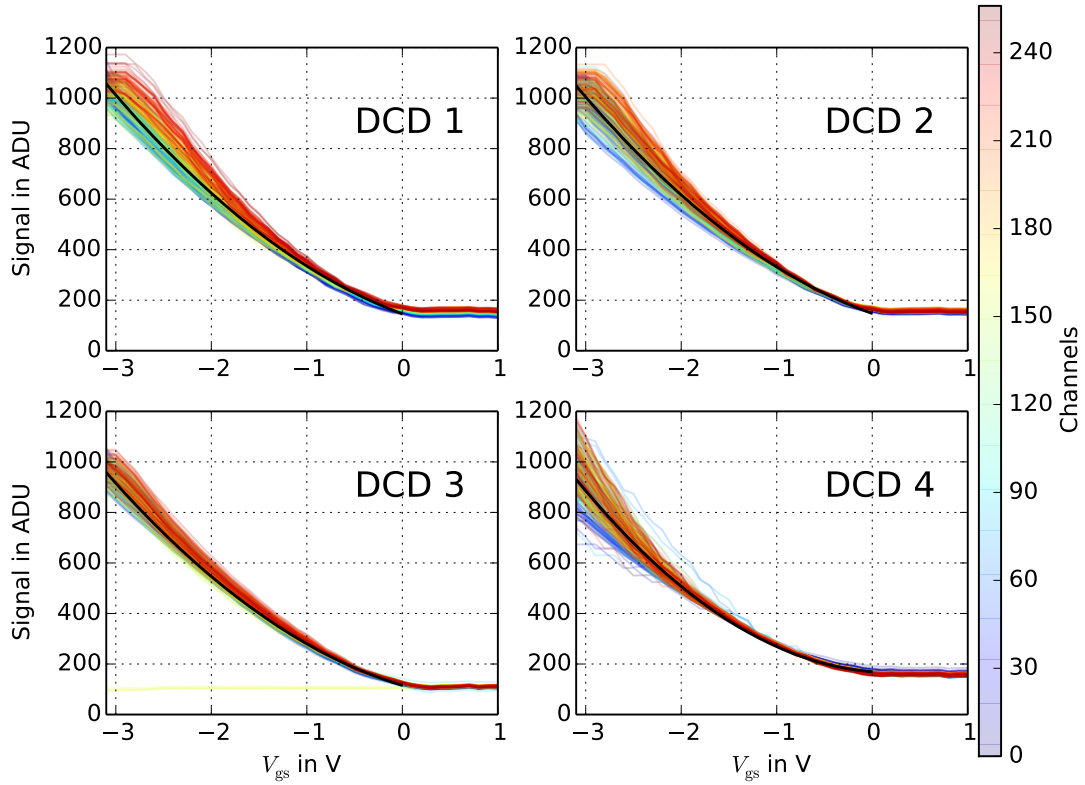


Figure 6.34: I-V transfer curve measured by the DCD by sweeping the GateOn voltage and the `VnSubin` DAC. The black line is the median of all connected Drain lines within a DCD.

The GateOn voltage is varied between +1 V and −3.1 V, in steps of 100 mV, for different settings of `VnSubin`. The DEPFET Drain currents are measured with the DCD. The resulting curves are shown in Fig. 6.33. Because of the limited precision (8-bits), a region between a lower (80 ADU) and an upper (180 ADU) boundary is chosen. The corresponding GateOn voltage values are marked with the red dashed line in Fig. 6.33. The transfer curve between the upper and lower boundary is added to a global curve, which results in a sufficient dynamic range of the digitizer (corresponding to 11-bit precision). The combined `VnSubin` curve is shown in Fig. 6.33. The markers correspond to the "gluing" points of the individual I-V curves.
Using this method for all channels, the transfer curves of all 250 Drain lines of each DCD are plotted in Fig. 6.34. The three broken Drain lines[10] in DCD 3 (column pair 5, channels 5–7) show constant ADU values at the lower dynamic range of the DCD. The transfer curves for DCD 4 show a non-linear behavior. This is caused by non-optimal DCD settings and a large number of transmission errors to the DHP. This causes the non-characteristic curves, behaving like a step-function for some channels of DCD 4.
The spread of the transfer curves also increases with decreasing GateOn voltage. The same behavior has already been observed for the measurements with the SMU.

[10]The defective Drain lines were already observed in the pedestal distribution in Sect. 6.6.

The spread is DCD-dependent, caused by thermal effects and voltage drops across the DCD, as already shown in the pedestal distribution (see Fig. 6.25), but also due to variations in the module production.

Conclusion Assuming a more homogeneous voltage distribution on the new modules with the latest generation of the DCD (DCDBv4.2), the pedestal spread across the DCD is expected to disappear due to a more homogeneous powering. This should result in I-V curves similar to those measured for DCD 3 (see Fig. 6.34). Measuring the I-V curve with the DCD, which has been introduced in this section, works properly and gives expected results. The comparison between the curves measured with the SMU and with the DCDs is shown in Fig. 6.35. A gain factor of $\sim 130\,\mathrm{nA/ADU}$ is used, where the precise value of the gain factor depends on the DCD (see Sect. 6.4). For static measurements using the SMU, the DEPFET matrix is powered only partially, i.e., bulk voltage=15 V, Source=0 V, ClearGate=5 V, Gateoff=2 V, Drain voltage=-5 V. The rest of the DEPFET voltages (see Tab. 6.2) are not applied.
In contrast, using the DCD method, the matrix is fully biased. Therefore, the threshold voltage, V_T, is shifted to more negative values. Furthermore, the observed threshold shift is also due to the applied Clear voltage, changing the transconductance of the MOSFET by approximately 1 µA/V [136].

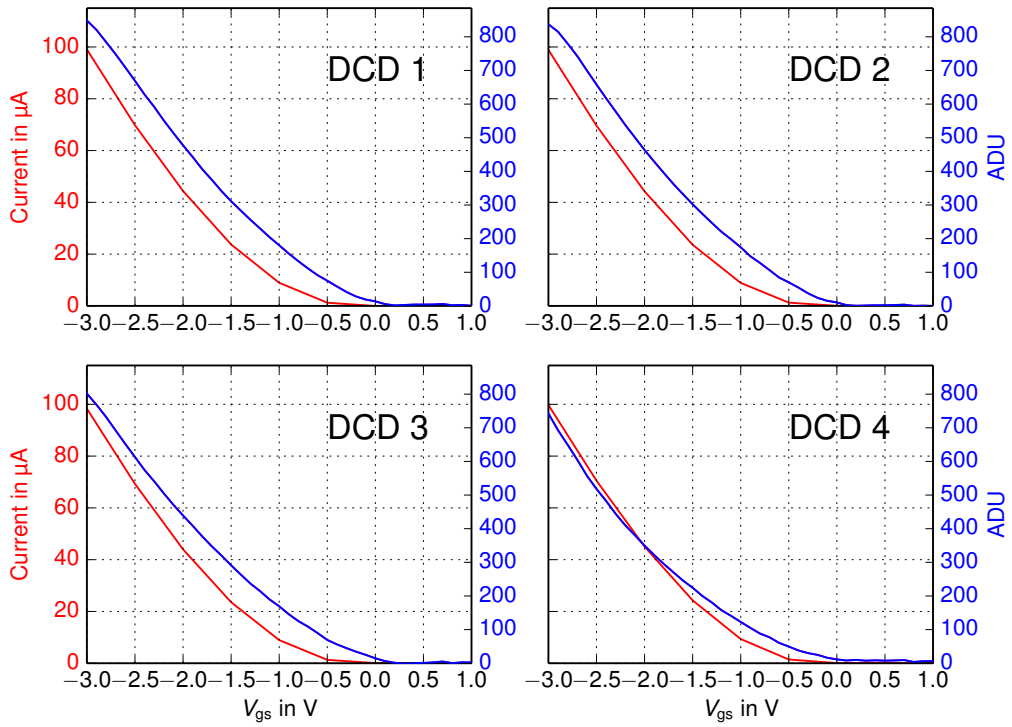


Figure 6.35: Comparison of I-V curves measured with SMU (red) and DCDs (blue). 1 ADU corresponds to 129.9 µA according to gain 1. DCD 4 behaves differently compared to the other three DCDs, which is most probably due to insufficient cooling.

6.9 Pedestal Compression

The pedestal distribution for a GateOn voltage of $-2.5\,\mathrm{V}$ is shown in Fig. 6.36. It is wide, $\simeq 200\,\mathrm{ADU}$, which corresponds to $\simeq 25\,\mu\mathrm{A}$. Approximately half of the spread originates from the matrix ($\sim 12.5\,\mu\mathrm{A}$, which was measured for a partially powered DEPFET matrix; see Sect. 6.8) and the other half is due to the DCD. For DCD 3 and DCD 4, the spread is less than 150 ADU ($\simeq 19.5\,\mu\mathrm{A}$). A large fraction of the spread is caused by the inhomogeneities in the ring-like structure, visible in the hitmap (see Fig. 6.36 right). Another reason for low pedestal values is a threshold shift of the GateOn voltage in the upper region ($\mathrm{row}_{\mathrm{geo}} \approx 700$) due radiation damages from measurements with a radioactive source.

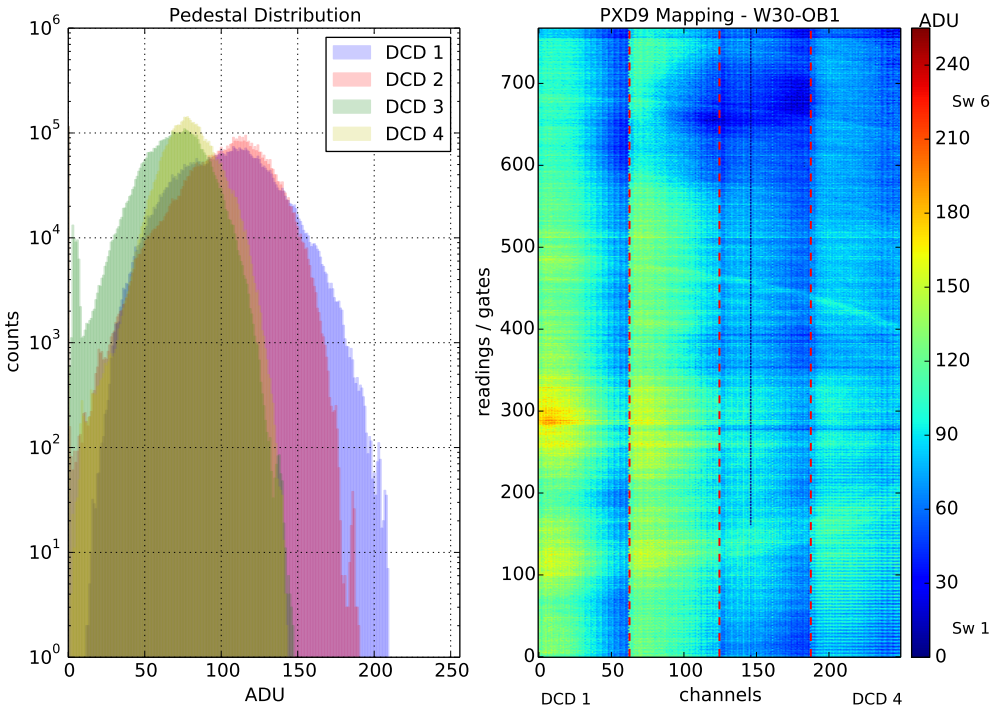


Figure 6.36: Pedestal distribution and hitmap of the W30-OB1 module without pedestal compression and disabled analog common mode correction. The dark blue line in the region connected to DCD 3 is a broken Drain line.

As already shown in Sect. 6.8, the pedestal spread of the matrix increases with decreasing GateOn voltage. Since the dynamic range of the DCD is limited (depending on the gain, see Sect. 6.4) the distribution of the pedestals should be ideally as narrow as possible in order to have a wider dynamic range for the signal detection. The theoretical concept of the pedestal compression has already been presented in Sect. 4.8.7.

6.9.1 Synchronization between DHP and DCD

To calibrate the delay elements for the data transmission from the DCD to the DHP, a digital test pattern can be enabled (within the DCD) and compared to the

readout data as described in Sect. 6.3.2. It is necessary to ensure that the pedestal offset values sent by the DHP are applied to the correct pixels by the DCD, i.e., the data transmission is now inverted from the DHP to the DCD. However, there is no digital test pattern to verify reliable data transmission. The delay settings must be tuned indirectly[11]: A pre-defined offset value ($0 \times I_{\text{DAQ-glo}}$, $1 \times I_{\text{DAQ-glo}}$, $2 \times I_{\text{DAQ-glo}}$, $3 \times I_{\text{DAQ-glo}}$, in the following it is abbreviated by 0, 1, 2, 3) can be assigned for each individual pixel, which can be added to the DEPFET pixel current. This is similar to defining a custom "test pattern" and applying it to the DCD input channels. Afterwards, the received data can be analyzed and the delay settings can be tuned until the pre-defined test pattern is read back. This is only possible if a fixed amount of current is subtracted globally from all pixels, i.e., the analog common mode correction within the DCD must be disabled (see Sect. 4.14.3).
In the first step, a calibration must be performed. For all 192,000 pixels of the matrix, the offset value 0 is added (which corresponds to the pedestal values) and

[11] For this procedure, the delay elements from the DCD to the DHP must be already tuned correctly.

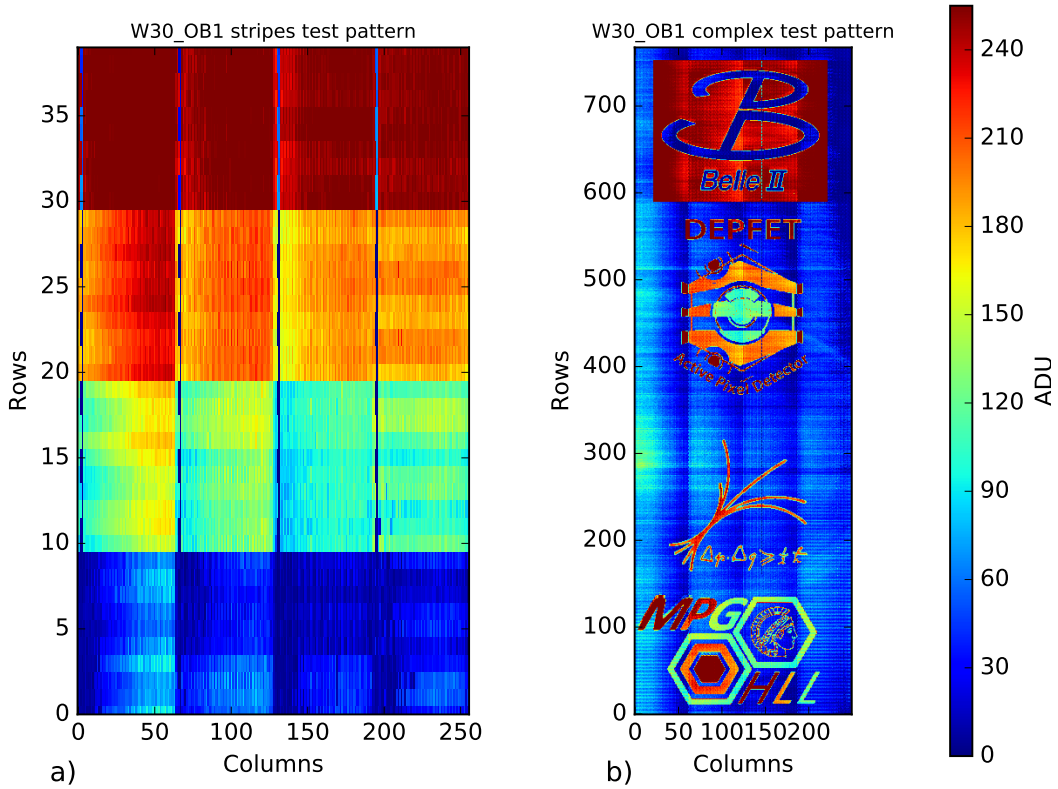


Figure 6.37: Measured pedestal values with enabled 2-bit offset compensation and defined test patterns. a): Stripes Test pattern – electrical mapping (row_{gate}, $\text{col}_{\text{drain}}$). For ten rows, a different offset value (0, 1, 2 ,3) is added. The dark blue columns correspond to the six DCD input channels that are not connected to the DEPFET pixels. b): More complex test pattern to verify correct delay settings – geometrical mapping (row_{geo}, col_{geo}). The dark blue columns (in DCD 3 section, column ~ 150) correspond to the broken Drain lines.

data is acquired. In the next step, the offset value 1 is added to all pixels and the data is recorded. Afterwards, the values 2 and 3 are added and recorded. Those data serve as calibration, since it is known exactly how the added current changes the ADU value of each individual pixel. Next, a pre-defined test pattern is written into the offset memory of the DHP. As it is known exactly how the pixel ($\mathrm{row_{geo}}$, $\mathrm{col_{geo}}$) is expected to react to the additional added offset current, the delay elements can be shifted to match the pedestals values with the pre-defined test pattern.

An example is given in the following: The ADU values for a cluster of 3×3 pixels are measured by adding the four possible offset values (0, 1, 2, 3), where each offset adds 10 ADU counts to the previous values:

Offsets = 0			Offsets = 1			Offsets = 2			Offsets = 3		
26	42	39	36	52	49	46	62	59	56	72	69
24	40	43	34	50	53	44	60	63	54	70	73
37	38	34	47	48	44	57	58	54	67	68	64

These data serve as the calibration. Afterwards, a pre-defined test pattern is written into the memory of the DHP offsets, which are then applied to the DCD. Using the calibration data, the expected signal is known for those pixels in ADU counts. Since the measured signals may show deviations from the expected signals because of lacking synchronization between DCD and DHP, another test pattern can be deduced:

Def. pattern			Expected ADU			Measured ADU			Meas. pattern		
2	1	0	46	52	39	46	62	49	2	2	1
0	2	1	24	60	53	24	70	63	0	3	2
1	3	2	47	68	54	47	38	34	1	0	0

Column 2 and column 3 are shifted by one row, i.e., the offsets values arrive too early. The delays are then varied until the measured signals correspond to the expected signals. Having optimized the offset delays settings, the timing for the `offset_frame_sync_dly` (see app. C.2) must be adjusted correctly. To do so, a simple test pattern is used, for instance:

row	added current
0 to 9	$0 \times I_{\mathrm{DAQ\text{-}glo}}$
10 to 19	$1 \times I_{\mathrm{DAQ\text{-}glo}}$
20 to 29	$2 \times I_{\mathrm{DAQ\text{-}glo}}$
30 to 39	$3 \times I_{\mathrm{DAQ\text{-}glo}}$

This pattern corresponds to stripes within the first 40 rows. Two examples of test patterns (stripes and more complex) are written into the memory of the DHP. The resulting pedestal distributions with the enabled 2-bit offset compensation are shown in Fig. 6.37.
Following the optimization of the `offset_frame_sync_dly` setting (see app. C.2; for GCK=62.5 MHz it should be set to 1536) and the delays for the individual transfer lines, the optimization of the offsets for the DEPFET pixels is performed.

6.9.2 Offset optimization

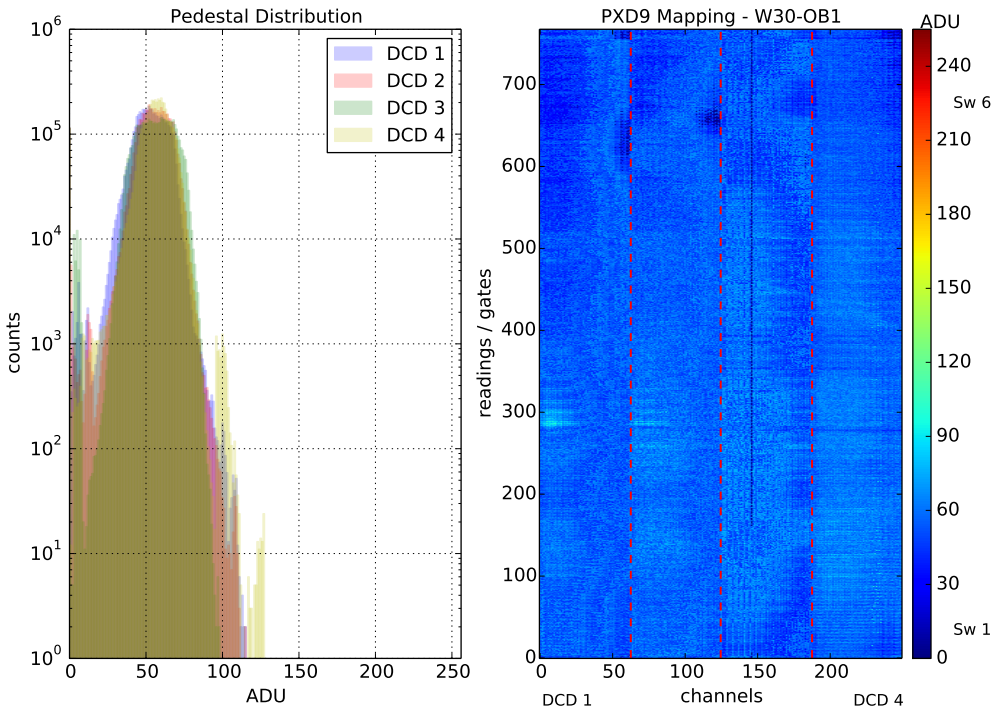


Figure 6.38: Pedestal distribution and hitmap with enabled offset compensation and current globally subtracted from all pixels.

After the delay optimization for the 2-bit offset compensation is performed, the correct offset values (i.e., $0, 1, 2, 3 \times I_{\text{DAQ-glo}}$) for each individual pixel need to be calculated. Finding the correct values for the offsets is a two dimensional problem, since the global $I_{\text{DAQ-glo}}$ value and the offset value for each individual pixel $(0, 1, 2, 3)$ can be selected. The goal is to find offset values, $I_{\text{DAQ-ind}}$, $(= 0, 1, 2, 3 \times I_{\text{DAQ-glo}})$ for each individual pixel, resulting in a very homogeneous distribution for all 192,000 DEPFETs of the entire module and thus narrowing the pedestal spread. Since four DCDs are mounted on a module, the optimization for the offset compression is done for each DCD individually.
The optimization is done by collecting data in the first step, i.e., to record the pedestals for all pixels by applying the offset values $0, 1, 2, 3 \times I_{\text{DAQ-glo}}$, where $I_{\text{DAQ-glo}}$ is varied. In the second step (analysis), different combinations of the recorded pedestals (with added current $I_{\text{DAQ-ind}}$) are compared in order to identify the narrowest pedestal distribution. This reveals the global current value, $I_{\text{DAQ-glo}}$, and the values $(0, 1, 2, 3)$ for the individual pixels. The details of the algorithm to find, $I_{\text{DAQ-glo}}$, and the offset values, $I_{\text{DAQ-ind}}$, for each individual pixel are described in [168].
The pedestal distributions for all four DCDs without any offset corrections are shown in Fig. 6.36. The pedestal spreads are listed in Tab. 6.5. The spreads of DCD 3 and DCD 4 are possibly broader than listed since the lowest values are outside of the dynamic ranges. When the pedestal compression is applied, as

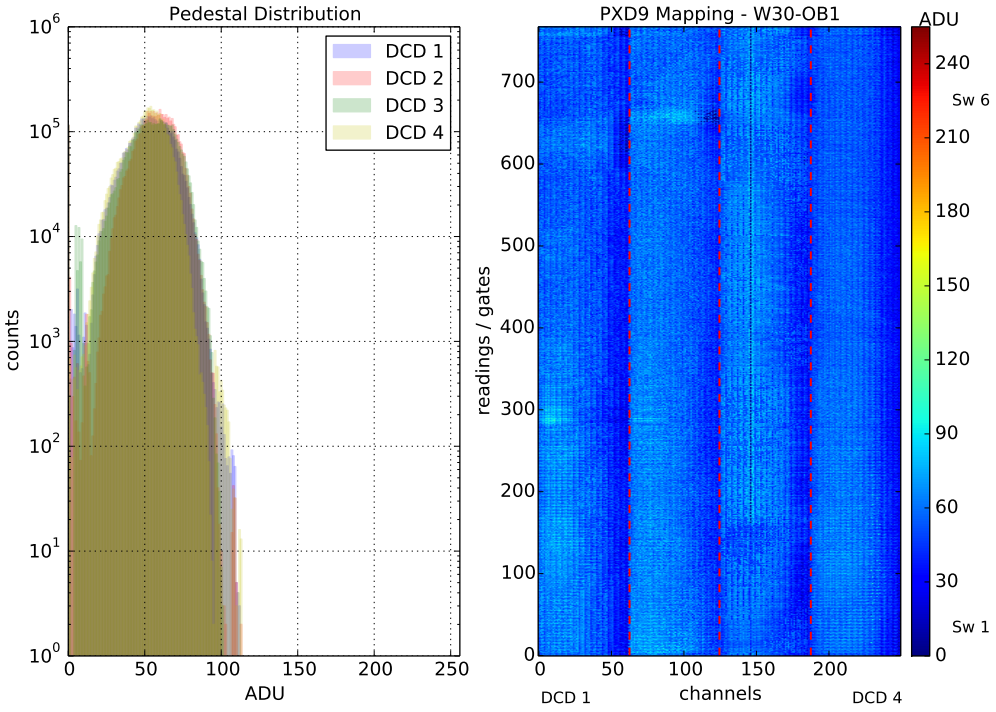


Figure 6.39: Pedestal distribution with enabled offset compensation and activated analog common mode correction. A spread within the four bands associated with the four DCDs on the matrix is visible. This can be caused by voltage drops within the DCD.

explained in Sect. 4.8.7, the distributions become narrower, as shown in Fig. 6.38. There are some outliers in the distributions of the pedestal values. They disappear when the analog common mode correction is applied (see Sect. 4.14.3) as it is visible in Fig. 6.39. However, when this is done, a gradient appears in the pedestals values for each DCD from left to right. This is most likely due to powering issues within the DCD, which are expected to be fixed in the latest version of the ASIC. Due to this gradient, the distributions are compressed only by a factor of approximately two. The resulting spreads are listed in Tab. 6.5. The rings and the threshold valley at the $\text{row}_{\text{geo}} \sim 700$ could be compensated and are almost not visible. The offset inhomogeneity due to the voltage drops across the DCD is studied in app. C.6.

Table 6.5: Spreads of pedestal distribution and hitmap with disabled and enabled pedestal compression.

Pedestal compression	DCD 1	DCD 2	DCD 3	DCD 4
disabled	191 ADU	190 ADU	153 ADU	127 ADU
enabled	103 ADU	110 ADU	96 ADU	107 ADU

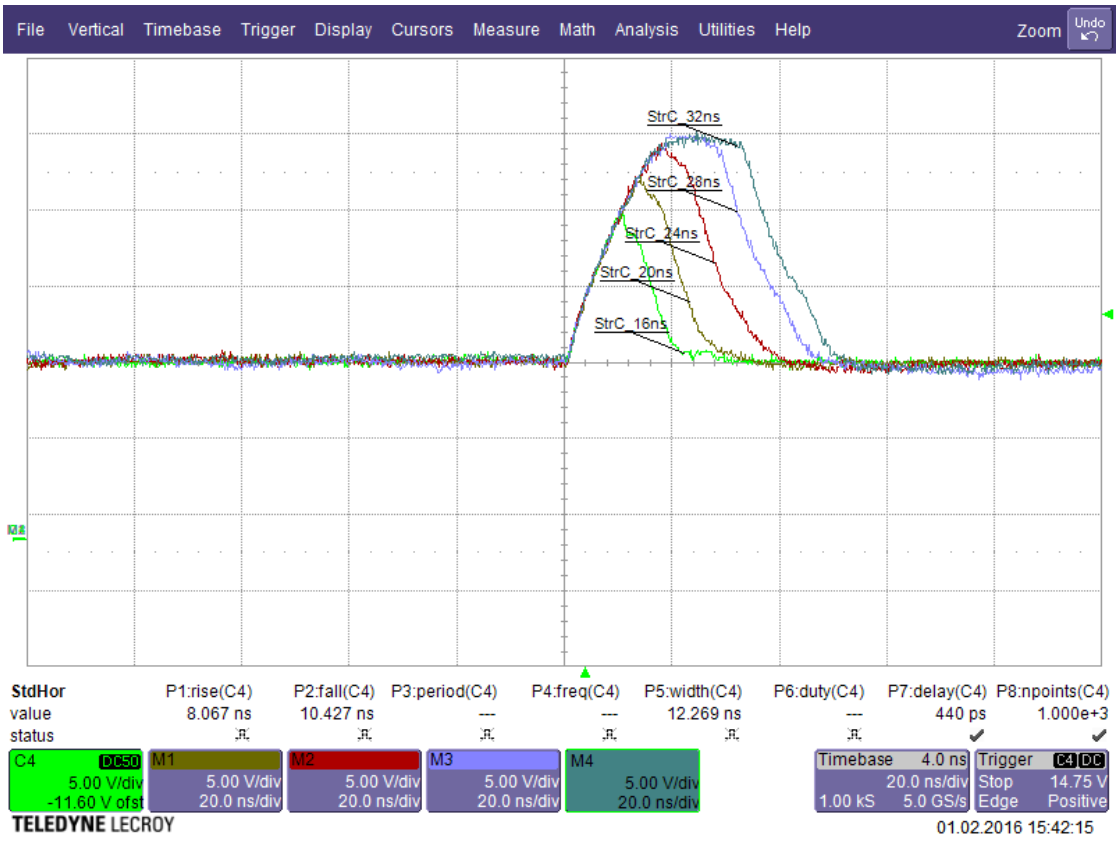


Figure 6.40: Clear pulse of the last Switcher Clear output driver ($\text{row}_{\text{gate}} = 192$) for different lengths of the `Strobe Clear` pulse.

6.10 Clear Behavior

For the final PXD, every pixel is read out within 105 ns (at GCK=76.33 MHz). For the matrix under study, the pixel readout time is 128 ns (at GCK=62.5 MHz). Within this period, the Clear pulse is applied for 32 ns in order to remove the accumulated signal charge from the *internal Gate*. In this section, the Clear behavior is studied, i.e., the amount of charge that remains in the *internal Gate* after the Clear pulse is applied. This behavior is studied as function of different Clear pulse lengths and operation voltages.

Length of the Clear Pulse

First, the optimal the length of the Clear pulse is investigated. To do so, a tiny needle is placed on the output pad of the last Clear output of the last Switcher ($\text{row}_{\text{gate}} = 192$). The ClearOn voltage is set to 20 V and the Clear pulse is measured for different lengths of the applied `Strobe Clear` signal. As it can clearly be seen in Fig. 6.40, the maximum Clear voltage is only reached for Clear pulse length of 28 ns or longer.
For shorter pulses, only a fraction of the total ClearOn voltage is measured. Taking into account the fact that the parasitic Clear capacitance is located behind the test pad, it has been decided to set the length of the Clear pulse to 32 ns in order to have the required ClearOn voltage also applied at the *Clear implants*. The parasitic

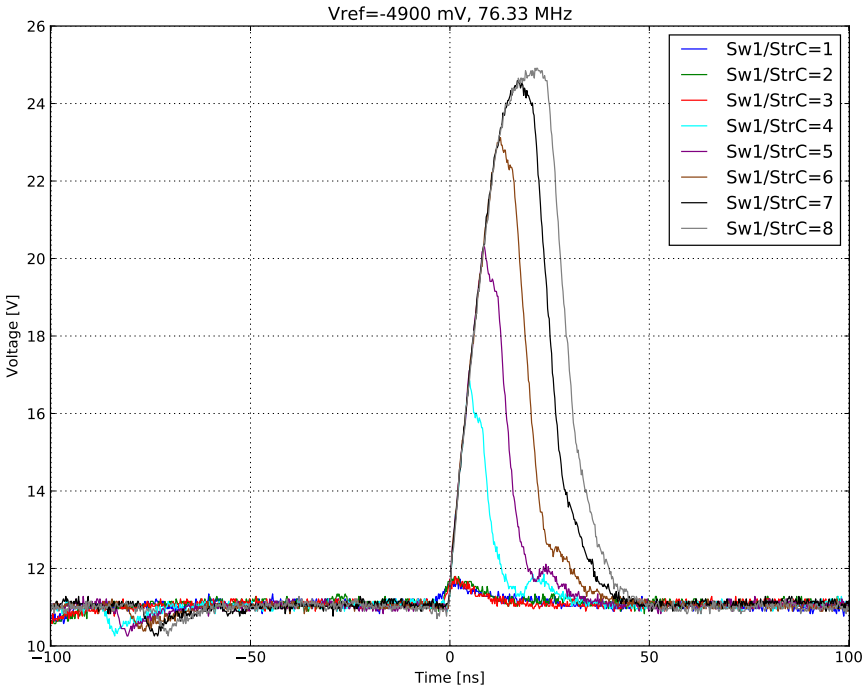
capacitance of the Clear routing determines the pulse shape. Applying the Clear pulse can be compared to charging (and discharging) a capacitor.
During the *Gated Mode* measurements (which are introduced in Sect. 6.12) it is observed that the Switcher that is mounted furthest away from the end-of-stave shows problems applying the Clear pulse, such that the Clear pulse is not applied properly: the rising and falling edges of the Clear pulse are rather flat and therefore the ClearOn voltage amplitude is not reached at the Switcher Clear outputs. According to the Switcher manual [147], the current consumption of the Switcher-Vref net should be 90 µA. However, as measurements show the power consumption of this net is approximately 30 mA. The metal on the module was designed to be quite narrow, causing a high ohmic resistance of approximately 172 Ω from the end-of-stave to the Switcher that is the furthest away from the end-of-stave. Consequently, a voltage drop of the required 1.8 V for the Switcher-Vref net leads to this problematic Switcher behavior, i.e., the level shifters within the Switcher (see [147] for more details) does not function properly. In order to fix this problem, the metal layout has been changed to decrease the ohmic resistance from 172 Ω to approximately 27 Ω. The old metal system is called PXD9-6 and the new system with the smaller resistance of the Switcher-Vref net is called PXD9-7. The module W31-OF1 (see Tab. 6.1) is equipped with the SwitcherBv2.0 and the new metal system resulting in steep rising and falling edges of the applied Clear pulses.
Furthermore, the Switcher-substrate voltage (−7 V) and the Switcher-Vref voltage (−4.9 V) of the Switchers are powered separately (see Sect. 4.8.9) unlike the shorting of Switcher-Vref with Switcher-DVDD and Switcher-substrate to digital ground. The resulting Clear pulses as function of the number of `Strobe Clear` ticks for the W31-OF1 module are shown in Fig. 6.41. The Source voltage is adjusted to 6 V. The difference of the Clear voltage amplitude for the various Switchers along the module (compare Fig. 6.41a and Fig. 6.41b) can be either due to the voltage drop along the balcony of the module or due to bad contact of the tiny needle of the probe contacting the copper pad.

Operation voltages

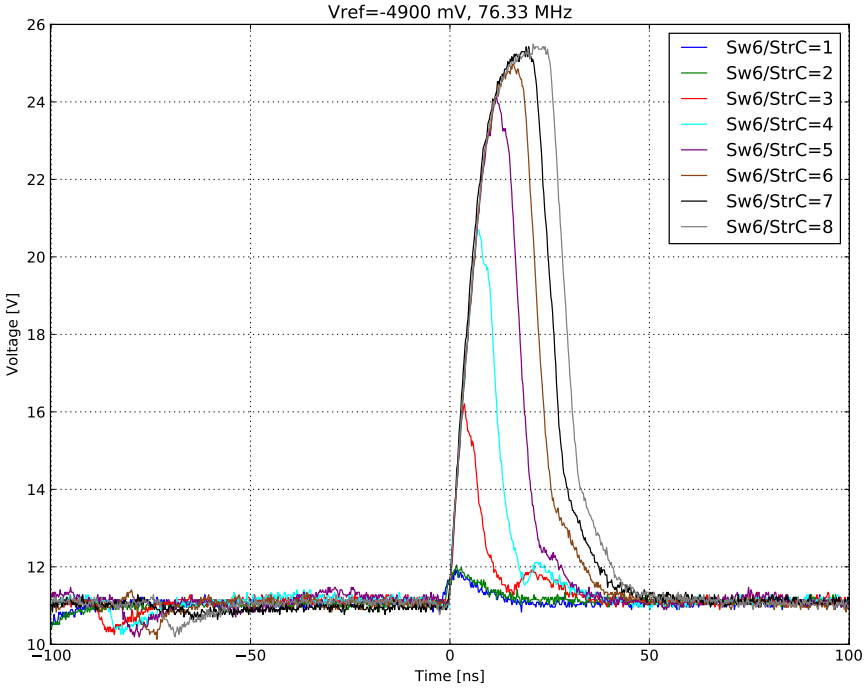
A sketch of the measurement for the Clear efficiency is shown in Fig. 6.42. The measurement is performed by shining a well collimated laser onto a single pixel in the matrix. Four consecutive frames are read out. The following timing variables are introduced:

$t_{\text{frame i}}$	Begin of the readout process of the i^{th} frame in rolling shutter mode.
t_{Laser}	The laser is switched on.
Δt_{Laser}	Duration of enabled laser pulse.
$t_{\text{pixel, i}}$	Pixel readout in frame i

The following procedure is used: The DEPFET matrix is read out continuously in the rolling shutter mode. The readout frequency for the entire matrix is 40.690 kHz (at GCK=62.5 MHz). The $\text{rows}_{\text{gate}}$ are enabled subsequently and the Clear pulse is applied. Once the trigger command is sent (which occurs every $\sim$ 10 s), four consecutive frames are recorded:



(a) Clear pulses of Switcher 1, which has the largest distance to the DCDs.



(b) Clear pulses of Switcher 6, which has the shortest distance to the DCDs.

Figure 6.41: Measured Clear pulses as function of the applied number of StrC ticks at the W31-OF1 module. Switcher 1 (a) has the largest distance to the DCDs while Switcher 6 (b) is located very close to the end-of-stave.

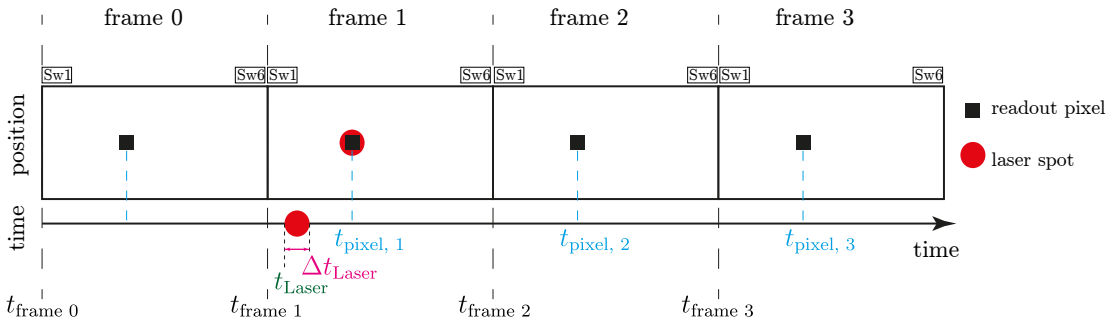


Figure 6.42: Sketch of the measurement of the Clear efficiency. A laser is triggered and shoots at a certain pixel before the pixel is read out. The signal in the consecutive frame is analyzed to study the efficiency of removing all electrons from the *internal Gate*.

- **Frame 0**: Pedestals are recorded and all pixels are cleared, i.e., no charge should be stored in the *internal Gate*.
- **Frame 1**: The laser is enabled before the pixel is read out in frame 1, i.e., $t_{\text{Laser}} + \Delta t_{\text{Laser}} < t_{\text{pixel, 1}}$. The laser signal is measured in frame 1 at $t_{\text{pixel, 1}}$, which is approximately 90 ADU. The Clear pulse is applied within the time interval $[t_{\text{pixel, 1}}, t_{\text{pixel, 1}} + 128\,\text{ns}]$.
- **Frame 2**: The same pixel is read out again. The signal difference between this frame and the pedestals yields the amount of charge that has not been removed during the Clear process in frame 1.
- **Frame 3**: The same pixel is read out again. The signal difference between this frame and the pedestals indicate how much charge is still stored in the *internal Gate* after clearing, i.e., performing the Clear process, twice.

The measurement is repeated multiple times and the averages of the pixel readouts are calculated. In order to understand the results, it is necessary to understand the principle of the Clear process shown in Fig. 4.5: the higher the ClearOn voltage, the larger the potential difference is between the *Clear implant* and the *internal Gate*. Thus, the higher the voltage, the more easily the electrons can drift from the *internal Gate* to the *Clear implant*. In addition, the Clear process is counteracted by a small potential barrier between the *internal Gate* and the *Clear implant*. A positive ClearGate voltage lowers this barrier. Therefore, the Clear process is improved for more positive ClearGate voltages.

All of the measurements are performed with enabled pedestal compression and analog common mode correction of the DCD. In addition, the common mode noise is calculated digitally and corrected. The Clear efficiency is studied as function of ClearOn and ClearGate operation voltages for two different pixel positions on the matrix (see Tab. 6.6 and Figs. 6.43 to 6.45).
The pixel that is connected to DCD 4 and Switcher 1 shows a better Clear behavior (Fig. 6.43) compared to the pixel connected to DCD 1 and Switcher 6 (Fig. 6.44). This is due to voltage drops of the ClearOn along the metal routing from the Switcher to the *Clear implant* and flat edges of the Clear pulse.

Table 6.6: Overview of the pixels for which the Clear efficiency is studied.

row_{geo}	col_{geo}	DCD	Switcher	comment
74	215	4	1	"best region"
753	10	1	6	"worst region"

In addition, the signal height, (i.e., the number of electrons remaining in the *internal Gate*) decreases after the Clear pulse is applied twice, as shown in Fig. 6.45. However, for the operation in Belle II, all of the electrons stored in the *internal Gate* need to be cleared within one Clear cycle. This corresponds to the dark blue regions, where the signal is approximately 0 ADU. More studies regarding the different behavior of the Switchers are presented in Sect. 6.12.
As shown in to Fig. 6.43 and Fig. 6.44, the operating voltages for a complete reset of the detector (complete Clear) must be chosen above the diagonal defined by (ClearGate=−1.5 V, ClearOn=19.5 V) and (ClearGate=0 V, ClearOn=15.5 V). Additional measurements without analog common mode correction and without offsets are presented in app. C.5.

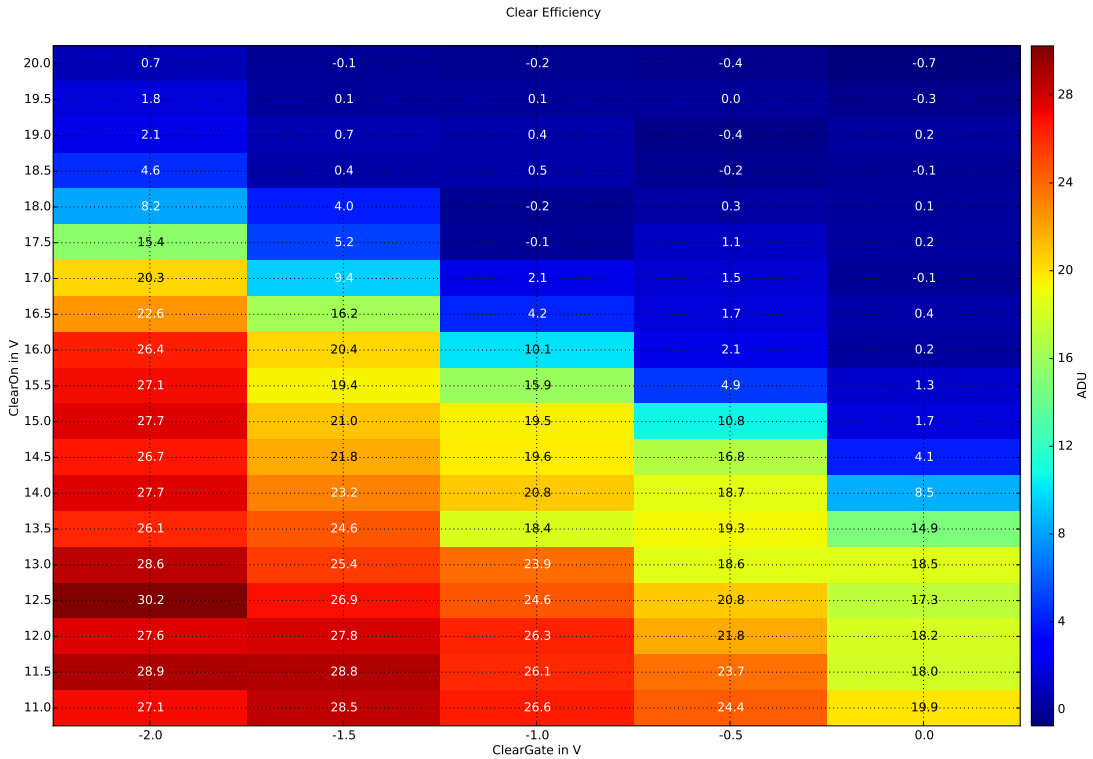


Figure 6.43: Pixel: row_{geo}=74, col_{geo}=215: Signal of pixels after being cleared once, corresponding to frame 2. All electrons are completely removed from the *internal Gate* where the signal is approximately 0 ADU.

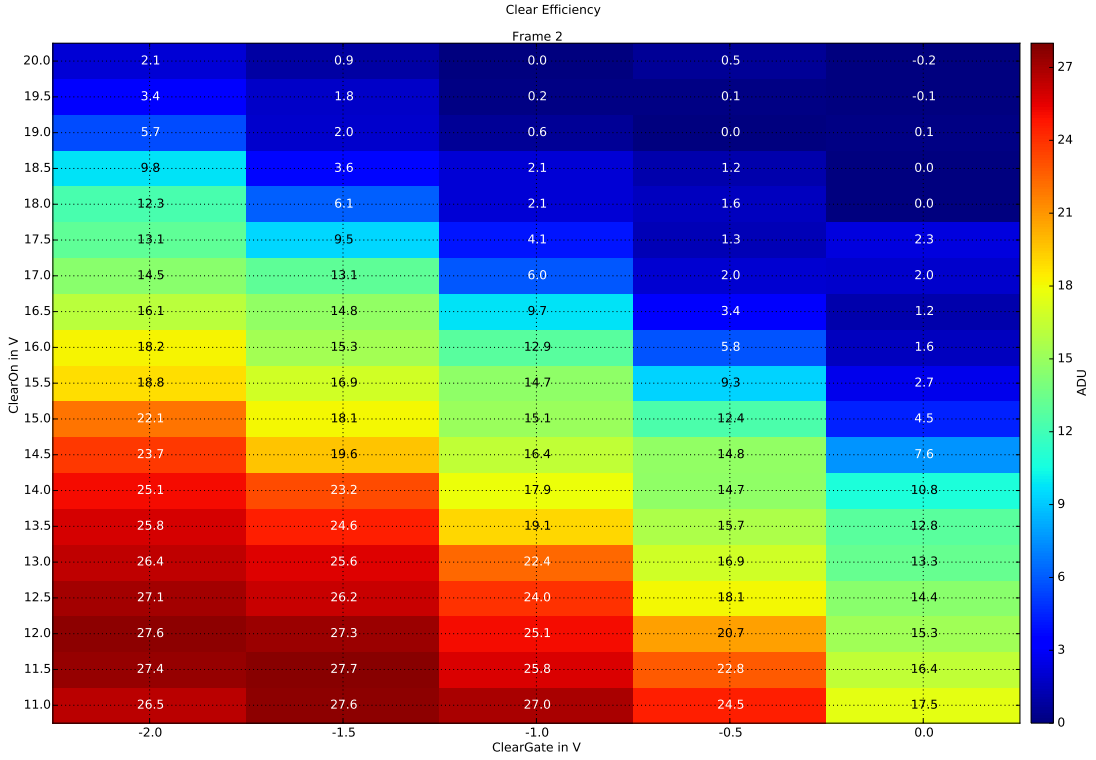


Figure 6.44: Pixel: row_{geo}=753, col_{geo}=10: Signal of pixels after being cleared once, corresponding to frame 2.

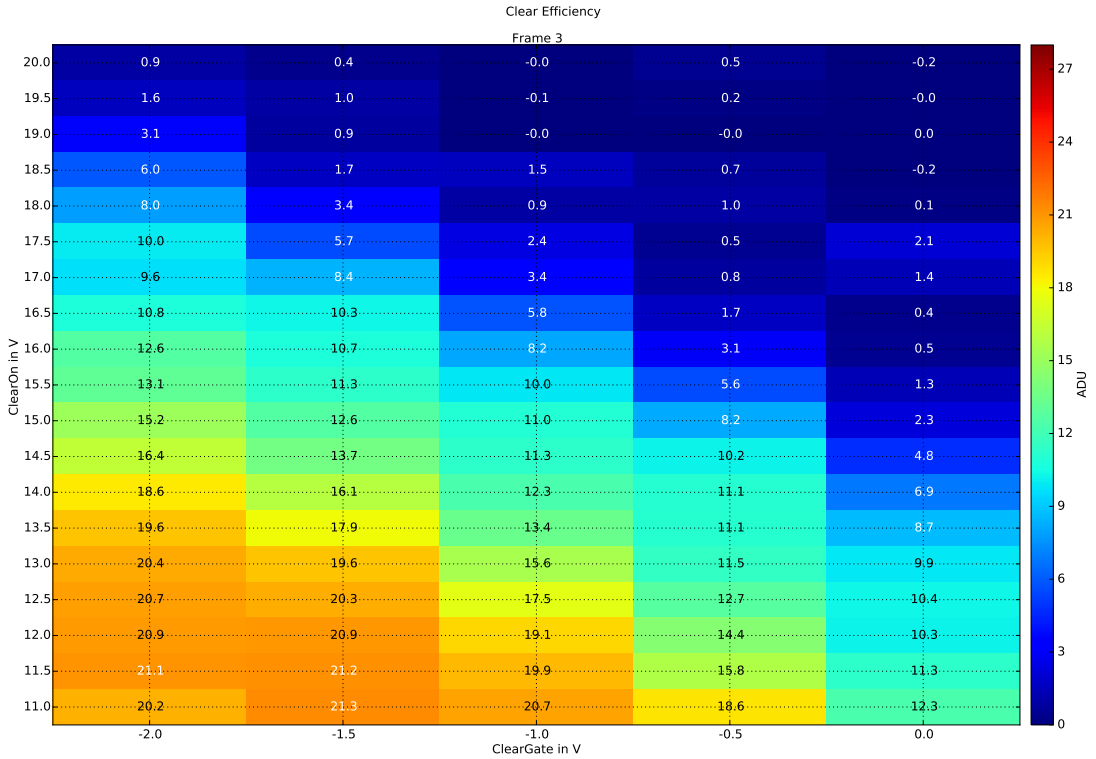


Figure 6.45: Pixel: row_{geo}=753, col_{geo}=10: Signal of pixels after being cleared twice, corresponding to frame 3.

6.11 Determination of Optimal Operation Voltages

The operating voltages are optimized by analyzing the response of the DEPFET matrix to a radioactive Cd-109 source. Averaging the spectrum, an emitted photon creates approximately 6300 electron-hole pairs in the sensitive silicon[12]. This corresponds approximately to a MIP.
Each DCD has been optimized previously in terms of INL, DNL and missing codes and has dedicated settings resulting in different gains and different offsets (and thus different dynamic ranges). For this reason, the calibration, i.e., the voltage sweeps are analyzed for each DCD individually. The nominal voltages listed in Tab. 6.7 are applied and varied individually.

Table 6.7: Default operating voltage values relative to Source (Source is referenced to analog ground, see Sect. 6.2).

Voltage	Value
ClearOn	20 V
ClearOff	5 V
GateOn	−2.5 V
GateOff	3 V
Source	7 V
ClearGate	0 V
HighVoltage	−70 V
Drift	−5 V
Guard	−5 V
Bulk	10 V

The ~ 20 keV γ-rays from the collimated Cd-109 source are primarily shot on the DEPFET pixels that are controlled DCD 1 and DCD 2. Due to many transmission errors in the communication between DCD 4 and DHP 4, only a small fraction of the overall signal can be analyzed. The analog common mode correction and the pedestal correction are enabled for all measurements except for the GateOn voltage scan. For each voltage sweep, pedestal frames are recorded and the noise is calculated. The internal amplification, g_q, of the DEPFET is calculated as (see Sect. 4.5.1):

$$\begin{aligned} g_\mathrm{q} &= \frac{\mu_\mathrm{fit}}{\langle E_{\text{Cd-109}} \rangle} \cdot \text{DCD gain} \cdot \langle E_{eh} \rangle \\ [g_\mathrm{q}] &= \frac{\text{ADU}}{\text{eV}} \cdot \frac{\text{nA}}{\text{ADU}} \cdot \frac{\text{eV}}{e^-} = \frac{\text{nA}}{e^-} \end{aligned} \tag{6.11.1}$$

where μ_fit denotes the mean value of the Gaussian fit of the signal distribution and $\langle E_{eh} \rangle = 3.64\,\text{eV}$ is the average energy to create an electron-hole pair in silicon.

[12] The weighted averaged energy of the emission lines 22.1 keV and 25.0 keV is assumed, i.e., $\langle E_{\text{Cd-109}} \rangle = 22.91\,\text{keV}$

A short overview of the presented voltage scans in this section as follows:
First, the GateOn voltage is varied, which has a direct impact on the internal amplification and consequently the signal-to-noise ratio. Next, the ClearOff voltage is varied to determine the threshold for back-injection. To study the depletion and the impact on electrons drifting through the silicon, the HighVoltage is scanned. The charge collection and the efficiency is studied as a function of the Drift voltage. Next, the Drift voltage and the ClearOff voltage are varied in a two-dimensional scan. Finally, the ClearGate voltage and the ClearOff voltage are stepped through.

GateOn scan

The GateOn voltage is varied, keeping all the other voltages constant. This voltage has a quadratic influence on the Drain current (see Sect. 4.5.1). The lower the voltage becomes the larger is the internal amplification, g_q. The GateOn voltage is swept between $-2.5\,\mathrm{V}$ and $-0.5\,\mathrm{V}$ in steps of 500 mV. For these measurements, the pedestal compression has been disabled since the pedestal spread (and the signal) are within the dynamic range for more positive GateOn voltages and the offset compensation would not affect the study of the internal amplification. Furthermore, the DCDs are tuned for each GateOn voltage individually. For this reason, the mean value and the signal-to-noise ratio (SNR) is slightly different compared to the voltage scans presented in the next sections. The SNRs for the four different DCDs as function of the GateOn voltage are shown in Fig. 6.46. The SNR varies between ~ 20 (for GateOn$=-0.5\,\mathrm{V}$) and ~ 37 (for GateOn$=-2.5\,\mathrm{V}$). The internal amplification is between $\sim 230\,\mathrm{pA}/e^-$ (for GateOn$=-0.5\,\mathrm{V}$) and $\sim 500\,\mathrm{pA}/e^-$ (for GateOn$=-2.5\,\mathrm{V}$). The resulting distributions and corresponding Gaussian fits are shown in app. C.7. The parameters and results (SNR and g_m) are listed in app. C.7. Due to transmission errors and low statistics, the calibration values of DCD 4 are not reliable.

Clear scan

There are two voltages applied at the *Clear implant*: The ClearOff voltage for the normal charge collection mode and the ClearOn voltage for removing the accumulated electrons from the *internal Gate*. Using a very low positive voltage for ClearOff (relative to the Source voltage), which is approximately $+1\,\mathrm{V}$ and applying a ClearGate voltage of $0\,\mathrm{V}$, back-injection occurs for some of the DEPFETs (see Sect. 4.4.2 and Fig. 4.5). This process is already clearly visible in the pedestal values (see Fig. 6.47). It is also the reason for the decreased number of counts for less positive ClearOff voltages. The distributions of the signals in terms of different ClearOff voltages are shown in Fig. 6.48. The values are listed in app. C.7.
According to this measurement, any ClearOff value between $1.5\,\mathrm{V}$–$5\,\mathrm{V}$ can be chosen. A small side peak of approximately 10 ADU is visible for all four DCDs. Since the radioactive source is encapsulated in a tungsten supporting structure, the peak originates from the tungsten, which has L-level emission lines between $8.40\,\mathrm{keV}$ and $11.29\,\mathrm{keV}$ [199].

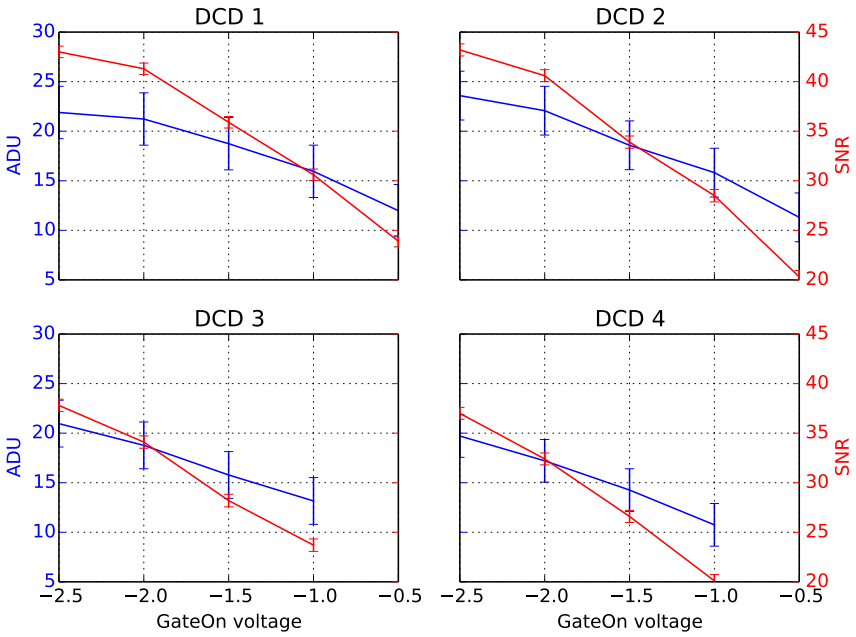


Figure 6.46: The mean values in ADU (blue) and the signal to noise ratios (red) for the four DCDs. DCD 3 and DCD 4 have lower gain (and thus lower signal-to-noise ratio) due to the optimized ADC settings of the DCD.

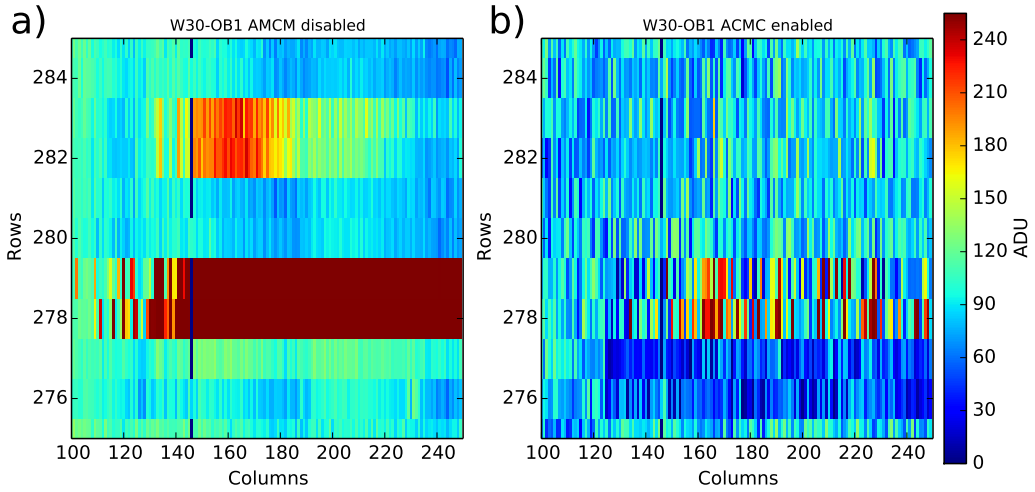


Figure 6.47: The back-injection process is visible as increased pedestal values for ClearOff=+1 V and ClearGate=0 V.
a) Analog common mode correction and pedestal compression are disabled. Some pixels in row_{geo} 278, 279, 282 and 283 show back-injection. b) Analog common mode correction and pedestal compression are enabled. The increased pedestal values are reduced by the analog common mode correction. For this reason, the pedestal values are very low. No signal can be detected for those pixels in either case because the *internal Gates* are full.

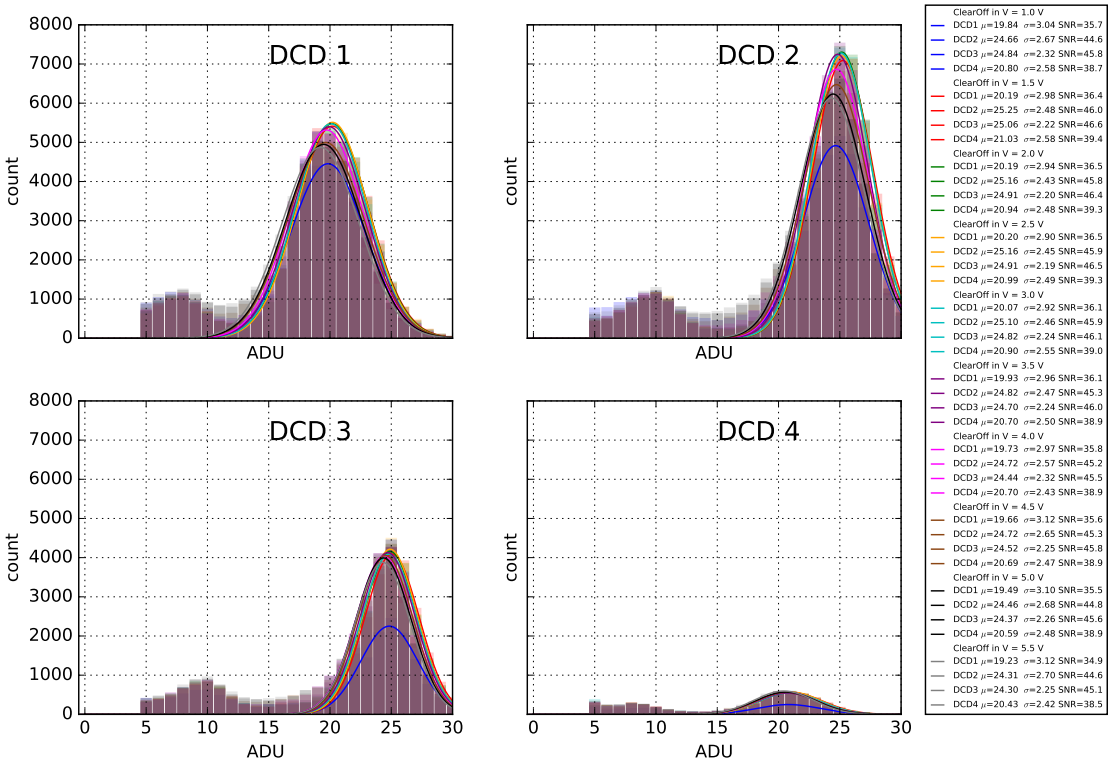


Figure 6.48: The signal distribution as function of the ClearOff voltage of the four DCDs. The parameters are summarized in app. C.7.

HighVoltage Scan

The HighVoltage, responsible for the depletion of the silicon bulk, is swept from −60 V to −80 V in steps of 2 V. In addition, the ClearOff voltage is varied. The SNR for different voltage combinations are shown in Fig. 6.49.

For more positive bias voltages of approximately −60 V, the bulk is not fully depleted, resulting in a lower SNR. The electrons, generated in the non-depleted region, cannot drift freely through the bulk to the *internal Gate*. When the voltage is decreased, the SNR increases. The maximum SNR $\simeq$ 40–50, depending on the DCD, is reached at approximately −70 V. For even more negative voltages, the potential minimum decreases, as already explained in Sect. 4.4.2. As a consequence, the SNR decreases. The optimal depletion voltage is approximately −70 V.

The combination of ClearOff and HighVoltage determines the potential distribution below the *Clear implant* (see Fig. 4.6). The more positive the ClearOff voltage, the smaller the potential barrier is that prevents the electrons to drift to the *Clear region*. For more positive ClearOff voltages ($\sim$ 5 V), a larger fraction of the created electrons in the silicon bulk can drift directly (i.e., they are not held back by this potential barrier) to the *Clear region* and fewer electrons accumulate in the *internal Gate*. Thus, the Drain current is lower, resulting in less signal and lower SNR.

As already shown in the pedestal distribution (Fig. 6.25), ring-like structures are visible across the entire matrix. This is most likely due to variable doping concentrations. The concentration has a direct impact on the required HighVoltage to deplete the bulk and to form the potential minimum (i.e., the *internal Gate*). Only one common HighVoltage can be applied for all pixels. For that reason, the ClearOff voltage should be chosen in a way that the operation window (i.e., high SNR for variable HighVoltages) is as large as possible. The lower limit of ClearOff is given by back-injection ($> 1\,\mathrm{V}$). This results in an optimal ClearOff voltage of approximately $2\,\mathrm{V}$.

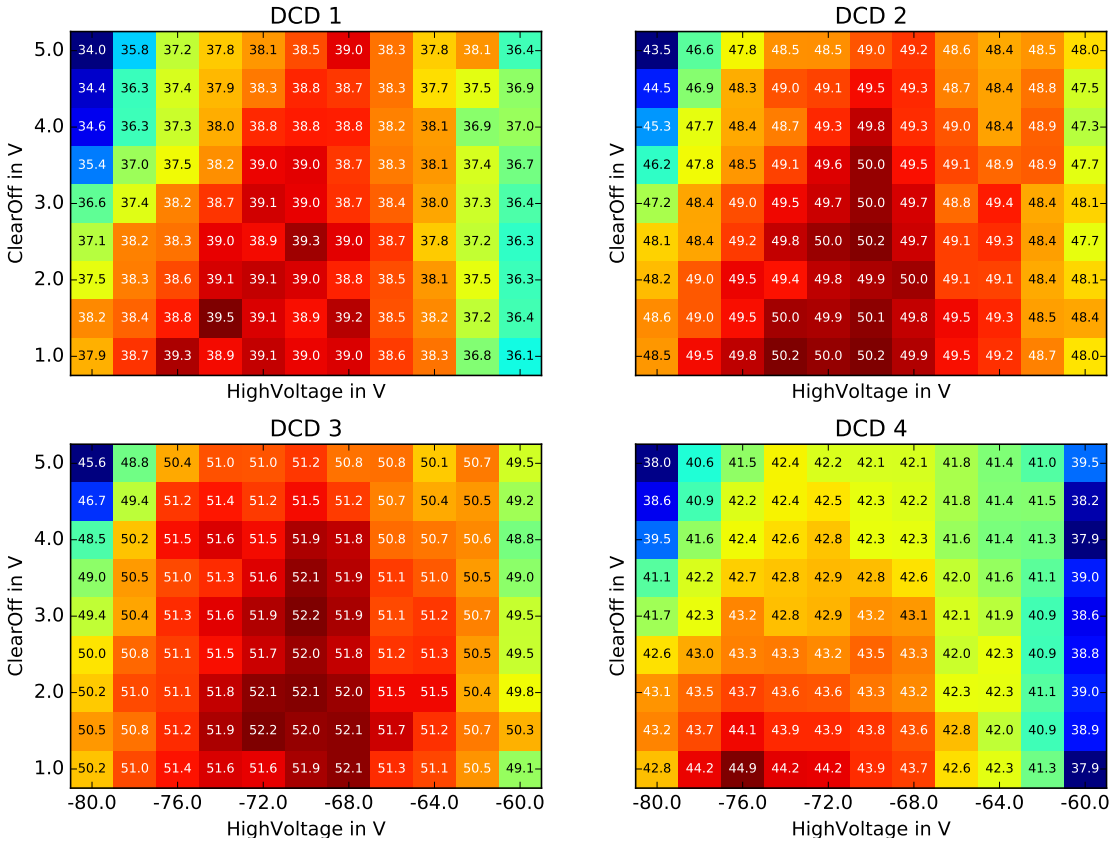


Figure 6.49: The signal-to-noise ratio is plotted as function of ClearOff and HighVoltage. The optimal HighVoltage is approximately $-70\,\mathrm{V}$ and the preferred ClearOff voltage is approximately $2\,\mathrm{V}$ for a large operation window with high SNR.

Drift scan

The Drift voltage is swept from $-3\,\mathrm{V}$ to $-7\,\mathrm{V}$ in steps of $500\,\mathrm{mV}$. The amount of collected electrons decreases for more positive Drift voltages. The mean values of the Gaussian fits and the number of hits do not change for very negative Drift voltages, i.e., in the range from $-7\,\mathrm{V}$ to $-5.5\,\mathrm{V}$. The signal distributions and the parameters for multiple different Drift voltages are shown in app. C.7. For more positive Drift voltages, some of the electrons are pushed below the *ClearGate structure*, i.e., they are trapped. An additional implant (below the *ClearGate*

structure) prevents the electrons from drifting to the boundary of silicon and silicon oxide. If the electrons were to reach the interface (Si/SiO_2) they would get "lost." The largest fraction of these trapped electrons are expected to reach the *internal Gate* regardless. However, the lateral drift fields are much weaker in this region such that the electrons tend to diffuse instead of drifting. When the electrons move to the *internal Gate*, they can be trapped by any potential minima, which could be created by the rough edges of the polysilicon *ClearGate structure*. As a consequence, the electrons drift to the *Clear region*. Furthermore, the increase of the peak width is more conspicuous than the decrease of the counts (amplitude). Thus, the efficiency does not suffer from this effect.

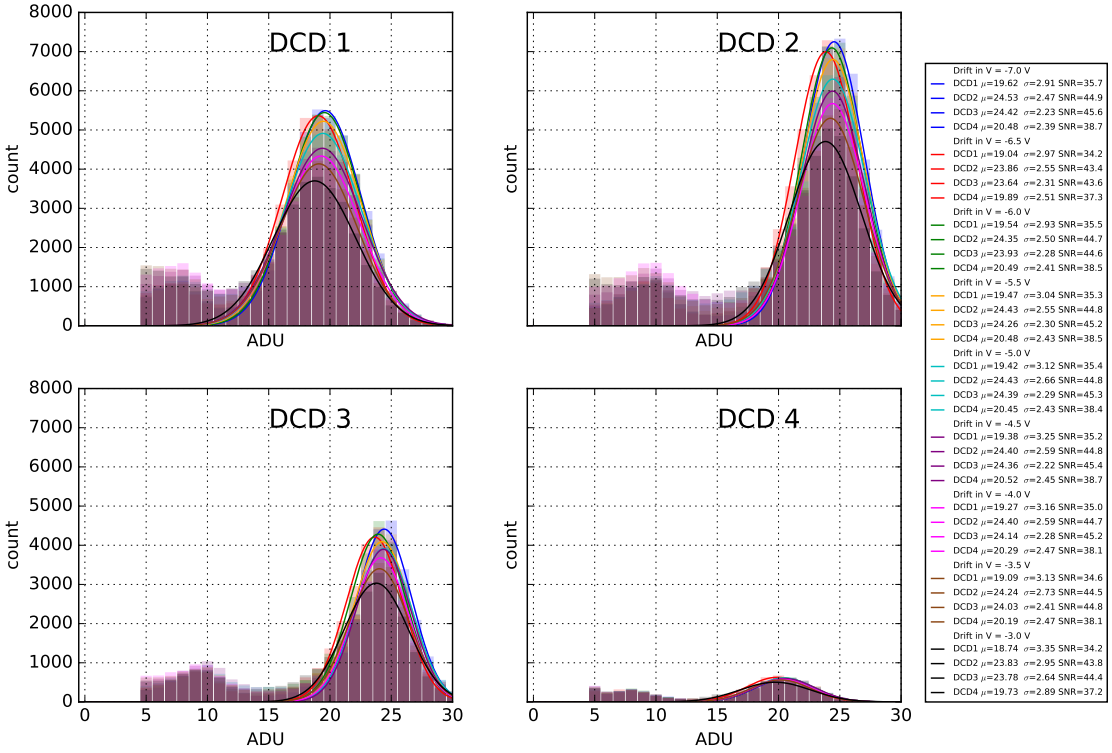


Figure 6.50: The signal distribution as function of the Drift voltage of the four DCDs. The parameters are summarized in app. C.7.

Drift (and ClearOff)

The Drift and ClearOff voltages are swept in a two-dimensional scan. The ClearOff voltage is swept from 1 V to 5 V in steps of 500 mV. The Drift voltage is swept between −7 V and −3 V in steps of 500 mV. The SNRs for different combinations of Drift and ClearOff are shown in Fig. 6.51. For Drift voltages closer to 0 V, the SNR decreases since electrons accumulate in the potential minimum below the *ClearGate structure*. In addition, a large positive ClearOff voltage prevents the charge collection. The electrons in the potential well below the *ClearGate structure* tend to drift to the *Clear implant* instead of moving to the *internal Gate*. Furthermore, the potential barrier below the deep p well implant, which is located below the *Clear implant*, is decreased as explained in Sect. 4.4.2. In

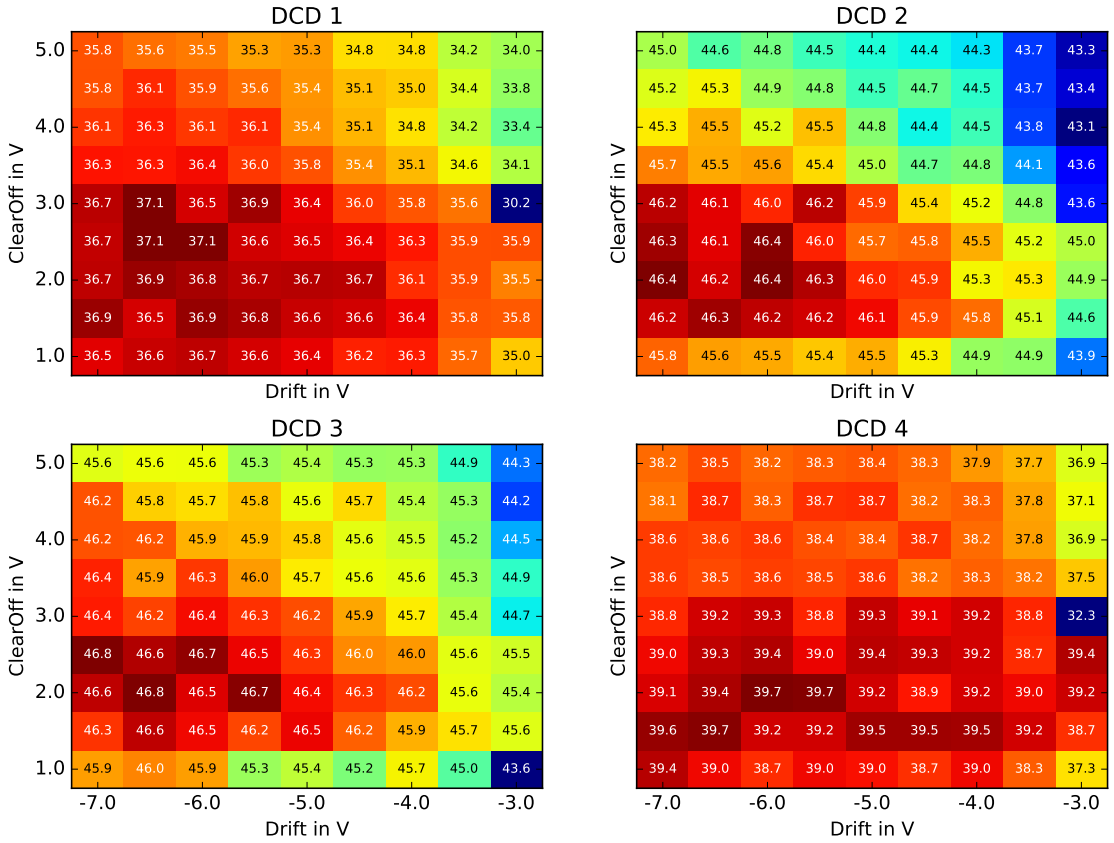


Figure 6.51: The signal-to-noise ratio is plotted as function of ClearOff and Drift. The optimal Drift voltage is $\leq -5.5\,\mathrm{V}$. The ClearOff is set to $2\,\mathrm{V}$.

conclusion, more negative Drift voltages ($\leq -5.5\,\mathrm{V}$) and less positive ClearOff voltages ($\sim 2\,\mathrm{V}$) should be used according to these measurements.

ClearGate (and ClearOff)

The ClearGate and ClearOff voltages are varied. The more positive the ClearGate voltage, the lower the barrier is between the *internal Gate* and the *Clear implant*. Thus, the more positive the ClearGate voltage, the easier can electrons drift to the *Clear region*. As mentioned above, large positive ClearOff voltages diminish the potential barrier at the deep p implant (below the *Clear region*). The SNR for different combinations of ClearGate and ClearOff voltages are shown in Fig. 6.52. The optimal ClearOff voltage is determined above (see HighVoltage scan), i.e., approximately $2\,\mathrm{V}$.
In addition, for low ClearOff voltages, the range of ClearGate voltages is large to obtain high SNR. This is favorable, in particular if the ClearGate potential will change inhomogeneously along the matrix due to radiation damages. Furthermore, the optimal ClearGate voltage is determined by the Clear efficiency (see Sect. 6.10) and by the *Gated Mode* operation.

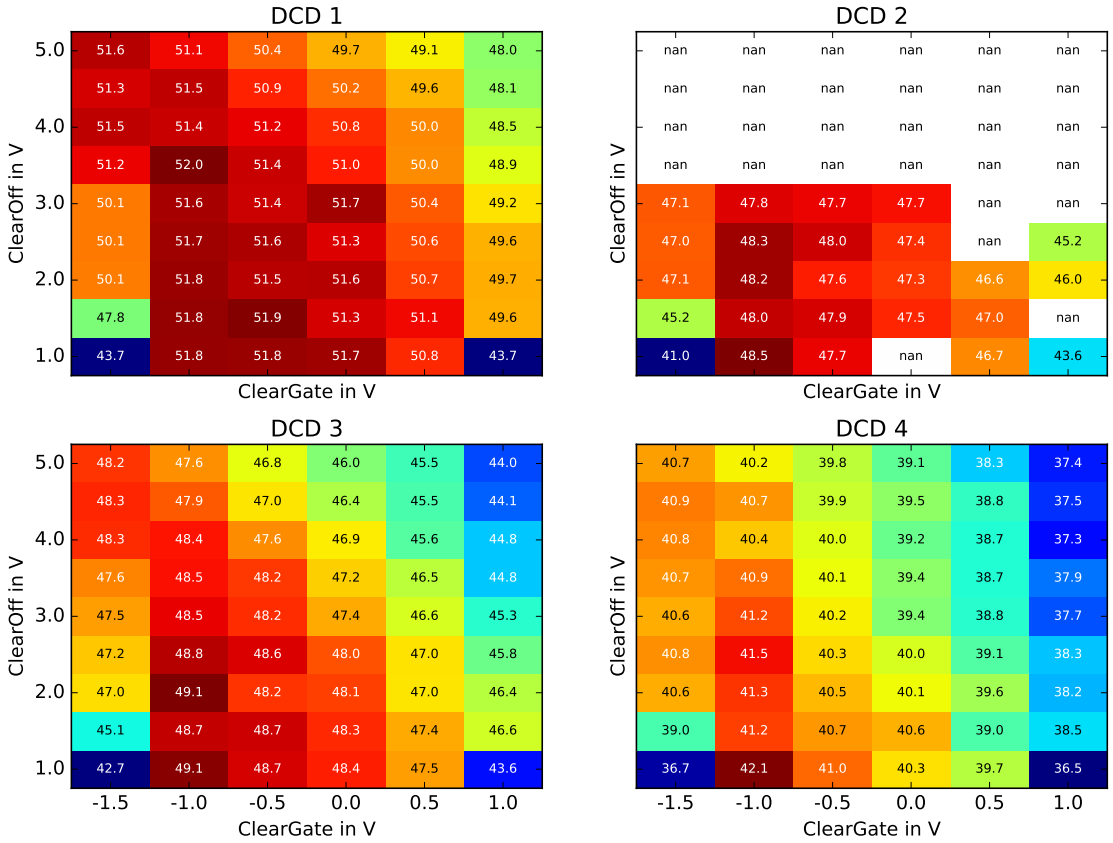


Figure 6.52: The signal-to-noise ratio is plotted as function of ClearGate and ClearOff. The optimal ClearGate voltage needs to be between 0 V and −1 V.

Conclusion

The optimal operation voltages for ClearOff, GateOn, HighVoltage and Drift are determined by source measurements and the Clear efficiency. They are summarized in Tab. 6.8. The guard and the bulk only affect the pixels at the boundary. The voltages chosen in Tab. 6.7 are suitable for proper operation. The pixels at the boundary are protected from electrons of the silicon module, which could unexpectedly drift into the *internal Gates* of the DEPFET pixels.

The ClearOn, ClearGate and GateOff voltages are determined in the next section, where the operation of the Gated Mode is studied. The internal amplification of the DEPFETs of the pilot run module is approximately 500 pA/e^-.

6.12 Gated Mode

In this section the *Gated Mode* (GM) is motivated and the concept of the PXD operation is introduced. Additionally, measurements of the pilot run modules W30-OB1 and W31-OF1 in the GM operation are presented.

Table 6.8: Recommended operation voltages after studies with the radioactive source. The ClearGate, ClearOn and GateOff voltages are studied in Sect. 6.12

Voltage	Value	Voltage	Value
Source	6 V	ClearGate	−0.5 V
ClearOff	2 V	ClearOn	20 V
GateOn	−2.5 V	GateOff	3 V
HighVoltage	−70 V	Drift	≤ −5 V
Guard	−5 V	Bulk	10 V

6.12.1 Physical Motivation

The SuperKEKB accelerator complex foresees electron and positron top-up injection frequencies of 25 Hz each, resulting in a total injection frequency of 50 Hz [85]. Thus, new bunches enter the storage rings every 20 ms. Usually, two bunches are injected 100 ns apart. The bunches have a revolution time of about 10 µs, traveling through the storage ring with a circumference of 3016.315 m. The spacing of two consecutive bunches is approximately 1.2 m [80, 95, 103, 104]. A sketch of the injection scheme, damping time and the filled-up bunches is shown in Fig. 3.9. The Liouville theorem states that two bunches, daughter (new) and mother (old), cannot be injected into the same phase space volume. Consequently, it is necessary to inject the daughter bunch into a different phase space element, typically offset transversely in the accelerator plane. Then the daughter bunch cools slowly into the mother bunch by emitting synchrotron radiation. The damping time is assumed to be approximately 4 ms, which was the value observed at KEKB.
During this "bunch stabilization time," particles get lost since they are not yet moving on the design orbit. These particles are denoted as *noisy particles*. Near the interaction point, the noisy particles are likely to hit the beam pipe and the created secondary particles add unwanted signals to the Belle II detector (called *background*). While other sub-detectors stop their readout process (for approximately 1 µs), the charge collection mode of the PXD cannot be stopped. This results in a huge amount of background.
In summary, two daughter bunches, out of 2500 bunches in total, are injected every 20 ms to top up the machine current with a damping time of about 4 ms. As a consequence, only 16 ms are available to detect clean events.

Tremendous effort has been spent to overcome the 20 % dead time in order to make the detector insensitive for short time periods (on the order of a few hundred nano seconds) when the noisy bunches are passing. The plan is to operate the pixels in the *Gated Mode*, i.e., in an insensitive blind mode.

Table 6.9: Overview of the different states; (enabled, disabled) Gate and the two Clear mechanisms (real and suppressed Clear mechanism). The nominal voltages are denoted by GateOff, GateOn, ClearOff, ClearOn and ClearGate.

Contact / Mode	Collection	Readout	Clear	Suppressed Clear
Gate voltage	GateOff	GateOn	GateOn	GateOff
Clear voltage	ClearOff	ClearOff	ClearOn	ClearOn
ClearGate volt.	ClearGate	ClearGate	>ClearGate	<ClearGate

6.12.2 Concept of the Gated Mode for the PXD

The concept of the GM is the application of a large positive voltage at the *Clear implants* (ClearOn voltage) while the MOSFETs of the DEPFET are disabled (GateOff voltage). This has two effects:

- The potential within the bulk changes such that newly generated electrons in the active silicon bulk do not accumulate in the *internal Gate*. Instead, they drift directly to the more attractive *Clear implant*.
- When the MOSFET is disabled, there is no conductive channel with holes between the *Source* and the *Drain* implants. Consequently, the *internal Gate* is not shielded from the *external Gate*. As a result, the potential minimum (*internal Gate*) is shifted when the ClearOn voltage is applied due to the strong capacitive coupling between the *internal Gate* and the *external Gate*. When the barrier between the *internal Gate* and the *Clear implant* (adjusted by the ClearGate voltage) is increased, the electrons stored in the *internal Gate* cannot overcome this barrier and remain there. This mechanism is called *suppressed clear*. The potential distribution between the *Clear implant* and the *internal Gate* is shown in Fig. 4.5 for the real Clear and the suppressed Clear mechanisms.
  Since the *ClearGate structure* and the *Clear implant* are capacitively coupled, it is necessary to preserve the potential barrier between the *internal Gate* and the *Clear implant* by selecting an appropriate ClearGate voltage [136]. This ensures that the signal charged stored in the *internal Gate* is maintained during the GM operation.

In order to support the suppressed Clear and real Clear mechanisms on a module, additional Switcher control lines and outputs (and more space) would be required. However, these are not available. An overview of the applied voltages (GateOff, GateOn, ClearOff, ClearOn and ClearGate) for the different operation modes (Collection, Readout, Clear, Suppressed Clear which is the same as the GM) are summarized in Tab. 6.9 (see also Fig. 4.5). Three-dimensional simulations are performed to study the behavior of the DEPFET pixel during the suppressed Clear mechanism [136, 141, 142]. The cross-sections of the DEPFET, illustrating the iso-potential lines and electron trajectories, are shown in Fig. 6.53 and Fig. 6.54. (The potential distribution and the drift trajectories of electrons for the real Clear mechanism are shown in Fig. 4.11 and Fig. 4.12). It can be clearly seen that generated electrons within the silicon bulk are "guided" to the *Clear implant*. In

contrast to the charge collection process, the electrons do not accumulate in the *internal Gate*. The saddle point (small potential barrier) beneath the *ClearGate structure*, between the *internal Gate* and the *Clear implant*, is almost 2 V. This barrier, as previously mentioned, can be shifted by changing the ClearGate and GateOff voltage (from 3 V to 5–6 V).

Three-dimensional simulations offer the major advantage of indicating the influence of the *Source* and *Drain implants* on the electric field distribution within the depleted silicon bulk. In addition, they offer more precise predictions about the charge collection, the real Clear and the suppressed Clear processes.

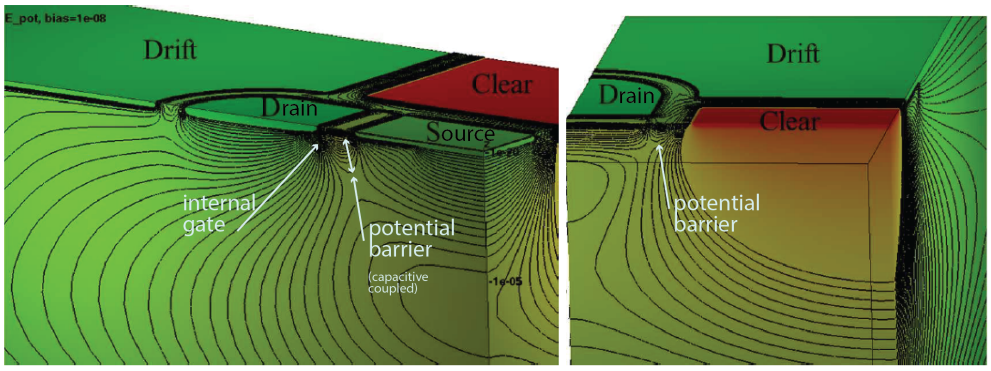


Figure 6.53: Suppressed Clear / Gated Mode operation: Potential distribution around the *internal Gate* for $V_{\mathrm{ClearOn}} = 19\mathrm{V}$, $V_{\mathrm{GateOff}} = 3\mathrm{V}$ [136, 141, 142].

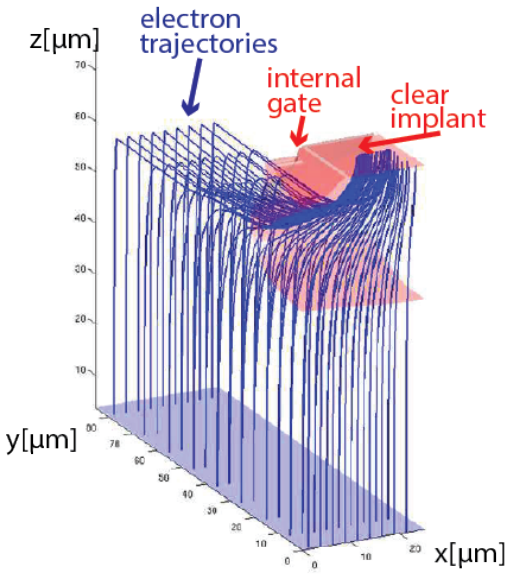


Figure 6.54: Suppressed Clear / Gated Mode operation: Electron-hole pairs are created at the backside of the DEPFET. The electron trajectories all end in the *Clear implant*. The *internal Gate* is shielded [136, 141, 142].

Implementing the GM operation to the PXD, it is necessary to take into account the system aspects related to the high currents (in particular for ClearOn and Source currents) and cross talk [200]. The Switchers that control the Clear and Gate voltages for the DEPFETs and the DHP have to support this blind-sequence. The details are introduced in the next section.

6.12.3 ASIC control

The DHH is synchronized by the Belle II trigger and time distribution system (B2TT) [164]. The information about noisy bunches passing the Belle II detector is provided by the B2TT. The *VETO* signal, i.e., the command to switch into the GM, is sent to the DHC.
The DHP has two different memory sections for storing two Switcher sequences. Each consists of 512 128-bit memory words. Each word is divided into four subgroups, 32 bits for each: `SerIn`, `Strobe Clear` (`StrC`), `Strobe Gate` (`StrG`) and `Clock`. The 32 control bits are called *ticks*. Each tick is applied for $T = 1/(4 \cdot \mathrm{GCK})$ (for GCK=62.5 MHz, one tick corresponds to 4 ns, for GCK=76.33 MHz, one tick corresponds to 3.27 ns). The Switcher control for the normal operation (rolling shutter mode), where only the first section of the DHP memory is used, is explained in detail in Sect. 4.8.1. Only the Switcher operation for the GM operation and the switching between the two sequences are discussed here.

To control the entire matrix for the normal readout, 192 out of the 512 available words need to be programmed. The address pointer "jumps" from the data word i to the next word $(i + 1)$ every 32 ticks, i.e., every 105 ns (using a GCK of 76.33 MHz). The pointer is reset to the first memory location when the state machine reset signal (generated by the DHE) is received at the DHP. Alternatively, the number of memory words that should be executed can be set individually in the DHP settings[13].
A sketch of the transition between the two Switcher memory sections is shown in Fig. 6.55 and explained in as follows. The matrix is read out in the rolling shutter mode until word k, which corresponds to $\mathrm{row}_{\mathrm{gate}}$ k. When the control signals of the 32 ticks of the word k are sent, the VETO signal is received at the DHP. The ASIC finishes sending the control signals stored in this word k and jumps to the second Switcher memory, i.e., to memory word 512. It continues by sending the sequence stored in the second section of the programmed Switcher sequence as long as the VETO signal is applied. After releasing the VETO command, the pointer jumps back to the Switcher memory section one. Assuming the VETO command is applied for three Gate rows ($\mathrm{rows}_{\mathrm{gate}}$), it jumps back to the address $k + 4$.
In the second section of the Switcher memory storage, the control signals are only sent during the GM operation. There is one exception: the sequence for the `SerIn` signal (gray in Fig. 6.55) is always read from Switcher memory section 1, although the GM sequence from section 2 is sent (`StrC`, `StrG`, `Clock`). This is done to keep the synchronization with the rolling shutter mode (since the `SerIn` signal is sent by the DHP only once per frame). In the latest version of the DHP (DHP1.2) it

[13] Using the register to set the number of data words for the Switcher allows reading out small matrices multiple times for a single trigger.

is possible to select whether the SerIn should be used from memory section 1 or section 2. However, this configuration is done via JTAG, which is slow (on the order of few micro seconds). Hence, this option is not suited for the operation in the Belle II experiment since the switching mechanism (for the SerIn signal) it is much too slow: the frame readout time is 20 µs, while the processing of the data in the DHE to be written in the DHPs is already estimated as 200 µs [161]. Consequently, the SerIn signal cannot be read from the second Switcher memory for only a single frame.

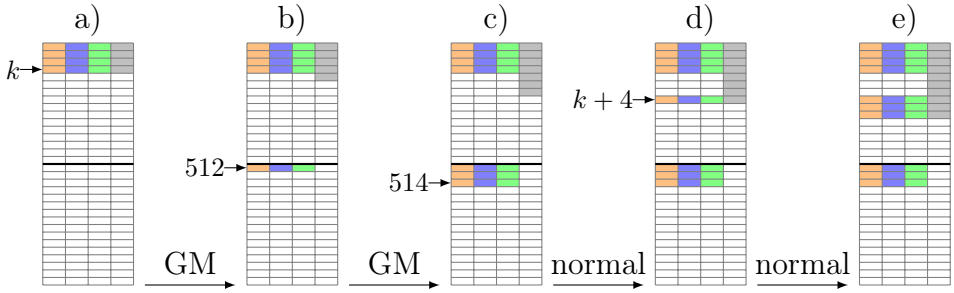


Figure 6.55: Sketch of the Switcher memory sequences for increasing time from left to right. Each row represents a 128-bit data word, consisting of the Clock (orange), StrG (blue), StrC (green) and SerIn (gray). The entire DHP Switcher memory is divided into two sections (0–511 and 512–1023, see text). The normal operation is performed until word k (a). The GM operation is performed between $k + 1$ and $k + 3$ (b-c). Afterwards, the normal sequence is resumed (d-e). The SerIn is always read from the first memory section.

6.12.4 Switcher sequence

The Switcher allows two different modi of the GM operation: The *GM without readout* and the *GM with readout*. The two different options with their associated (dis)advantages are discussed in this section.

Gated Mode without readout

The GM without readout is initiated by stopping the Switcher Clock, i.e., stopping the rolling shutter, StrC is *high* and StrG is toggling [147]. When enabling the GM, all Clear output drivers apply the ClearOn potential except the active Gate output driver, i.e., the active Gate row when the GM is enabled[14]. Thus, these DEPFET pixels which are connected to this row_{gate} are not shielded and electrons can be collected in the *internal Gates*. The control signals and the corresponding output drivers for Clear and Gate are shown in Fig. 6.56. Eight falling edges of StrG are required for a GM cycle [147]. The Switcher changes back to normal operation at the next falling edge of StrG when the StrC is *low*.

[14] Otherwise the charge would be removed since this scenario corresponds to the real Clear mechanism

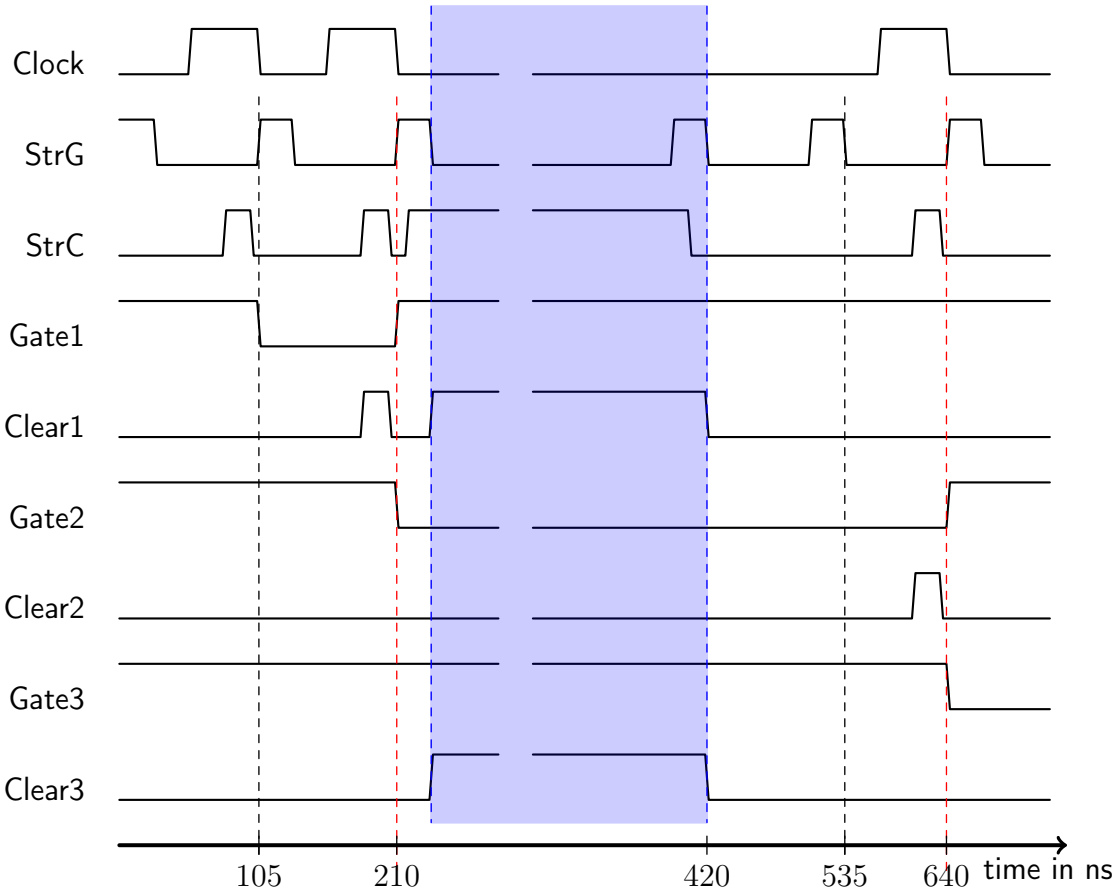


Figure 6.56: GM Switcher sequence. The wave forms of the control signals and the output drivers are shown schematically [147]. The blue time interval represents the active time period of the GM. The length of the GM sequence is chosen arbitrarily. It is enabled by *low* `Clock`, *high* `StrC` and the falling edge of `StrG`. The GM is disabled by the falling `StrG` edge after switching `StrC` to *low*. The red lines indicate the time period of activating row_{gate} 2 (Gate 2).

When the GM is activated, the parasitic Clear capacitance of the DEPFET matrix must be loaded. Therefore, large capacitors (100 nF) are placed around the Switchers, connected to the ClearOn voltage and to the Source voltage. In addition, the activation of the GM is done in four groups, each consisting of eight out of the 32 Clear output drivers. This is expected to guarantee a smooth transition in the GM. The time interval for enabling these groups is controlled by the `StrG` signal, as shown in Fig. 6.57.

Switcher Logic Problem

The GM without readout should not be enabled when the `SerIn` signal is received, i.e., when $\text{row}_{\text{gate}} = 191$ is enabled. According to the Switcher design, the `Clock` must be *high* when the `SerIn` signal is received (see Fig. 4.18) [147]. Although the `SerIn` signal is always sent at the correct time (since it is read from section 1 of the Switcher sequencer), the Switcher does not respond since the `Clock` signal is *low* during the GM operation. A change in the Switcher logic is required to

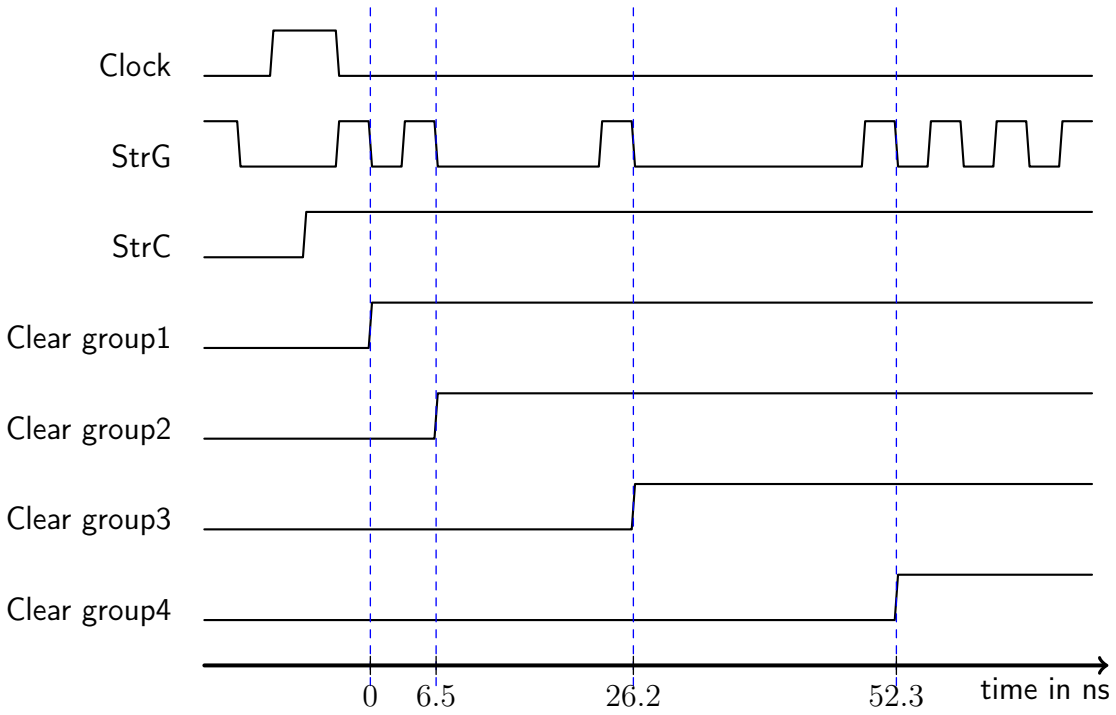


Figure 6.57: The Switcher is divided into four groups (Clear outputs ($\text{rows}_{\text{gate}}$) 1–8, 9–16, 17–24, 25–32) switching subsequently into the GM. The time difference is given by the falling edges of `StrG`, indicated by the blue lines. In this case, the enabling of the first two Switcher groups is as short as possible, i.e., two ticks.

remove this problem for the GM operation without readout. In the case that the GM is enabled around $\text{row}_{\text{gate}} = 190$, there is no rolling shutter readout in the next frame since the Gates are all switched off. Thus, the charge integration time doubles from 20 µs to 40 µs (at GCK= 76.33 MHz) for all DEPFET pixels.
Simulations are performed to confirm this behavior (see Fig. 6.59a). The GM is activated when $\text{row}_{\text{gate}} = 191$ (Gate5[30]) is enabled. The `SerIn` signal is sent when the `Clock` is *low*. In the next frame, the first row_{gate} of the first Switcher (Gate[0]0), is not enabled. Thus the next frame is missing.
It can also be seen that the GM is activated in groups. The first group (ClearOn0[0]) is enabled 24 ns (using a GCK of 62.5 MHz) before the Clear voltage is raised for the last group (ClearOn5[i], $i \in \{24, 25, 26, 37, 28, 29, 30, 31\}$).

In order to overcome the problem of the "missing next frame," the GM operation with readout concept is introduced.

Gated Mode with readout

The Switcher offers the possibility of being operated also in the *GM with readout*. The rolling shutter mode readout continues during the GM operation. The $\text{rows}_{\text{gate}}$ that are read out are not shielded. The readout period for a single Gate is 128 ns for GCK=62.5 MHz and $\sim$ 105 ns for GCK=76.33 MHz. The four Switcher groups switching into the GM, i.e., applying the ClearOn voltage at the Switcher output drivers of the Clear outputs, are activated consecutively with the subsequent

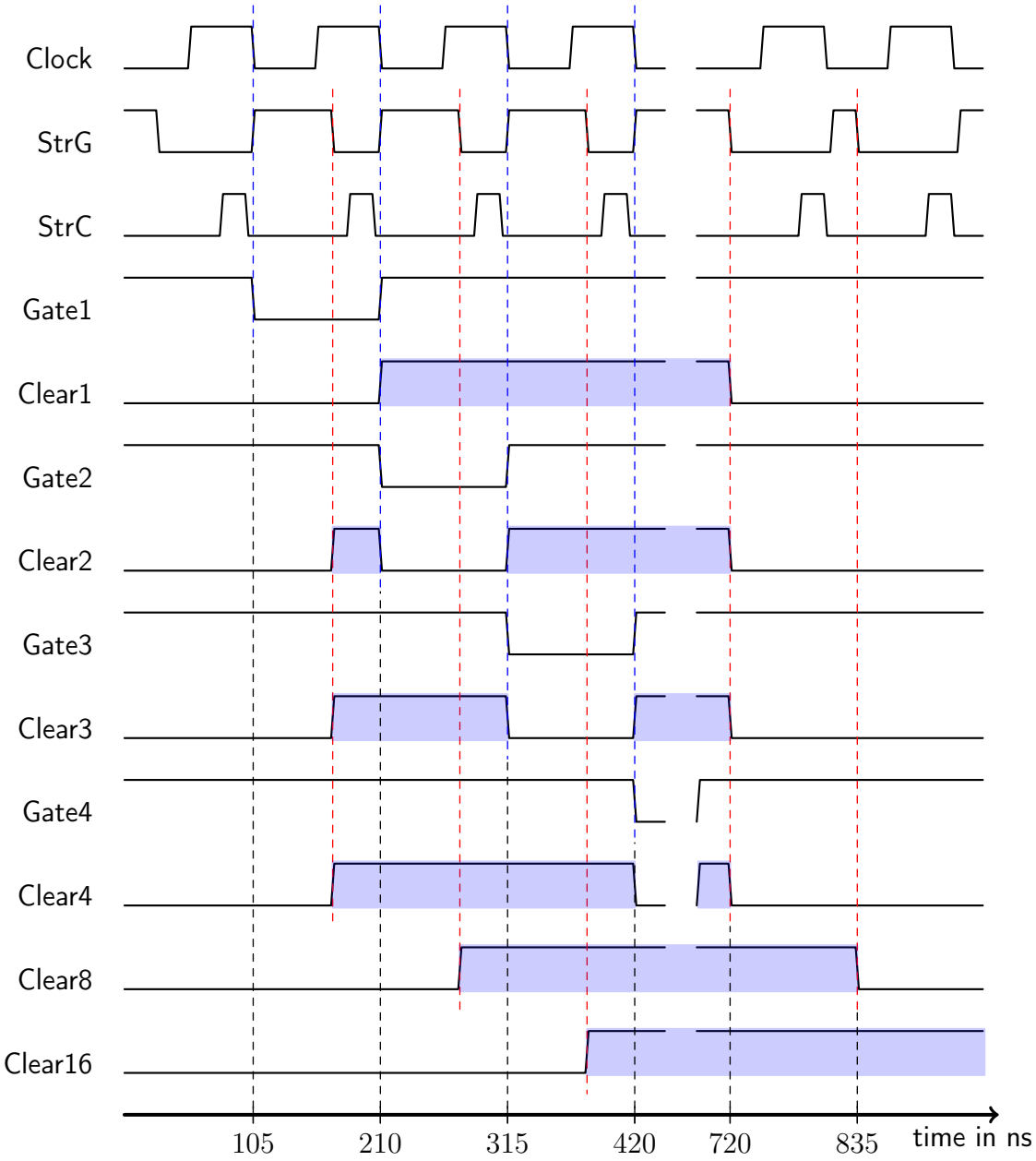
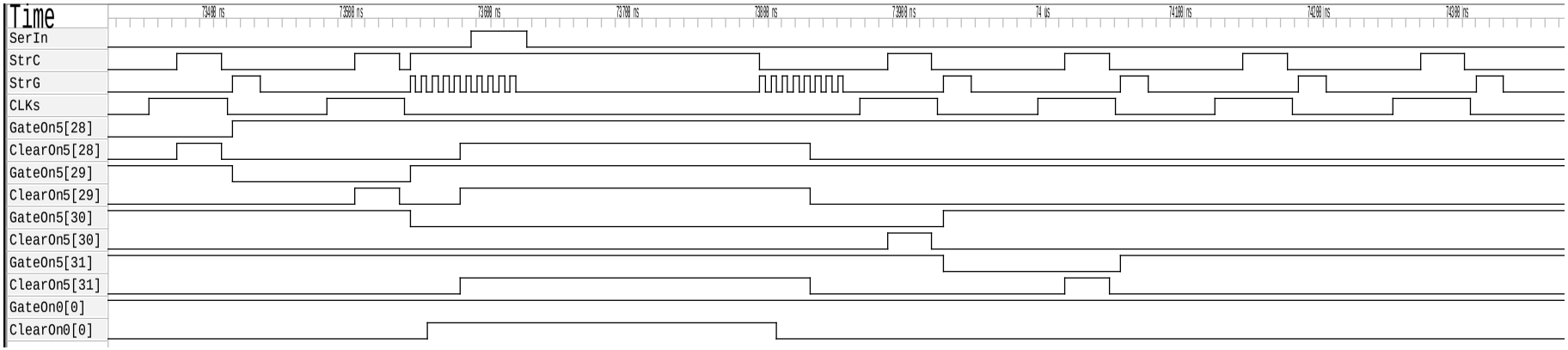
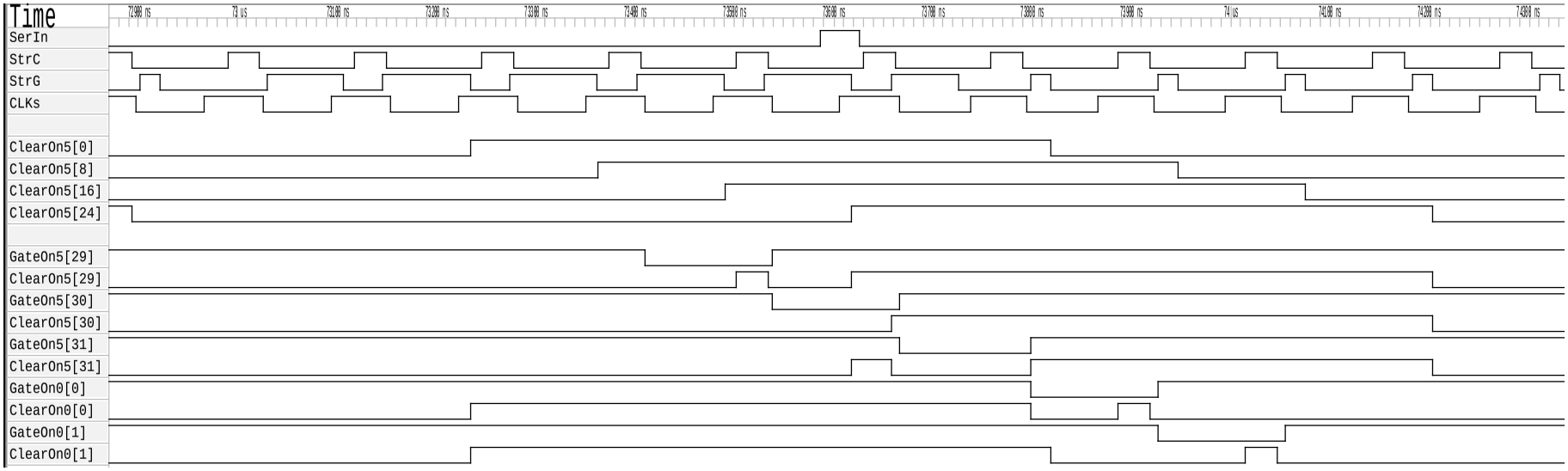


Figure 6.58: Gated Mode Switcher sequence with readout. The wave forms of the control signals and the output drivers are shown schematically [147]. The blue time interval represents the active time period of the GM, which is chosen arbitrarily. It is enabled by *high* `Clock` or *high* `StrC` and the falling edge of `StrG`. The `Clock` continues to toggle. The GM is disabled by the falling `StrG` edge which must be applied when the `Clock` is *low*. The red lines indicate activation of the gating of the different Switcher groups. The four Switcher groups (Clear 1, Clear 2–4, Clear 8 and Clear 16) are shown. The blue lines represent the Gate switching.



(a) Gated Mode without readout ("next missing frame,"): `SerIn` is received when the GM is active. Gate0[0] is not enabled in the next frame.



(b) Gated Mode with readout: The `SerIn` signal is received when the GM with readout is enabled. The rows are subsequently read out during the GM operation. The four Switcher groups apply the ClearOn voltage with every new row_{gate}.

Figure 6.59: Simulations of the Switcher logic for the GM operation.

Gate switching. All groups are enabled and disabled (to shield the entire matrix) within four $\text{rows}_{\text{gate}}$, corresponding to 384 ns for GCK=62.5 MHz and 315 ns for GCK=76.33 MHz. The GM with readout is enabled by *high* `Clock` or *high* `StrC` and the falling edge of the `StrG` signal [147]. The schematic is shown in Fig. 6.58. The `Clock` continues to run. For this reason, the `SerIn` signal is recognized by the Switcher and thus the next frame is always read out. This is in contrast to the GM without readout where the `SerIn` signal is not recognized during the GM. The Switcher simulation for this sequence is shown in Fig. 6.59b.

Advantages and Disadvantages of the different Gated Mode operations

The GM without readout is fast in terms of enabling and disabling the four Switcher groups. From the Switcher logic point of view, the four groups can be activated (and deactivated) within four clock cycles corresponding to eight ticks (six ticks for the edges of `StrG`), i.e., 20 ns (for GCK=76.33 MHz). However, the disadvantage is the "missing next frame" problem, i.e., the rolling shutter mode is not executed in the next frame if the `SerIn` signal is received during the active GM without readout. Thus, the integration time doubles. The activation time in relation to the rolling shutter mode is distributed homogeneously, i.e., the GM can be activated for any row_{gate}. Assuming a non-toggling `Clock` for three $\text{rows}_{\text{gate}}$ (for the GM without readout) would result in a doubled integration time of 1.6 % of all recorded frames.

The GM with readout processes all SerIn signals, i.e., there is no "missing next frame", since the `Clock` continues to run. However, the time interval for enabling (disabling) one of the four Switcher groups into the GM, i.e., applying the ClearOn voltage to the DEPFET pixels, corresponds to the `Clock` period (105 ns for GCK=76.33 MHz). For this reason, the activation (deactivation) time for the entire matrix is 315 ns. Assuming a required shielding time for the entire matrix of at least 200 ns results in 945 ns for the GM operation for the Switcher control from the Switcher logic point of view. Additionally, the parasitic capacitances of the Clear metal lines must be taken into account, resulting in flat edges of the applied ClearOn voltage. Furthermore, pedestal oscillations presented in Sect. 6.12.8 need to be taken into account for the overall GM operation.

6.12.5 Lab setup

For the lab measurements, the B2TT signal is not available. To emulate triggers (for switching into the GM), a dedicated firmware has been generated [161]. A sequence consisting of 8000 lines, which are called *steps* (each line corresponds to a global clock cycle), is uploaded into the memory of the DHE. Within this sequence, it can be defined when the triggers for the zero suppressed readout are sent to the DHPs, when the VETO signal is applied (at the DHPs) and at which time an external pulse (which serves as trigger for a laser) is sent to a hardware interface.
The maximum number of 8000 steps allows the readout of out five complete consecutive frames, i.e., $\sim 123\,\mu s$ (at GCK=62.5 MHz), abbreviated by *cframes*.

A laser pulse, which simulates a traversing charged particle, is triggered and is shot onto the top side of the matrix. The trigger NIM signal from the DHE is converted to a TTL signal, which is received by the pulse generator. It sends a voltage pulse with a defined amplitude and length to the laser. The laser pulse is guided by optical fibers to a mounting support, which shoots the laser pulse onto the matrix. The support is adjusted by a xyz-stage with micrometer resolution. A sketch of the setup is shown in Fig. 6.60.

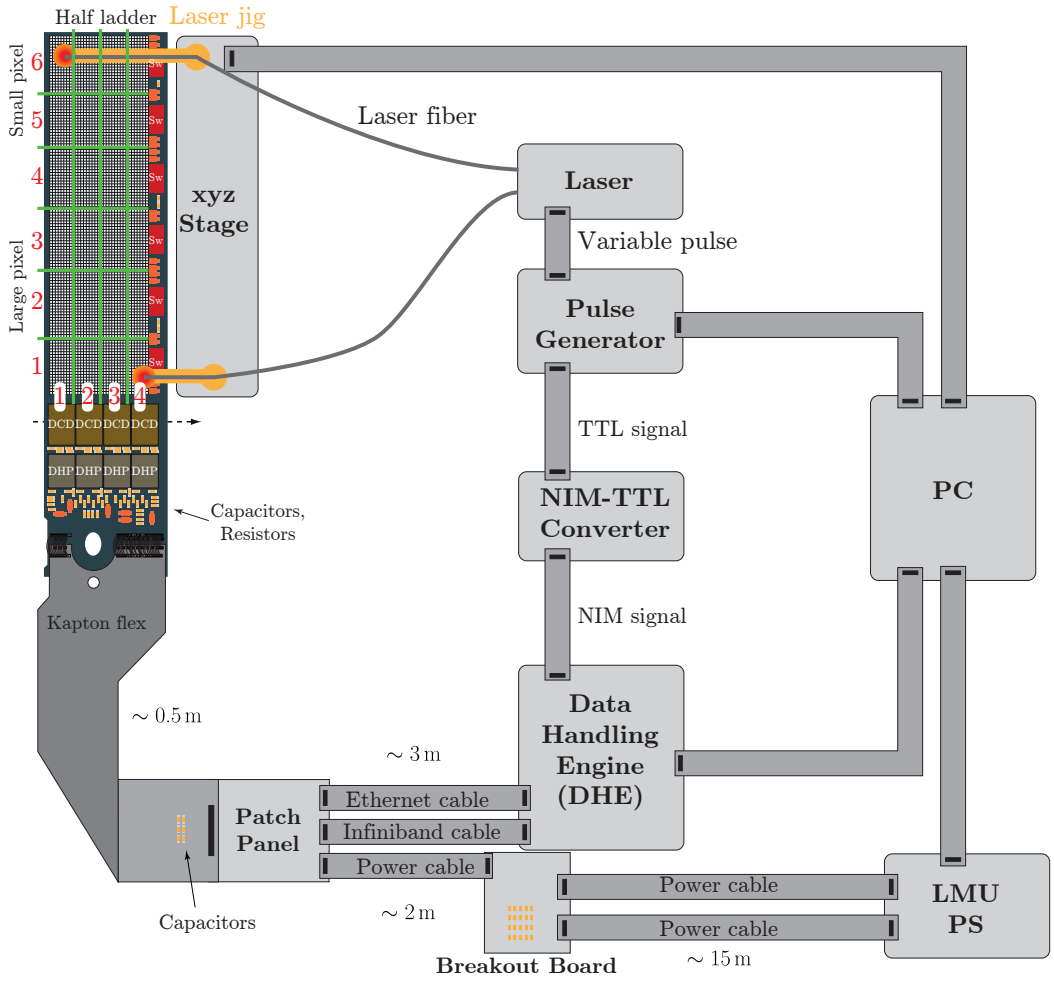


Figure 6.60: Sketch of the lab setup for the Gated Mode measurements.

6.12.6 Clear Pulses

As already shown in Sect. 6.10, the length of the Clear pulse determines the amplitude of the voltage applied at the *Clear implants* of the pixels. For the experiment, the GM should be enabled, i.e., the ClearOn voltage should be applied for approximately 200 ns (when noisy bunches pass the detector). Enabling the GM, shielding the *internal Gate* and switching back to normal operation is required to take a total of $\sim 1\,\mu s$, as determined by the other sub-detectors of Belle II. The Clear pulses are studied on the W30-OB1 and the W31-OF1 (with the improved metal routing of Switcher-Vref net) modules.

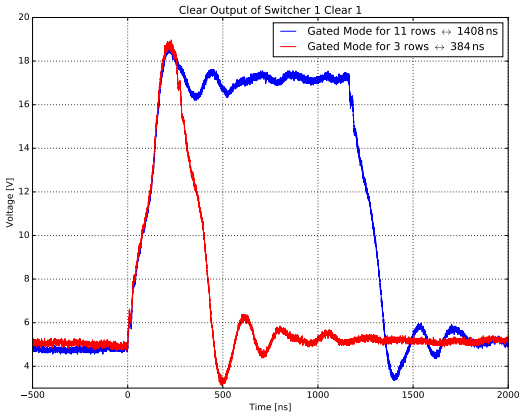
W30-OB1 (old metal system)

This module still has the old metal layout (PXD9-6, see Sect. 6.1). The pulses of the applied ClearOn voltage for the GM without readout are studied in the following. The Clear pulse for the first Switcher ($\text{row}_{\text{gate}} = 1$) is studied for different GM sequences of 384 ns and 1408 ns, i.e., the ClearOn voltage is applied for different lengths. The maximum amplitude for the Clear voltage of $\sim 17.5\,\text{V}$ is reached in both cases. The oscillations of the Clear voltages seen in Fig. 6.61a are due to the missing grounding of the probe. The maximum of 20 V is not reached for three reasons. First, the ground of the probe is not connected, i.e., it is floating. Second, the probe is operated outside of its specifications. Voltages can be measured between $-7\,\text{V}$ and $+10\,\text{V}$, i.e., a maximum voltage range of 17 V according to the manual [201][15]. Third, the contact between the needle and the probe pad is not adequate since oxidation on the copper probe pad causes partial insulation. For these reasons, the measured voltage is lower than the expected voltage. The total voltage of ClearOn, relative to ground, is 27 V (7 V source and additional 20 V for ClearOn). The rise and fall times of the Clear pulses are approximately 170 ns. This is much longer than the Clear pulses measured in the normal Switcher sequence ($\sim 20\,\text{ns}$) in Sect. 6.10. In that case, the ClearOn voltage is applied on a single Clear output, connected to 1000 pixels. In contrast, for the GM, the ClearOn voltage is applied at 48 Clear outputs (8 outputs for the first Switcher group times six Switchers) corresponding to 48,000 pixels. In addition, the next groups (2, 3, 4) are enabled in steps of 8 ns. This causes much more parasitic capacitance (due to the Clear routings and implants), which must be charged. These are the reasons for longer edges of the suppressed Clear pulse, i.e., the GM operation.

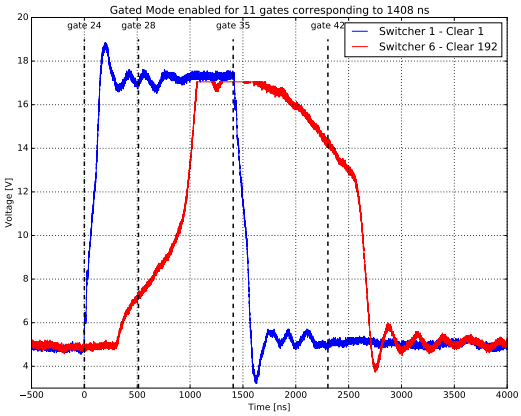
In Fig. 6.61b the Clear pulses of the first Switcher ($\text{row}_{\text{gate}} = 1$, Switcher group 1) and of the last Switcher ($\text{row}_{\text{gate}} = 192$, Switcher group 4) are compared. The GM period has been extended to 1408 ns (corresponding to the length of eleven gates) to reach the maximum ClearOn voltage and analyzing the rising and falling edges of the Clear pulse. It can be clearly seen that the rising and falling edges of the last Switcher are much more elongated. This is due to several reasons:

- The last Switcher output ($\text{row}_{\text{gate}} = 192$) corresponds to Switcher group 4, which is enabled 24 ns after applying the ClearOn voltage to the first group.
- The decoupling capacitors, mounted on the silicon module close to the Switchers, do not have the expected capacitance of 100 nF. The idea is to "load" the charge, stored in these capacitors, into the Clear capacitance of the matrix.
- The Switcher is furthest away from the supply nets, i.e., the Kapton cable attachment. The ohmic resistance of the sw-Vref net along the balcony cause voltage drops. Calculating the ohmic resistance of the sw-Vref net from the end-of-stave (Kapton attachment) to the individual Switchers results in $\sim 55\,\Omega$ to the first Switcher and $\sim 172\,\Omega$ to the last Switcher.

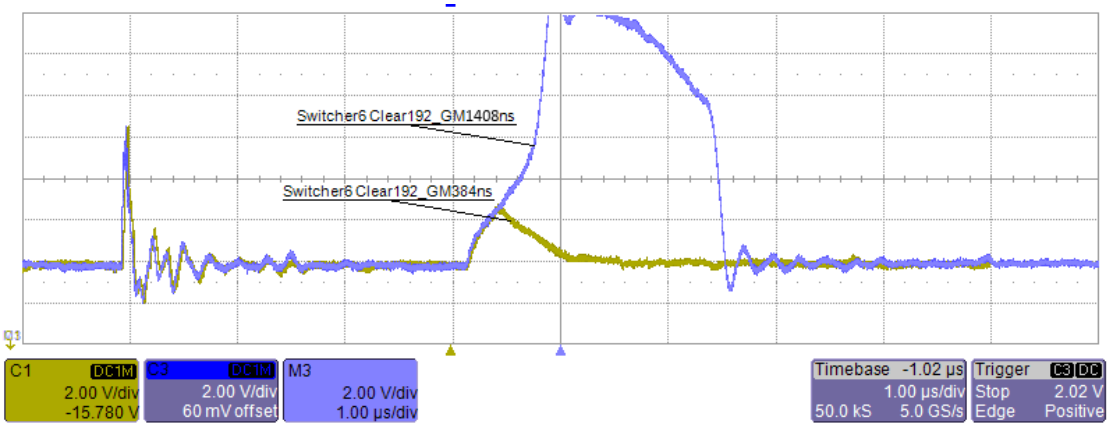
[15] No other probes with those (or better) electric properties for measuring short pulses (few nano seconds) of amplitudes of approximately $\sim 30\,\text{V}$ and a tiny needle (radius $< 5\,\mu\text{m}$) was found in industry.



(a) First Clear output of Switcher 1 ($\text{row}_{\text{gate}} = 1$) for different lengths (384 ns and 1408 ns) of GM operation. The maximum value is reached for both lengths. The oscillations are due to non-existing grounding of the single-ended probe of the oscilloscope. The rise and fall times are approximately ~ 170 ns.



(b) First Clear output of Switcher 1 ($\text{row}_{\text{gate}} = 1$) and last Clear output of Switcher 6 ($\text{row}_{\text{gate}} = 192$) for a GM operation of 1408 ns corresponding to eleven $\text{rows}_{\text{gate}}$ lengths. The Clear pulse of the last Switcher output has long rising ($\sim$ 760 ns) and falling ($\sim$ 1050 ns) edges compared to the first Switcher.



(c) Last Clear output of Switcher 6 $\text{row}_{\text{gate}} = 192$ for a GM operation of 384 ns and 1408 ns. For short GM operations only a small fraction of the ClearOn voltage is applied at the *Clear* outputs of the Switchers.

Figure 6.61: W30-OB1: Clear Outputs for the first output driver of Switcher 1 ($\text{row}_{\text{gate}} = 1$) and the last output driver of Switcher 6 ($\text{row}_{\text{gate}} = 192$) for different lengths of GM operation.

The major reason for the elongated edges is due to the voltage drop of the Switcher Vref net (last bullet). The impact of the different Clear pulses along the module is discussed in detail in Sect. 6.12.9.

W31-OF1 (new metal system)

This module already has the new metal layout (PXD9-7, see Sect. 6.1). With the updated layout of the Switcher-Vref traces, the ohmic resistance to the Switcher 6

(closest to DCDs) is $\sim 10.5\,\Omega$ while the resistance to Switcher 1 (largest distance to DCDs) is $\sim 26.5\,\Omega$. The W31-OF1 is operated at the nominal global reference clock of 76.33 MHz.

Gated Mode without readout The Switcher arrangement on the OF module is flipped compared to the OB module (as shown in Fig. 4.47). The first group of the Switcher 1 has the largest distance to the DCDs and the fourth group of Switcher 6 has the shortest distance to the DCDs. The Clear pulses of the GM is again

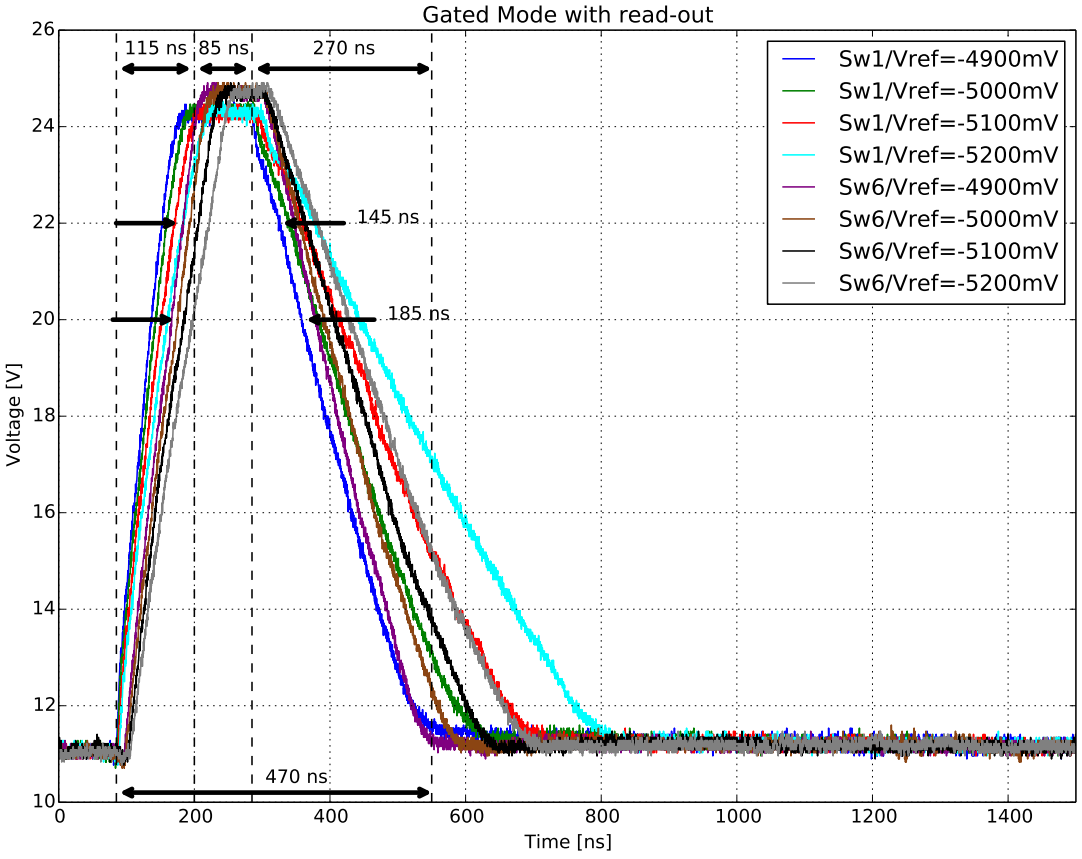


Figure 6.62: Measured Clear pulses of Switcher 1 (group 1) and Switcher 6 (group 4) for the GM without readout on the W31-OF1 module. The voltage has an offset of +6 V (Source voltage).

measured as function of the the sw-Vref voltage. The measured Clear pulses for the GM without readout are shown in Fig. 6.62. The ClearOn voltage is set to 20 V, the ClearOff voltage is adjusted to 5 V (relative to the Source voltage of 6 V). A sw-Vref voltage of -4.9 V is recommended to obtain the same timing (the same steep edges of the Clear pulses) for enabling and disabling the GM for both Switchers. The entire gating time in the Switcher sequence is programmed for ~ 187 ns. The enabling of the GM at the four Switcher groups (i.e., rising the Clear potential to the ClearOn voltage) should require 20 ns. The rising edge is measured with 115 ns while the switching from GM to normal operation requires approximately double, 270 ns. In conclusion, only the enabling and disabling of the GM without readout

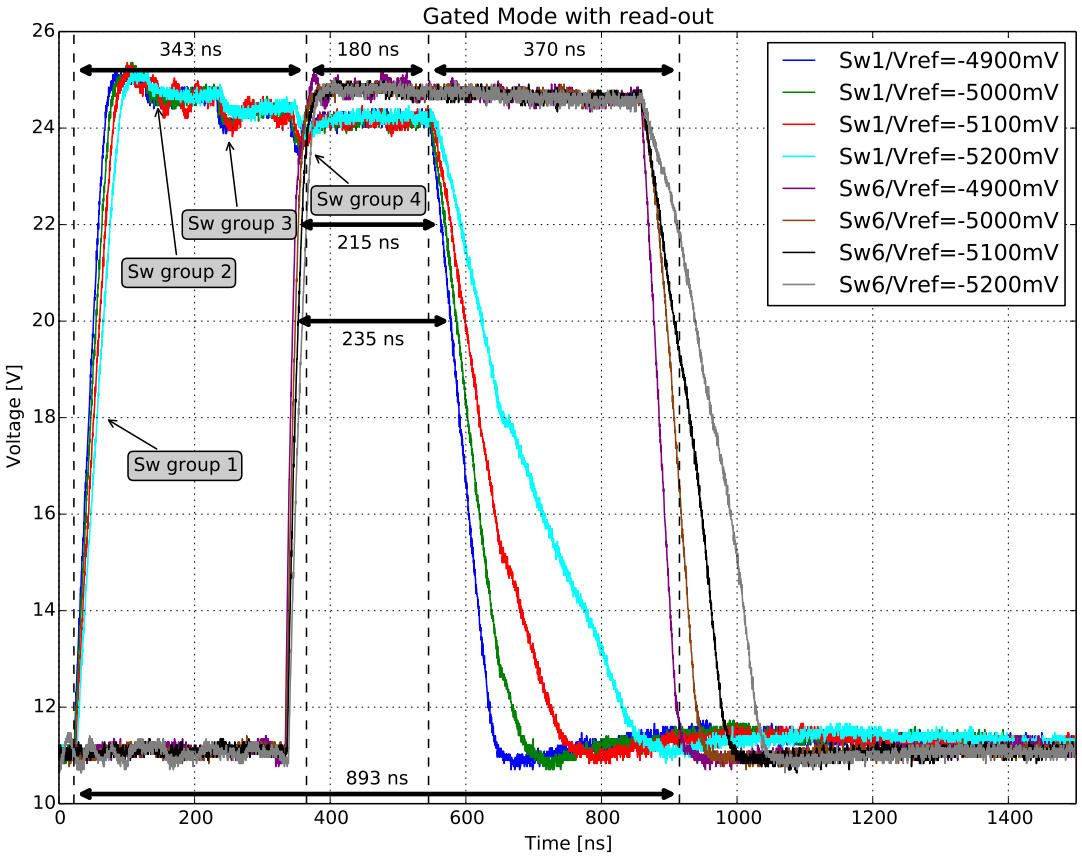


Figure 6.63: Measured Clear pulses of Switcher 1 (group 1) and Switcher 6 (group 4) for the GM with readout on the W31-OF1 module for different Switcher-Vref voltages. The voltage has an offset of +6 V (Source voltage).

requires 385 ns. The total time for the GM operation needs, in this case, $\sim$ 470 ns. The overlap of reaching the plateau of the maximum voltage for both Switchers (1 and 6) and both Switcher groups (1 and 4) is $\sim$ 85 ns. If a ClearOn voltage of 18 V is sufficient to shield the matrix, the GM is activated for 145 ns. Furthermore, if ClearOn=16 V is sufficient, the GM is activated for 185 ns. However, the period of Gating can be extended by increments of ticks (i.e., 3.28 ns at GCK=76.33 MHz) according to the required gating length, which is about 200 ns when noisy bunches pass. However, the total time of enabling, shielding (for $\sim$ 200 ns) and disabling the GM can be performed well below 1 µs. This short Gating period would not be feasible with the previous version of the metal routing since the edges are not steep enough. The timing values for the simulation and measurements of the W31-OF1 module are summarized in Tab. 6.10.

Gated Mode with readout In addition, the GM with readout is studied for different sw-Vref voltages. The preferred voltage for sw-Vref is again −4.9 V. The same ClearOn, ClearOff and Source voltages are applied as for the study of the GM without readout. The wave forms of the Clear output drivers are shown in Fig. 6.63. The four Switcher groups, which are activated for the GM operation, cause small voltage ripples in the measured Clear voltage. The third ripple of Switcher 1 crosses

Table 6.10: Overview of the timing constants for the GM operation with and without readout (RO) at the nominal global frequency of 76.33 MHz. The enabling of the GM, the time of Gating the entire matrix, i.e., all pixels, the time to switch back to normal operation (disable the GM) and the total times are shown. The measurements are performed on W31-OF1 (new metal layout).

	Enabling	Gating	Disabling	Total
Simulation w/o RO	20 ns	187 ns	20 ns	227 ns
Measured w/o RO	115 ns	85 ns	270 ns	470 ns
Simulation w/ RO	315 ns	164 ns	315 ns	794 ns
Measured w/ RO	343 ns	180 ns	370 ns	893 ns

with the rising edge of the forth group of Switcher 6. The entire GM sequence is measured with 893 ns, where the time interval in which the entire matrix is completely shielded is only approximately 180 ns. The enabling of the four Switcher groups requires 343 ns, while the disabling requires 370 ns. If a ClearOn voltage of 18 V is sufficient, the GM will be active for 215 ns. Furthermore, if 16 V are sufficient, the GM will be activated for 235 ns. According to the simulation, the GM requires 794 ns where the phase of having the entire matrix gated is 164 ns. The enabling and disabling of the four Switcher groups require 315 ns.
Concluding, the GM with readout extends the enabling and disabling phase of the Switcher groups dramatically by roughly a factor of two from 470 ns (with shielding of 85 ns) to 893 ns (with shielding of 180 ns) relative to the GM without readout. However, the GM can be performed even in the version with readout within 1 µs where the Gating period of the entire matrix is approximately 180 ns. The timing values are also summarized in Tab. 6.10.
The shielding time for the entire matrix can be extended in steps of the Switcher clock, i.e., 105 ns at GCK=76.33 MHz for the GM with readout, while the sequence can be extended in steps of 3.27 ns for the GM without readout. However, although the GM operation can be performed for the entire matrix within 1 µs the pixels should be read out afterwards. Due to the applied ClearOn voltage and the resulting changes in the Drain currents, the DCD starts to oscillate which in addition requires a "recovery time" of a few hundreds of nano seconds. The measurements regarding these oscillations will be presented in Sect. 6.12.8.

6.12.7 Timing Issues for GM without readout

When applying the GM operation without readout, special attention should be given to the timing and the synchronization of the rolling shutter mode. Figure 6.64 shows a simulation of the GM operation of the Switcher. The GM is enabled when $\text{row}_{\text{gate}} = 77$ (= GateOn2[12]) is activated. This corresponds to the second Switcher group (of Switcher 2). It is activated by toggling the `StrG`, stopping the `Clock` and activating the `StrC`, as explained in Sect. 6.12.4. The GM is enabled for 228 ns. This corresponds to the time interval between enabling the Clear of the last Switcher group and disabling the Clear of the first Switcher group. The row_{gate} GateOn2[12] is activated during the GM operation. In order to preserve

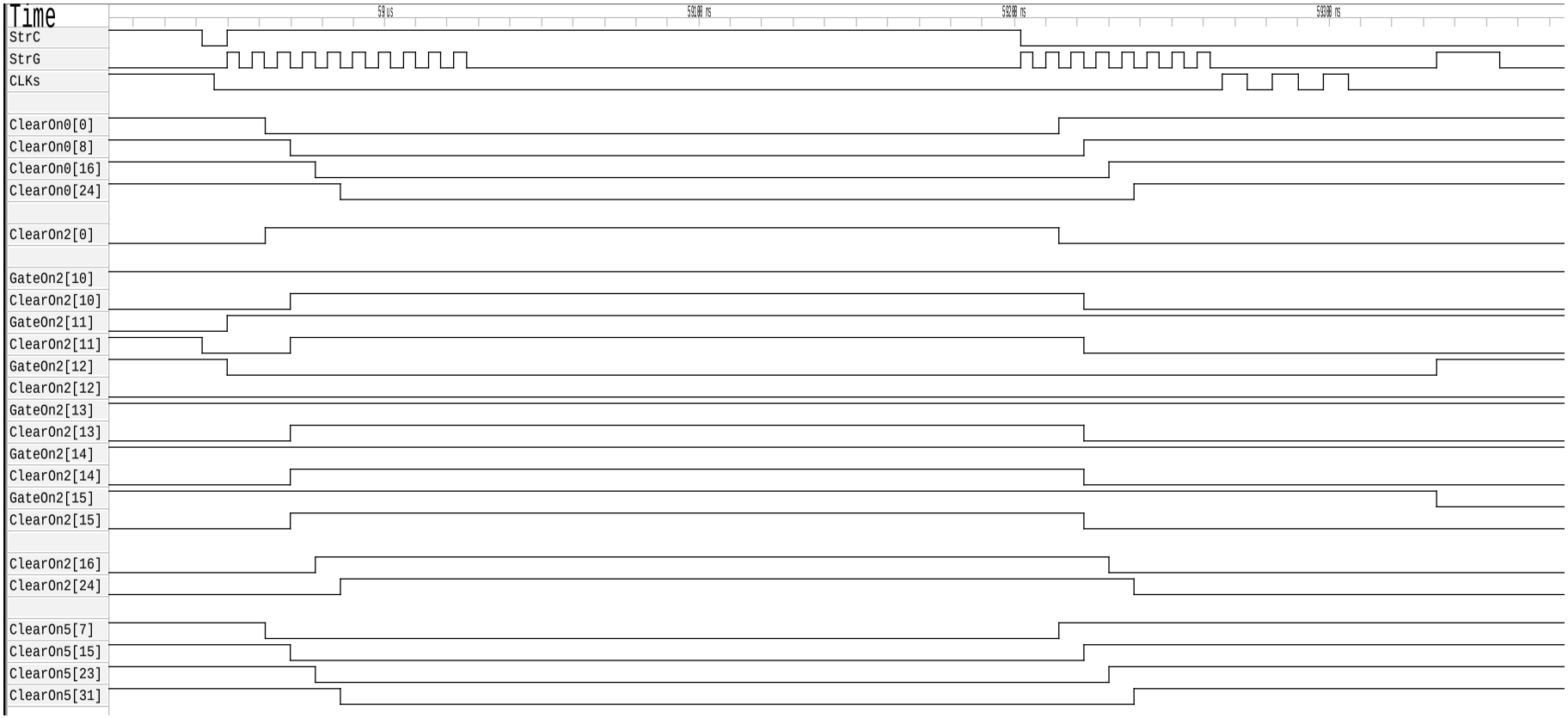


Figure 6.64: Simulation of the GM without readout operation for the Switcher. The GM is activated when GateOn2[12] is read out. The pixels, which are connected to GateOn2[13] and GateOn2[14], are not read out in this frame. The four groups of the Switcher to apply the ClearOn voltage (with the falling edges of `StrG`) are visible. To get in synchronization with the rolling shutter mode (i.e., not extending the frame time) the fast clocking is performed at the end of the GM sequence.

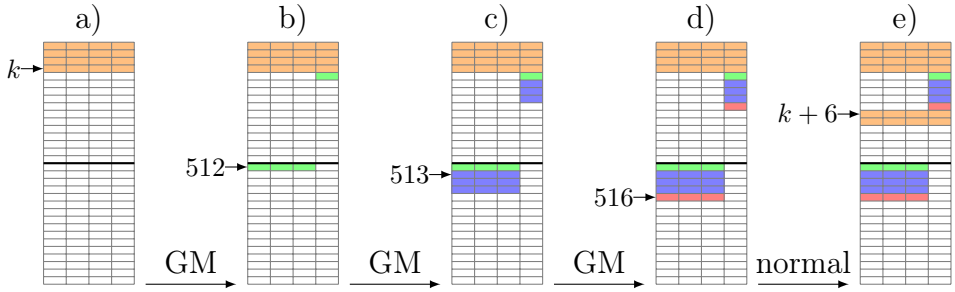


Figure 6.65: Sketch of the Switcher memory sequences for GM without readout, including the fast toggling of `StrG` and fast clocking, for increasing time from left to right. Each row represents a 128-bit data word, consisting of the `Clock`, `StrG`, `StrC` and `SerIn` (shown by the four columns). The entire DHP Switcher memory is divided into two sections (0–511 and 512–1023, see text). The normal operation is performed until data word k (a). The GM operation is executed between $k+1$ and $k+5$ (b-d). The green data word represents the fast toggling of `StrG`, the blue lines indicate the data words for the active GM operation without readout and the red line illustrates the fast clocking. Afterwards, the normal sequence continues (e). The `SerIn` is always read from the first memory section.

the signal (i.e., not clearing) the Clear voltage for this particular output driver (ClearOn2[12]) is not switched on[16]. Two $\text{rows}_{\text{gate}}$ (GateOn2[13] and GateOn2[14]) are not enabled during the active time interval of the GM. Thus, they are also not read out in this frame.
During the GM period without readout, the `Clock` is stopped. As a consequence, the `SerIn` is not shifted within the internal shift register of the Switcher. This would extend the readout time of an entire frame by additional 210 ns (at a GCK of 76.33 MHz). In addition, this would result in losing the synchronization between the frame readout and the revolution time of the bunches in SuperKEKB (bunch 0). In order to keep the pre-defined readout time and to keep the synchronization to bunch 0, two additional clock cycles (called *fast clocking*) are applied at the end of the GM sequence to shift the `SerIn` signal in the correct shift register position (see Fig. 6.64). To do so, the correct row_{gate} is read out afterwards and the defined frame time is kept of 20 µs (for a GCK of 76.33 MHz). Using this method, the two $\text{rows}_{\text{gate}}$, connected to (GateOn2[13] and GateOn2[14]) are not read out in this frame. Hence, the integration time for these row_{gate} double, i.e., 40 µs (for GCK=76.33 MHz) if the GM is not applied at the same readout position in the next frame.
In the following the impact of the sequence (to activate the GM) and the fast clocking (to get in synchronization) on the memory in the DHP (to control the Switchers) are discussed. In the second section of the Switcher memory (of the DHP) the following sequences are stored:

- In order to activate (or deactivate) the GM without readout, the `StrG` is toggled multiple times (see Fig. 6.57 and Fig. 6.64). This is called *fast toggling of `StrG`*.

[16]For this reason the DEPFET pixels connected to this row_{gate} are sensitive to noisy bunches.

- GM sequence (*low* `Clock`, *low* `StrG`, *high* `StrC`).
- Fast clocking of the Switcher clock to re-synchronize with the normal Switcher sequence of the rolling shutter mode.

As a consequence, the length of the applied VETO command (defined in the sequence of the DHE), which shifts the Switcher sequence memory pointer to the second Switcher memory section, must match the length of the entire GM operation. In other words, the length of the GM sequence must be in accordance to the sequence, which is written in the second section of the DHP memory. Changing the length of the GM operation requires uploading a new Switcher sequence into the second Switcher memory section of the DHP. Thus, the sketch of Fig. 6.55 changes to Fig. 6.65 due to the fast toggling of `StrG` and the fast clocking.
For the GM with readout, an extended `StrG` signal is required. It requires two extended `StrG` signals to activate the GM with readout. The Switcher `Clock` continues to run (see simulation in Fig. 6.59b).

6.12.8 Pedestal relaxation

When the ClearOn voltage is applied for all pixels at the same time, the Drain currents increase resulting in larger signals of the DEPFETs. Switching back to normal operation (rolling shutter readout mode) the Drain currents decrease to their nominal values. The DCD has to cope with the sudden increase and decrease of almost all (250 of 256) input channels. This can cause oscillations of the ADCs, which requires some time to damp (*pedestal relaxation*). This pedestal relaxation is studied with the W31-OF1 module with the new metal layout (PXD9-7) routing at the nominal speed (GCK=76.33 MHz).
A sketch of the sequence for studying the pedestal relaxation is shown in Fig. 6.66. Four consecutive frames are acquired, where the signals of the first frame serve as pedestal values. In the last three frames, the GM is enabled twice per frame (10 µs revolution time for the noisy bunches, 20 µs readout time for a full frame). The pedestal relaxation is studied for both operational modes, i.e., GM without readout and GM with readout.

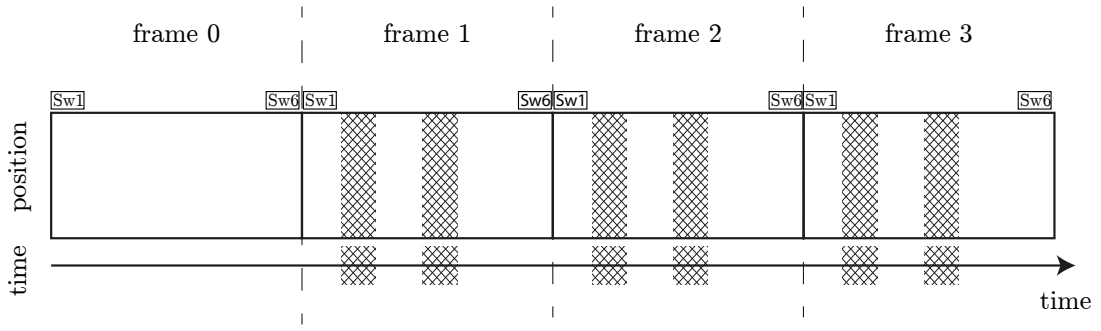


Figure 6.66: Illustration of the measurement procedure. The pedestals are recorded in frame 0. The GM is activated twice (hatched area) in each of the three consecutive frames corresponding to an periodic GM operation of 10 µs. In the Belle II experiment, the GM is enabled every 10 µs (revolution time of noisy bunches) for 4 ms (i.e., $\sim$ 200 frames).

Gated Mode without readout

The total GM sequence, including fast toggling of `StrG` and fast clocking, is enabled for three $\text{rows}_{\text{gate}}$ corresponding to 315 ns. The ClearOn voltage is applied for 226 ns to all DEPFET pixels (according to the simulation). The GM is enabled when $\text{row}_{\text{gate}} = 31$ is activated, i.e., 3253 ns after starting the readout of this frame. In addition, it is enabled again $\sim 10\,\mu\text{s}$ later for 315 ns.

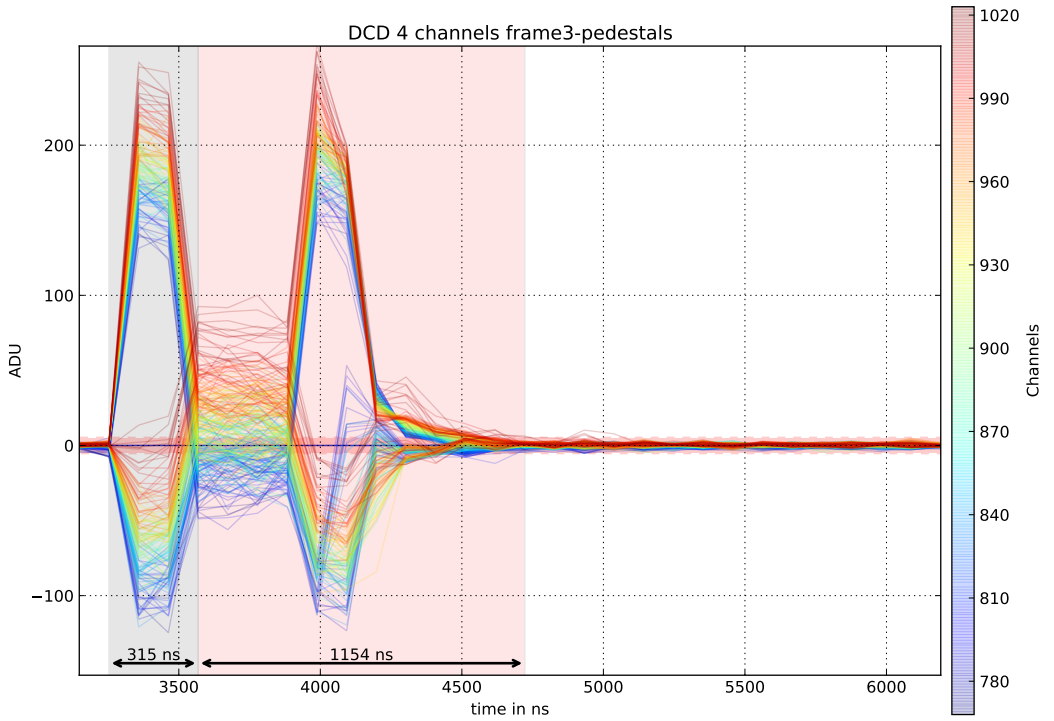


Figure 6.67: The GM without readout is enabled for 226 ns. The pedestal values change by the increased Drain currents. The gray area represents the active GM sequence (315 ns), while the red area represents the relaxation time (1154 ns). The drain currents are measured every 105 ns.

The DEPFET signals (with subtracted pedestal values) are shown for all Drain columns ($\text{cols}_{\text{drain}} = 0$–$256$) and $\text{rows}_{\text{gate}}$=30–60, corresponding to 3148–6296 ns after starting the readout of this frame, of DCD 4 of frame 3 in Fig. 6.67. When the GM is active, half of the entire ADCs show increased signal values while the other half show decreased signal values ($\text{rows}_{\text{gate}} = 31$–$34$, corresponding to 3358–4722 ns after starting the frame readout) The signals of the input channels of the DCD, which are arranged like the footprint of the ASIC, are shown in Fig. 6.68. This representation is called the *pinmap* of the DCD.
Furthermore, the ADCs start to oscillate. The decreased ones show increased signals while the increased ones show decreased values. The gray area in Fig. 6.67 indicates the active GM operation. The red area marks the relaxation time of the pedestal values. The Drain current (signals of the DEPFET pixels) are measured every 105 ns. As a result, the period of the activated GM can be even shorter as

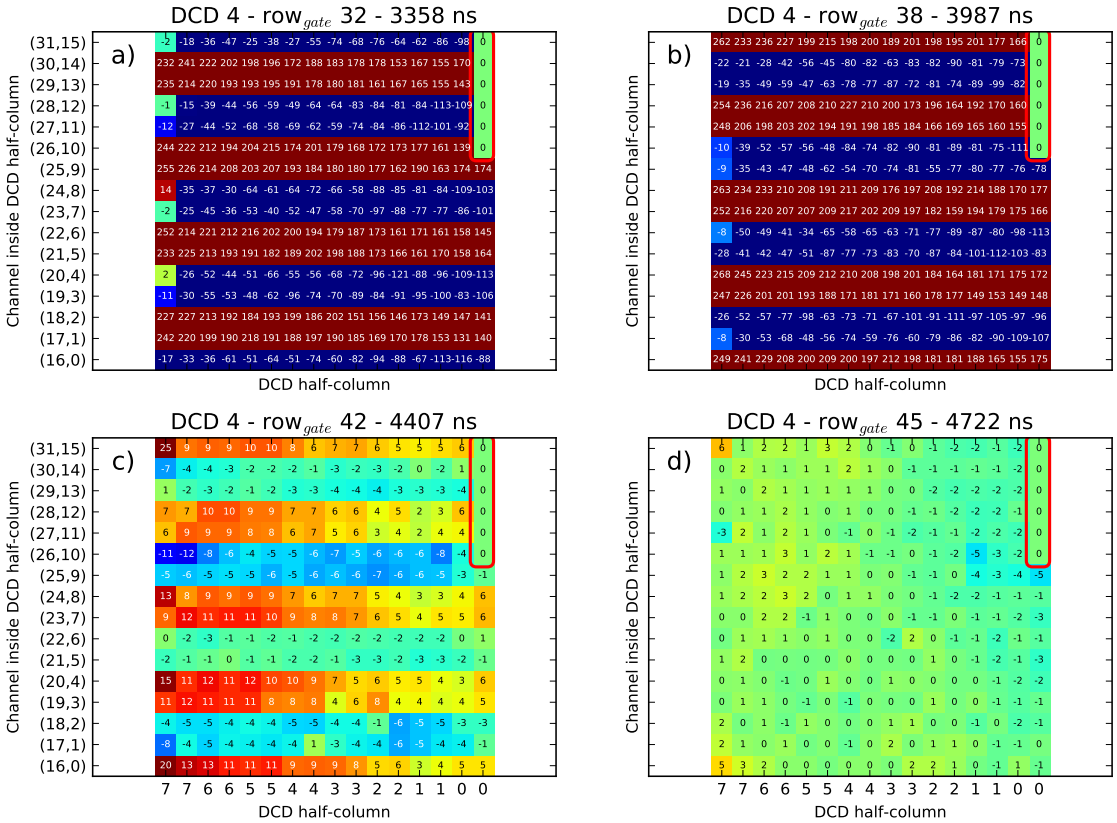


Figure 6.68: Pinmap of the DCD for different readout times. a) DCD signals at readout of $\text{row}_{\text{gate}} = 32$ (3358 ns). b) DCD signals at readout of $\text{row}_{\text{gate}} = 38$ (3987 ns). c) DCD signals at readout of $\text{row}_{\text{gate}} = 42$ (4407 ns). d) DCD signals at readout of $\text{row}_{\text{gate}} = 45$ (4722 ns). Comparing (a) and (b) one can clearly recognize a pattern. Every second ADC shows an opposite behavior, i.e., the ADCs oscillate. The plots (c) and (d) show the relaxation of the ADCs. The oscillation amplitudes (i.e., the signals) decrease and vanish completely at $\text{row}_{\text{gate}} = 45$. The red rectangle represents the six unconnected input channels.

shown in Fig. 6.67 with 315 ns. Switching back to normal operation, the values reach their nominal pedestal values (approximately ±5 ADU) 1154 ns later. This corresponds approximately to a total gating and relaxation time of 1.47 µs.

Gated Mode with readout

The GM can also be operated (from the Switcher point of view) while continuing the rolling shutter readout. For the current row_{gate} that is read out, the Clear pulse is disabled, i.e., this row_{gate} is not shielded. The GM is enabled in row_{gate} 31 (3358 ns after starting the readout of this frame) for 794 ns, according to the simulation. The entire GM sequence including the accompanied pedestal relaxation takes 2 µs as shown in Fig. 6.69. However, further studies have to be performed in order to possibly decrease the pedestal relaxation time somewhat. Additional capacitors on the Kapton cable and on the breakout board do not decrease the time.

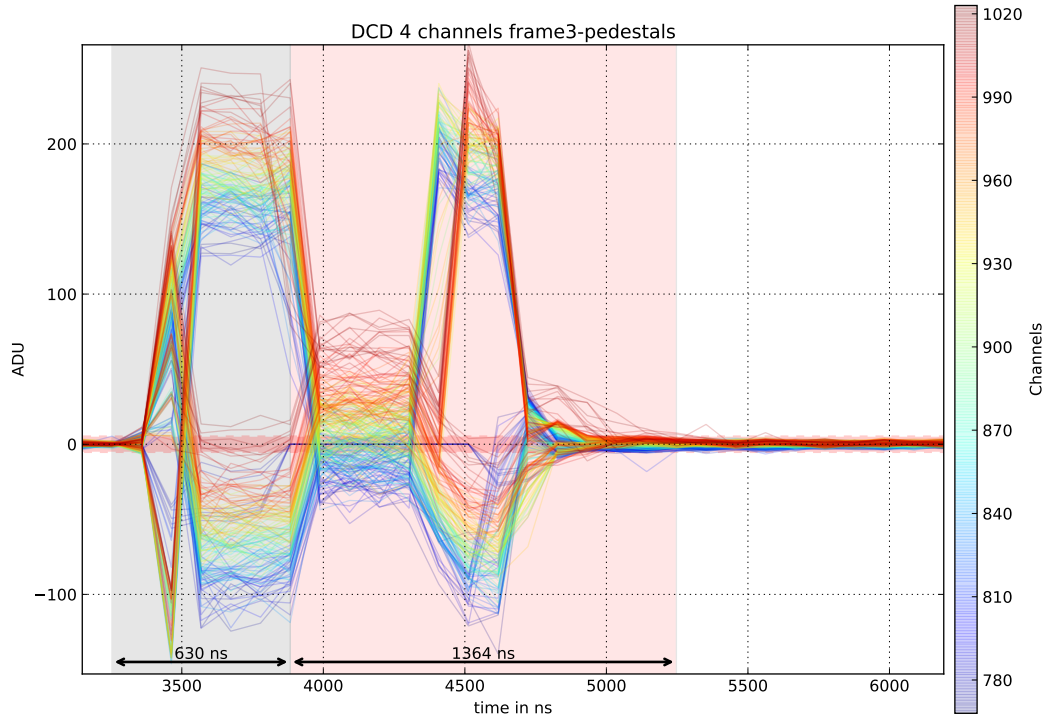


Figure 6.69: The GM is enabled on for 794 ns (according to the simulation). The gray area marks the active GM with increased ADU signals, which is approximately (630 ns). The red area marks the disabling of the GM and the pedestal value oscillation, which takes approximately 1364 ns.

6.12.9 Gated Mode Timing Window

In this section it is studied how fast the DEPFET pixels can be shielded, i.e., how fast the transition between the normal operation mode and the GM (and vice versa) can be performed. The time required to enable and disable the GM should be as short as possible. In the optimal case, the rising and falling edges of the ClearOn voltage, applied at the DEPFET pixels, are very steep in order to switch quickly (couple of tens of nano seconds) between the different operation modes. As already shown in Sect. 6.12.7, the Clear pulses of the Switcher groups 1 and 4 and of the Switcher locations along the module have different shapes. The behavior of the Switcher groups and Switcher positions is investigated, as well as their impact on the applied Clear voltage to the pixels.

Sequence

As shown in Fig. 6.60, the positions of the laser spots are chosen such that a single pixel of the first, second, third and fourth Switcher group is hit for the first Switcher (1) and for the last Switcher (6). Two consecutive frames are acquired. In frame 0 the pedestal values are recorded and the GM is enabled. The laser is shot for a few nano seconds (< 10 ns) either before during or after the GM. Its pulse is swept as a function of time (*laser pulse delay*) along the duration of the

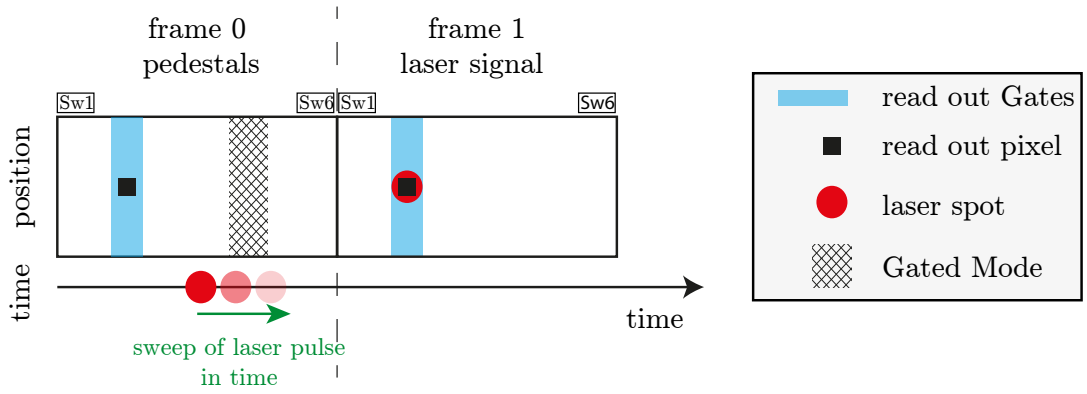


Figure 6.70: Illustration of the measurement procedure. The laser pulse is swept as function of time along the active GM operation.

GM. A sketch is shown in Fig. 6.70. The entire row_{gate} of the pixel upon which the laser shoots is read out in order to subtract the common mode digitally. For comparison, the measurements are performed for the old metal routing (PXD9-6) on W30-OB1 and the new metal routing (PXD9-7) on W31-OF1.

W30-OB1 (old metal system)- Gated Mode without readout

Figure 6.71 shows the results of the measured signal after the GM as function of time of the laser pulse delay setting. The measured ADU values are normalized to the laser signal. The generated charge by the laser corresponds to 3–4 MIPs.

Measurements and Results Five different behaviors can be observed (see Fig. 6.70):

- **0–560 ns:** The laser pulse is shot on the detector before the activation of the GM. The charge stored in the *internal Gate* (before the onset of the GM) is mostly preserved during the GM operation. Up to 4 % of the charge is lost in the pixels of Switcher group region 1 and 2.
- **Falling edges:** When the ClearOn voltage is applied to all pixels, the newly created electrons (by the laser) drift to the *internal Gate*. Depending on the voltage, a fraction of the electrons still accumulates in the *internal Gate*. The edges of Switcher 1 (all four groups) are rather steep. Thus, the pixels are gated within 190 ns. In contrast, the rising times of Switcher 6 are rather flat. It requires approximately 640 ns to apply the suppressed Clear mechanism.
- **1200–1720 ns:** The DEPFETs are gated. All newly created electrons drift to the *Clear region* connected to Switcher 1. In contrast, since the ClearOn voltage is not fully applied at the last Switcher, these pixels are not fully shielded. Roughly 8 % of the charge accumulates in the *internal Gate* for the last Switcher. For this reason the signal level is above 0 ADU.
- **Rising edges:** Disabling the GM the ClearLow potential is applied. Thus, the created electrons (in the silicon bulk) should accumulate in the *internal Gate*. The process takes 200 ns for the first Switcher and approximately 880 ns for the last Switcher. Depending on the ClearOn voltage, the pixel is partially gated.

- **After GM:** Switching back to normal operation (i.e., rolling shutter mode) the charge collection process is activated.

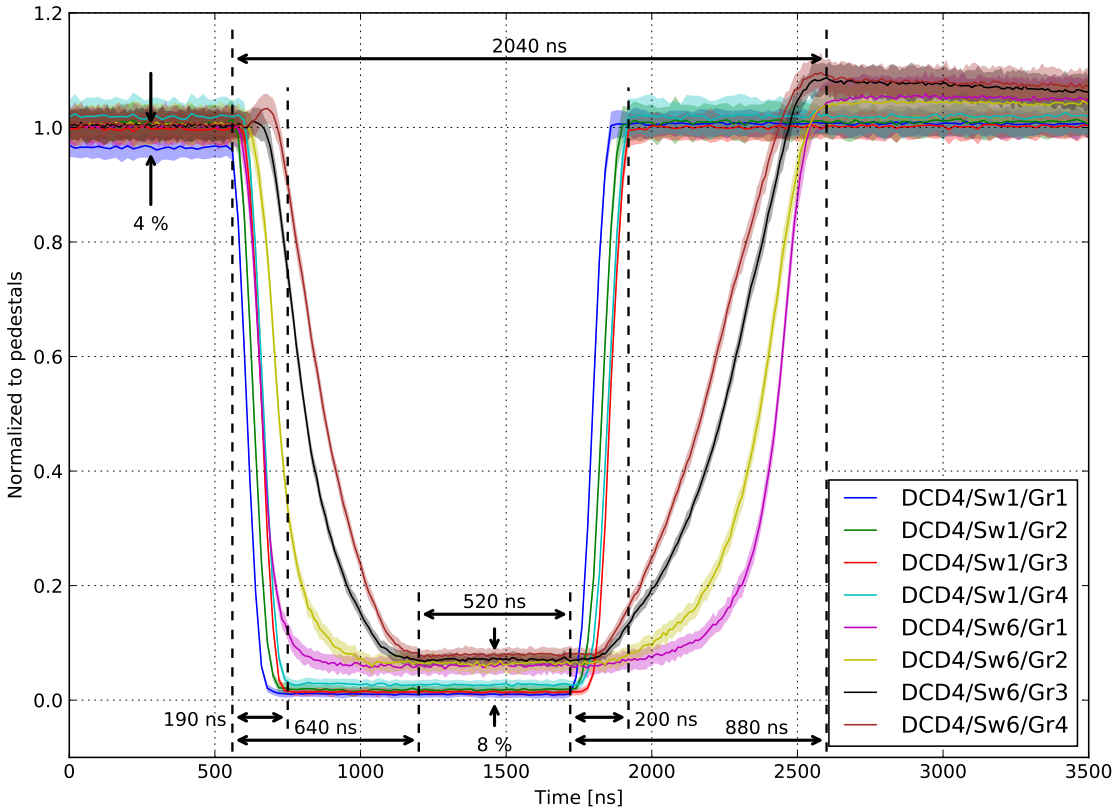


Figure 6.71: Laser sweep for pixels of different Switcher regions (Switcher 1 and 6) and groups (1, 2, 3, 4) on the W30-OB1 for the GM without readout.

As can be seen for Switcher 1, group 1 (blue curve) roughly 4 % of the charge is lost during the GM operation. For the last Switcher some charge accumulates in the *internal Gate* during the GM operation. The amount of collected charge during the suppressed Clear mechanism corresponds to approximately 8 % compared to the normal charge collection mode. As already mentioned above, this is due to the partially applied amplitude of the ClearOn voltage at the last Switcher. Thus, the pixels are not fully shielded. The entire GM sequence requires 2040 ns although the largest fraction of the ClearOn voltage is applied only for 520 ns, where only the pixels connected to the first Switcher are completely shielded. The purpose of this measurement was to see the differences of the ClearOn voltage, applied at the pixels for different Switchers and different activating groups.
The behavior of the slow rising and falling edges is caused by the large ohmic resistance of the Switcher-substrate routing along the module ($\sim 172\,\Omega$). To solve this, a design change (PXD9-7) has been performed in the layout. The routing was broadening resulting in an ohmic resistance of $\sim 27\,\Omega$ for this supply net.

W31-OF1 (new metal system) - Gated Mode without readout

Next, the module with the new metal system (PXD9-7) has been studied (see Fig. 6.72). The module is again operated at full speed (GCK=76.33 MHz). With the new metal system and the reduced ohmic resistance of the sw-Vref net, both Switchers (1 and 6) and all four Switcher sections (1–4) could apply the large ClearOn voltage. This results in a total shielding (gating) of the entire matrix. The pixels connected to the four Switcher groups are shielded within 160 ns. The matrix is completely protected for 360 ns. Switching back to normal operation takes another 320 ns resulting in a total GM without readout operation of 840 ns. The signals are studied for the DCD, which has the largest distance to the Switchers. All the created electrons by the laser is completely removed. The applied laser signals correspond to approximately 3–4 MIPs.

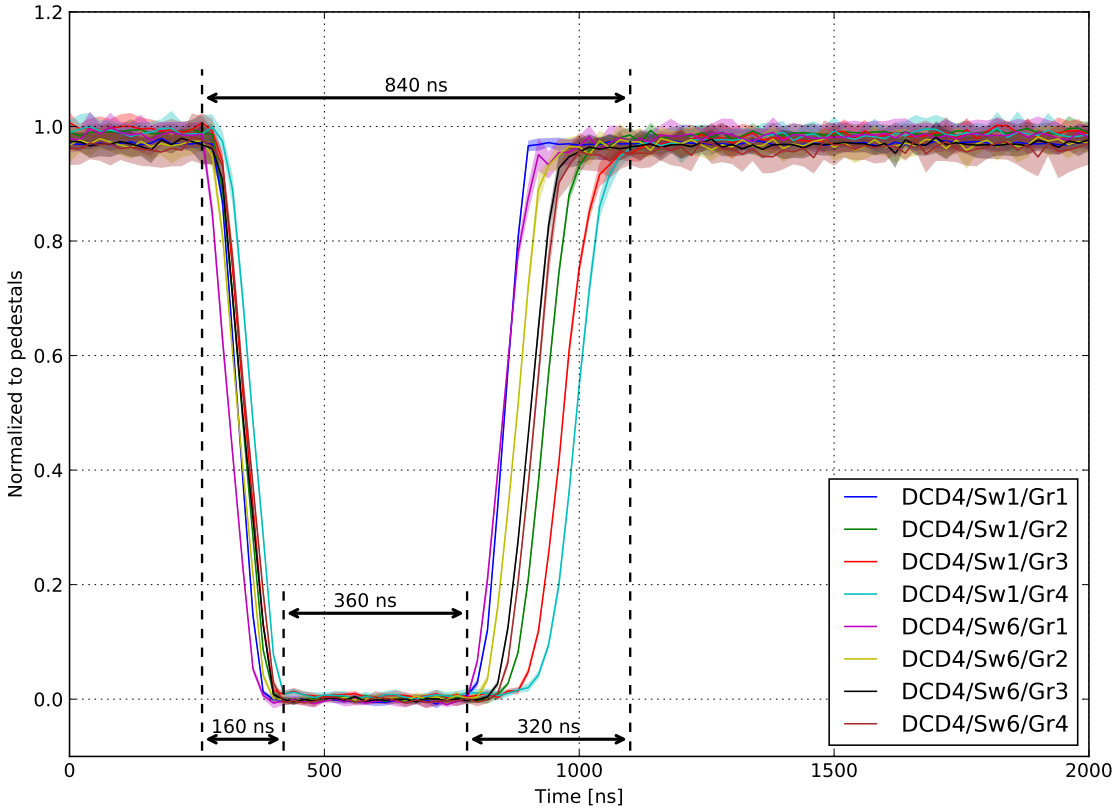


Figure 6.72: Laser sweep for pixels of different Switcher regions (Switcher 1 and 6) and groups (1, 2, 3, 4) on the W31-OF1 for the GM without readout.

W31-OF1 - Gated Mode with readout

The same procedure was repeated for the GM with readout sequence. The resulting signals for the different timings of the Switchers are shown in Fig. 6.73. Since the four Switcher groups are enabled subsequently with each Switcher clock of 105 ns, the process to shield all pixels takes 430 ns. The time interval to gate the entire matrix is only 100 ns (the shortest possible gating time period), i.e., the overlap of putting the first and the last Switcher into the GM. The disabling of the GM with

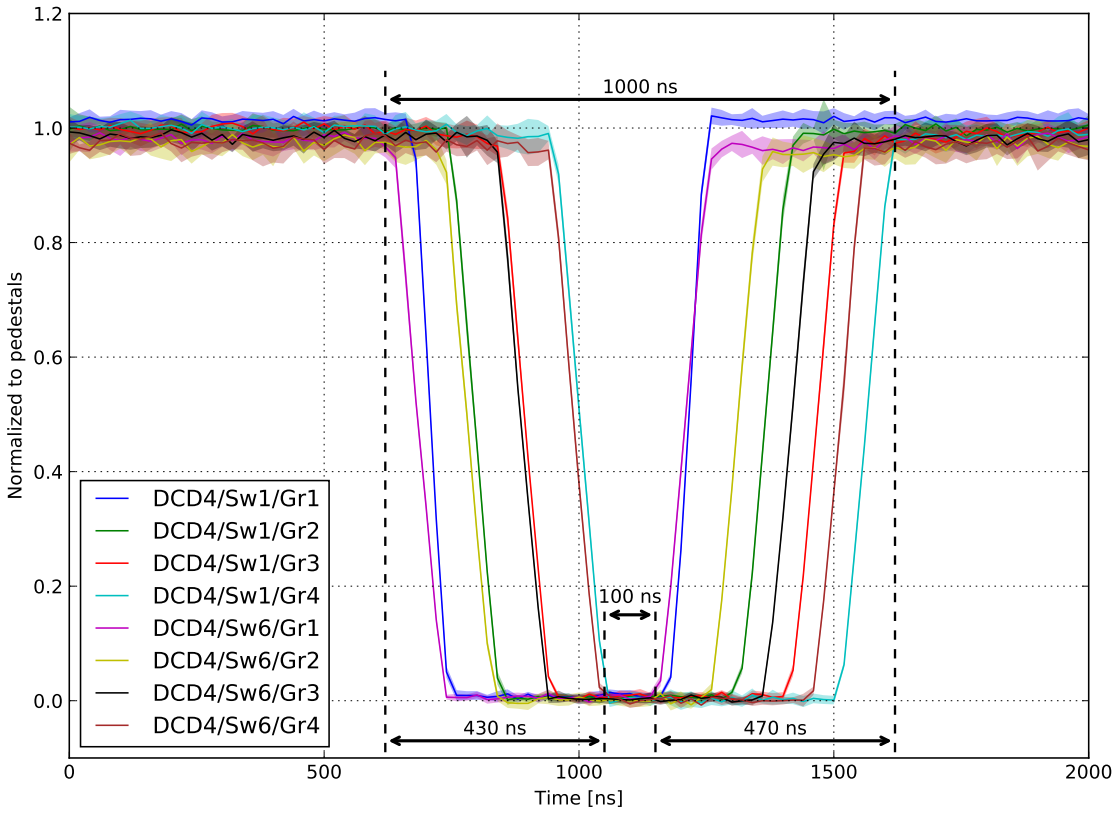


Figure 6.73: Laser sweep for pixels of different Switcher regions (Switcher 1 and 6) and groups (1, 2, 3, 4) on the W31-OF1 for the GM with readout.

readout and switching back to normal operation requires another 470 ns resulting in a total GM operation of 1 µs.
The number of stored electrons in the *internal Gate* should not be changed, i.e., neither additional charge should be collected nor any charge should be removed, when the GM operation is performed. Two different scenarios are studied in the following: the number of removed electrons from the *internal Gate* during the GM, called *signal charge preservation* and the number of additional electrons, which accumulates in the *internal Gate* due to junk charge, called *junk charge prevention*. Both studies are performed for different GateOff, ClearOn and ClearGate voltage combinations. The measurements have been performed with the old metal system (PXD9-6) on module W30-OB1 with the GM without readout sequence. Regarding optimal voltages the GM with and the GM without readout are equivalent since the behavior of the DEPFET pixel sensor is studied. The major difference from the pixel cell point of view is the length of the applied ClearOn voltage. In order to create a signal, a laser shoots at the matrix for a few tens (< 50 ns) of nano seconds.

6.12.10 Signal Charge Preservation

A certain number of electrons are accumulated in the *internal Gate* before the onset of the GM. During the GM, electrons should not be removed from the *internal Gate*, i.e., the number of stored electrons should not be diminished. The study of

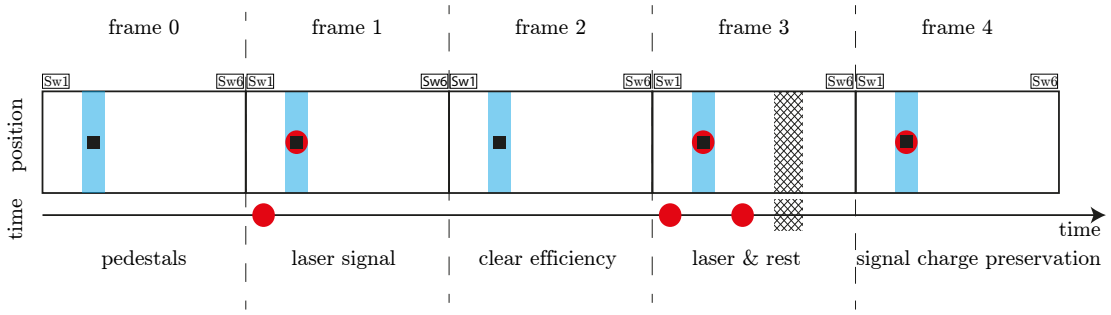


Figure 6.74: Five consecutive frames are read out in the rolling shutter mode. The first frame (0) serves as reference frame, i.e., pedestal values. Frame 1 reveals the laser signal. Frame 2 allows studying the Clear efficiency. In frame 3 charge is created in a pixel and the GM is activated. In frame 4 the remaining charge is measured.

this behavior is called *signal charge preservation (SCP)*.

The procedure of the measurement is presented in the following. Five consecutive frames are recorded. A sketch of the sequence is shown in Fig. 6.74.

- **frame 0:** Normal operation, i.e., rolling shutter mode. The signals recorded in this frame are pedestal values.
- **frame 1:** Normal operation, i.e., rolling shutter mode. The laser light is switched on a pixel (row_{geo}, col_{geo}) before this pixel is read out. Consequently, the charge generated by the laser is determined. After having recorded the Drain current, the Clear pulse is applied to reset the DEPFET pixel.
- **frame 2:** Normal operation, i.e., rolling shutter mode. In the case of inappropriately chosen voltage combinations for ClearOn and ClearGate, the charge previously stored in the *internal Gate* has not been removed completely when applying the Clear pulse in frame 1. Thus, some electrons still remain in the *internal Gate*. This leads to a signal in frame 2. This frame is also suited for Clear efficiency studies.
- **frame 3:** The laser is switched on again and the data is read out. The generated charge is measured. In the case the Clear efficiency is below 100 %, the signal in frame 3 is even higher than in frame 1. This will be used as a reference signal. After the readout (and applying the Clear pulse), the laser is switched on again on the same pixel. The GM is enabled for $\sim$ 400 ns (gray hatched area in Fig. 6.74).
- **frame 4:** The pixel is read out again. Comparing the two frames (4 and 3) yields the amount of "lost" charge during the operation of the GM.

Figure 6.75 shows the difference between frame 4 and frame 3 for various ClearGate voltages. The difference reveals the charge that was lost during the GM operation. The signal of frames 1–4 are shown in app. C.8.
The behavior of the sensor can be grouped into three regions (see Fig. 6.76) characterized by different ClearOn, ClearGate and GateOff voltage combinations:

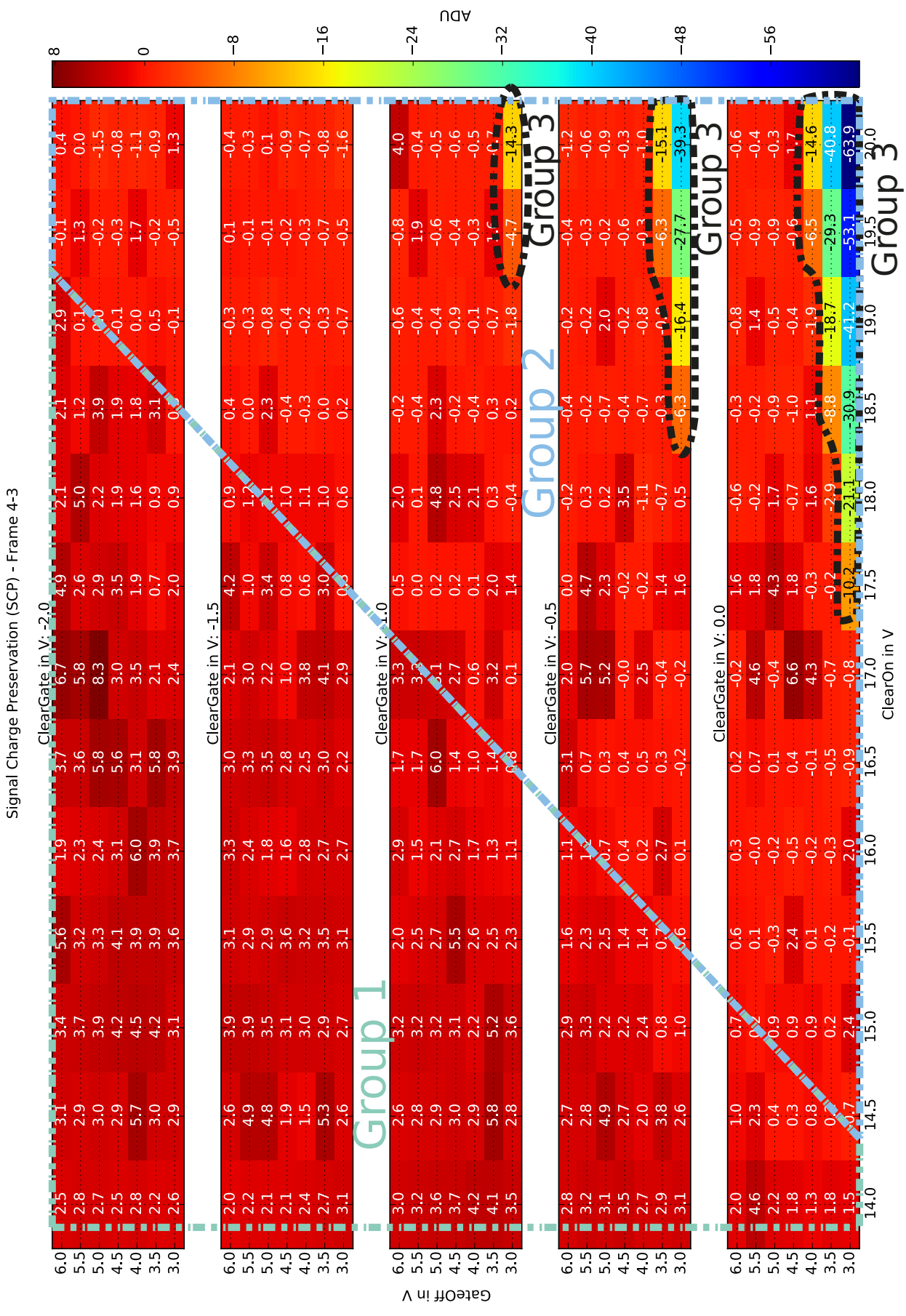


Figure 6.75: Study of the signal charge preservation for different combinations of ClearGate, GateOff and ClearOn voltages. The difference between frame 4 and frame 3 is plotted (see Fig. 6.74).

- The first group is for low ClearOn voltages. The charge stored in the *internal Gate* is removed step-by-step with each Clear cycle. A small fraction of the electrons remains, although the Clear pulse was applied thousands of times. According to Fig. 6.75 it seems that additional charge is added to the *internal Gate* during the GM operation. This is actually not the case (see Fig. 6.76): In frame 1 the laser pulse creates a certain amount of charge. This amount of charge is independent from the voltage combinations (ClearOn, ClearGate). After reading the pixel the Clear pulse is applied. As already observed in the Clear efficiency studies (see Sect. 6.10) not all electrons that are stored in the *internal Gate* are removed for certain ClearGate and ClearOn voltage combinations. Applying the Clear pulse twice (in frame 2), more charge is removed from the *internal Gate* but still not all. In frame 3 the laser creates the same amount of charge as in frame 1. Thus, one can see the remaining charge (after applying two Clear pulses from frame 1 and frame 2) and the additional charge created by the laser in frame 3. Applying the Clear pulse again in frame 3 (after the readout), a fraction of the charge stored in the *internal Gate* is removed. The rest charge (in the *internal Gate*) is not the same as in frame 2, since the additional charge that has not been removed in frame 2 is added. Having applied the Clear pulse in frame 3 (after readout the pixel), the laser creates again electron-hole pairs. Before switching into the GM, the amount of charge stored in the *internal Gate* is approximately the same as the signal that has been read out in this frame (frame 3). It is slightly more, because the Clear pulse was only applied once. Having read out the pixel in frame 3, the Clear pulse was applied twice. This additional charge appears in frame 4, which is also seen in the difference of frame 4 and 3.

- The second group is for low ClearOn voltages that are greater than those in group 1, where the signal difference is approximately 0 ADU. As was shown in Fig. 6.43, the Clear efficiency for those voltage combinations is $\geq\sim 95\,\%$. For the voltage combinations with 100 % Clear efficiency, the charge in frame 3 before enabling the GM corresponds to the same amount of charge which is stored in the *internal Gate* in frame 3 before reading out the pixel. These voltage combinations correspond to the optimal operation voltages.

- The third group is determined by charge loss, i.e., in frame 4 there is less charge stored in the *internal Gate* as in frame 3. This strongly depends on the ClearGate voltage. If it is too positive, electrons can overcome the potential barrier (between the *internal Gate* and the *Clear region*) and can drift from the *internal Gate* to the *Clear region*. The more positive the ClearOn voltage, the more attractive the *Clear region* becomes. In addition, the lower (less positive) the GateOff voltage, the more the potential of the *internal Gate* is shifted such that the barrier (caused by the ClearGate) decreases.

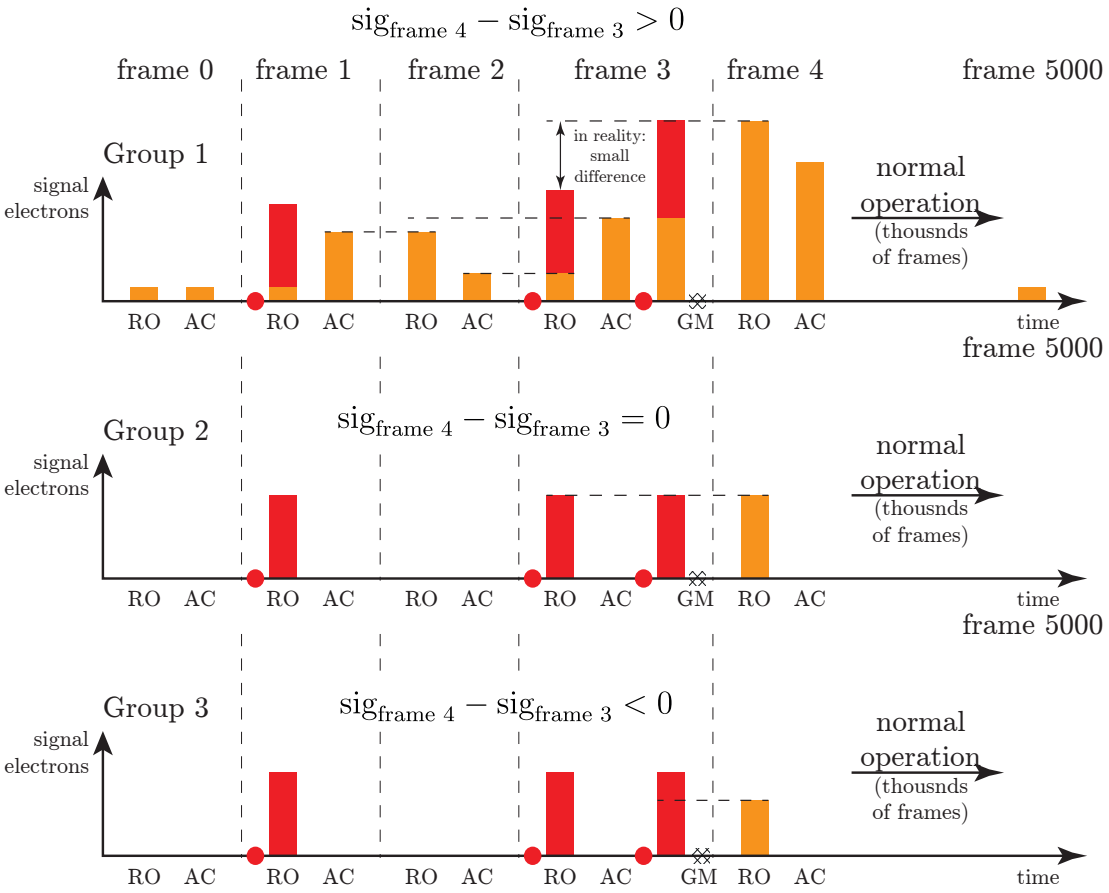


Figure 6.76: Illustration of the results of the three groups of the signal charge preservation measurement. The number of electrons that is read out is abbreviated as *RO*, while the number of electrons after applying the Clear pulse is called *AC*. The GM is applied in frame 3. The laser shoots at the matrix in frame 1 and frame 3 (two times).

6.12.11 Junk Charge Prevention

During the GM operation, newly generated charge (*junk charge*) should drift directly to the *Clear implant* and should not accumulate in the *internal Gate*. Detailed voltage scans are performed in order to study the operational voltages for the this scenario, called *junk charge prevention (JCP)*. This time a laser shoots at the DEPFET matrix during the GM operation, emulating noisy particles, which create electron-hole pairs in the silicon bulk. Five consecutive frames are recorded with a time sequence as shown in Fig. 6.77. The procedure is presented in the following. Again, five consecutive frames are recorded.

- **frame 0:** Normal operation, i.e., rolling shutter mode. The signals recorded in this frame are pedestal values.
- **frame 1:** Normal operation. The signals recorded in this frame are pedestal values.
- **frame 2:** Normal operation. The laser light hits the pixel before it is read out. The generated charge is measured in this frame. In the case of inap-

propriately chosen combinations for ClearOn and ClearGate voltage combinations, some charge could remain in the *internal Gate* although the Clear pulse is applied.

- **frame 3:** The same pixel is read out again. The Clear efficiency can be studied by comparing this frame with frame 2. After having read out this pixel the GM is enabled for $\sim 400\,\text{ns}$ (gray hatched area in Fig. 6.77). During that time, the laser is switched on again (emulation of noisy particles).
- **frame 4:** Normal operation. In the ideal case the charge should be the same as in frame 3.

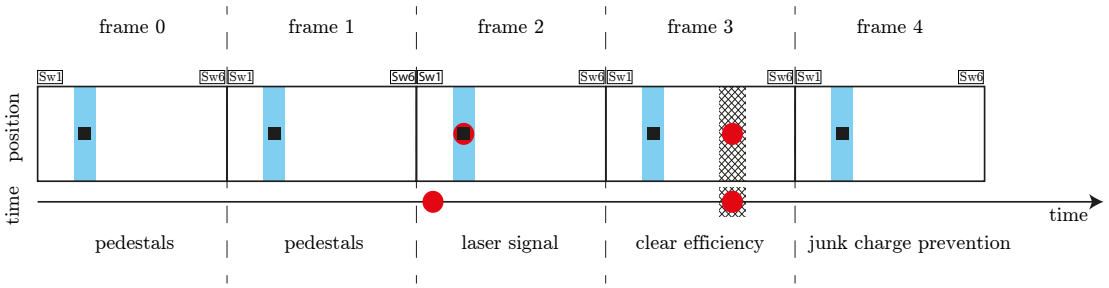


Figure 6.77: Five consecutive frames are read out in the rolling shutter mode. The first and second frames (0 and 1) serve as reference frame, i.e., pedestal values. Frame 2 reveals the laser signal. Frame 3 allows studying the Clear efficiency. Charge is created during the GM. In frame 4 the additional junk charge is measured.

In order to calculate the additional charge from the laser during the GM operation, frame 3 is subtracted from frame 4. The difference for various voltage combinations of ClearGate, GateOff and ClearOn is shown in Fig. 6.78.
It can be grouped into two regions:

- The first group is for low ClearOn voltages. According to Fig. 6.78 additional charge is added to low ClearOn voltages. The measured signal must be interpreted as a combination of two effects. On the one hand, the generated junk charge accumulates in the *internal Gate*. On the other hand, not all electrons are removed from the *internal Gate* within one Clear cycle for low ClearOn voltages. Some fraction of the charge is removed gradually, with subsequent Clear mechanisms, corresponding to frame 2 and frame 3. Group 1 can be divided into three subgroups to explain the results. Figure 6.79) shows qualitatively the electrons stored in the *internal Gate* when the DEPFET pixel is read out (RO) and after having applied the Clear pulse (AC).

  Group 1a are the regions in Fig. 6.78 with positive ADU values. Assuming a not completely empty *internal Gate* (since the ClearOn voltage is too low to attract all electrons from the *internal Gate* to the *Clear implant*) in frame 1 the laser creates electrons in frame 2, which are collected in the *internal Gate* and visible in frame 2 (see Fig. 6.79a). This increases the signal, which is read out (frame 2-RO). After having sampled the Drain current, the Clear pulse

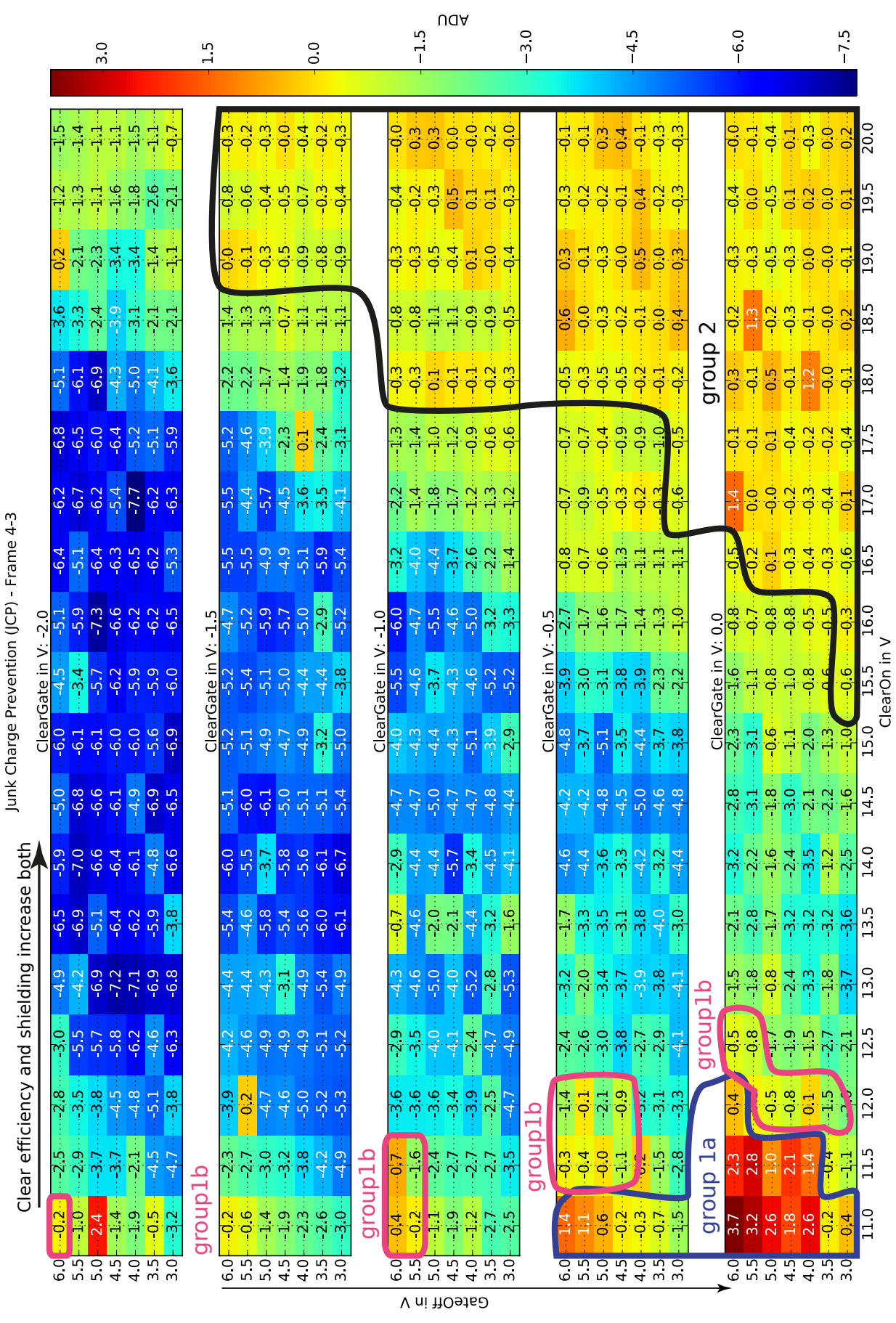


Figure 6.78: Study of the junk charge generation for different combinations of ClearGate, GateOff and ClearOn voltages. The difference between frame 4 and frame 3 is plotted (see Fig. 6.77).

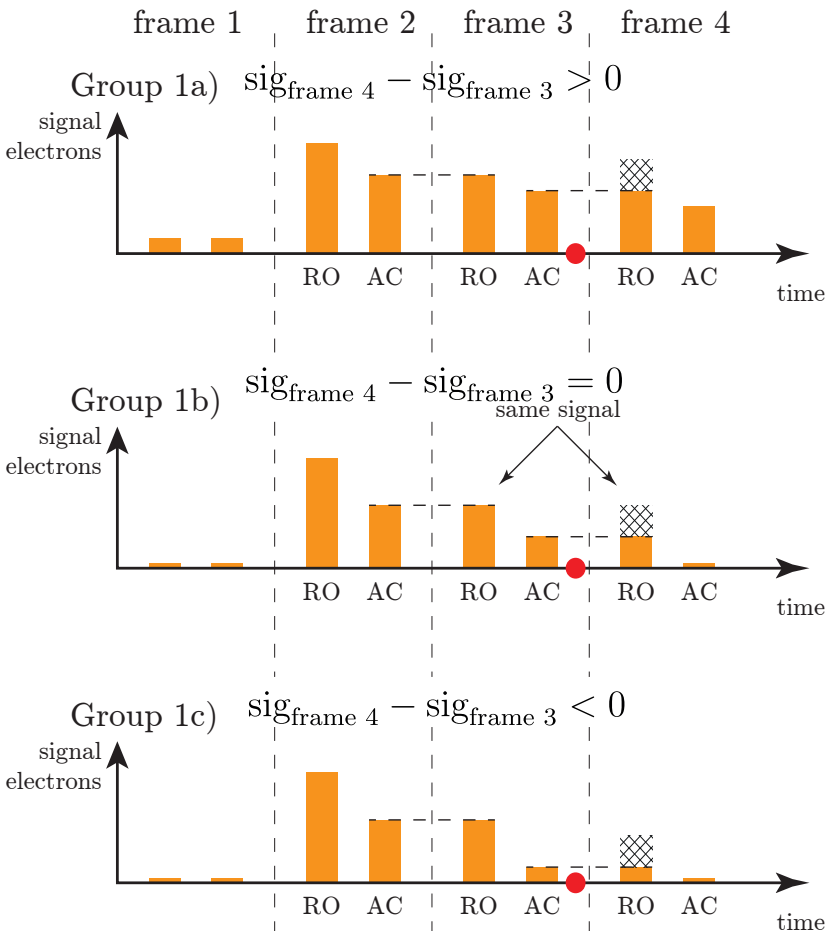


Figure 6.79: Junk charge prevention measurements: the number of electrons stored in the *internal Gate* for the different frames (see Fig. 6.77) are qualitatively shown. For each frame the number of electrons which are read out (RO), i.e., the measured signal, and the number of electrons after having applied the Clear pulse (AF) are shown for the three different groups. The red dot represents the laser, which is applied during the GM. The hatched rectangles correspond to the additional electrons accumulating in the *internal Gate* by the laser during the GM operation.

is applied. Since the ClearOn voltage is low, only a fraction of the stored electrons move to the *Clear implant* (frame 2-AC). In frame 3 the number of the remaining electrons corresponds to the readout signal (frame 3-RO). Having applied the Clear pulse, again only a fraction of the stored electrons move to the *Clear implant*. Afterwards the GM is enabled and the laser shoots at the matrix. Since the pixel is not completely shielded, additional electrons drift to the *internal Gate*. Reading out the signal of frame 4, it is larger compared to the one in frame 3.

Group 1b shows no signal difference between frame 4 and frame 3 for low ClearOn voltages (11–12 V). The number of electrons stored in the *internal Gate* decreases with each Clear cycle (see Fig. 6.79b). The number of created electrons by the laser drifting into the *internal Gate* in frame 3 (i.e., the pixel is not completely shielded) corresponds to the same number of electrons, which are removed by the Clear pulse. As a consequence, the sum of the

remaining electrons (in frame 3-AC) and the additional one by the laser during the GM results in the same number (frame 4-RO) as the signal read in frame 3-RO.

Group 1c is the largest region in Fig. 6.78. It corresponds to the negative ADU values. The number of electrons stored in the *internal Gate* also decreases with each Clear cycle. The number of additional electrons (created by the laser during the GM) and the number of electrons in the *internal Gate* (in frame 4-RO) is less than the number of electrons that are measured in frame 3-RO, resulting in negative signals in Fig. 6.78.

The two subsequent Clear cycles are in frames 2 and 3. The more negative the ClearGate voltage and the less positive the ClearOn voltage, the less charge is removed within a single Clear cycle. If the Clear pulse is not applied in frame 3, no negative values would be visible in the difference of frame 4 and frame 3. In addition, the amount of junk charge would be further increased, in particular, for less positive ClearOn voltages. Due to the design of the ASIC, a Switcher sequence without applying the Clear pulse in frame 3 is not possible.

- The second group shows almost no difference in the signal, i.e., the amount of charge stored in frame 3 is the same as in frame 4. In this case the *internal Gate* is completely shielded and the created electrons move directly to the *Clear implant*. These voltage combinations correspond to the optimal operating voltages, which are marked by the black area in Fig. 6.78, i.e., ClearOn voltages equal or larger than 15.5 V, ClearGate more positive or equal than −1.5 V and any GateOff voltage between 3–6 V.

6.12.12 Summary of the Gated Mode and Outlook

The voltages for the GM operation have to be chosen such that on the one hand, the signal is preserved, and on the other hand, the *internal Gate* must be protected from junk charge. Only voltages for which the *internal Gate* is emptied completely by applying the Clear pulse once must be considered, i.e., 100 % Clear efficiency. The ClearGate should be chosen around −0.5 V. The ClearOn must be at least 18 V to ensure a proper Clear mechanism. The GateOff voltage should be 5 V.

With the PXD9-6 layout on module W30-OB1 and the latest electronics, the required time for applying the GM without readout is approximately 2 µs (gate the pixels and switching back to normal operation) while the goal for the operation in Belle II is to achieve 1 µs. The main reason for the flat rising and falling edges of the Clear pulses during the GM operation, in particular, for the last Switcher and the last Switcher groups, is the metal routing for the Switcher-substrate net, which is rather narrow resulting in a high ohmic resistance ($\sim 55\,\Omega$ for Switcher 1 and $\sim 172\,\Omega$ for Switcher 6). The problem was identified and the metal routing has been changed (from PXD9-6 to PXD9-7), i.e., the substrate routing has been widened in order to decrease the ohmic resistance to $\sim 10\,\Omega$ for Switcher 1 and $\sim 27\,\Omega$ for Switcher 6.

Measurements of the two modules W30-OB1 (old metal system) and W31-OF1 incorporating the new metal layout showed that the GM without readout could be shortened considerably from 2 µs (W30-OB1) to 840 ns (W31-OF1). The 840 ns include the rising and falling edges of the applied ClearOn voltage and the gating of all DEPFET pixels (approximately 360 ns). The gating time for all pixel is adjustable by increments of 3.27 ns. Additionally, oscillations in the DCD occur, caused by the increased Drain currents during the applied ClearOn voltage (of approximately 20 V, relative to the Source voltage). Taking these pedestal oscillations into account and assuming to shield all DEPFET pixels for 200 ns results in a total GM time of approximately 1.5 µs. However, the GM without readout has a serious "missing next frame problem." If the GM operation is active when the `SerIn` signal is sent by the DHP, the Switcher "ignores" this signal because the Switcher `Clock` is *low*. Consequently, the next frame will not be read out and the integration time doubles from 20 µs to 40 µs. A design change of the Switcher logic is required to enable the GM in the last $\text{rows}_{\text{gate}}$ of the last Switcher.

In order to solve this problem, the GM with readout is the preferred operation mode. The Switcher `Clock` is always toggling such that every received `SerIn` signal is processed correctly, i.e., the rolling shutter mode always continues, also during the GM operation. The major disadvantage is the elongated time for switching on the four Switcher groups, which happens every 105 ns. Consequently, measurements showed that the entire GM with readout requires 1 µs, where all pixels are shielded for only 100 ns. The shielding time for all pixels can be extended by increments of 105 ns. Additional oscillations of the DCD results in a total of 2 µs.

Comparing these two GM operation modes, the GM without readout is 0.5 µs faster than the GM with readout. However, the GM without readout has the problem of the "next missing frame" and cannot be used.

A new Switcher version (SwitcherB18v2.1) was produced with improved output drivers such that the ClearOn voltage should be applied even faster, resulting in even steeper voltage edges. This should shorten the GM operation somewhat. Furthermore the new DCD version (DCDB4.2) is assembled on the module W31-OF1. The DCD might be more optimized in order to decrease the damping time of the pedestal oscillations. Studies are ongoing, but the chances are small to reach the required 1 µs.

The optimal ClearOn, ClearGate and GateOff voltages have been determined for the PXD9 sensor matrix (module W30-OB1) to preserve the signal charge over the GM operation and to shield the pixel from additional junk charge.

The amount of charge drifting to the *internal Gate* during the GM operation as function of the laser position would be interesting to study. When the laser penetrates the silicon close to the *internal Gate*, more charge should accumulate in the *internal Gate* compared to the case where the laser creates electron-hole pairs in the drift region. Therefore, the laser spot should hit the matrix from the backside, which is without any metallization or polysilicon structures. A new fabrication of the mounting and cooling jigs is currently ongoing to perform these studies.

6.13 Conclusion of the Pilot Run Modules

In this chapter the measurements and results for the characterization of the pilot run module W30-OB1 have been presented. In addition, the GM has been studied on the W31-OF1 module with the improved metal routing.

For these studies a software framework for the control and read out of the sensor modules has been developed. The measurement procedures, analysis and optimization algorithms for a proper operation of the modules, which were established, can be used for the complete characterization of the final modules, which will be produced for the pixel vertex detector[17].

A proper synchronization between the six control and the eight readout ASICs was achieved. The inter-ASIC communication has been studied and optimization algorithms for proper data transmission between DHP and DCD have been elaborated.

Some issues with the DHP harmed the operation at the nominal clock frequency of 76.33 MHz with the W30-OB1. First, the high-speed links to the DHE were not stable for the data transmission from the sensor module. Second, transmission errors between the DCD and DHP required the system to be run at a $\sim 20\,\%$ slower global clock, corresponding to 62.5 MHz. Another issue is the phase shift between the global clock and the generated clocks for the DCDs within the DHP. This effect causes shifts in the sampling point as function of time to a maximum of 12 ns. These problems have been recognized and are solved in the latest version of the DHP.

The metallization system regarding the interconnections between the 14 ASICs, the 192,000 DEPFETs and the Kapton cable has been tested and verified with the pilot run modules. The edges of the applied ClearOn voltage for the GM, which is designed to be roughly 30 ns in the simulations, were rather flat (up to 880 ns) depending on the Switcher position on the module W30-OB1. In addition, the pixels connected to Switcher 6 furthest away from the end-of-stave could not be completely shielded. The problem has been identified and solved. Due to the unexpected high current of the Switcher-Vref net, which was stated to be a factor of 60 lower than the measured value of $\sim 30\,\mathrm{mA}$, and the high ohmic resistance ($\sim 172\,\Omega$) of the metal routing (PXD9-6) on the module, a voltage drop of the Switcher-Vref net occurred along the Switchers. Consequently, the level shifters of Switcher 6 did not work properly. Due to changes in the metal layout (to PXD9-7) the resistance was reduced by roughly a factor of seven to $27\,\Omega$.

Measurements with the W31-OF1 module, incorporating the changed metal routing PXD9-7, have shown steep edges of the applied Clear pulses (160–320 ns). Thus, the GM can be activated and deactivated below 1 µs to shield the detector from noisy bunches during the cooling process of the top-up injection. After switching back from GM to normal operation, however, the DCD starts to oscillate. This means that the time interval for applying the GM without readout, shielding all DEPFET pixels for 200 ns and reading out pixels afterwards, requires in total approximately 1.5 µs.

[17] Minor changes may be required due to small changes in the digital logic blocks of the ASICs.

In the course of investigations, a Switcher logic problem has been found, which prevents the GM operation without readout from being enabled at the end of the frame readout. Otherwise, the integration time would be doubled to $\sim 40\,\mu s$ at the nominal clock of 76.33 MHz. For this reason, the GM without readout cannot be used in the PXD. This problem does not exist when the GM operation with readout is used. The drawback is an extended GM sequence, which enables (and disables) the four Switcher groups within 430 ns. This results in approximately 1 µs to enable the GM and shield all DEPFET pixels. Taking the DCD oscillations into account, the time interval for applying the GM with readout, shielding all DEPFET pixels for 200 ns, and reading out pixels afterwards requires in total around 2 µs, which exceeds the requirement of 1 µs imposed by Belle II.
In order to reduce cross-talk and avoid transmission errors between the DCD and the DHP, the spacing between the metal traces on the modules has been increased from 4 µm to 21 µm. The change in the metal system is also included in PXD9-7. In addition to this, a sophisticated power up (down) sequence for detector module has been developed. It ensures a safe operational procedure to put the modules into operation.
The I-V curves of the DEPFET pixels on the pilot run module W30-OB1 have been recorded, revealing information about the threshold voltages and providing information about the operational parameters. This becomes important with increasing radiation doses, which in particular, causes surface damages to the silicon oxide.
Moreover, the voltage settings have been selected for an optimal performance by carrying out thorough measurements with a radioactive Cd-109 source. Signal-to-noise ratios between 40–50 could be achieved by using appropriate voltages. The contributions of the noise have been studied and minimized by the assembly of decoupling capacitors for filtering the common mode noise.
Further measurements regarding in-pixel studies should be performed in order to see the charge sharing and charge collection behaviors. In addition to this, the shielding of the *internal Gate*, by switching into the Gate Mode operation, depending on the position of the traversing noisy particle (which could be emulate by an infrared laser, illuminating from the backside) would be interesting to study. This could even reduce the operation voltage windows to achieve a homogeneous behavior for a large part of the entire active sensor volume.

Chapter 7

Beam Test

7.1 Introduction

Prototype modules of the PXD were operated in an electron beam at the DESY facility between April and May 2016. The goals of the "beam test" were the system integration and practicing the phase 2 commissioning (see Sect. 3.2.8). One module of each of the two PXD layers (IB and OB) was assembled and combined with four layers of the SVD. The goal was to operate a section of the VXD, which includes sensors from all six layers from the interaction point of Belle II to the CDC. A reduced version of the entire readout chain of the VXD was used to verify the correct operation and data acquisition of all of the sub-components, which were developed by different research groups. A downscaled, simplified version of the high-level trigger (HLT), the DAQ, event builder and monitoring were combined. The entire VXD was cooled by a prototype of the final CO_2 cooling unit. All sub-detectors, the cooling unit, the power supplies and environmental sensors were controlled by a common slow-control system. The purpose of the beam test was to verify not only the combination of the individual hardware components, but also the integration of the different software parts. Furthermore, the online event reconstruction, tracking, data quality monitoring and the determination of ROIs were the tasks and validations for the software group.

The DESY beam test facility provides an electron beam between 1–6 GeV with a particle flux of up to 3 kHz. In addition, a solenoid with variable magnetic field of up to 1 T, which is oriented at 90 ° horizontal to the incident electron beam, can be activated.

7.2 Setup

The PXD modules are mounted on the SCB, introduced in Sect. 4.3. Circulating CO_2 (within the SCB) cools the readout and control ASICs. A picture of the assembly is shown in Fig. 7.1. Four SVD ladders are placed on top of the DEPFET sensor. A CAD drawing of the arrangement of the ladders SVD layers and the two PXD ladders is shown in Fig. 7.2.
For the beam test campaign, the two backward PXD modules were installed. The sensor properties of the different VXD ladders, which are used in the beam test campaign, are briefly listed in the following:

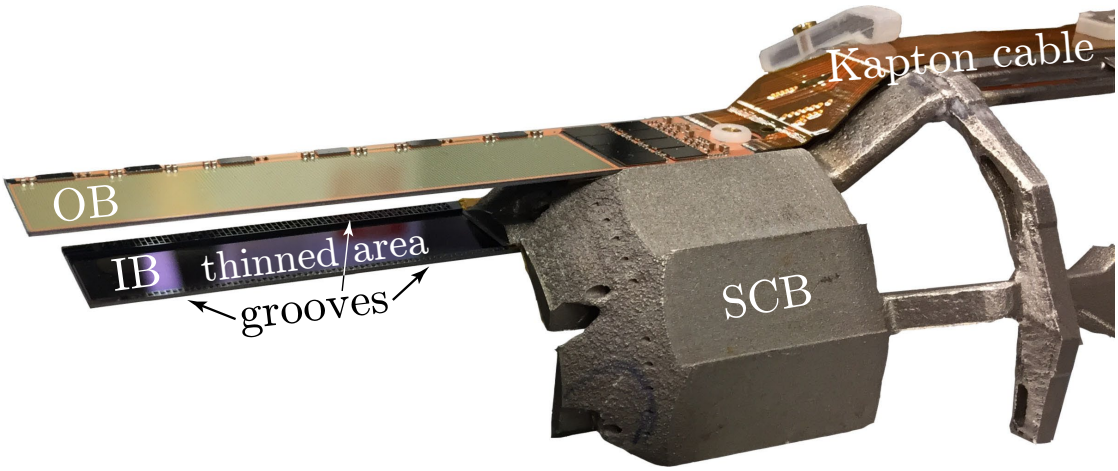


Figure 7.1: Both PXD modules (IB and OB) are mounted on the SCB, which cools the readout ASICs at the end of the modules. Kapton cables connect the modules to the data acquisition system and the power supplies.

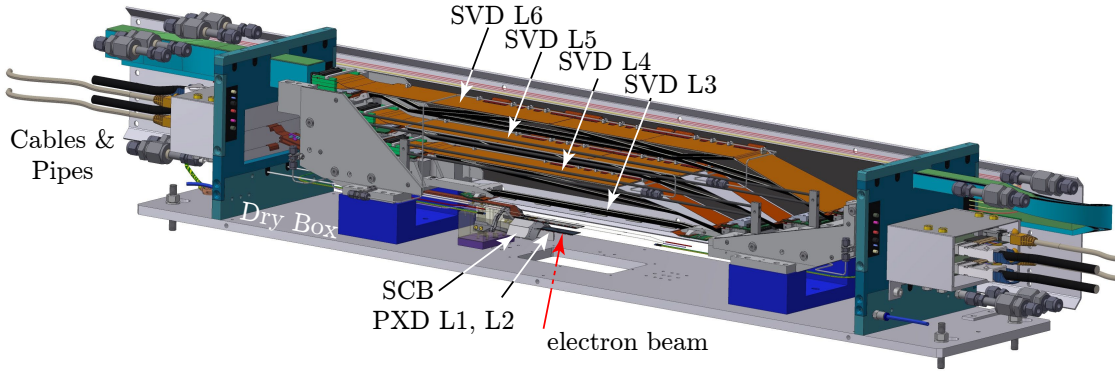


Figure 7.2: CAD drawing of the combined PXD (inner and outer backward modules) and four SVD ladders for the beam test [1]. The particles pass the entrance window (hole in the aluminum on the bottom part) and move in the upward direction.

Layer 1 PXD inner backward module: The inner backward module is the first layer of the stacked sensor arrangement for traversing particles. The sensitive area is $12.50 \times 44.80\,\mathrm{mm}^2$. The pixel sizes are $55 \times 50\,\mu\mathrm{m}^2$ and $60 \times 50\,\mu\mathrm{m}^2$.

Layer 2 PXD outer backward module: The outer backward module is the second silicon detector layer. Its sensitive area is $12.50 \times 61.44\,\mathrm{mm}^2$ and the pixel pitches are $70 \times 50\,\mu\mathrm{m}^2$ and $85 \times 50\,\mu\mathrm{m}^2$.

Layer 3 The third layer of the VXD corresponds to the innermost layer of the SVD. The sensitive area is $123 \times 38\,\mathrm{mm}^2$. It is equipped with 768×768 strips. The pitches are $50\,\mu\mathrm{m}$ for the p-side and $160\,\mu\mathrm{m}$ for the n-side.

Layer 4 (also ladder 5 and 6): The remaining three layers of the SVD each have a sensitive area of $7442.85\,\mathrm{mm}^2$ and are equipped with 768×512 stripes (p-side and n-side). The pitches are $75\,\mu\mathrm{m}$ for the p-side and $240\,\mu\mathrm{m}$ for the n-side.

The sensitive area of the PXD modules is 75 µm thick, while the silicon of the sensitive SVD modules are 320 µm thick. The PXD sensors are connected with a Kapton cable to a PCB, called a patch panel. The data cable (Infiniband) and power cable are connected to this PCB. The setup is the same as in the lab, which is shown in Fig. 6.2. The two sensors, W30-IB and W35-OB1, are used. They were delivered very shortly before the start of the beam test. For this reason, no detailed optimization and characterization could be performed in advance. Due to the limited amount of time, it was even not possible to fully characterize the modules during the beam test campaign. However, the inter-ASIC communication, in terms of proper data transmission between DCD and DHP, was optimized. The nominal voltages, which were listed in Tab. 6.7, were applied. The offset correction and analog common mode correction were disabled. Furthermore, the DCDs were not optimized in terms of INL, DNL and missing codes. Default settings for all DCDs have been applied, based on the experience with the previous pilot run module, introduced in chapter 6.

Three EUDET telescope layers each are placed in front and behind the stacked PXD–SVD system. The telescope consists of six CMOS sensors, called MIMOSA, with a pixel size of $18.4 \times 18.4\,\mu m^2$ and an active area of $21.2 \times 10.6\,mm^2$ [202, 203]. It offers an excellent track resolution of the traversing particles due to its low material budget. The DUT (in this case the combined parts of the PXD and SVD) is mounted between the three telescope layers in front and the three telescope layers behind. Two scintillators are mounted in front and behind the entire arrangement. A sketch of the setup is shown in Fig. 7.3. Additional sensors controlling the temperature and humidity were installed around the test setup. A cover encloses the entire VXD system (without the telescope and without the scintillators). It is flooded by dry nitrogen. The entire structure is placed within a 1 T solenoid. A photo of the complete detector system before placing it into the coil is shown in Fig. 7.4. The incoming electron beam hits the magnet coil

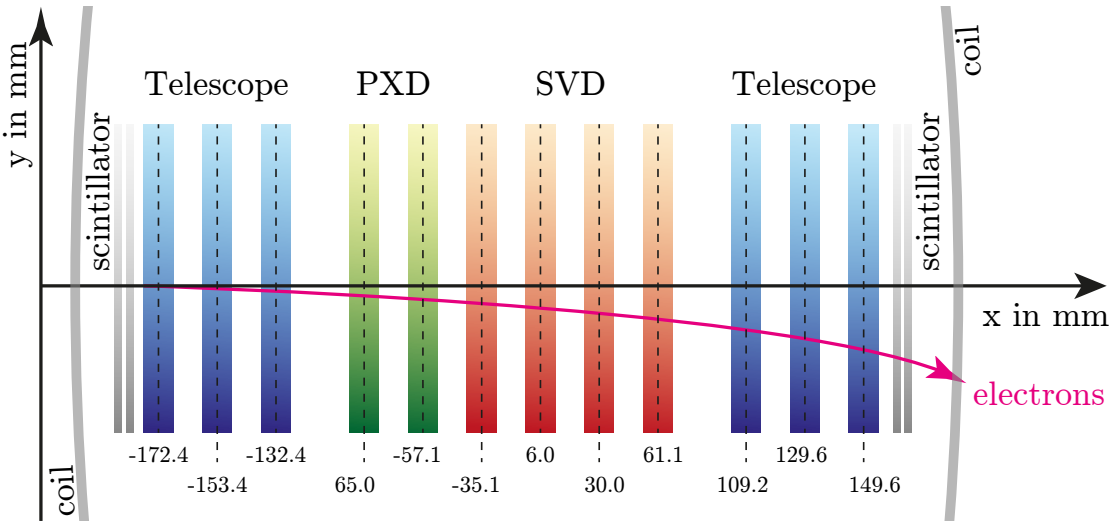


Figure 7.3: Arrangement of the detectors in the beam test. The beam hits the coil of the magnet. The particles pass the detector from the left and are bent by the magnetic field [204].

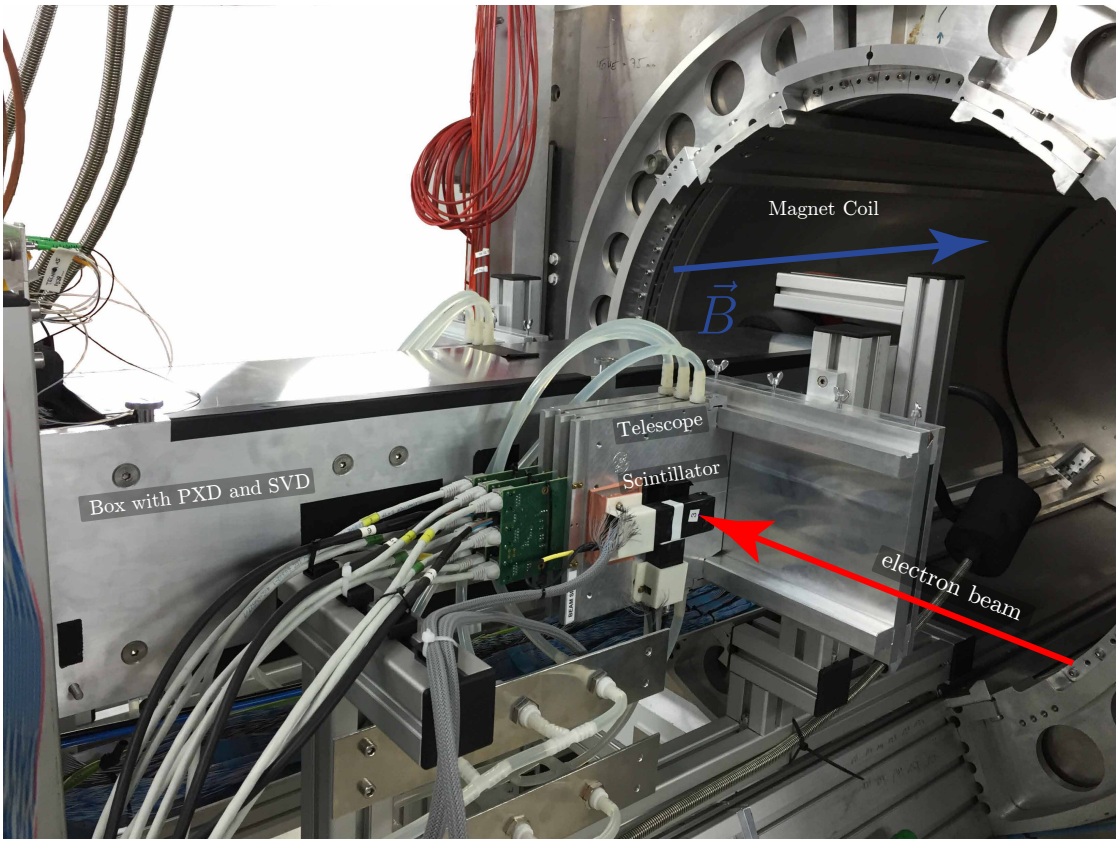


Figure 7.4: Installation of the stacked detector system. The PXD and SVD modules are enclosed in a box, which is flooded by dry nitrogen. The content of the box is shown in Fig. 7.2. The entire arrangement is put into the magnetic coil, which generates a magnetic field of up to 1 T.

and creates bremsstrahlung. This results in a broad momentum distribution of particles traversing the sensors.
The readout of the VXD chain is triggered by coincidence of the scintillators. The entire data acquisition chain is shown in Fig. 7.5. The scintillators are connected to the trigger logic unit (TLU), which sends a trigger to the FTSW. The FTSW distributes the command to acquire data from the sensors to the SVD and PXD readout chains. The ONSEN buffers the PXD data (at maximum for 5 s) until the ROIs are determined by the HLT and by the data acquisition tracking and concentrator online node (DATCON). A reconstructed track, based on the information from the four SVD ladders, is extrapolated to the active area of the PXD. The intersection point between the extrapolated track and the PXD defines the center of the ROI. An ROI is a rectangular area with a defined length and width. To test the data reduction scheme (see Sect. 4.10 and Fig. 7.5), only clusters that are (partially) within an ROI are read out.

Afterwards, the data from the VXD is further processed, merged with the data from the telescope stream and written to disk. A fraction is immediately processed for the data quality monitor and event display. More details are found in [205]. The DHC has two data output streams: One to the ONSEN, which receives information about ROIs and sends the data to the scaled Belle II DAQ. The other output is a

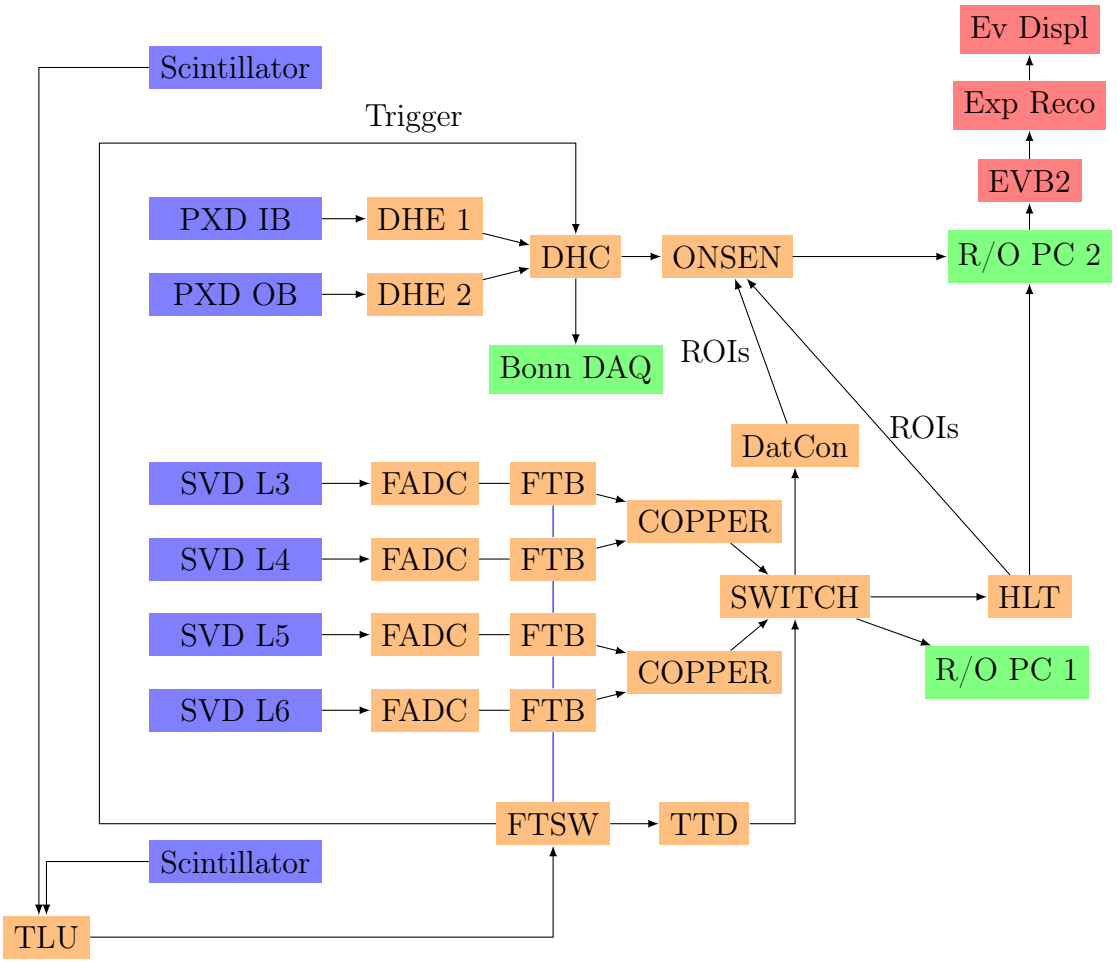


Figure 7.5: Sketch of the data acquisition system. The different sub-detectors are on the left (blue). The scintillators give the command for the readout of data of the VXD and telescope system. The data processing devices (orange) receive the data stream from the detectors, further process the data and send them to the next instance in the acquisition chain. In the end it is written to disk (green) or directly processed for the event display (red).

User Datagram Protocol (UDP) data stream, which is directly sent to a computer running the *Bonn DAQ*. The *Bonn DAQ* is the DAQ system of the lab framework, which can dump all received data to a local disk and thus enables stand-alone data quality monitoring.

7.3 Results

The data is recorded and the analysis is performed offline. Three different software frameworks providing different features are available:

- The Belle Analysis Software Framework 2 (BASF2) framework, used to analyze data in the Belle II experiment [206]. The geometry of the test beam is fully implemented. The track finder does not use the data provided by the

telescope planes. The software is used for the alignment, to study the charge distribution, residuals and efficiencies, tracking and event reconstruction.

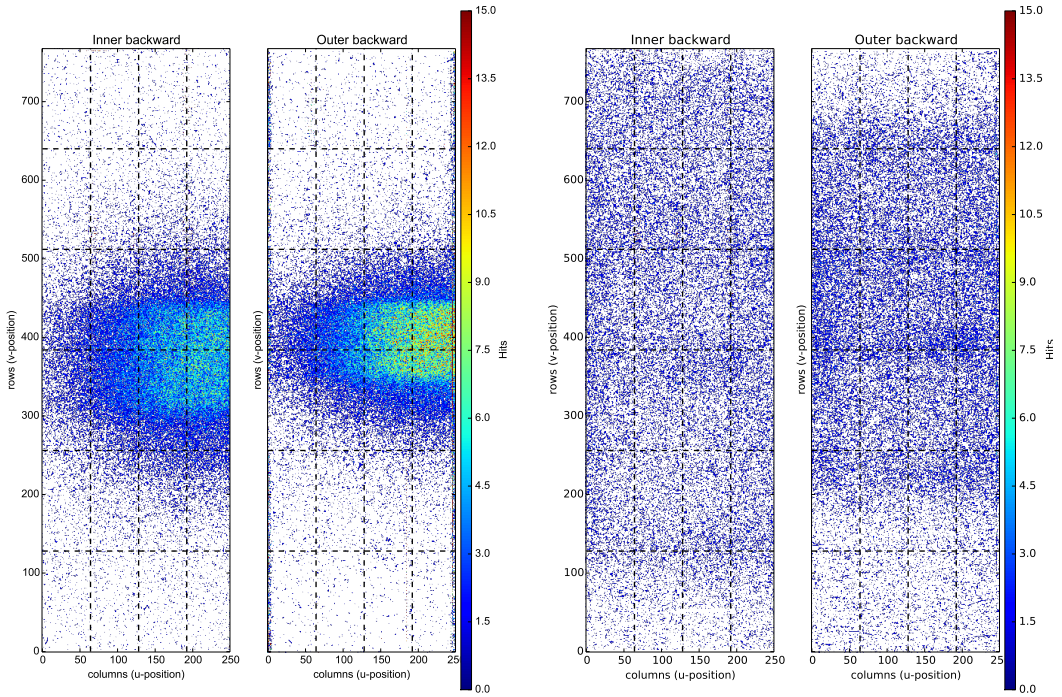
- A dedicated framework to analyze beam test data [207]. It includes the entire geometry of the beam test setup. The data from the PXD layers, the SVD layers and the telescope are merged. Thus, it provides in total twelve layers for tracking. It offers a large spectrum of detailed analyses possibilities, such as in-pixel studies[1], X_0 studies, efficiency studies, residuals or charge distribution.
- The lab framework, which is used to characterize the detector (see chapter 5 and chapter 6) in the lab. It does not provide any tracking, efficiency studies, residuals, etc. It is a stand-alone system. (It could also control multiple modules and performs the data analysis for each module separately). It can be used for charge distribution studies. The data is sent directly from the DHC to the Bonn DAQ. No data reduction in terms of ROIs is performed. For this reason, the data is "unfiltered," i.e., when the DHC receives a trigger, all data is sent from the modules to the computer. Therefore, the number of events is much larger compared to the amount of data, which is written to the reduced Belle II DAQ.

The data is separated into *runs* each with a defined *run number*. A run is a set of recorded data within a user-defined time interval. For each run number, the configuration of the detectors and the environment, such as the electron beam energy and the magnetic field, are constant and documented in a log book. This allows the analysis of the data for various scenarios. Furthermore, the slow control system monitors all voltages and settings, which are applied at the ASICs and reads out the environmental sensors.
The module data recorded in the beam test campaign allows the study of the position resolutions, the efficiencies and the cluster charge distribution and consequently, the internal amplification g_{q} (see Sect. 4.5.1) of the PXD modules. The internal amplification could also be studied in lab with radioactive sources, as shown in Sect. 6.11. In contrast, for the determination of the position resolutions, the position of the traversing charged particle through the module (true hits) must be known. The stacked setup, i.e., the PXD and SVD modules and the telescope system, allows the reconstruction of a *track* such that the position of the incident charged particle in the sensor plane can be calculated. Furthermore, the combined detector system is also required to investigate the efficiencies of the PXD sensors since it must be known whether a charged particle hit the detector.

7.3.1 Hitmap

The hitmap is a 2D-histogram where each bin corresponds to a DEPFET pixel. For each individual pixel, the number of hits above a certain cutoff is counted within a run. This number is color-coded as a third dimension in the hitmap. The events are determined by the HLT and DATCON, as already described in the

[1] Unfortunately, in-pixel studies are not possible for the beam test data since the number of tracks is not sufficient.



(a) Hitmap of the inner backward and outer backward module with disabled magnet and 3 GeV incident beam.

(b) Hitmap of the inner backward and outer backward module with enabled magnet and 3 GeV incident beam.

Figure 7.6: The dashed black lines indicate the regions for the different control and readout ASIC combinations. On the vertical axis, six Switchers control the 768 geometrical rows. Four DCDs read the 250 geometrical columns.

previous section. The triggers are generated by the two scintillators, located in front of and behind the stacked SVD and PXD ladders. They have a rectangular shape. In addition to single beam particle hits, secondary particles can be created with a wide momentum distribution when the incident electron beam traverses the magnet coil.

The hitmaps are plotted for the inner backward and outer backward modules for an incident 3 GeV beam for the two cases: disabled magnet (Fig. 7.6a) and enabled magnet (Fig. 7.6b). A part of the beam spot, limited by the rectangular trigger counter, is clearly visible in Fig. 7.6a. If the magnet is enabled, the electrons are bent in the upward direction in Fig. 7.4. An incident electron beam of 3 GeV, which passes the magnetic coil and traverses the magnetic field for 61.7 cm before hitting the PXD layers, is deflected by 19.1 mm. (The width of the sensitive active PXD area is only 12.5 mm.) The particles are deflected from the higher column numbers in the direction to the lower column numbers in Fig. 7.6. Thus, the main particle beam, which passes the scintillators, misses the sensor. However, an almost homogeneous distribution of hits can be seen along the center part of the PXD ladders. The length of the sensitive area of the outer backward module is 16.64 mm longer than the sensitive area of the inner backward module. As it is clearly visible in Fig. 7.6b, the upper part and lower part of the outer backward module show a

reduced number of hits resulting in lower statistics in those sections. This should be considered when studying the cluster charge distributions and efficiencies for the different Switcher and DCD regions. The two PXD ladders are spaced by 8 mm. Within that spatial difference, the electrons of 3 GeV are deflected additionally by 200 µm, corresponding to four pixels.
The four DCDs have all the same settings, thus the offset and gains are the same four all eight readout ASICs, which are mounted on both modules.

7.3.2 Cluster Charge Distribution

When a particle traverses the detector, the created electrons within the PXD sensor either accumulate in a single pixel or they distribute over multiple pixels, known as *charge sharing*. In the latter case, the pixel with the highest signal is called a *seed pixel*. Only those pixels whose signals are above a defined threshold are read out. The others are neglected.
In this section, the cluster charge is studied. In order to obtain a rough approx-

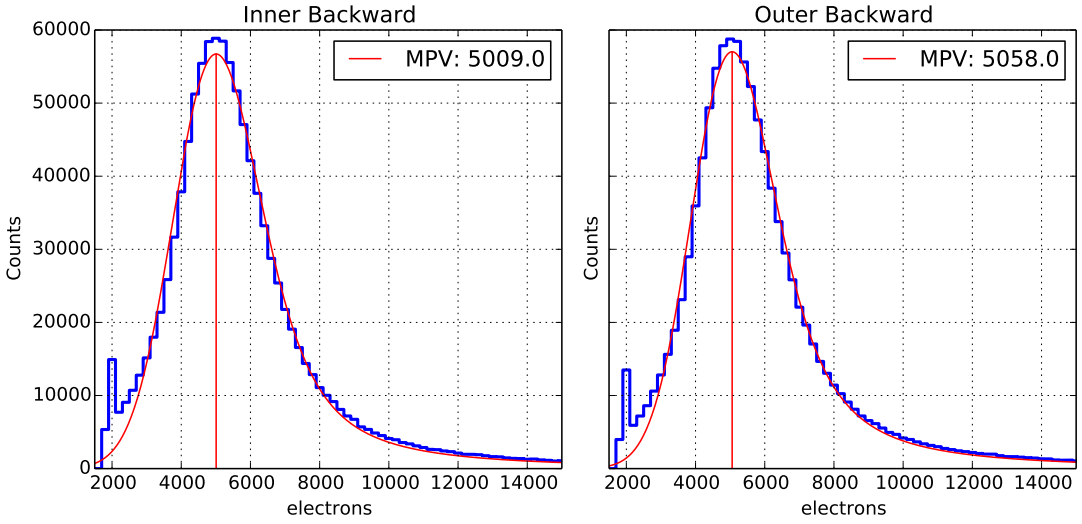


Figure 7.7: Simulation of the number of created electron-hole pairs within the sensitive bulk of the PXD layers. A convolution of a Gaussian and a Landau distribution is used as the fit function. The MPV values is 5009 for the inner backward and 5058 electrons for the outer backward.

imation for the internal in-pixel amplification g_q (see Sect. 4.5.1), the number of electrons created within the detector must be estimated[2]. In order to estimate the number of electron-hole pairs created for the incident beam, simulations are performed in BASF2 using geometry and tracking (GEANT4) [208]. The GEANT4 software simulates the passage of particles through matter. The number of electrons within the PXD layers for 1×10^6 events is shown in Fig. 7.7. The origin of the small peak on the left side of the plots (approximately 2000 electrons) is most likely a photon emission line; however, this is not important for the study

[2] A general introduction on the interaction between charged particles and thin silicon absorbers is given in app. B.5.

and has not been followed further. The histogram is fitted with the convolution of a Landau and a Gaussian. This results in a most probable value (MPV) of 5009 electrons for IB (layer 1) and 5058 electrons for OB (layer 2). Figure 7.8 shows the measured cluster charge distributions in the beam test for both layers, using the BASF2 framework. Additional peaks at lower ADU values are visible, for the IB below 15 ADU and for the OB at 12 ADU. These peaks are discussed later. Since

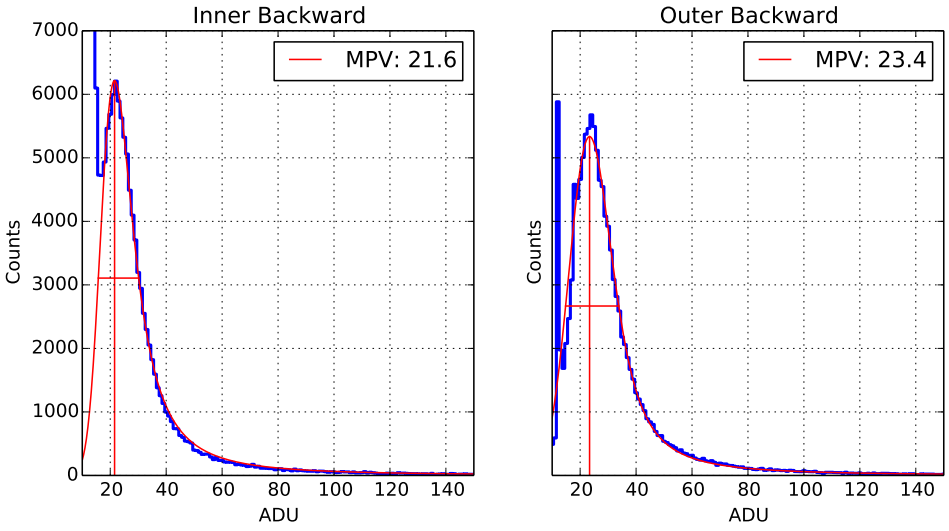


Figure 7.8: Cluster charge distribution for both PXD layers using BASF2. A convolution of a Gaussian and a Landau distribution is used as the fit function. The MPV values are 21.6 ADU and 23.4 ADU.

the number of created electrons within the modules and the measured MPVs are known, the internal amplification of both backward modules can be calculated. Assuming a DCD gain of $\sim$ 130 nA/ADU (see Sect. 6.4) results in an internal amplification of:

$$g_{\text{q, Inner Backward}} = \frac{20.9\,\text{ADU}}{5009\,e^-} \cdot 130\,\frac{\text{nA}}{\text{ADU}} = 542\,\frac{\text{pA}}{e^-} \tag{7.3.1}$$

$$g_{\text{q, Outer Backward}} = \frac{23.4\,\text{ADU}}{5058\,e^-} \cdot 130\,\frac{\text{nA}}{\text{ADU}} = 601\,\frac{\text{pA}}{e^-} \tag{7.3.2}$$

The internal amplifications of both modules differ slightly since the operation voltages, in particular the GateOn voltages, were chosen differently. As previously mentioned, due to time constraints, the outer backward and inner backward modules could not be characterized with radioactive source and laser measurements before being installed in the beam test campaign. Consequently, the operation voltages based on the experience of the W30-OB1 module have been applied and the pedestal distribution has been adjusted to be rather small in the lower dynamic range of the DCD. This procedure was done for both modules separately. The internal amplifications of the beam test modules agree well with the module characterized in the lab ($\sim 500\,\text{pA}/e^-$).

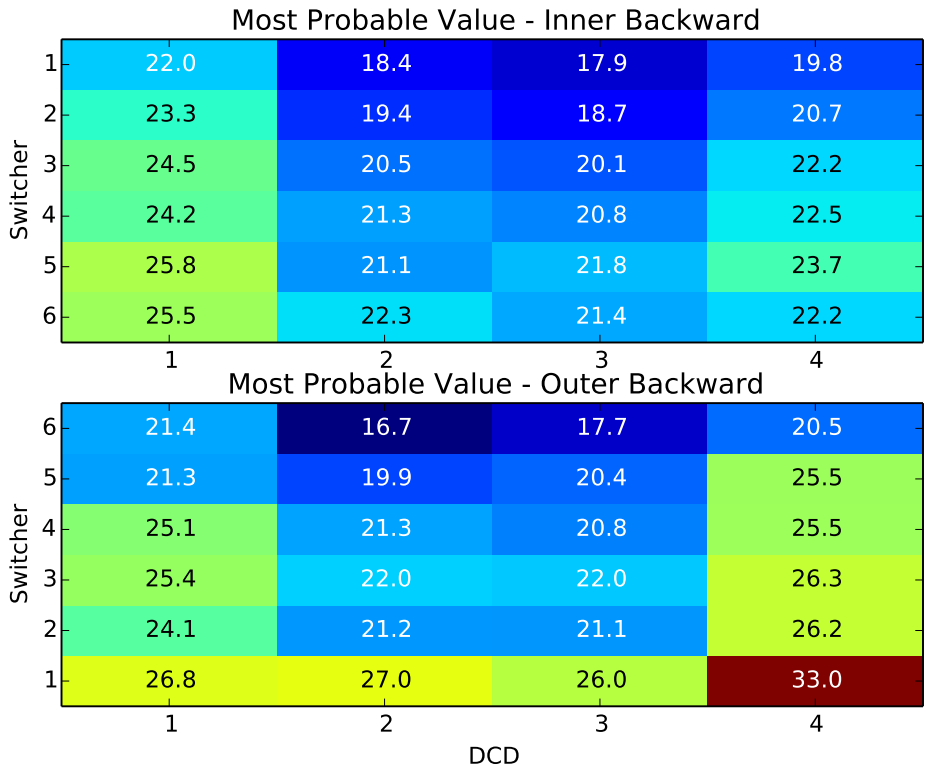


Figure 7.9: Most probable values of the cluster charges for the Switcher and DCD regions using BASF2.

For a more detailed analysis, the DEPFET sensor response can be studied for 24 sections, where each is controlled and read out by another combination of Switcher and DCD. The distributions and the corresponding MPVs for the different areas are shown in Fig. 7.9. For some areas the amplitude, i.e., the number of events, is rather low (missing statistics), resulting in non-optimal fits. The cluster distributions for both layers are shown in Fig. C.18 and Fig. C.19. As shown in Fig. C.18, there is increased noise for some of the pixels, approximately 12–15 ADU for the DCD and Switcher areas (DCD 1 & Switcher 4, DCD 1 & Switcher 5, DCD 2 & Switcher 4, DCD 2 & Switcher 5, DCD 3 & Switcher 4 DCD 4 & Switcher 4). Those contributions are responsible for the dominant peak at the lower dynamic range $\sim$ 15 ADU of the IB in Fig. 7.8. Furthermore, for the OB module there is a noisy input channel in DCD 1 (Fig. C.19) resulting in the peak at 12 ADU as shown in Fig. 7.8.

These results of the MPVs are compared with the lab framework in app. C.9. The data analyzed by the two frameworks (BASF2 and the lab framework) differs. The ROI selection was only performed for the data, which is analyzed with BASF2. Every time the DHH received a trigger signal, the data was directly written to disk and is analyzed by the lab framework. Consequently, for the local DHH data acquisition, there was no further data reduction involved. The results, presented in this section, are analyzed only with BASF2. The results for both frameworks are quite similar. The calculated MPVs show an average deviation of 2 %. The corresponding cluster size distribution for the entire sensitive area is shown in Fig. 7.10. Most of the clusters are single-pixel clusters.

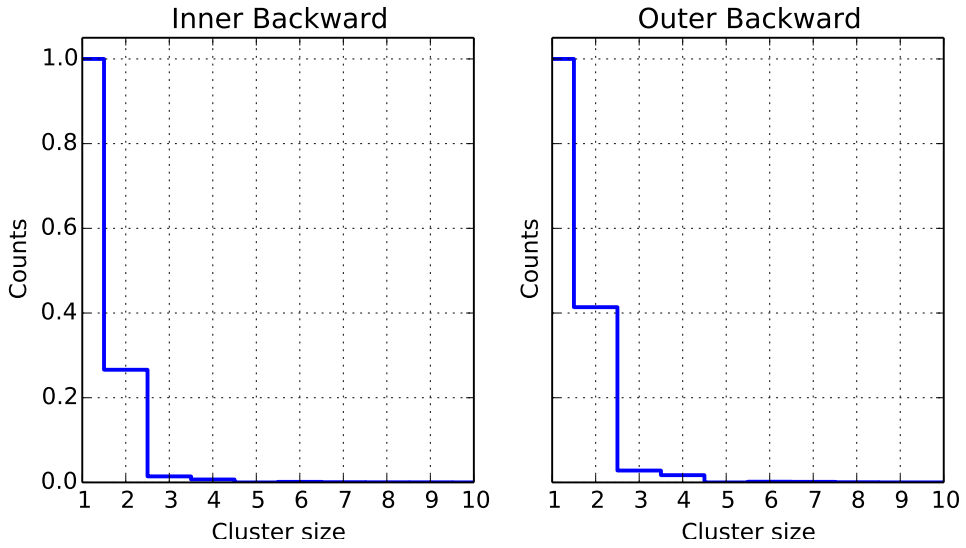


Figure 7.10: Cluster size distribution, normalized to the maximum value. Most of the clusters are single-pixel clusters.

For the regions with high statistics, i.e., many hits (for Switchers 3–5 for the OB and Switcher 2–4 for the IB), the difference of the measured MPVs between both modules is approximately 3–4 ADU. Since the settings of the DCDs differ, they have different gains.

However, for the modules that will be used in the Belle II experiment, all regions of the matrix will be pre-characterized with radioactive sources in the laboratory and the internal amplifications will be calculated serving as calibration values.

7.3.3 Position Resolution

Each detector module has its own internal coordinate system, with u- and v-axes. The v-axis is always in the readout direction (as shown in Fig. 4.47).
The position resolution can be determined from the histogram of the *residuals*, which are given by the average spatial difference between the measured and the true particle positions. The true particle position is calculated as follows: The track is reconstructed using the position measurements of all other layers. The intersection between the reconstructed track and the PXD layer yields the predicted position. A sketch is shown in Fig. 7.11.
The position resolution depends on the number of pixels which show a signal. There are two cases that can be distinguished:

Single Pixel Signal (binary readout)

It is assumed that the real position of the incident particle is distributed uniformly within the pixel cell around the pixel center, μ_{pix}. The particle can traverse the pixel between the position $-p/2, p/2$, which cannot be determined more precisely due to the lack of information.

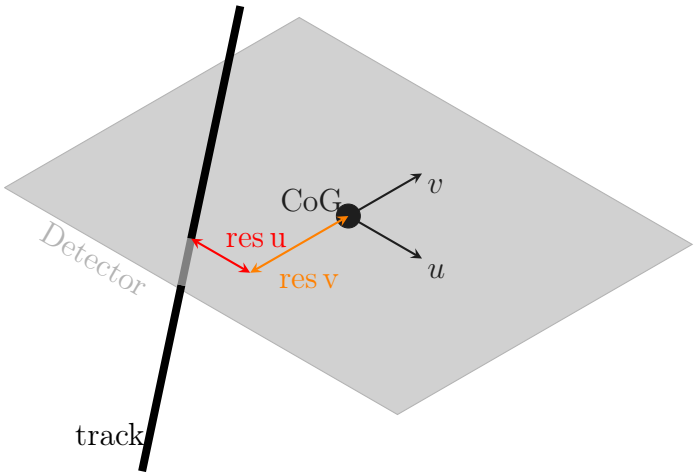


Figure 7.11: A track (black line) represents the trajectory of the traversing particle. The distances (in u- and v-directions) between the track and the calculated position of the CoG are called residuals.

The density function is mathematically described as:

$$f(x) = \begin{cases} 1 & \text{for } x \in [-p/2, p/2] \\ 0 & \text{else} \end{cases} \tag{7.3.3}$$

Assuming that the measurement errors are normally (Gaussian) distributed, the position resolution (also called RMS), $\sigma(x)$, is estimated as (*binary readout*):

$$\sigma(x) = \sqrt{\mathrm{Var}(x)} = \sqrt{\frac{\int_{-p/2}^{p/2} (x - \mu_{\mathrm{pix}})^2 \, f(x) \, \mathrm{d}x}{\int_{-p/2}^{p/2} f(x) \, \mathrm{d}x}} \overset{\mu_{\mathrm{pix}}=0}{=} \frac{p}{\sqrt{12}} \tag{7.3.4}$$

where $\mu_{\mathrm{pix}} = 0$ is the pixel center.

Cluster Pixel Signal

If a charged particle or photon hits the detector close to a pixel boundary, charge sharing occurs, i.e., the generated electrons accumulate in multiple internal gates. The *center-of-gravity (CoG)* algorithm is used to determine the position incident position.

$$(x_{\mathrm{CoG}},\ y_{\mathrm{CoG}}) = \left(\frac{\sum_i x_i s_i}{\sum_i s_i},\ \frac{\sum_j y_j s_j}{\sum_j s_j} \right) \tag{7.3.5}$$

where x_i, y_j denotes the pixel positions and s_i, s_j are the corresponding signals in the pixels. Applying error propagation leads to:

$$\sigma_{x_{\mathrm{CoG}}} = \sqrt{\sum_i \left(\frac{\partial x_{\mathrm{CoG}}}{\partial s_i} \right)^2 \sigma_{s_i}^2} = \sqrt{\sum_i \left(\frac{x_i}{\sum_k s_k} - \frac{\sum_k s_k x_k}{\sum_k s_k^2} \right)^2 \sigma_{s_i}^2} \tag{7.3.6}$$

where i and k are the indices of the signals included in the cluster for the CoG algorithm and σ_{s_i} denote the variances of the signals of the pixel i. The same algorithm is used for the y position.
Assuming a cluster of two pixels, in the end the equation reads [209]:

$$\frac{\sigma_{x_{\mathrm{CoG}}}}{p} = \frac{1}{SNR}\sqrt{1 - 2\frac{x_{\mathrm{CoG}}}{p} + 2\left(\frac{x_{\mathrm{CoG}}}{p}\right)^2} \tag{7.3.7}$$

where SNR denotes the signal-to-noise ratio and p is the pixel pitch. Using the CoG algorithm, the position resolution improves, i.e., $\sigma_{x_{\mathrm{CoG}}} < \sigma_x = \frac{p}{\sqrt{12}}$.
Using this algorithm, a number of assumptions are made. The charge between the pixels is distributed homogeneously, i.e., linearly and the generated charge distribution is box-shaped. However, in reality, the charge distribution is Gaussian. Moreover, the amount of created charge fluctuates, i.e., the signal distribution between the pixels is inhomogeneous. In addition to this, the signals, which are below the threshold (for the zero suppressed readout), are not taken into account since they are not read out. These effects harm the position resolution.
The residuals for both PXD layers (inner backward and outer backward) are shown in Fig. 7.12. Most of the signals are created in a single pixel, since the electron beam hits the PXD ladders orthogonally (see Fig. 7.10). For fewer than 20 % of the tracks, clusters are generated consisting of two pixels. For clusters containing two or more pixels, the CoG algorithm is used. The theoretically calculated ($p/\sqrt{12}$) and measured residuals agree well (see Tab. 7.1): the measured residuals are even more precise (in the range of sub-micrometer) compared to the theoretical binary values. This improvement is due to the applied CoG algorithm for pixel clusters.
The beam test framework [207] is used since all twelve layers are included in the

Table 7.1: Predicted ($p/\sqrt{12}$, where p denotes the pixel pitch) and measured resolutions, using the CoG method, of the two PXD modules in both (u- and v-) directions - see Fig. 7.12.

Layer	pitch	direction	pred. RMS	meas. RMS
Inner	50 µm	u	14.4 µm	14.3 µm
Inner	60 µm	v	17.3 µm	18.3 µm
Outer	50 µm	u	14.4 µm	13.2 µm
Outer	85 µm	v	24.5 µm	24.1 µm

track finding. In contrast, the BASF2 only allows the inclusion of the four SVD layers for the track finder and tracking, which harms the position resolution. Using the η-algorithm [172], the position resolution of the incident particles may be further improved. This method has been successfully applied for prototype DEPFET matrices with a pixel size of $22 \times 36\,\mu\mathrm{m}^2$, 450 µm thick and an incident charged pion (π^+) beam of 180 GeV. It improved the detector resolutions by more than 20 % [210]. Such improvements, however, are not expected for the modules used in this beam test campaign due to the geometric pixel dimensions. The modules

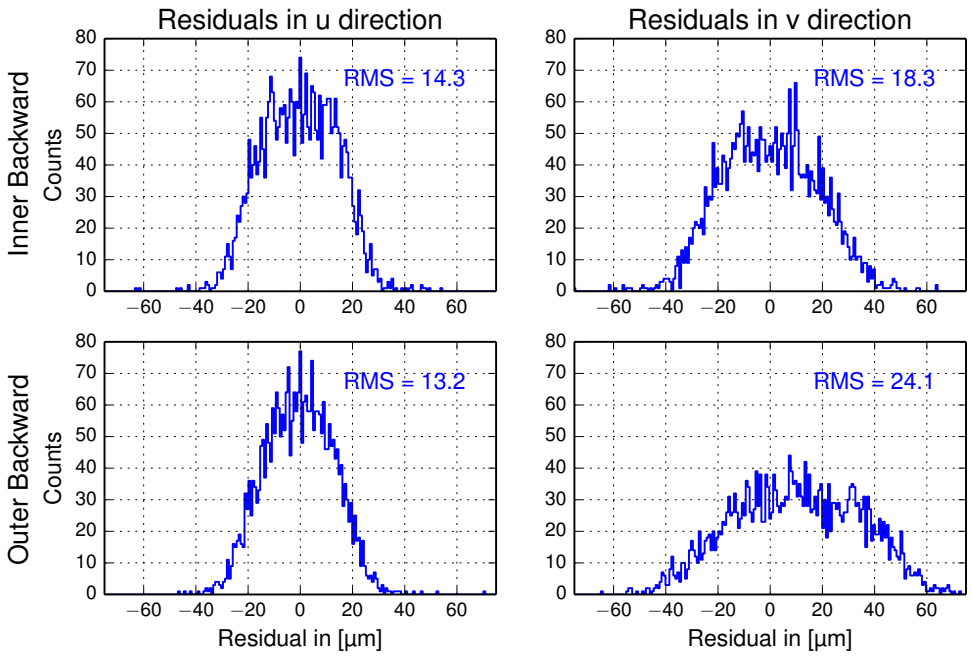


Figure 7.12: Residuals of the inner backward and outer backward modules for the u- and v-directions. The pixel pitches and corresponding digital resolutions are summarized in Tab. 7.1.

presented in this chapter are thinner by a factor of 6 compared to those used for the beam test with pions. Consequently, the number of created signal electrons is decreased significantly. Additionally, the charge sharing between neighboring pixels is reduced since their pitches in both dimensions are increased by roughly a factor of 2 ($22 \times 36\,\mu m^2 \rightarrow 50 \times 55$–$85\,\mu m^2$). Another idea to improve the position resolution, is to classify the residuals according to their cluster charges [211]. This study is currently ongoing.

According to the requirements of the PXD, a single point resolution of roughly 10 µm is required. The measured residuals of this beam test campaign are between $\sim$ 14 µm and 24 µm for a perpendicular incident electron beam. However, if particles hit the sensor with an angle $0\,° < \alpha < 90\,°$, clusters that contain two or more pixels are more likely to be generated. Using the CoG algorithm, the position resolution can be further improved. Residuals of 9.1 µm (with the same pixel layout and matrix thickness) of an incident beam with an angle of 30 ° were achieved in a previous beam test campaign [212].

7.3.4 Efficiency

An important key characteristic of the detector is its efficiency. The efficiency study is performed for both PXD ladders individually.
The efficiency is studied the following way. A track that passes the PXD layer i is selected. The intersection coordinates, u_i, and, v_i, are calculated based on the track calculated using the other detector layers. For these coordinates, a cluster

charge must also exist on the PXD layer i. This procedure is repeated for multiple tracks. The number of clusters found divided by the number of expected clusters (by the track interpolation) yields the efficiency η:

$$\eta = \frac{\#(\text{found clusters})}{\#(\text{expected clusters})} \cdot 100\,\% \tag{7.3.8}$$

As an example, if 100 tracks are selected and cluster charges are found in 98 of the tracks (in PXD layer i), this results in an efficiency of 98 %. The projected efficiency for the rows (v cells) and the columns (u cells) are shown for both layers in Fig. 7.13.

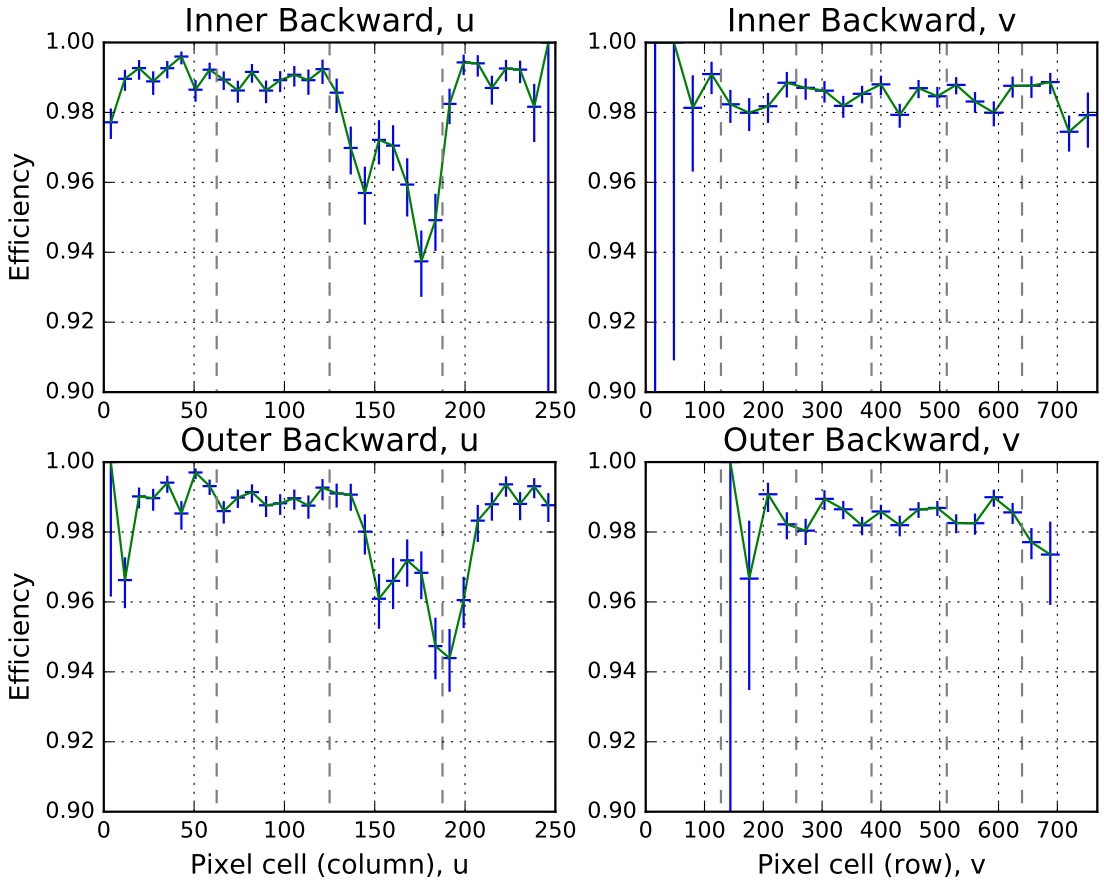


Figure 7.13: Efficiencies on the projected u- and v-axes for both PXD layers. For the u-direction each bin contains eight geometrical columns, while for the v-direction each bin includes 32 geometrical rows. A significant efficiency drop of DCD 3 is visible. They gray dashed lines separate the DCDs (in u-direction) and the Switchers (in v-direction).

The efficiencies for the sensitive areas are shown in Fig. 7.14. Each DCD is divided in eight bins, i.e., one bin represents eight pixel columns$_{\text{geo}}$. Each Switcher is divided into four bins, i.e., one bin corresponds to 32 pixel rows$_{\text{geo}}$. For some areas (in particular for the outer module), no tracks are found in certain DCD-Switcher sections. An efficiency drop occurs on both modules for DCD 3. Since the modules were not optimized, there could be hits out of the dynamic range of the DCD or

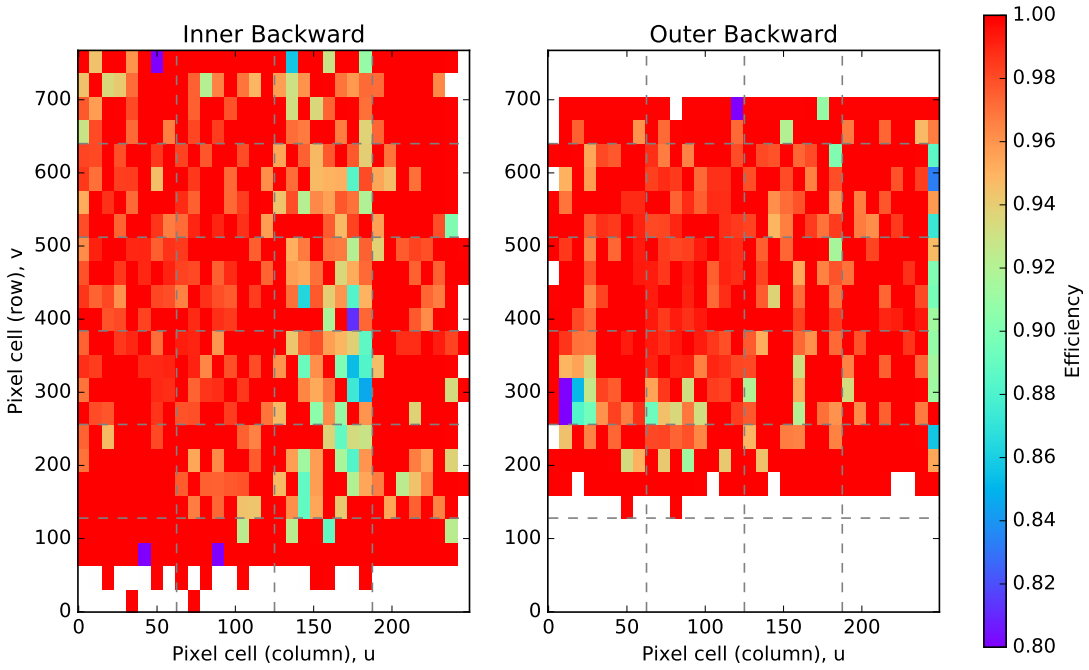


Figure 7.14: Efficiencies of the sensitive areas of both PXD layers. There are eight bins for each DCD and four bins per Switcher. The gray dashed lines separate the areas which are controlled and read out by different Switchers and DCDs.

below the zero-suppressed threshold, especially for pixels where charge sharing occurs.
The total efficiency for both modules is approximately 98 %–99 % (except for the pixels which are read out by DCD 3 where the efficiency drops to $\sim$ 94 %). The length (v-direction) of the sensitive area of the OB module is larger (61.44 mm) compared to the sensitive area of the IB module (44.80 mm). Due to the shape of the beam spot, i.e., the rectangular shape of the scintillators generating the triggers, only a small fraction of tracks pass the upper ($> 700\,\mathrm{row_{geo}}$) and lower ($< 150\,\mathrm{row_{geo}}$) region of the outer backward module. Only a small fraction of tracks pass the lower region of the inner backward module ($< 80\,\mathrm{row_{geo}}$). Thus, it is not possible to calculate the efficiencies in these areas.

7.4 Summary and Outlook

For the first time, two large PXD sensor modules (IB and OB) with 192,000 active DEPFET pixels, which are controlled by 14 ASICs, were operated in a beam test. Both modules fully worked. The Landau cluster charge distributions for both layers give most probable values of between 22 ADU and 24 ADU ($\approx 220\,e^-$/ADU) and the internal amplification is between 540–600 $\frac{\mathrm{pA}}{e^-}$. The different MPVs across the matrices of the final modules for the PXD will be calibrated in the lab by detailed scans with radioactive source and laser measurements before installation in Belle II. This assures a well known ratio between the deposited energy and the ADU.

The position resolutions yield residuals between 13.2 µm (for 50 µm pixel pitch) and 24.1 µm for (85 µm pixel pitch). The measured values agree well with the theoretically predicted values for binary readout, i.e., $p/\sqrt{12}$. However, the position resolution can be further improved by charge sharing and by using the CoG algorithm. Charge sharing occurs in about 20 % of the traversing particles.
The efficiency for most columns and rows is approximately 98 % with the exception of DCD 3, where it drops to approximately 94 %. This could be due to incorrect settings of the DCD (such that some pixels are out of the dynamic range to detect signals). Assuming a decay into three charged particles in the Belle II experiment that traverse both PXD layers, six hits would be expected. If the overall efficiency of a single ladder were 98 %, the probability to detect all six hits in both layers would be 88.6 %. In the case the analysis requires only one hit on both layers (which would decrease the position resolution), the efficiency is 99.9 %. However, the modules were not characterized before being installed in the beam test campaign due to lack of time. The ASIC settings and operation voltages must still be optimized. Once that has been completed, the efficiency could be increased to greater than 99 %.
Although the detector has not been optimized before (due to time constraints) the overall performance is very good. Due to various problems in the data acquisition chain, data processing and slow control a permanent setup at DESY (PERSY) was created. Its goal is to improve the interaction and integration of all of the different sub-systems and thoroughly test and debug the entire DAQ system for the coming phases 2 and 3.

Chapter 8

Conclusion and Outlook

The SuperKEKB asymmetric electron-positron collider will increase the instantaneous luminosity by a factor of 40 compared to its predecessor KEKB using the nano-beam scheme to reach a new world-record of $\mathcal{L} = 8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. In order to study the rich physics program focusing on New Physics beyond the Standard Model by means of precise measurements of the $\mathcal{CP}$ violation and search for rare decays, the Belle detector is upgraded to Belle II. While the outer sub-detectors are reused from the predecessor Belle experiment, the tracking systems are replaced by newly developed sub-detectors.
The innermost detector of the Belle II experiment involves a novel pixel vertex detector (PXD), consisting of 75 µm thick monolithic active DEPFET sensors. A DEPFET pixel consists of a p-channel MOSFET on a sidewards depleted n-doped silicon bulk. The traversing charged particles create electrons, which accumulate in a potential minimum, the so-called *internal Gate*. It is located less than a micrometer below the external Gate of the MOS structure. The Source-Drain current is modulated depending on the amount of signal electrons stored in the *internal Gate*. The variation of the Drain current is measured, yielding the number of stored electrons. In this way, the DEPFET pixel directly amplifies the signal. In order to remove the charge from the *internal Gate* an n^+ implant is located in each DEPFET pixel serving as *Clear region*. Applying a sufficiently large voltage at the *Clear implant* attracts the electrons from the *internal Gate* and prepares the DEPFET pixel for the next measurement.
The DEPFET pixels are combined to a *DEPFET sensor matrix*. The matrix is controlled and read out by ASICs, which are directly mounted on the sensor substrate support structure, i.e., next to the active pixel cells. The all-silicon module is comprised of 192,000 pixels with all of the metallic interconnections for power and data communication between the ASIC. The module is attached to a Kapton cable at one of the short edges for power and off-module data communication. The PXD consists of 40 *modules*. Each module is equipped with 14 ASICs to control all DEPFET pixels, digitize their signals and apply a sophisticated data reduction. Two of the modules are glued together at the short edge, forming a ladder parallel to the beam pipe of SuperKEKB. The ladders are arranged in two layers at radii 14 mm and 22 mm around the beam pipe. The PXD offers an unprecedented low material budget, corresponding to $0.2\,\%\ X_0$, a self-supporting sensor structure, high signal-to-noise ratio, low power consumption, excellent spatial resolution and a fast readout speed of 20 µs for all 8×10^6 pixels.
The operation of the control and readout electronics for the DEPFET sensors have been verified and proven with a so-called *Electrical Multi-Chip Module* (EMCM).

For this purpose, a sophisticated software framework was developed and is presented in this thesis, which has been distributed within the entire DEPFET collaboration. Common efforts of various researchers contribute to the steadily growing software framework, which allows the characterization and optimization of the modules for the PXD and the surrounding slow control and data acquisition systems.

Procedures and algorithms have been developed in order to optimize and characterize the EMCM and real pilot run modules. The synchronization between the three different types of ASICs, namely the Switcher, DCD and DHP, was adjusted to ensure a proper control and readout of the sensor. The most important parameters were the time-critical communication between the ASICs, i.e, the correct sampling point of the digital waveform sent by the DCD, adjusting the ADCs in the readout ASICs, applying the correct offset compensation values for the pedestal compression and optimizing the Switcher sequence, supported by simulations. Due to a bug in the digital processing ASIC (DHP), the data can be sent from the DHP to the DHE (the DAQ system in lab) only with a $\sim 20\,\%$ lower clock frequency compared to the nominal value of 76.33 MHz. The lower clock frequency did not only ensure stable data transfer, but also led to less cross-talk between the ASICs. In order to reduce cross-talk to a minimum, a detailed measurement program was set up leading to a widening of the spacing of the metal traces between the DCD and DHP from 4 µm to 21 µm for future pilot run modules and for the final modules for the PXD. In order to sample the signal Drain current of the DEPFET pixels at the correct timing, the sampling point curves were studied in detail. Due to the large parasitic capacitances of the Clear and Drain lines, no flat plateau could be found. However, as it was shown in this thesis, the signal could be also well-detected if the sampling point was chosen on rising or falling edges of the Drain currents. An additional bug that was found in the DHP could shift the DCD clock relative to the global clock by up to 12 ns. The phase shift changes randomly with every power cycle of the ASICs. As a consequence, the sampling point as a function of time of the Drain currents is directly affected. For this reason, the pedestals would have to be acquired at every new power up sequence. In the latest version of the DHPT this bug is fixed.
The noise of the system was studied in detail. The largest contribution is due to the electronics and power supply, i.e., the common mode noise. It can be effectively diminished to approximately 130 electrons, corresponding to 0.5 LSB. Due to the increasing pedestal spread with more negative GateOn voltages, a 2-bit offset compensation was successfully implemented, which compresses the pedestal spread by roughly a factor of two. Nevertheless, a gradient across the DCD was observed, which is most likely caused by voltage drops within the ASIC. This problem should be solved in the final DCD version (DCDB4.2). The Clear pulse was measured for different Switcher output drivers. Moreover, the Clear performance for different sections of the large module was studied and the control of the Switchers, i.e., the Clear pulse and the operation voltages, was optimized. One prototype module (W30-OB1) was characterized successfully and its optimal operation voltages were determined. A radioactive cadmium source has been used and the signals for various voltages have been analyzed. A signal-to-noise ratio between 40–50 was achieved with an internal amplification of the DEPFET pixels

around 500 pA/e^-. The optimal voltages for proper operation were suggested in the source measurements and the Gated Mode measurements.
A special mode of operation, the Gated Mode (GM) was introduced, which puts the pixel detector into an insensitive mode when "noisy" bunches, caused by the top-up injection scheme of SuperKEKB, pass the Belle II detector. The particles from the noisy bunches will cause large background in the PXD. The two main performances critical for the GM were studied: the preservation of the signal, i.e., the electrons already stored in the *internal Gate* and the junk charge prevention, i.e., the amount of additional charge caused by the noisy particles.
Problems in the GM were observed regarding the Clear pulse, which is applied by the Switcher that is furthest away from the end-of-stave. The nominal amplitude of the applied Clear voltage was not reached within the required time of a few hundreds of nanoseconds. The problem was identified within this thesis and led to a change of the metal system of the modules for the final PXD. The changes were verified on the W31-OF1 pilot run module ensuring a proper GM operation. However, a Switcher logic problem remains in "fast" GM operation (*without readout*). For this reason, a "slower" GM (*with readout*) must be used. Although the Switchers are able to protect all pixels from the module, pedestal oscillations prevent the application of the GM within the required 1 µs from the other Belle II sub-detectors. The dead time of the GM, rather, turns out to be approximately 2 µs. A possible remedy is to further optimize the various internal current sources of the DCD to decrease the damping time, or even a possible rework in a future DCD version.
Two pilot run modules (layer 1 and layer 2) were successfully commissioned during a beam test campaign using an electron beam of up to 6 GeV at DESY. Both modules were operated, combined with four layers of the foreseen Belle II silicon strip detector. The cluster charge distributions of all sections, controlled and read out by different combinations of Switchers and DCDs, were studied, the position resolutions (between 13 µm and 24 µm) for both pixel pitch dimensions (50 µm and 85 µm) were investigated and hit efficiencies above 98 % (except for one problematic readout ASIC) were obtained.

Outlook

Within this thesis, the first pilot run modules are characterized thoroughly and the software framework was successfully developed, incorporating measurements and analysis. Nevertheless, a small number of further studies regarding in-pixel properties would still be valuable.
Of particular interest are investigations of charge sharing between neighboring pixels as well as charge collection. For these studies, a laser moving in micrometer steps would be required, illuminating the backside and avoiding the metallization on top of the sensitive silicon. Additional mounting structures and jigs are being prepared to perform such measurements. In connection to this, the shielding of the *internal Gate* in the GM operation, depending on the position of traversing particles, is an interesting study. The in-pixel studies could even reduce the operation windows of applied voltages to maintain homogeneous behaviors (in terms of Clear efficiency, charge collection, shielding of the *internal Gate*) over the entire

sensitive pixel area.
Moreover, the GM is a crucial operation mode, in particular, if the bunch stabilization process requires more than the 4 ms, as observed at KEKB.
A new iteration of the Switcher with a modified logic would be desirable in order to apply the GM without readout for short times in the range of a few hundreds of nanoseconds and some rework on the DCD would be valuable to reduce the pedestal oscillations. Besides, not only the optimization of the sensor but also the entire data acquisition is essential for a proper operation of the PXD at Belle II. Proceeding from the exercises accomplished in the beam test campaign in April 2017, a setup (*PERSY*) was introduced to practice the entire acquisition, triggering, data reduction, slow control and data quality monitoring with the accompanying interlock and logging systems. With PERSY the entire PXD will be built up module by module and, finally, fully commissioned before it is brought to KEK and installed into Belle II. If everything goes well, this will happen by the summer of 2018.

Appendix A

Physics at Belle II

A.1 Parity conjugation of Legendre Polynomial

The Legendre Polynomial under parity conjugation (see Sect. 2.2.1) are studied [213].

$$\begin{aligned} Y_l^m(\theta,\phi) &= \frac{(-1)^m}{2^l l!}\sqrt{\frac{(2l+1)}{4\pi}\frac{(l-m)!}{(l+m)!}}e^{\mathrm{i}m\phi}(1-\eta^2)^{m/2}(d_\eta)^{l+m}(\eta^2-1)^l \\ &= \sqrt{\frac{(2l+1)}{4\pi}\frac{(l-m)!}{(l+m)!}}e^{\mathrm{i}m\phi}P_l^m(\cos(\theta)) \end{aligned}$$

where P_l^m denotes the Legendre polynomial. Applying the parity operator transforms $\eta = \cos(\theta) \to \cos(\pi-\theta) = -\cos(\theta) = -\eta$ and $\phi \to \pi + \phi$. One will use the relation $P_l^m(-\cos(\theta)) = (-1)^{l+m}P_l^m(\cos(\theta)$[1] in the following. Hence, one obtains for the radial part $Y_l^m(\theta,\phi)$:

$$\begin{aligned} Y_l^m(\theta,\phi) &\xrightarrow{\mathcal{P}} \sqrt{\frac{(2l+1)}{4\pi}\frac{(l-m)!}{(l+m)!}}e^{\mathrm{i}m\phi}\underbrace{e^{\mathrm{i}m\pi}}_{(-1)^m}(-1)^{l+m}P_l^m(\cos(\theta)) \\ Y_l^m(\theta,\phi) &\xrightarrow{\mathcal{P}} (-1)^m(-1)^{l+m}Y_l^m(\theta,\phi) \\ Y_l^m(\theta,\phi) &\xrightarrow{\mathcal{P}} (-1)^l Y_l^m(\theta,\phi) \end{aligned}$$

In the last step the relation $(-1)^{2m} = 1$ for $m \in \mathbb{Z}$ (since $2m$ is an even number) has been used.

A.2 CKM matrix and its four parameters

In this section the number of free parameters of a unitary matrix is determined. In addition, the phase transformations are explained to obtain the reduction of the nine free parameters to three angles and one complex phase, which describes the CKM matrix.

[1] The Legendre polynomial can be obtained form a generating function $f(t,x) = (1-2xt+t^2)^{-0.5} = \sum_n P_n(x)t^n = (1-2(-x)(-t)+(-t)^2)^{-0.5} = \sum_n P_n(-x)(-t)^n = \sum_n P_n(-x)t^n(-1)^n$, hence $P_n(x) = (-1)^n P_n(-x)$.

A.2.1 Number of free parameters of a unitary matrix

Let $U \in \mathbb{C}^{N\times N}$ be a unitary complex $N \times N$ matrix. Unitarity states:

$$\begin{aligned}
&(U^H U)_{ij} \\
&\quad = U^H_{ik} U_{kj} \\
&\quad = (a_{ik} + ib_{ik})^*(a_{kj} + ib_{kj}) \\
&\quad = (a_{ki} - ib_{ki})(a_{kj} + ib_{kj}) \\
&\quad = a_{ki}a_{kj} + b_{ki}b_{kj} + i\underbrace{(a_{ki}b_{kj} - a_{kj}b_{ki})}_{=0} = \delta_{ij} \\
&\quad \Rightarrow a_{ki}a_{kj} + b_{ki}b_{kj} = \delta_{ij} \quad \text{(I)} \\
&\quad \Rightarrow a_{ki}b_{kj} - a_{kj}b_{ki} = 0 \quad \text{(II)}
\end{aligned}$$

From equation (I) the number of fixed parameters is:

$$\underbrace{N}_{\text{diagonal}} + \underbrace{\frac{\overbrace{N^2}^{\text{all}} - \overbrace{N}^{\text{diagonal}}}{\underbrace{2}_{\text{upper/lower half}}}}_{\text{off-diagonal}} = \frac{N^2+N}{2} \tag{A.2.1}$$

Moreover, equation (II) states the symmetry under i, j exchange. Hence, the number of fixed parameters is

$$\frac{\overbrace{N^2}^{\text{all}} - \overbrace{N}^{\text{diagonal}}}{\underbrace{2}_{\text{upper/lower half}}} \tag{A.2.2}$$

Due to unitarity, for the off-diagonal elements of U hold: $u_{ij} = \overline{u}_{ji}$.
In total we have N^2 real parameters and N^2 imaginary parameters, resulting in $2N^2$. Due to the upper constraints the number of free parameters reduces from $2N^2$ to N^2:

$$2N^2 - \left(\frac{N^2-N}{2} + \frac{N^2+N}{2}\right) = 2N^2 - N^2 = N^2 \tag{A.2.3}$$

For N^2 free remaining parameters, $\frac{N^2-N}{2}$ elements are Euler angles and $\frac{N^2+N}{2}$ are phases. For the 3×3 CKM matrix, there are nine free parameters, three angles and six phases.

A.2.2 Phases in CKM Matrix

A unitary 3×3 matrix has three rotation angles and six complex phases. Five out of these six phases can be absorbed into a single global phase.

For any unitary $n \times n$ matrix one can multiply phases from the right. It is assumed that V is a unitary matrix:

$$V \to V \begin{pmatrix} e^{i\alpha_1} & & \\ & \ddots & \\ & & e^{i\alpha_n} \end{pmatrix} \tag{A.2.4}$$

Adding nine phases to a 3×3 unitary matrix yields that only five are linearly independent. Hence, the most general form of a CKM matrix is [214]:

$$\begin{aligned} V = & \begin{pmatrix} 1 & & \\ & e^{i(\alpha_{23}-\alpha_{13})} & \\ & & e^{i(\alpha_{33}-\alpha_{13})} \end{pmatrix} \\ & \cdot \begin{pmatrix} c_{12}c_{13} & s_{12}c_{13} & s_{13}e^{-i\delta} \\ -s_{12}c_{23} - c_{12}s_{23}s_{13}e^{i\delta} & c_{12}c_{23} - s_{12}s_{23}s_{13}e^{i\delta} & s_{23}c_{13} \\ c_{12}s_{23} - c_{12}c_{23}s_{13}e^{i\delta} & -c_{12}s_{23} - s_{12}c_{23}s_{12}e^{i\delta} & c_{23}c_{13} \end{pmatrix} \\ & \cdot \begin{pmatrix} e^{i\alpha_{11}} & & \\ & e^{i\alpha_{22}} & \\ & & e^{i\alpha_{33}} \end{pmatrix} \end{aligned} \tag{A.2.5}$$

The charged current (CC) part of the electroweak Lagrangian states:

$$\mathcal{L}_{CC} = -\frac{g}{\sqrt{2}} \bar{\tilde{u}}_{Li} \gamma^\mu (\tilde{V}_{\mathrm{CKM}})_{ij} \tilde{d}_{Lj} \tilde{W}_\mu + h.c. \tag{A.2.6}$$

where g is the universal (weak) coupling constant associated with the $\mathrm{SU(2)_L}$ gauge group (representing the coupling strength),
γ^μ are the gamma matrices

$$\begin{aligned} \gamma^0 &= \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & -1 \end{pmatrix}, \qquad \gamma^1 = \begin{pmatrix} 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & -1 & 0 & 0 \\ -1 & 0 & 0 & 0 \end{pmatrix} \\ \gamma^2 &= \begin{pmatrix} 0 & 0 & 0 & -i \\ 0 & 0 & i & 0 \\ 0 & i & 0 & 0 \\ -i & 0 & 0 & -1 \end{pmatrix}, \qquad \gamma^3 = \begin{pmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 \\ -1 & 0 & -1 & 0 \\ 0 & 1 & 0 & 0 \end{pmatrix} \end{aligned} \tag{A.2.7}$$

$\tilde{W}_\mu$ is the field of the charged $W^\pm$ bosons,
$\tilde{u}_{Li} = (\tilde{u}_L, \tilde{c}_L, \tilde{t}_L)^T$ and $\tilde{d}_{Li} = (\tilde{d}_L, \tilde{s}_L, \tilde{b}_L)^T$ (so the indices i, j represent the quark generations.
One can redefine the phases of the quark fields, since the phases can be rotated freely. The phase is a convention-dependent quantity that does not have any physical meaning.

$$\begin{aligned} &\tilde{u}_L \to e^{i\Phi_u} u_L \qquad \tilde{d}_L \to e^{i\Phi_d} d_L \qquad \tilde{c}_L \to e^{i\Phi_c} c_L \\ &\tilde{s}_L \to e^{i\Phi_s} s_L \qquad \tilde{t}_L \to e^{i\Phi_t} t_L \qquad \tilde{b}_L \to e^{i\Phi_b} b_L \end{aligned} \tag{A.2.8}$$

Hence, the Lagrangian states:

$$\mathcal{L}_{CC} = -\frac{g}{\sqrt{2}}(\bar{u}_L, \bar{c}_L, \bar{t}_L)\,\gamma^\mu \begin{pmatrix} e^{-i\Phi_u} & & \\ & e^{-i\Phi_c} & \\ & & e^{-i\Phi_t} \end{pmatrix} \begin{pmatrix} 1 & & \\ & e^{i(\alpha_{23}-\alpha_{13})} & \\ & & e^{i(\alpha_{33}-\alpha_{13})} \end{pmatrix}$$
$$\cdot \begin{pmatrix} c_{12}c_{13} & s_{12}c_{13} & s_{13}e^{-i\delta} \\ -s_{12}c_{23} - c_{12}s_{23}s_{13}e^{i\delta} & c_{12}c_{23} - s_{12}s_{23}s_{13}e^{i\delta} & s_{23}c_{13} \\ c_{12}s_{23} - c_{12}c_{23}s_{13}e^{i\delta} & -c_{12}s_{23} - s_{12}c_{23}s_{12}e^{i\delta} & c_{23}c_{13} \end{pmatrix}$$
$$\cdot \begin{pmatrix} e^{i\alpha_{11}} & & \\ & e^{i\alpha_{22}} & \\ & & e^{i\alpha_{33}} \end{pmatrix} \begin{pmatrix} e^{i\Phi_d} & & \\ & e^{i\Phi_s} & \\ & & e^{i\Phi_b} \end{pmatrix} \begin{pmatrix} d_L \\ s_L \\ b_L \end{pmatrix} W_\mu + h.c.$$

Choosing appropriate phase transformation:

$$\begin{array}{lll} \Phi_u = 0 & \Phi_d = -\alpha_{11} & \Phi_c = \alpha_{23} - \alpha_{13} \\ \Phi_s = -\alpha_{12} & \Phi_t = \alpha_{33} - \alpha_{13} & \Phi_b = -\alpha_{13} \end{array} \tag{A.2.9}$$

Hence, one can remove the five phases α_{11}, α_{22}, α_{33}, α_{13}, α_{23} resulting in the Lagrangian

$$\mathcal{L}_{CC} = -\frac{g}{\sqrt{2}}\bar{\tilde{u}}_{Li}\gamma^\mu \left(V_{\mathrm{CKM}}\right)_{ij} d_{Lj}\tilde{W}_\mu \tag{A.2.10}$$

with

$$\begin{pmatrix} c_{12}c_{13} & s_{12}c_{13} & s_{13}e^{-i\delta} \\ -s_{12}c_{23} - c_{12}s_{23}s_{13}e^{i\delta} & c_{12}c_{23} - s_{12}s_{23}s_{13}e^{i\delta} & s_{23}c_{13} \\ c_{12}s_{23} - c_{12}c_{23}s_{13}e^{i\delta} & -c_{12}s_{23} - s_{12}c_{23}s_{12}e^{i\delta} & c_{23}c_{13} \end{pmatrix} \tag{A.2.11}$$

Hence, there are four parameters to describe the CKM matrix, (due to unitarity conditions nine parameters vanish and due to the relative quark phases five parameters disappear).

A.3 Eigenvectors and Eigenvectors of the Hamiltonian

In this section the eigenvalues and eigenvectors of the Hamiltonian $\mathcal{H}$, according to Sect. 2.4, eq. (2.4.10) are calculated.

A.3.1 Eigenvalues of the Hamiltonian

Calculating the eigenvalues of the Hamiltonian yields:

$$\begin{vmatrix} \mathcal{H} - \lambda & \mathcal{H}_{12} \\ \mathcal{H}_{21} & \mathcal{H} - \lambda \end{vmatrix} = \begin{vmatrix} M - \frac{i}{2}\Gamma - \lambda & M_{12} - \frac{i}{2}\Gamma_{12} \\ M_{12}^* - \frac{i}{2}\Gamma_{12}^* & M - \frac{i}{2}\Gamma - \lambda \end{vmatrix} =$$
$$(M - \frac{i}{2}\Gamma - \lambda)^2 - \underbrace{(M_{12} - \frac{i}{2}\Gamma_{12})(M_{12}^* - \frac{i}{2}\Gamma_{12}^*)}_{:=c} =$$
$$M^2 - \frac{i}{2}M\Gamma - M\lambda - \frac{i}{2}M\Gamma - \frac{1}{4}\Gamma^2 + \frac{i}{2}\Gamma\lambda - M\lambda + \frac{i}{2}\Gamma\lambda + \lambda^2 - c =$$

$$\begin{aligned}
&\lambda^2 + M^2 - iM\Gamma - 2M\lambda + i\Gamma\lambda - \frac{1}{4}\Gamma^2 - c = \\
&\lambda^2 + (i\Gamma - 2M)\lambda + M^2 - iM\Gamma - \frac{1}{4}\Gamma^2 - c \stackrel{!}{=} 0 \\
\lambda_{1,2} =& \frac{1}{2}\left(2M - i\Gamma \pm \sqrt{-\Gamma^2 - 4iM\Gamma + 4M^2 - 4M^2 + 4iM\Gamma + \Gamma^2 + 4c}\right) = \\
&\frac{2M - i\Gamma \pm \sqrt{4c}}{2} = \underbrace{M - \frac{i}{2}\Gamma}_{\mathcal{H}} \pm \sqrt{\underbrace{(M_{12} - \frac{i}{2}\Gamma_{12})}_{\mathcal{H}_{12}}\underbrace{(M_{12}^* - \frac{i}{2}\Gamma_{12}^*)}_{\mathcal{H}_{21}}} \\
&= \mathcal{H} \pm \sqrt{\mathcal{H}_{12}\mathcal{H}_{21}}
\end{aligned}$$

Hence, the eigenvalues are $\lambda_{1,2} = \mathcal{H} \pm \sqrt{\mathcal{H}_{12}\mathcal{H}_{21}}$
Next, the eigenvectors are calculated:

$$\begin{pmatrix} \mathcal{H} - \lambda_{1,2} & \mathcal{H}_{12} \\ \mathcal{H}_{21} & \mathcal{H} - \lambda_{1,2} \end{pmatrix} \begin{pmatrix} x \\ y \end{pmatrix} = \begin{pmatrix} \mp\sqrt{\mathcal{H}_{12}\mathcal{H}_{21}} & \mathcal{H}_{12} \\ \mathcal{H}_{21} & \mp\sqrt{\mathcal{H}_{12}\mathcal{H}_{21}} \end{pmatrix} \begin{pmatrix} x \\ y \end{pmatrix} = 0$$

$$\begin{aligned}
\lambda_1: \quad & -\sqrt{\mathcal{H}_{12}\mathcal{H}_{21}}x + \mathcal{H}_{12}y = 0 \quad \Leftrightarrow -\sqrt{\tfrac{\mathcal{H}_{21}}{\mathcal{H}_{12}}}x + y = 0 \\
& \mathcal{H}_{21}x - \sqrt{\mathcal{H}_{12}\mathcal{H}_{21}}y = 0 \quad \Leftrightarrow x - \sqrt{\tfrac{\mathcal{H}_{12}}{\mathcal{H}_{21}}}y = 0 \\
& \Rightarrow EV_1 = \begin{pmatrix} -\sqrt{\frac{\mathcal{H}_{21}}{\mathcal{H}_{12}}} \\ 1 \end{pmatrix}, \begin{pmatrix} 1 \\ -\sqrt{\frac{\mathcal{H}_{12}}{\mathcal{H}_{21}}} \end{pmatrix} \\
\lambda_2: \quad & \sqrt{\mathcal{H}_{12}\mathcal{H}_{21}}x + \mathcal{H}_{12}y = 0 \quad \Leftrightarrow \sqrt{\tfrac{\mathcal{H}_{21}}{\mathcal{H}_{12}}}x + y = 0 \\
& \mathcal{H}_{21}x + \sqrt{\mathcal{H}_{12}\mathcal{H}_{21}}y = 0 \quad \Leftrightarrow x + \sqrt{\tfrac{\mathcal{H}_{12}}{\mathcal{H}_{21}}}y = 0 \\
& \Rightarrow EV_2 = \begin{pmatrix} \sqrt{\frac{\mathcal{H}_{21}}{\mathcal{H}_{12}}} \\ 1 \end{pmatrix}, \begin{pmatrix} 1 \\ \sqrt{\frac{\mathcal{H}_{12}}{\mathcal{H}_{21}}} \end{pmatrix}
\end{aligned}$$

Using the definition:

$$\frac{q}{p} = \sqrt{\frac{\mathcal{H}_{21}}{\mathcal{H}_{12}}} = \sqrt{\frac{M_{12}^* - \frac{i}{2}\Gamma_{12}^*}{M_{12} - \frac{i}{2}\Gamma_{12}}} \neq \sqrt{\frac{\mathcal{H}_{12}^*}{\mathcal{H}_{12}}} \tag{A.3.1}$$

A.3.2 Eigenvectors of the Hamiltonian

The eigenvectors (eigenstates) can be written as:

$$EV_1 = \begin{pmatrix} -\frac{q}{p} \\ 1 \end{pmatrix} \Longrightarrow \begin{pmatrix} -q \\ p \end{pmatrix} \qquad EV_2 = \begin{pmatrix} \frac{q}{p} \\ 1 \end{pmatrix} \Longrightarrow \begin{pmatrix} q \\ p \end{pmatrix}$$

The normalization of the eigenvectors yield:

$$\langle EV_1 | EV_1 \rangle = \begin{pmatrix} -q \\ p \end{pmatrix} \cdot \begin{pmatrix} -q \\ p \end{pmatrix} = (-q)^2 + p^2 = 1$$

$$\langle EV_2|EV_2\rangle = \begin{pmatrix} q \\ p \end{pmatrix} \cdot \begin{pmatrix} q \\ p \end{pmatrix} = q^2 + p^2 = 1$$

A.4 Time evolution of $X^0(t)$

The expression $|\overline{X}^0\rangle$ will be derived as linear combination of the states $|X_1\rangle = p|X^0\rangle - q|\overline{X}^0\rangle$ (see eq. (2.5.5))and $|X_2\rangle = p|X^0\rangle + q|\overline{X}^0\rangle$ (see eq. (2.5.6)):

$$|X_1\rangle \overset{(2.5.5)}{=} p|X^0\rangle - q|\overline{X}^0\rangle \Rightarrow q|\overline{X}^0\rangle = p|X^0\rangle - |X_1\rangle \tag{A.4.1}$$

$$\begin{aligned} |X_2\rangle &\overset{(2.5.6)}{=} p|X^0\rangle + q|\overline{X}^0\rangle \\ \Rightarrow |X_2\rangle &= p|X^0\rangle + p|X^0\rangle - |X_1\rangle \\ \Rightarrow |X_2\rangle &= 2p|X^0\rangle - |X_1\rangle \\ \Rightarrow |X^0\rangle &= \frac{|X_1\rangle + |X_2\rangle}{2p} \end{aligned} \tag{A.4.2}$$

$$\Rightarrow |\overline{X}^0\rangle \underset{(A.4.2)}{\overset{(A.4.1)}{=}} \frac{p}{q}\frac{|X_1\rangle + |X_2\rangle}{2p} - \frac{|X_1\rangle}{q} = \frac{|X_2\rangle - |X_1\rangle}{2q} \tag{A.4.3}$$

The time evolution of $|X^0(t=0)\rangle$ will be calculated, starting with eq. (A.4.2).

$$\begin{aligned} |X^0(t=0)\rangle &\overset{A.4.2}{=} \frac{1}{2p}\left(|X_1\rangle + |X_2\rangle\right) \\ |X^0(t)\rangle &= \frac{1}{2p}\left(e^{-i(m_1-\frac{i}{2}\Gamma_1)t}|X_1\rangle + e^{-i(m_2-\frac{i}{2}\Gamma_2)t}|X_2\rangle\right) \\ &= \frac{1}{2p}\left(e^{-i(m_1-\frac{i}{2}\Gamma_1)t}(p|X^0\rangle - q|\overline{X}^0\rangle) + e^{-i(m_2-\frac{i}{2}\Gamma_2)t}(p|X^0\rangle + q|\overline{X}^0\rangle)\right) \\ &= \underbrace{\frac{1}{2}\left(e^{-i(m_2-\frac{i}{2}\Gamma_2)t} + e^{-i(m_1-\frac{i}{2}\Gamma_1)t}\right)}_{g^+}|X^0\rangle + \dots \\ &\quad \dots \frac{q}{p}\underbrace{\frac{1}{2}\left(e^{-i(m_2-\frac{i}{2}\Gamma_2)t} - e^{-i(m_1-\frac{i}{2}\Gamma_1)t}\right)}_{g^-}|\overline{X}^0\rangle \\ &= g^+|X^0\rangle + \frac{q}{p}g^-|\overline{X}^0\rangle \end{aligned}$$

Similar for $|\overline{X}^0(t)\rangle$:

$$\begin{aligned} |\overline{X}^0(t=0)\rangle &\overset{A.4.3}{=} \frac{1}{2q}\left(|X_2\rangle - |X_1\rangle\right) \\ |\overline{X}^0(t)\rangle &= \frac{1}{2q}\left(e^{-i(m_2-\frac{i}{2}\Gamma_2)t}|X_2\rangle - e^{-i(m_1-\frac{i}{2}\Gamma_1)t}|X_1\rangle\right) \\ &= \frac{1}{2q}\left(e^{-i(m_2-\frac{i}{2}\Gamma_2)t}(p|X^0\rangle + q|\overline{X}^0\rangle) - e^{-i(m_1-\frac{i}{2}\Gamma_1)t}(p|X^0\rangle - q|\overline{X}^0\rangle)\right) \\ &= \frac{p}{q}\underbrace{\frac{1}{2}\left(e^{-i(m_2-\frac{i}{2}\Gamma_2)t} - e^{-i(m_1-\frac{i}{2}\Gamma_1)t}\right)}_{g^-}|X^0\rangle + \underbrace{\frac{1}{2}\left(e^{-i(m_2-\frac{i}{2}\Gamma_2)t} + e^{-i(m_1-\frac{i}{2}\Gamma_1)t}\right)}_{g^+}|\overline{X}^0\rangle \end{aligned}$$

$$= \frac{p}{q} g^- |X^0\rangle + g^+ |\overline{X}^0\rangle$$

A.5 Detailed calculations of $|g^{\pm}|^2$

The products of all combinations of eq. (2.5.9) and eq. (2.5.10) are calculated here, resulting in eqs. (2.5.11) to (2.5.13)), which are required for the probability to obtain a final state of $|X^0\rangle$ or $|\overline{X}^0\rangle$.

$$\begin{aligned}
g^{\pm^*} g^{\pm} &= \left(\frac{1}{2}\right)^2 \left| e^{-im_2 t} e^{-\frac{\Gamma_2}{2}t} \pm e^{-im_1 t} e^{-\frac{\Gamma_1}{2}t} \right|^2 \\
&= \frac{1}{4}\left(e^{-\Gamma_2 t} + e^{-\Gamma_1 t} \pm e^{i(m_1-m_2)t} e^{-\frac{\Gamma_2+\Gamma_1}{2}t} \pm e^{-i(m_1-m_2)t} e^{-\frac{\Gamma_2+\Gamma_1}{2}t} \right) \\
&= \frac{1}{4}\left(e^{-\Gamma_2 t} + e^{-\Gamma_1 t} \pm (e^{i\Delta m t} + e^{-i\Delta m t}) e^{-\frac{\Gamma_2+\Gamma_1}{2}t} \right) \\
&= \frac{1}{4}\left(e^{-\Gamma_2 t} + e^{-\Gamma_1 t} \pm 2\cos(\Delta m t) e^{-\frac{\Gamma_2+\Gamma_1}{2}t} \right) \\
&= \frac{1}{4}\left(e^{-\frac{\Gamma_2+\Gamma_1}{2}t} e^{-\frac{\Gamma_2-\Gamma_1}{2}t} + e^{-\frac{\Gamma_2+\Gamma_1}{2}t} e^{\frac{\Gamma_2-\Gamma_1}{2}t} \pm 2\cos(\Delta m t) e^{-\frac{\Gamma_2+\Gamma_1}{2}t} \right) \\
&= \frac{1}{4}\left(e^{-\Gamma t} (e^{-\frac{\Gamma_2-\Gamma_1}{2}t} + e^{\frac{\Gamma_2-\Gamma_1}{2}t}) \pm 2\cos(\Delta m t) e^{-\Gamma t} \right) \\
&= \frac{1}{2} e^{-\Gamma t} \left(\cosh\left(\frac{\Delta\Gamma t}{2}\right) \pm \cos(\Delta m t) \right)
\end{aligned}$$

$$\begin{aligned}
g^{+^*} g^- &= \frac{1}{4}\left(e^{-im_2 t - \frac{\Gamma_2}{2}t} + e^{-im_1 t - \frac{\Gamma_1}{2}t} \right)^* \left(e^{-im_2 t - \frac{\Gamma_2}{2}t} - e^{-im_1 t - \frac{\Gamma_1}{2}t} \right) \\
&= \frac{1}{4}\left(e^{im_2 t - \frac{\Gamma_2}{2}t} + e^{im_1 t - \frac{\Gamma_1}{2}t} \right) \left(e^{-im_2 t - \frac{\Gamma_2}{2}t} - e^{-im_1 t - \frac{\Gamma_1}{2}t} \right) \\
&= \frac{1}{4}\left(e^{-\Gamma_2 t} - e^{-\Gamma_1 t} - e^{-i(m_1-m_2)t - \frac{\Gamma_2+\Gamma_1}{2}t} + e^{i(m_1-m_2)t - \frac{\Gamma_2+\Gamma_1}{2}t} \right) \\
&= \frac{1}{4}\left(e^{-\frac{\Gamma_2+\Gamma_1}{2}t} e^{-\frac{\Gamma_2-\Gamma_1}{2}t} - e^{-\frac{\Gamma_2+\Gamma_1}{2}t} e^{\frac{\Gamma_2-\Gamma_1}{2}t} - e^{-i\Delta m t - \frac{\Gamma_2+\Gamma_1}{2}t} + e^{i\Delta m t - \frac{\Gamma_2+\Gamma_1}{2}t} \right) \\
&= \frac{1}{4}\left(e^{-\Gamma t}\left(e^{-\frac{\Gamma_2-\Gamma_1}{2}t} - e^{\frac{\Gamma_2-\Gamma_1}{2}t} \right) + \left(e^{i\Delta m t} - e^{-i\Delta m t} \right) e^{-\Gamma t} \right) \\
&= \frac{1}{2} e^{-\Gamma t} \left(-\sinh\left(\frac{\Delta\Gamma t}{2}\right) + i\sin(\Delta m t) \right)
\end{aligned}$$

$$\begin{aligned}
g^+ g^{-^*} &= \frac{1}{4}\left(e^{-im_2 t - \frac{\Gamma_2}{2}t} + e^{-im_1 t - \frac{\Gamma_1}{2}t} \right) \left(e^{-im_2 t - \frac{\Gamma_2}{2}t} - e^{-im_1 t - \frac{\Gamma_1}{2}t} \right)^* \\
&= \frac{1}{4}\left(e^{-im_2 t - \frac{\Gamma_2}{2}t} + e^{-im_1 t - \frac{\Gamma_1}{2}t} \right) \left(e^{im_2 t - \frac{\Gamma_2}{2}t} - e^{im_1 t - \frac{\Gamma_1}{2}t} \right) \\
&= \frac{1}{4}\left(e^{-\Gamma_2 t} - e^{-\Gamma_1 t} - e^{i(m_1-m_2)t - \frac{\Gamma_2+\Gamma_1}{2}t} + e^{-i(m_1-m_2)t - \frac{\Gamma_2+\Gamma_1}{2}t} \right) \\
&= \frac{1}{4}\left(e^{-\frac{\Gamma_2+\Gamma_1}{2}t} e^{-\frac{\Gamma_2-\Gamma_1}{2}t} - e^{-\frac{\Gamma_2+\Gamma_1}{2}t} e^{\frac{\Gamma_2-\Gamma_1}{2}t} - \left(e^{i\Delta m t - \frac{\Gamma_2+\Gamma_1}{2}t} - e^{-i\Delta m t - \frac{\Gamma_2+\Gamma_1}{2}t} \right) \right)
\end{aligned}$$

$$= \frac{1}{4} e^{-\Gamma t} \left(\left(e^{-\frac{\Gamma_2 - \Gamma_1}{2} t} - e^{\frac{\Gamma_2 - \Gamma_1}{2} t} \right) - \left(e^{i\Delta m t} - e^{-i\Delta m t} \right) \right)$$
$$= \frac{1}{2} e^{-\Gamma t} \left(-\sinh\left(\frac{\Delta\Gamma t}{2} \right) - i \sin\left(\Delta m t \right) \right)$$

A.6 Detailed calculation of $|K_L^0\rangle$, $|K_S^0\rangle$, $|K^0\rangle$ and $|\overline{K}^0\rangle$

For the experiment performed by Cronin and Fitch (see Sect. 2.6) the states K_L^0, K_S^0, K^0 and $\overline{K}^0$ as linear combinations of each other are derived.

A.6.1 Detailed calculation of $|K_L^0\rangle$

Expression of K_L^0 as linear combination of K^0 and $\overline{K}^0$.

$$\begin{aligned}
|K_L^0\rangle &\overset{(2.6.12)}{=} \frac{1}{1+\varepsilon} \left(\frac{1}{\sqrt{2}} \left(|K_2\rangle + \varepsilon |K_1\rangle \right) \right) \\
&\underset{(2.6.4)}{\overset{(2.6.5)}{=}} \frac{1}{\sqrt{1+\varepsilon}} \frac{1}{\sqrt{2}} \left(|K^0\rangle + |\overline{K}^0\rangle + \varepsilon |K^0\rangle - \varepsilon |\overline{K}^0\rangle \right) \\
&= \frac{1}{\sqrt{1+\varepsilon}} \frac{1}{\sqrt{2}} \left((1+\varepsilon) |K^0\rangle + (1-\varepsilon) |\overline{K}^0\rangle \right) \\
&= \underbrace{\frac{1+\varepsilon}{\sqrt{2(1+\varepsilon)}}}_{=:p} |K^0\rangle + \underbrace{\frac{1-\varepsilon}{\sqrt{2(1+\varepsilon)}}}_{=:q} |\overline{K}^0\rangle \\
&= p|K^0\rangle + q|\overline{K}^0\rangle
\end{aligned} \tag{A.6.1}$$

A.6.2 Detailed calculation of $|K_S^0\rangle$

Expression of K_S^0 as linear combination of K^0 and $\overline{K}^0$.

$$\begin{aligned}
|K_S^0\rangle &\overset{(2.6.13)}{=} \frac{1}{1+\varepsilon} \left(\frac{1}{\sqrt{2}} \left(|K_1\rangle + \varepsilon |K_2\rangle \right) \right) \\
&\underset{(2.6.4)}{\overset{(2.6.5)}{=}} \frac{1}{\sqrt{1+\varepsilon}} \frac{1}{\sqrt{2}} \left(|K^0\rangle - |\overline{K}^0\rangle + \varepsilon |K^0\rangle + \varepsilon |\overline{K}^0\rangle \right) \\
&= \frac{1}{\sqrt{1+\varepsilon}} \frac{1}{\sqrt{2}} \left((1+\varepsilon) |K^0\rangle - (1-\varepsilon) |\overline{K}^0\rangle \right) \\
&= \underbrace{\frac{1+\varepsilon}{\sqrt{2(1+\varepsilon)}}}_{=:p} |K^0\rangle - \underbrace{\frac{1-\varepsilon}{\sqrt{2(1+\varepsilon)}}}_{=:q} |\overline{K}^0\rangle \\
&= p|K^0\rangle - q|\overline{K}^0\rangle
\end{aligned} \tag{A.6.2}$$

A.6.3 Detailed calculation of $|K^0\rangle$ and $|\overline{K}^0\rangle$

Expression of K^0 and $\overline{K}^0$ as linear combinations of K_S^0 and K_L^0.

$$|K_S^0\rangle \overset{(2.6.14)}{=} p|K^0\rangle - q|\bar{K}^0\rangle \Rightarrow q|\bar{K}^0\rangle = p|K^0\rangle - |K_S^0\rangle \tag{A.6.3}$$

$$\begin{aligned}
|K_L^0\rangle &\overset{(2.6.14)}{=} p|K^0\rangle + q|\bar{K}^0\rangle \\
\Rightarrow |K_L^0\rangle &= p|K^0\rangle + p|K^0\rangle - |K_S^0\rangle \\
\Rightarrow |K_L^0\rangle &= 2p|K^0\rangle - |K_S^0\rangle \\
\Rightarrow |K^0\rangle &= \frac{|K_L^0\rangle + |K_S^0\rangle}{2p} \qquad \text{(A.6.4)} \\
\Rightarrow |\overline{K}^0\rangle &\underset{(A.6.3)}{\overset{(A.6.4)}{=}} \frac{p}{q}\frac{|K_L^0\rangle + |K_S^0\rangle}{2p} - \frac{|K_S^0\rangle}{q} = \frac{|K_L^0\rangle - |K_S^0\rangle}{2q} \qquad \text{(A.6.5)}
\end{aligned}$$

A.7 The decay rates for neutral B mesons

In this section the decay rates are calculated (see eq. (2.9.3) and eq. (2.9.4)). It is done in general, i.e., the cosh and sinh term do not disappear.

$$\begin{aligned}
\Gamma_{X^0\to f} &= |\langle f_f|X^0(t)\rangle|^2 \\
&= |g^+A_f + \tfrac{q}{p}g^-\bar{A}_f|^2 \\
&= |g^+A_f + g^-\lambda A_f|^2 \\
&= (g^+A_f + g^-\lambda A_f)(g^{+^*}A_f + g^{-^*}\lambda^* A_f) \\
&= |A_f|^2\left(|g^+|^2 + |\lambda|^2|g^-|^2 + g^+g^{-^*}\lambda^* + g^{+^*}g^-\lambda\right) \\
&\quad \text{using (2.5.11), (2.5.12) and (2.5.13) yield:} \\
&= |A_f|^2\frac{1}{2}e^{-\Gamma t}\left(\cosh\left(\tfrac{\Delta\Gamma t}{2}\right) + \cos(\Delta m t) + |\lambda|^2\left[\cosh\left(\tfrac{\Delta\Gamma t}{2}\right) - \cos(\Delta m t)\right]\right. \\
&\quad \left. + \left[-\sinh\left(\tfrac{\Delta\Gamma t}{2}\right) - i\sin(\Delta m t)\right]\lambda^* + \left[-\sinh\left(\tfrac{\Delta\Gamma t}{2}\right) + i\sin(\Delta m t)\right]\lambda\right) \\
&= |A_f|^2\frac{1}{2}e^{-\Gamma t}\left((1+|\lambda|^2)\cosh\left(\tfrac{\Delta\Gamma t}{2}\right) + (1-|\lambda|^2)\cos(\Delta m t)\right. \\
&\quad \left. - \sinh\left(\tfrac{\Delta\Gamma t}{2}\right)(\lambda^* + \lambda) + i\sin(\Delta m t)(\lambda - \lambda^*)\right) \\
&= |A_f|^2\frac{1}{2}e^{-\Gamma t}\left((1+|\lambda|^2)\cosh\left(\tfrac{\Delta\Gamma t}{2}\right) - 2\Re(\lambda)\sinh\left(\tfrac{\Delta\Gamma t}{2}\right)\right. \\
&\quad \left. + (1-|\lambda|^2)\cos(\Delta m t) - 2\Im(\lambda)\sin(\Delta m t)\right)
\end{aligned}$$

In the last line of the equation, the following first two relations have been used. Moreover, the third relation will be used in the next equation $\Gamma_{\overline{X}^0\to f}$:

$$\begin{aligned}
\lambda + \lambda^* &= (a - ib) + (a + ib) = 2a = \Re(\lambda) \\
\lambda - \lambda^* &= (a + ib) - (a - ib) = 2ib = 2i\Im(\lambda) \\
\lambda^* - \lambda &= (a - ib) - (a + ib) = -2ib = -2i\Im(\lambda)
\end{aligned}$$

$$\Gamma_{\overline{X}^0\to f} = |\langle f_{CP}|\overline{X}^0(t)\rangle|^2$$

$$
\begin{aligned}
&= \left|\frac{p}{q} g^- A_{CP} + g^+ \bar{A}_{CP}\right|^2 \\
&= \left|\frac{p}{q}\frac{A_{CP}}{\bar{A}_{CP}} g^- \bar{A}_{CP} + g^+ \bar{A}_{CP}\right|^2 \\
&= \left|\frac{1}{\lambda}\bar{A}_{CP}(g^- + \lambda g^+)\right|^2 \\
&= \left|\frac{p}{q}\frac{A_{CP}}{\bar{A}_{CP}}\bar{A}_{CP}(g^- + \lambda g^+)\right|^2 \\
&= |A_{CP}|^2 \left|\frac{p}{q}\right|^2 \left|g^- + \lambda g^+\right|^2 \\
&= |A_{CP}|^2 \left|\frac{p}{q}\right|^2 \left(g^- + \lambda g^+\right)\left(g^{-^*} + \lambda^* g^{+^*}\right) \\
&= |A_{CP}|^2 \left|\frac{p}{q}\right|^2 \left(g^{-^2} + |\lambda|^2 g^{+^2} + \lambda^* g^- g^{+^*} + \lambda g^+ g^{-^*}\right) \\
&\quad \text{using (2.5.11), (2.5.12) and (2.5.13) yield:} \\
&= |A_{CP}|^2 \left|\frac{p}{q}\right|^2 \tfrac{1}{2} e^{-\Gamma t}\left(\cosh\left(\tfrac{\Delta\Gamma t}{2}\right) - \cos(\Delta m t) + |\lambda|^2\left[\cosh\left(\tfrac{\Delta\Gamma t}{2}\right) + \cos(\Delta m t)\right]\right. \\
&\quad \left. + \left[-\sinh\left(\tfrac{\Delta\Gamma t}{2}\right) + i\sin(\Delta m t)\right]\lambda^* + \left[-\sinh\left(\tfrac{\Delta\Gamma t}{2}\right) - i\sin(\Delta m t)\right]\lambda\right) \\
&= |A_{CP}|^2 \left|\frac{p}{q}\right|^2 \tfrac{1}{2} e^{-\Gamma t}\left((1 + |\lambda|^2)\cosh\left(\tfrac{\Delta\Gamma t}{2}\right) - 2\Re(\lambda)\sinh\left(\tfrac{\Delta\Gamma t}{2}\right)\right. \\
&\quad \left. - (1 - |\lambda|^2)\cos(\Delta m t) + 2\Im(\lambda)\sin(\Delta m t)\right)
\end{aligned}
$$

A.8 Probability density for B meson

One starts from eq. (2.9.3) and eq. (2.9.4) describing the decay rates.
Moreover, the GIM cancellations are taken into account, i.e., $\frac{p}{q} \approx 1$
Using $|\frac{p}{q}| \approx 1$

$$
\begin{aligned}
\Gamma(f_{CP}, q) =& \frac{1}{4} e^{-\Gamma(t_1+t_2)} A_1^2 A_2^2 \cdots && \text{(A.8.1)} \\
& \cdots \left[(|\lambda|^2 + 1) + q\left[(|\lambda|^2 - 1)\cos(\Delta m \Delta t) + 2\Im(\lambda)\sin(\Delta m \Delta t)\right]\right] && \text{(A.8.2)}
\end{aligned}
$$

We want to calculate the probability density function $\mathcal{P}(\Delta t, q)$ of finding f_{CP} for any Δt for and a given flavor tag $q = \pm 1$.
The sum of both contributions, i.e., finding the different flavors have to be normalized to 1, i.e.,

$$
\sum_q P(t_1, t_2, q) = \frac{1}{N}\sum_q \Gamma(t_1, t_2, q) = 1 \qquad \text{(A.8.3)}
$$

Since only the time difference $\Delta t = t_2 - t_1$ is experimentally accessible and $t_1, t_2 \in [0, \infty[$, one normalizes to unity in the region $-\infty < \Delta t < \infty$. Hence, the norm

factor is calculated by:

$$N = \int_{-\infty}^{\infty} \sum_q \Gamma(t_1, t_2, q) d\Delta t \tag{A.8.4}$$

$$= \int_{-\infty}^{\infty} \frac{1}{2} e^{-\Gamma(t_1+t_2)} A_1^2 A_2^2 [1 + |\lambda|^2] d\Delta t \tag{A.8.5}$$

$$\text{with } c := \frac{1}{2} A_1^2 A_2^2 [1 + |\lambda|^2] \tag{A.8.6}$$

$$= \int_{-\infty}^{\infty} c e^{-\Gamma(t_1+t_2)} \tag{A.8.7}$$

for $t_1 < t_2$:

$$N = c e^{-2\Gamma t_1} \int_0^{\infty} e^{-\Gamma \Delta t} d(\Delta t) \tag{A.8.8}$$

for $t_1 < t_2$:

$$N = c e^{-2\Gamma t_2} \int_{-\infty}^{0} e^{\Gamma \Delta t} d(\Delta t) \tag{A.8.9}$$

Now, we define $t' = \min(t_1, t_2)$:

$$N = c e^{-2\Gamma t'} \int_{-\infty}^{\infty} e^{-\Gamma |\Delta t|} d(\Delta t) \tag{A.8.10}$$

$$= \frac{2}{\Gamma} c e^{-2\Gamma t'} \tag{A.8.11}$$

$$= A_1^2 A_2^2 [1 + |\lambda|^2] e^{-2\Gamma t'} \tau \tag{A.8.12}$$

where $\tau := \frac{1}{\Gamma}$
Rewriting eq. (A.8.1) we obtain:

$$\Gamma(t_1, t_2, q) = \Gamma(t', |\Delta t|, q) = \frac{1}{4} e^{-2\Gamma t'} e^{-\Gamma |\Delta t|} A_1^2 A_2^2 \cdots \tag{A.8.13}$$

$$\cdots \left[(|\lambda|^2 + 1) + q \left[(|\lambda|^2 - 1) \cos(\Delta m \Delta t) + 2\Im(\lambda) \sin(\Delta m \Delta t) \right] \right] \tag{A.8.14}$$

Hence, one obtains for P:

$$P(\Delta t, q) = \frac{1}{N} \Gamma(t', |\Delta t|, q) \tag{A.8.15}$$

$$= \frac{1}{4} \frac{e^{-2\Gamma t'}}{\tau} \frac{e^{-\Gamma |\Delta t|} A_1^2 A_2^2}{e^{-2\Gamma t'} A_1^2 A_2^2} \left[\frac{|\lambda|^2 + 1}{|\lambda^2| + 1} + q \left[\frac{|\lambda|^2 + 1}{|\lambda^2| - 1} \cos(\Delta m \Delta t) + \frac{2\Im(\lambda)}{\lambda^2 + 1} \sin(\Delta m \Delta t) \right] \right] \tag{A.8.16}$$

$$= \frac{e^{-\Gamma |\Delta t|}}{4\tau} \left[1 + q \left[\mathcal{A}_{\mathcal{CP}} \cos(\Delta m \Delta t) + \mathcal{S}_{\mathcal{CP}} \sin(\Delta m \Delta t) \right] \right] \tag{A.8.17}$$

Appendix B

Theory - Accelerator and Detector

B.1 Derivation of Emittance equation

In Sect. 3.2.4 the emittance is introduced. The equation of motion for a particle beam is given by the Hill's differential equation

$$h''(s) - k(s)h(s) = 0 \tag{B.1.1}$$

with the solution

$$h(s) = \sqrt{\varepsilon}\sqrt{\beta(s)}\cos\big(\Psi(s) + \Phi(s)\big) \tag{B.1.2}$$

$$h'(s) = -\frac{\sqrt{\varepsilon}}{\sqrt{\beta}}\big[\alpha\cos(\Psi(s) + \Phi) + \sin(\Psi(s) + \Phi)\big] \tag{B.1.3}$$

where A denotes the amplitude and Φ the phase. Those parameters are determined by boundary conditions. Further, $\alpha(s) := -\frac{\beta'(s)}{2}$ and one defines the function for the amplitude $\beta(s)$, the betafunction, given by

$$\beta(s) := u^2(s) \tag{B.1.4}$$

and the factor for the amplitude by $\sqrt{\varepsilon}$:

$$A := \sqrt{\varepsilon} \tag{B.1.5}$$

Rewriting eq. (B.1.2) and putting into eq. (B.1.3) yields

$$-\sin(\Psi(s) + \Phi) = \frac{h'(s)\sqrt{\beta(s)}}{\sqrt{\varepsilon}} + \frac{\alpha h}{\sqrt{\varepsilon\beta}}$$

Applying the relation $\sin^2(x) + \cos^2(x) = 1$ yields:

$$\frac{h^2}{\beta(s)} + \left(\frac{\alpha(s)}{\sqrt{\beta(s)}}h + \sqrt{\beta(s)}h'\right) = \varepsilon \tag{B.1.6}$$

Moreover one defines $\gamma(s) := \frac{q+\alpha(s)}{\beta(s)}$ resulting in:

$$\gamma(s)h^2(s) + 2\alpha(s)h(s)h'(s) + \beta(s)h'^2(s) = \varepsilon \tag{B.1.7}$$

B.2 Derivation of Ellipse equation in phase space

The ellipse in the phase space (see Sect. 3.2.4) is mathematically described by the polar coordinates:

$$\tilde{x}(\varphi) = a\cos(\varphi) \tag{B.2.1}$$
$$\tilde{x}'(\varphi) = b\sin(\varphi) \tag{B.2.2}$$

Applying a transformation by multiplying a 2×2 rotation matrix results in

$$\begin{pmatrix} h \\ h' \end{pmatrix} = \begin{pmatrix} \cos(\Psi) & \sin(\Psi) \\ -\sin(\Psi) & \cos(\Psi) \end{pmatrix} \cdot \begin{pmatrix} a\cos(\varphi) \\ b\sin(\varphi) \end{pmatrix} \tag{B.2.3}$$
$$h = a\cos(\varphi)\cos(\Psi) + b\sin(\varphi)\sin(\Psi) \tag{B.2.4}$$
$$h' = -a\cos(\varphi)\sin(\Psi) + b\sin(\varphi)\cos(\Psi) \tag{B.2.5}$$

Rewriting those equations and using $\sin^2(x) + \cos^2(x) = 1$ yields:

$$\begin{aligned} a^2b^2 &= b^2(h\cos\Psi - h'\sin\Psi)^2 + a^2(h\sin\Psi + h'\cos\Psi)^2 \\ &= (b^2\sin^2\Psi + a^2\cos^2\Psi)h'^2 + 2(a^2 - b^2)\cos\Psi\sin\Psi hh' + (b^2\cos^2\Psi + a^2\sin^2\Psi)h^2 \\ ab &= \underbrace{\left(\frac{b}{a}\sin^2\Psi + \frac{a}{b}\cos^2\Psi\right)}_{=:\beta} h'^2 + 2\underbrace{\left(\frac{a}{b} - \frac{b}{a}\right)\cos\Psi\sin\Psi}_{=:\alpha} hh' + \underbrace{\left(\frac{b}{a}\cos^2\Psi + \frac{a}{b}\sin^2\Psi\right)}_{\gamma} h^2 \\ \frac{A}{\pi} &= \beta h'^2 + 2\alpha hh' + \gamma h^2 = \varepsilon \end{aligned}$$

where A denotes the area of the ellipse $A = ab\pi$ and $\gamma = \frac{1+\alpha^2}{\beta}$.

B.3 Electric properties of the DEPFET

In this section a mathematical description will be derived according to Lutz [143]. The first Maxwell and Poisson equation states:

$$\Delta\phi - \underbrace{\frac{\partial\vec{A}}{\partial t}}_{=0} = -\nabla\vec{\tilde{E}} \overset{\text{1-dim}}{=} \frac{\mathrm{d}}{\mathrm{d}x}\tilde{E}_x = \frac{\rho}{\varepsilon_0\varepsilon_\mathrm{r}}, \tag{B.3.1}$$

where ϕ denotes the electric potential, $\vec{A}$ is the magnetic vector potential, $\tilde{E}$ is the electric field, $\varepsilon_0 = 8.85 \cdot 10^{-12}\,\mathrm{As/Vm}$ is the permittivity in vacuum and ε_r is the material dependent permittivity. The charge density ρ is equal to $N_\mathrm{D}e$, with $e = 1.60 \cdot 10^{-19}\,\mathrm{As}$ the elementary charge and N_D the donor concentration.
The electric field $\tilde{E}_s$ and the potential ψ_s are calculated at the semiconductor surface by integration over the depletion layer depth d_s:

$$\tilde{E}_s = \int_0^{d_s} \frac{\mathrm{d}}{\mathrm{d}x}\tilde{E}_x \mathrm{d}x = \int_0^{d_s} -\frac{eN_\mathrm{D}(x)}{\varepsilon_0\varepsilon_\mathrm{r}}\mathrm{d}x \overset{N_\mathrm{D}(x)=N_\mathrm{D}}{=} -\frac{eN_\mathrm{D}}{\varepsilon_0\varepsilon_\mathrm{r}}\mathrm{d}_s \tag{B.3.2}$$

$$\psi_{\mathrm{s}} = \int_0^{d_{\mathrm{s}}} \frac{eN_{\mathrm{D}}}{\varepsilon_0\varepsilon_{\mathrm{r}}} \mathrm{d}_s x \mathrm{d}x = \frac{eN_{\mathrm{D}}}{\varepsilon_0\varepsilon_{\mathrm{r}}} \frac{\mathrm{d}_s^2}{2} \tag{B.3.3}$$

At the beginning of "strong inversion," i.e., at the formation of a hole inversion layer in the n-doped bulk, the surface potential ψ_{s} is shifted twice the distance of the Fermi level from the intrinsic level in the undepleted bulk, i.e.,

$$\psi_{\mathrm{s}} = -2\psi_{\mathrm{B}}. \tag{B.3.4}$$

The depth of the space charge region (d_{s}) of the channel and the substrate is calculated from the difference of the substrate potential V_{sub} and the surface potential ψ_{s}. Since the DEPFET is a p-channel transistor a negative voltage must be applied for its normal operation, i.e., current flows from the *Source implant* to the *Drain implant*.

$$V_{\mathrm{sub}} - \psi_{\mathrm{s}} = \frac{eN_{\mathrm{D}}}{\varepsilon_0\varepsilon_{\mathrm{r}}} \frac{d_{\mathrm{s}}^2}{2} \quad \Leftrightarrow \quad d_{\mathrm{s}} = \sqrt{\frac{2\varepsilon_0\varepsilon_{\mathrm{r}}}{eN_{\mathrm{D}}}(V_{\mathrm{sub}} - \psi_{\mathrm{s}})} \tag{B.3.5}$$

The surface electric field can be calculated by:

$$\tilde{E}_{\mathrm{s}} \overset{(B.3.2)}{=} -\frac{eN_{\mathrm{D}}}{\varepsilon_0\varepsilon_{\mathrm{r}}} d_{\mathrm{s}} \overset{(B.3.5)}{=} -\sqrt{\frac{2eN_{\mathrm{D}}}{\varepsilon_0\varepsilon_{\mathrm{r}}}(V_{\mathrm{sub}} - \psi_{\mathrm{s}})} \tag{B.3.6}$$

The electric field in the oxide is given by:

$$\tilde{E}_{\mathrm{ox}} = \frac{V_{\mathrm{G}} - V_{\mathrm{FB}} - \psi_{\mathrm{s}}}{d_{\mathrm{ox}}}, \tag{B.3.7}$$

where V_{G} is the voltage applied at the *external Gate*, V_{FB} is the flat-band voltage and d_{ox} is the thickness of the oxide. (The flat-band voltage is equal to the work function difference between metal and semiconductor in absence of charge in the oxide.) The surface charge density Q_{c} is introduced:

$$\begin{aligned} Q_{\mathrm{c}} &= -\varepsilon_{\mathrm{ox}}\varepsilon_0\tilde{E}_{\mathrm{ox}} + \varepsilon_{\mathrm{r}}\varepsilon_0\tilde{E}_{\mathrm{s}} - f\frac{Q_{\mathrm{sig}}}{WL} \\ &= -\left[C_{\mathrm{ox}}(V_{\mathrm{G}} - V_{\mathrm{FB}} - \psi_{\mathrm{s}}) + f\frac{Q_{\mathrm{sig}}}{WL} + \sqrt{2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}(V_{\mathrm{sub}} - \psi_{\mathrm{s}})}\right] \end{aligned} \tag{B.3.8}$$

Here, the oxide capacitance per unit area $C_{\mathrm{ox}} = \varepsilon_0\varepsilon_{\mathrm{r}}/d_{\mathrm{ox}}$ was introduced. The term $f\frac{Q_{\mathrm{sig}}}{WL}$ is a very rough approximation describing the influence of the Source-Drain current due to the *internal Gate* being close to the conduction channel. Its effect is treated as a change of the *external Gate* voltage, where W denotes the width of the inversion channel, L the length of the inversion channel, Q_{sig} is the charge accumulated in the *internal Gate* and $0 \leq f \leq 1$ is an undetermined scale factor. The threshold (Gate voltage) can be derived by setting $Q_{\mathrm{c}} = 0$ and $\psi_{\mathrm{s}} = -2\psi_{\mathrm{B}}$ (at the onset of strong inversion). From eq. (B.3.8) one obtains:

$$0 = V_{\mathrm{G}} - V_{\mathrm{FB}} - \psi_{\mathrm{s}} + f\frac{Q_{\mathrm{sig}}}{WL} + \frac{1}{C_{\mathrm{ox}}}\sqrt{2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}(V_{\mathrm{sub}} + 2\psi_{\mathrm{B}})} \tag{B.3.9}$$

$$\Leftrightarrow V_{\mathrm{T}} = V_{\mathrm{G}} = V_{\mathrm{FB}} - 2\psi_{\mathrm{B}} - f\frac{Q_{\mathrm{sig}}}{WL} - \frac{1}{C_{\mathrm{ox}}}\sqrt{2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}(V_{\mathrm{sub}} + 2\psi_{\mathrm{B}})} \tag{B.3.10}$$

Applying a small voltage V_{ds} between the *Source implant* and the *Drain implant* results in a shift of the channel potential between $2\psi_{\mathrm{B}}$ and $2\psi_{\mathrm{B}} + V_{\mathrm{ds}}$. Parameterizing the channel potential yields:

$$\psi_{\mathrm{s}}(y) = V_{\mathrm{c}}(y) - 2\psi_{\mathrm{B}} \qquad V_{\mathrm{c}}(0) = 0,\ V_{\mathrm{c}}(L) = V_{\mathrm{ds}} \tag{B.3.11}$$

The calculation for the Drain current of the transistor gives:

$$\begin{aligned} I_{\mathrm{ds}} = -\mu_{\mathrm{h}}\tilde{E}_{\mathrm{y}}(y)Q_{\mathrm{c}}(y)W = \mu_{\mathrm{h}}\frac{\partial V_{\mathrm{c}}(y)}{\partial y}Q_{\mathrm{c}}(y)W \overset{(B.3.8),(B.3.11)}{=} \\ -\mu_{\mathrm{h}}\frac{dV_{\mathrm{c}}(y)}{\mathrm{d}y}W\Bigg[C_{\mathrm{ox}}\Big(V_{\mathrm{G}} - V_{\mathrm{FB}} - V_{\mathrm{c}}(y) + 2\psi_{\mathrm{B}} + f\frac{Q_{\mathrm{sig}}}{WLC_{\mathrm{ox}}}\Big) + \dots \\ \sqrt{2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}(V_{\mathrm{sub}} - V_{\mathrm{c}}(y) + 2\psi_{\mathrm{B}})}\Bigg] \end{aligned} \tag{B.3.12}$$

Rewriting the Drain current by integrating the Drain current between Source and Drain and dividing it by its length L yields:

$$I_{\mathrm{ds}} = \frac{1}{L}\int_{y=0}^{L} I'_{\mathrm{ds}}\mathrm{d}y \overset{(B.3.12)}{=} -\frac{1}{L}\int_{y=0}^{L} W\mu_{\mathrm{h}}Q_{\mathrm{c}}(y)\frac{\mathrm{d}V_{\mathrm{c}}}{\mathrm{d}y}\mathrm{d}y = -\frac{W}{L}\mu_{\mathrm{h}}\int_{V_{\mathrm{c}}=0}^{V_{\mathrm{ds}}} Q_{\mathrm{d}}(V'_{\mathrm{d}})\mathrm{d}V'_{\mathrm{c}} \tag{B.3.13}$$

$$\begin{aligned} = -\frac{W}{L}\mu_{\mathrm{h}}C_{\mathrm{ox}}\int_{V_{\mathrm{c}}=0}^{V_{\mathrm{ds}}}\Bigg(\Big(V_{\mathrm{G}} - V_{\mathrm{FB}} - V'_{\mathrm{c}} + 2\psi_{\mathrm{B}} + f\frac{Q_{\mathrm{sig}}}{C_{\mathrm{ox}}WL}\Big) + \dots \\ + \frac{\sqrt{2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}}}{C_{\mathrm{ox}}}\sqrt{V_{\mathrm{sub}} - V'_{\mathrm{c}} + 2\psi_{\mathrm{B}}}\Bigg)\mathrm{d}V'_{\mathrm{c}} \\ = -\frac{W}{L}\mu_{\mathrm{h}}C_{\mathrm{ox}}\Bigg[\Big(V_{\mathrm{G}} - V_{\mathrm{FB}} - \frac{V'_{\mathrm{c}}}{2} + 2\psi_{\mathrm{B}} + f\frac{Q_{\mathrm{sig}}}{C_{\mathrm{ox}}WL}\Big)V_{\mathrm{c}}\Big|_{V_{\mathrm{c}}=0}^{V_{\mathrm{ds}}} - \dots \\ - \frac{2}{3}\frac{\sqrt{2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}}}{C_{\mathrm{ox}}}\Big(V_{\mathrm{sub}} - V'_{\mathrm{c}} + 2\psi_{\mathrm{B}}\Big)^{3/2}(-1)\Big|_{V_{\mathrm{c}}=0}^{V_{\mathrm{ds}}}\Bigg] \\ = -\frac{W}{L}\mu_{\mathrm{h}}C_{\mathrm{ox}}\Bigg[\Big(V_{\mathrm{G}} - V_{\mathrm{FB}} - \frac{V_{\mathrm{ds}}}{2} + 2\psi_{\mathrm{B}} + f\frac{Q_{\mathrm{sig}}}{C_{\mathrm{ox}}WL}\Big)V_{\mathrm{ds}} - \dots \\ \frac{2}{3}\frac{\sqrt{2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}}}{C_{\mathrm{ox}}}\Big[(V_{\mathrm{sub}} - V_{\mathrm{ds}} + 2\psi_{\mathrm{B}})^{3/2} - (V_{\mathrm{sub}} + 2\psi_{\mathrm{B}})^{3/2}\Big]\Bigg] \end{aligned} \tag{B.3.14}$$

Setting $Q_{\mathrm{c}} = 0$ and $\psi_{\mathrm{s}} = V_{\mathrm{ds}} - 2\psi_{\mathrm{B}}$ to obtain the saturation voltage, yields:

$$Q_{\mathrm{c}} = -\left[C_{\mathrm{ox}}\Big(V_{\mathrm{G}} - V_{\mathrm{FB}} - \psi_{\mathrm{s}} + f\frac{Q_{\mathrm{sig}}}{C_{\mathrm{ox}}WL}\Big) + \sqrt{2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}(V_{\mathrm{sub}} - \psi_{\mathrm{s}})}\right]$$

$$= -\Bigg[C_{\rm ox}\Big(V_{\rm G} - V_{\rm FB} - V_{\rm ds} + 2\psi_{\rm B} + f\frac{Q_{\rm sig}}{C_{\rm ox}WL}\Big) + \dots$$

$$\cdots + \sqrt{2eN_{\rm D}\varepsilon_0\varepsilon_{\rm r}(V_{\rm sub} - V_{\rm ds} + 2\psi_{\rm B})}\Bigg] \stackrel{!}{=} 0 \tag{B.3.15}$$

$$\Leftrightarrow -\Bigg[C_{\rm ox}\Big(V_{\rm G} - V_{\rm FB} - V_{\rm sub} + V_{\rm sub} - V_{\rm ds} + 2\psi_{\rm B} + f\frac{Q_{\rm sig}}{C_{\rm ox}WL}\Big) + \sqrt{\dots}\Bigg] = 0$$

$$u := \sqrt{V_{\rm sub} - V_{\rm ds} + 2\psi_{\rm B}}$$

$$\Leftrightarrow -\Bigg[C_{\rm ox}u^2 + \sqrt{2eN_{\rm D}\varepsilon_0\varepsilon_{\rm r}}u + C_{\rm ox}(V_{\rm G} - V_{\rm FB} - V_{\rm sub} + f\frac{Q_{\rm sig}}{C_{\rm ox}WL})\Bigg] = 0$$

$$\Leftrightarrow u_{1,2} = \frac{\sqrt{2eN_D\varepsilon_0\varepsilon_{\rm r}} \pm \sqrt{2eN_{\rm D}\varepsilon_0\varepsilon_{\rm r} - 4C_{\rm ox}^2(V_{\rm G} - V_{\rm FB} - V_{\rm sub} + f\frac{Q_{\rm sig}}{C_{\rm ox}WL})}}{-2C_{\rm ox}}$$

$$\Leftrightarrow u^2 = V_{\rm sub} - V_{\rm ds} + 2\psi_{\rm B} = \frac{1}{4C_{\rm ox}^2}\Bigg[2eN_{\rm D}\varepsilon_0\varepsilon_{\rm r} \pm \sqrt{2eN_{\rm D}\varepsilon_0\varepsilon_{\rm r}}\cdot\dots$$
$$\cdot\sqrt{2eN_{\rm D}\varepsilon_0\varepsilon_{\rm r} - 4C_{\rm ox}^2(V_{\rm G} - V_{\rm FB} - V_{\rm sub})} + \dots$$
$$2eN_{\rm D}\varepsilon_0\varepsilon_{\rm r}\cdot 4C_{\rm ox}^2\Big(V_{\rm G} - V_{\rm FB} - V_{\rm sub} + f\frac{Q_{\rm sig}}{WLC_{\rm ox}}\Big)\Bigg]$$

$$V_{\rm ds_{sat}} = V_{\rm sub} + 2\psi_{\rm B} + V_{\rm G} - V_{\rm FB} - V_{\rm sub} + f\frac{Q_{\rm sig}}{C_{\rm ox}WL} + \frac{eN_{\rm D}\varepsilon_0\varepsilon_{\rm r}}{C_{\rm ox}^2}\cdot\Bigg[1 + \dots$$
$$+ \frac{\sqrt{(2eN_{\rm D}\varepsilon_0\varepsilon_{\rm r})^2 - 2eN_{\rm D}\varepsilon_0\varepsilon_{\rm r} - 4C_{\rm ox}^2(V_{\rm G} - V_{\rm FB} - V_{\rm sub})}}{2eN_{\rm D}\varepsilon_0\varepsilon_{\rm r}}\Bigg]$$

$$= 2\psi_{\rm B} + V_{\rm G} - V_{\rm FB} + f\frac{Q_{\rm sig}}{C_{\rm ox}WL} + \frac{eN_{\rm D}\varepsilon_0\varepsilon_{\rm r}}{C_{\rm ox}^2}\Bigg[1 + \sqrt{1 + \frac{C_{\rm ox}^2(-V_{\rm G} + V_{\rm FB} + V_{\rm sub})}{2eN_{\rm D}\varepsilon_0\varepsilon_{\rm r}}}\Bigg] \tag{B.3.16}$$

Thus, saturation current is calculated by:

$$I_{\rm ds_{sat}} = -\frac{W}{L}\mu_{\rm h}C_{\rm ox}\Bigg[\Big(V_{\rm G} - V_{\rm FB} + 2\psi_{\rm B} + f\frac{Q_{\rm sig}}{WLC_{\rm ox}}\Big)V_{\rm ds_{sat}} - \dots$$
$$\frac{2}{3}\frac{\sqrt{2eN_{\rm D}\varepsilon_0\varepsilon_{\rm r}}}{C_{\rm ox}}\Big[(V_{\rm sub} - V_{\rm ds_{sat}} + 2\psi_{\rm B})^{2/3} - \Big(\mathrm{V}_{\rm sub} + 2\psi_{\rm B}\Big)^{2/3}\Big]\Bigg] \tag{B.3.17}$$

In the following the important DEPFET parameters, transconductance $g_{\rm m}$ (external amplification), the internal amplification $g_{\rm q}$, the output conductance g and the influence of the substrate on the current $g_{\rm sub}$ will be derived for the threshold

region $V_{\mathrm{ds}} < V_{\mathrm{ds_{sat}}}$:

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{G}}} = -\frac{W}{L}\mu_{\mathrm{h}} C_{\mathrm{ox}} V_{\mathrm{ds}} \tag{B.3.18}$$

$$g_{\mathrm{q}} = \frac{\partial I_{\mathrm{ds}}}{\partial Q_{\mathrm{sig}}} = -\frac{W}{L}\mu_{\mathrm{h}} C_{\mathrm{ox}} f \frac{V_{\mathrm{ds}}}{WLC_{\mathrm{ox}}} = -\frac{\mu_{\mathrm{h}} f V_{\mathrm{ds}}}{L^2} \tag{B.3.19}$$

$$g = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{ds}}} = -\frac{W}{L}\mu_{\mathrm{h}} C_{\mathrm{ox}} \Bigg[\Big(V_{\mathrm{G}} - V_{\mathrm{FB}} + 2\psi_{\mathrm{B}} + f\frac{Q_{\mathrm{sig}}}{WLC_{\mathrm{ox}}} - V_{\mathrm{ds}} \Big) + \dots + \frac{\sqrt{2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}}}{C_{\mathrm{ox}}} \Big(\sqrt{V_{\mathrm{sub}} - V_{\mathrm{ds}} + 2\psi_{\mathrm{B}}} \Big) \Bigg] \tag{B.3.20}$$

$$g_{\mathrm{sub}} = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{sub}}} = -\frac{W}{L}\mu_{\mathrm{h}} C_{\mathrm{ox}} \left[V_{\mathrm{G}} - V_{\mathrm{FB}} - V_{\mathrm{ds}} + 2\psi_{\mathrm{B}} + \frac{\sqrt{2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}}}{C_{\mathrm{ox}}} \sqrt{V_{\mathrm{sub}} - V_{\mathrm{ds}} + 2\psi_{\mathrm{B}}} \right] \tag{B.3.21}$$

Here, the parameters for the saturation region will be calculated:

$$\begin{aligned} g_{\mathrm{m_{sat}}} &= \frac{\partial I_{\mathrm{ds_{sat}}}}{\partial V_{\mathrm{G}}} \overset{B.3.17}{=} -\frac{W}{L}\mu_{\mathrm{h}} C_{\mathrm{ox}} V_{\mathrm{ds_{sat}}} \\ &\overset{(B.3.13)}{=} \frac{W}{L}\mu_{\mathrm{h}} \frac{\partial}{\partial V_{\mathrm{G}}} \int_{V_{\mathrm{c}}=0}^{V_{\mathrm{ds_{sat}}}} Q_{\mathrm{c}}(V_{\mathrm{c}}')\, dV_{\mathrm{c}}' \\ &= \frac{W}{L}\mu_{\mathrm{h}} \left[\int_{V_{\mathrm{c}}=0}^{V_{\mathrm{ds_{sat}}}} \frac{\partial Q_{\mathrm{c}}(V_{\mathrm{c}}')}{\partial V_{\mathrm{G}}} \mathrm{d}V_{\mathrm{c}}' + \frac{\partial}{\partial V_{\mathrm{G}}} [Q_{\mathrm{c}}(V_{\mathrm{ds_{sat}}}) V_{\mathrm{ds_{sat}}} - Q_{\mathrm{c}}(0)0] \right] = \\ &= \frac{W}{L}\mu_{\mathrm{h}} \left[\int_{V_{\mathrm{c}}=0}^{V_{\mathrm{ds_{sat}}}} \frac{\partial Q_{\mathrm{c}}(V_{\mathrm{c}}')}{\partial V_{\mathrm{G}}} \mathrm{d}V_{\mathrm{c}}' + Q_{\mathrm{c}}(V_{\mathrm{ds_{sat}}}) \frac{\partial V_{\mathrm{ds_{sat}}}}{\partial V_{\mathrm{G}}} \right] \end{aligned} \tag{B.3.22}$$

$$\begin{aligned} g_{\mathrm{sub_{sat}}} &= \frac{\partial I_{\mathrm{V_{ds_{sat}}}}}{\partial V_{\mathrm{G}}} \overset{B.3.17}{=} \frac{W}{L}\mu_{\mathrm{h}} C_{\mathrm{ox}} \frac{\sqrt{2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}}}{C_{\mathrm{ox}}} \left[\sqrt{V_{\mathrm{sub}} - V_{\mathrm{ds_{sat}}} + 2\psi_{\mathrm{B}}} - \sqrt{V_{\mathrm{sub}} + 2\psi_{\mathrm{B}}} \right] \\ &\overset{(B.3.13)}{=} \frac{W}{L}\mu_{\mathrm{h}} \frac{\partial}{\partial V_{\mathrm{sub}}} \int_{V_{\mathrm{c}}=0}^{V_{\mathrm{ds_{sat}}}} Q_{\mathrm{c}}(V_{\mathrm{c}}')\mathrm{d}V_{\mathrm{c}}' \\ &= \frac{W}{L}\mu_{\mathrm{h}} \left[\int_{V_{\mathrm{c}}=0}^{V_{\mathrm{ds_{sat}}}} \frac{\partial Q_{\mathrm{c}}(V_{\mathrm{c}}')}{\partial V_{\mathrm{sub}}} \mathrm{d}V_{\mathrm{c}}' + \frac{\partial}{\partial V_{\mathrm{sub}}} (Q_{\mathrm{c}}(V_{\mathrm{ds_{sat}}}) V_{\mathrm{ds_{sat}}} - Q_{\mathrm{c}}(0)0) \right] \\ &= \frac{W}{L}\mu_{\mathrm{h}} \left[\int_{V_{\mathrm{c}}=0}^{V_{\mathrm{ds_{sat}}}} \frac{\partial Q_{\mathrm{c}}(V_{\mathrm{c}}')}{\partial V_{\mathrm{sub}}} \mathrm{d}V_{\mathrm{c}}' + Q_{\mathrm{c}}(V_{\mathrm{ds_{sat}}}) \frac{\partial V_{\mathrm{ds_{sat}}}}{\partial V_{\mathrm{sub}}} \right] \end{aligned} \tag{B.3.23}$$

$$g_{\mathrm{q_{sat}}} = \frac{\partial I_{\mathrm{ds_{sat}}}}{\partial Q_{\mathrm{sig}}} = -\frac{W}{L}\mu_{\mathrm{h}} C_{\mathrm{ox}} f \frac{V_{\mathrm{ds_{sat}}}}{WLC_{\mathrm{ox}}} = -\frac{\mu_{\mathrm{h}} f V_{\mathrm{ds_{sat}}}}{L^2} \tag{B.3.24}$$

$$g_{\mathrm{m_{sat}}} + g_{\mathrm{sub_{sat}}} = \frac{W}{L}\mu_{\mathrm{h}} \left[\int_{V_{\mathrm{c}}=0}^{V_{\mathrm{ds_{sat}}}} \Big(\frac{\partial Q_{\mathrm{c}}}{\partial V_{\mathrm{G}}} + \frac{\partial Q_{\mathrm{c}}}{\partial V_{\mathrm{sub}}} \Big) \mathrm{d}V_{\mathrm{c}} + \underbrace{Q_{\mathrm{c}}(V_{\mathrm{ds_{sat}}}) \Big(\frac{\partial V_{\mathrm{ds_{sat}}}}{\partial V_{\mathrm{G}}} + \frac{\partial V_{\mathrm{ds_{sat}}}}{\partial V_{\mathrm{sub}}} \Big)}_{=0 \text{ for } V_{\mathrm{ds_{sat}}}=0} \right]$$

$$\overset{(B.3.26)}{=} -\frac{W}{L}\mu_{\mathrm{D}}\int_{V_{\mathrm{c}}=0}^{V_{\mathrm{ds_{sat}}}}\frac{\partial Q_{\mathrm{c}}(V_{\mathrm{c}}')}{\partial V_{\mathrm{c}}'}\mathrm{d}V_{\mathrm{c}} = -\frac{W}{L}\mu_{\mathrm{D}}\Big[Q_{\mathrm{c}}(V_{\mathrm{ds_{sat}}}=0) - Q_{\mathrm{c}}(V_{\mathrm{c}}=0)\Big] = \frac{W}{L}\mu_{\mathrm{D}}Q_{\mathrm{c}}(0) = g(V_{\mathrm{ds}}=0) \tag{B.3.25}$$

where the following relation was used

$$\frac{\partial Q_{\mathrm{c}}}{\partial V_{\mathrm{G}}}+\frac{\partial Q_{\mathrm{c}}}{\partial V_{\mathrm{sub}}} = -\frac{\partial Q_{\mathrm{c}}}{\partial V_{\mathrm{c}}}Q_{\mathrm{c}} \overset{(B.3.15)}{=} \tag{B.3.26}$$
$$-\frac{\partial}{\partial V_{\mathrm{c}}}\left[C_{\mathrm{ox}}\Big(V_{\mathrm{G}}-V_{\mathrm{FB}}-V_{\mathrm{C}}+2\psi_{\mathrm{s}}+f\frac{Q_{\mathrm{sig}}}{WLC_{\mathrm{ox}}}\Big) - \sqrt{2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}(V_{\mathrm{sub}}-V_{\mathrm{c}}+2\psi_{\mathrm{s}})}\right]$$
$$\frac{\partial Q_{\mathrm{c}}}{\partial V_{\mathrm{G}}} = C_{\mathrm{ox}}$$
$$\frac{\partial Q_{\mathrm{c}}}{\partial V_{\mathrm{sub}}} = \frac{1}{2}\big(2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}(V_{\mathrm{sub}}-V_{\mathrm{c}}+2\psi_{\mathrm{s}})\big)^{-1/2}2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}} = \sqrt{\frac{eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}}{2(V_{\mathrm{sub}}-V_{\mathrm{c}}+2\psi_{\mathrm{s}})}}$$
$$\frac{\partial Q_{\mathrm{c}}}{\partial V_{\mathrm{c}}} = C_{\mathrm{ox}} + \frac{1}{2}2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}(V_{\mathrm{sub}}-V_{\mathrm{c}}+2\psi_{\mathrm{s}})^{-1/2}(-2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}) = C_{\mathrm{ox}} - \sqrt{\frac{eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}}{2(V_{\mathrm{sub}}-V_{\mathrm{c}}+2\psi_{\mathrm{s}})}} \tag{B.3.27}$$

B.3.1 Simplification

In this section, a simplification of the DEPFET's electric properties will be derived. The Source-Drain current is much more influenced by the Gate voltage compared to the Bulk voltage. In addition, the Bulk voltage can be seen approximately constant. Thus, the Drain current can be rewritten:

$$I_{\mathrm{ds}} = -\frac{W}{L}\mu_{\mathrm{h}}C_{\mathrm{ox}}\Bigg[\underbrace{\Big(V_{\mathrm{G}}\underbrace{-V_{\mathrm{FB}}-2\psi_{\mathrm{B}}-\frac{\sqrt{2eN_{\mathrm{D}}\varepsilon_0\varepsilon_{\mathrm{r}}}}{C_{\mathrm{ox}}}\sqrt{2\psi_{\mathrm{B}}-V_{\mathrm{sub}}}}_{V_{\mathrm{T}}}+f\frac{Q_{\mathrm{sig}}}{WLC_{\mathrm{ox}}}-\frac{V_{\mathrm{ds}}}{2}\Big)V_{\mathrm{ds}}}_{V_{\mathrm{g_{eff}}}=V_{\mathrm{G}}-V_{\mathrm{T}}}\Bigg]$$
$$I_{\mathrm{ds}} = -\frac{W}{L}\mu_{\mathrm{h}}C_{\mathrm{ox}}\left(V_{\mathrm{g_{eff}}}+f\frac{Q_{\mathrm{sig}}}{WLC_{\mathrm{ox}}}-\frac{V_{\mathrm{ds}}}{2}\right)V_{\mathrm{ds}} \tag{B.3.28}$$

The saturation voltage and current is calculated as:

$$\frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{ds}}} \overset{!}{=} 0 \quad\Leftrightarrow\quad V_{\mathrm{ds_{sat}}} = f\frac{Q_{\mathrm{sig}}}{WLC_{\mathrm{ox}}}+V_{\mathrm{g_{eff}}} \tag{B.3.29}$$
$$\Rightarrow I_{\mathrm{ds_{sat}}} = I_{\mathrm{ds}}(V_{\mathrm{ds_{sat}}}) = -\frac{W}{L}\mu_{\mathrm{h}}C_{\mathrm{ox}}\left(\underbrace{V_{\mathrm{g_{eff}}}+f\frac{Q_{\mathrm{sig}}}{WLC_{\mathrm{ox}}}}_{V_{\mathrm{ds_{sat}}}}-\frac{V_{\mathrm{ds_{sat}}}}{2}\right)V_{\mathrm{ds_{sat}}} \tag{B.3.30}$$
$$= -\frac{W}{L}\mu_{\mathrm{h}}C_{\mathrm{ox}}\frac{V_{\mathrm{ds_{sat}}}^2}{2} \tag{B.3.31}$$
$$= -\frac{W}{L}\mu_{\mathrm{h}}C_{\mathrm{ox}}\frac{1}{2}\left[f\frac{Q_{\mathrm{sig}}}{WLC_{\mathrm{ox}}}+V_{\mathrm{G}}-V_{\mathrm{T}}\right]^2 \tag{B.3.32}$$

$$\Rightarrow g_{\mathrm{m_{sat}}} = \frac{\partial I_{\mathrm{ds_{sat}}}}{\partial V_{\mathrm{G_{eff}}}} - \frac{W}{L}\mu_{\mathrm{h}} C_{\mathrm{ox}} V_{\mathrm{ds_{sat}}} = \sqrt{\frac{2W\mu_{\mathrm{h}} C_{\mathrm{ox}}}{L}}\sqrt{-I_{\mathrm{ds_{sat}}}} \tag{B.3.33}$$

$$\Rightarrow g_{\mathrm{q_{sat}}} = \frac{\partial I_{\mathrm{ds_{sat}}}}{\partial Q_{\mathrm{sig}}} = -\frac{W}{L}\mu_{\mathrm{h}} f \frac{1}{WL} V_{\mathrm{ds_{sat}}} = f\sqrt{\frac{2\mu_{\mathrm{h}}}{WL^3 C_{\mathrm{ox}}}}\sqrt{-I_{\mathrm{ds_{sat}}}} \tag{B.3.34}$$

This yields to the relation:

$$\frac{g_{\mathrm{q}}}{g_{\mathrm{m}}} = \frac{1}{LWC_{\mathrm{ox}}} f \tag{B.3.35}$$

B.4 Interaction between matter and photons

An infrared laser with a wavelength of 1060 nm shoots at the DEPFET matrix to create a signal for sensor studies and characterization. Furthermore, a radioactive γ source is used for the characterization of the modules. In this section, the interaction between photons and silicon is briefly presented.

The band gap of silicon (with an energy of $E_{\mathrm{g}} = 1.12\,\mathrm{eV}$) is indirect, i.e., the maximum energy level of the valence band and the minimum energy level of the conduction band do not have the same position in the momentum space (see Fig. B.1). For band gap transitions (of electrons and holes), the energy and the momentum are conserved. For silicon, a phonon[1] is required to conserve momentum. The energy for photons is large compared to the momentum. In contrast, the momentum of phonons is large compared to its energy.
Depending on the energy of the incident photon, different interaction effects can occur. Two direct light absorption processes are possible: The excitation of the lattice (without creating electron-hole pairs) and the photoelectric effect, which is discussed in the following.

Photoelectric effect Photons with an energy lower than the band gap ($E_\gamma < E_{\mathrm{g}}$) mostly traverse the silicon without being absorbed, i.e., the silicon seems to be transparent. However, there are two exceptions resulting in photon absorption. The two photons process (explained below) and impurities within the silicon bulk, which lower the band gap. There are three possibilities for optical excitation of an electron from the valence band to the conduction band (see Fig. B.1).

1. An incident photon of energy

$$E_\gamma = E_{\mathrm{g}} \pm E_{\mathrm{ph}} \tag{B.4.1}$$

   excites an electron from the valence band to the conduction band using a phonon, which supplies the missing momentum. The phonon can either be absorbed ($E_\gamma = E_{\mathrm{g}} + E_{\mathrm{ph}}$, purple transition in Fig. B.1) or emitted ($E_\gamma = E_{\mathrm{g}} - E_{\mathrm{ph}}$, blue transition in Fig. B.1).
2. The absorbed photon has an energy, which is much larger than the band gap ($E_\gamma \gg E_{\mathrm{g}}$). The electron from the valence band is excited into the

[1] A phonon is a quasi-particle describing lattice vibrations.

conduction band with the same momentum. It releases its kinetic energy by *thermalization*, i.e., scattering with the lattice and transferring momentum to phonons (orange transition in Fig. B.1).

When electrons are excited to the conduction band, they leave holes in the valence band. This basically describes the process of the electron-hole pair creation. The mean energy to create an electron-hole pair in silicon is $\langle E_{eh} \rangle = 3.64\,\text{eV}$ [215]. This corresponds to a vertical excitation of the electron from the valence band to the conduction band, where $E_\gamma > E_\text{g}$ (orange transition in Fig. B.1).

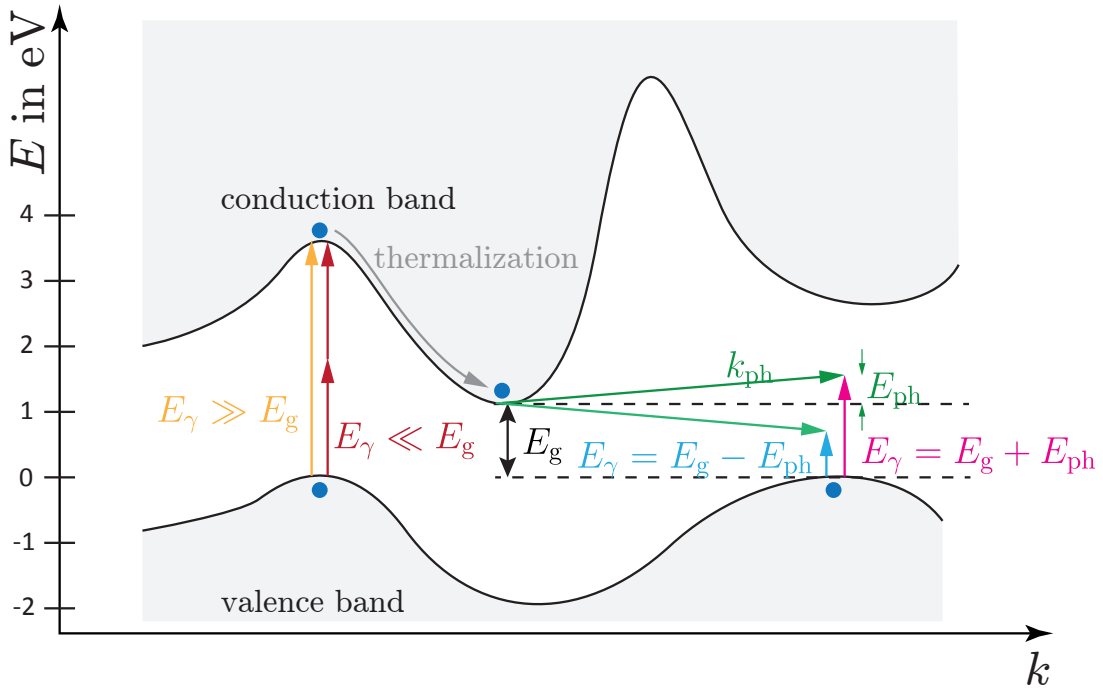


Figure B.1: Energetic band structure of silicon as function of the electron wave vector k. It has an indirect band gap (of energy E_g), i.e., the maximum of the valence band and the minimum of the conduction band are located at different momenta k.
Left transition (orange): An incident photon lifts the electron directly to the conduction band (without change of the momentum). The momentum is transferred to phonons (by lattice excitation), called thermalization. (red): Two photons are absorbed simultaneously. One creates an intermediate state (between valence and conduction band) and the other one lifts it to the conduction band.
Right transition: A photon of energy $E_\text{g} \pm E_\text{ph}$ and a phonon are required to "lift" an electron from the valence to the conduction band.

The absorption coefficient α describes the reduction of the incident flux when photons traverse matter. It strongly depends on the wavelength λ of the incident photons. The absorption depth (penetration depth) $\delta(\lambda)$ is defined as the depth at which the flux is reduced to $1/e$ (corresponding to approximately 37 %, where e denotes the Euler's number). It is given by the inverse of the absorption coefficient $\delta(\lambda) = \frac{1}{\alpha(\lambda)}$. Figure B.2 shows both coefficients as function of the wavelength of

Table B.1: Absorption coefficients, penetration depths and reduced flux (after passing 75 µm silicon) for different wavelengths.

wavelength	abs. coef. α	pen. depth (δ)	transmission $I(y = 75\,\mu\text{m})$
680 nm	$2.2 \cdot 10^{-1}\ \frac{1}{\mu\text{m}}$	4.55 µm	$6.83 \cdot 10^{-6}$ %
1060 nm	$1.1 \cdot 10^{-3}\ \frac{1}{\mu\text{m}}$	900.90 µm	92.01 %

the incident photon. The transmission, i.e., the remaining flux after passing the silicon of thickness d, depending on the incident flux I_0, is given by Beer–Lambert's law:

$$I(d) = I_0 \exp\big(-\alpha(\lambda)d\big) \tag{B.4.2}$$

For the PXD with a thickness of 75 µm, the reduction of the incident flux, the penetration depth and the absorption coefficient for different wavelengths (680 nm red light and 1060 nm infrared light) are summarized in Tab. B.1. The majority of the photons ($\lambda = 680$ nm) are absorbed within 5 µm below the surface.

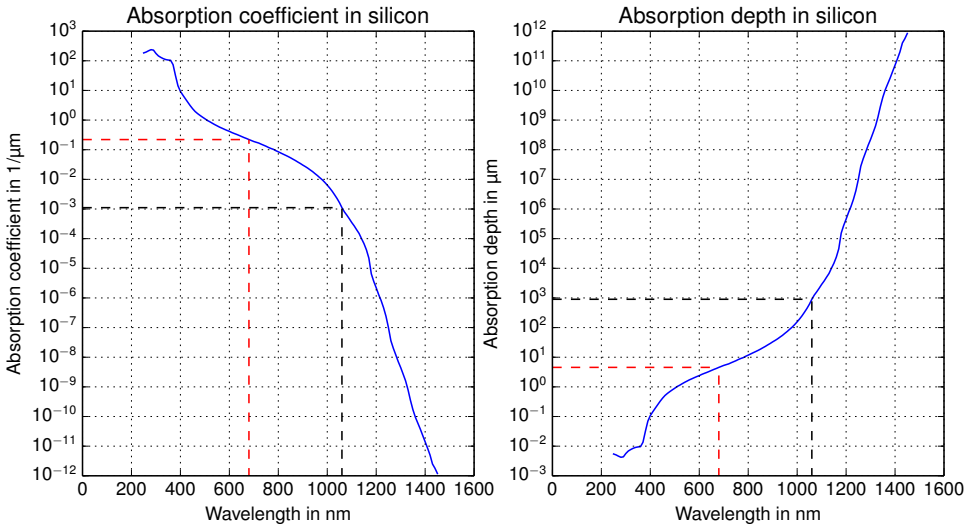


Figure B.2: Absorption coefficient and absorption length as function of the wavelength of the incident light [216]. The red line marks 680 nm (red light) and the black one is at 1060 nm (infrared light).

However, not every incident photon on the DEPFET is absorbed and does not contribute to the overall signal. The probability η that an incident photon generates an electron-hole pair, which adds to the signal, is called *quantum efficiency*, given as [217]:

$$\eta = (1 - R)\xi\Big(1 - \exp\big(-\alpha(\lambda)d\big)\Big) \tag{B.4.3}$$

where R is the reflection at the surface, ξ is the number of separated electron-hole pairs[2], and $1 - \exp\big(-\alpha(\lambda)d\big)$ is the fraction of the total incident absorbed flux.

Effects other than the photoelectric effect also contribute to the entire attenuation. The different effects are plotted for silicon as function of energy in Fig. B.3.

- **Rayleigh scattering:** The photon scatters at the bound electrons of the atom. The atom is neither excited nor ionized. This effect can occur for photons of any energy.
- **Compton scattering:** An incident photon of energy E_γ scatters with a free or weakly bound electron, i.e., $E_\gamma \gg E_{\text{binding}}$. The photon is deflected and has less energy $E'_\gamma < E_\gamma$. A free electron is created if the transferred energy of the photon exceeds the binding energy. The scattered electron has a kinetic energy of $E_{\text{kin}} = (E_\gamma - E'_\gamma) - E_{\text{binding}}$. Compton scattering can occur multiple times subsequently. The contribution of Compton scattering for low energetic particle is negligible. It becomes the dominant effect for photons in silicon around 60 keV.
- **Pair creation:** Photons with an energy beyond 1022 MeV can create electron-positron pairs. In the case a photon of energy, E_γ, creates a pair in the detector, the electron and positron share the excess energy as kinetic energy, i.e., $E_{\text{kin}} = E_\gamma - 1022\,\text{MeV}$. The particles can create additional electron-hole pairs by scattering. This effect does not occur in the lab because no high energetic γ source is available.

Laser in the lab For the lab measurements, the laser can only shoot the DEPFETs from the top side. Since the mounting and cooling jigs are below the sensitive region the laser cannot hit the detector from the back side. On the top side of the module there are the polysilicon structures and the metal routings (see Fig. 4.13). The laser cannot penetrate them. Therefore, it is extremely difficult to shoot the laser on a gap of silicon between the structures from the top side and hit a single pixel (of $70 \times 50\,\mu\text{m}^2$). An infrared laser of (1060 nm) is selected since the infrared light creates electron-hole pairs not only at the surface but in the entire silicon bulk (75 µm) of the DEPFET. A picture of the setup with a laser shooting on the module is shown in Fig. 6.3.

Cadmium source in the lab Radioactive source measurements are performed with a cadmium 109 isotope. A cadmium source is used since the energy of created electrons corresponds approximately to a MIP, introduced in app. B.5. The source is encapsulated in a Beryllium jacket coated with silver, which only emits photons. The emitted photons from the cadmium source create roughly 6300 electron-hole pairs in silicon.

[2] A fraction of the created electron-hole pairs recombine.

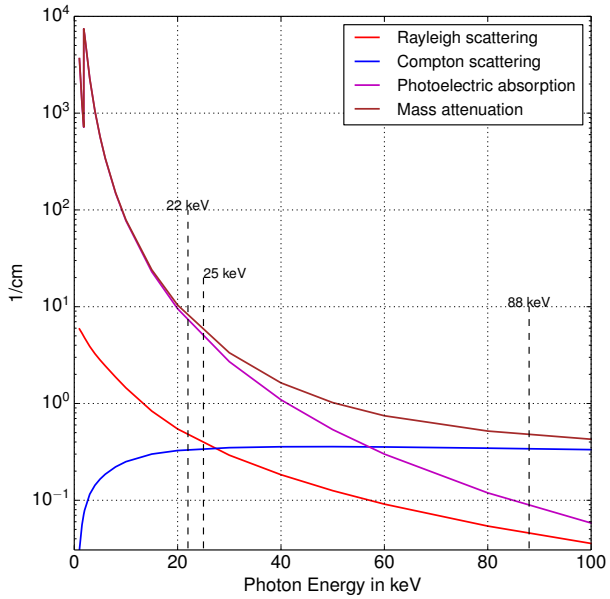


Figure B.3: Mass attenuation/energy-absorption coefficients of the different effects of interaction between photons and silicon as function of the photon energy [218]. The mass attenuation corresponds to the sum of all effects (except the coherent scattering). The dashed lines correspond to the emission spectrum of a cadmium 109 radioactive source.

B.5 Interaction between charged particles and silicon

Charged particles traversing silicon detectors interact with the atoms and create electron-hole pairs. This section will describe briefly the interaction between charged particles and silicon, mainly based on [32]. Incident charged particles, traversing matter either excite or ionize the atoms. In particular in thin absorbers, the energy loss is rather small. The mean value of the loss in energy has a large variance [32, 219]. The interaction between charged particles and matter can be further separated.

Electrons and Positrons

The fractional energy loss of electrons and positrons for lead is shown in Fig. B.4. For low energies Bhabha and Møller scattering occurs, while ionization is the dominating contribution. For higher energies bremsstrahlung contributes most to the energy loss. For the beam test, the dominating effect is bremsstrahlung, since the energies are in the GeV range (up to 6 GeV at DESY). The characteristic material property is the *radiation length* X_0. It describes the distance, which an electron (positron) must traverse in matter to lose all but $1/e$ of its energy, where e denotes the Euler's number. For silicon it is 9.36 cm. The overall material budget of a PXD layer (including thick rim, ASICs, passive components) corresponds to approximately 0.2 % of X_0.

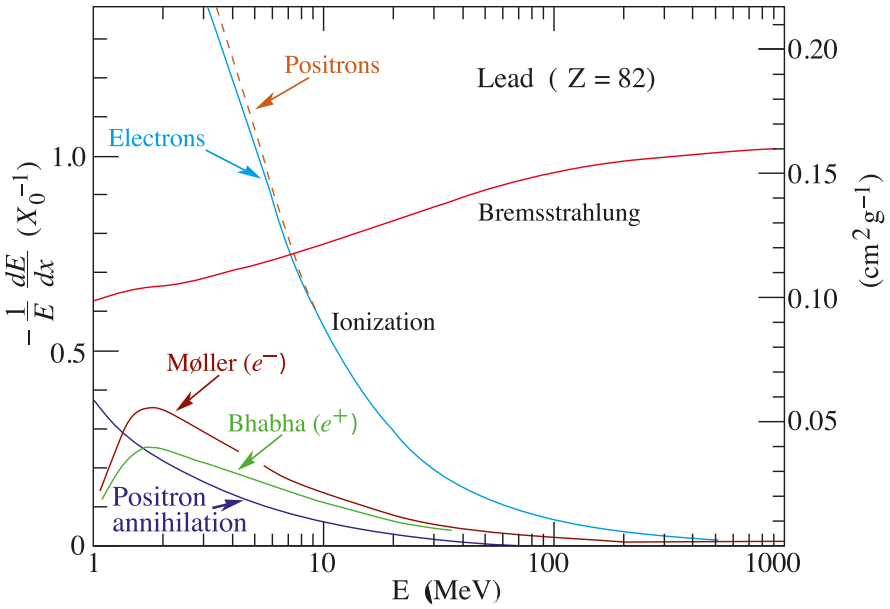


Figure B.4: Fractional energy loss for traversing particles in lead, depending on its energy [32].

Other Charged Particles

The average stopping power, i.e., the energy loss of the traversing charged particle through the absorber can be calculated by the Bethe-Bloch formula. The unit is given in MeV $\mathrm{g}^{-1}\,\mathrm{cm}^2$.

$$\left\langle -\frac{dE}{dx} \right\rangle = K z^2 \frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\frac{2m_{e^-}c^2\beta^2\gamma^2 W_{\max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right] \tag{B.5.1}$$

The variables are defined as following:

Symbol	Definition	Units or value
K	$4\pi N_\mathrm{A} r_{e^-}^2 m_{e^-}c^2/A$	$0.307\,075\,\mathrm{MeV mol}^{-1}\mathrm{cm}^2$
z	charge number of incident particle	
Z	atomic number of absorber	
A	atomic mass of absorber	
β	$\frac{v}{c}$	
$m_{e^-}c^2$	electron mass $\times c^2$	0.511 MeV
c	speed of light	299,792,458 m/s
γ	$(\sqrt{1-\beta^2})^{-1/2}$ Lorentz factor	
$W_{\max}$	max. energy transfer in a single collision	
I	mean excitation energy	MeV
$\delta(\beta\gamma)$	density effect correction	

The stopping power in copper as function of the muon momentum is shown in Fig. B.5. The minimum stopping power is given at $\sim 3\beta\gamma$ (minimum ionization), which is independent from the type of the incident particle. The average stopping power decreases with the inverse square of the incident particle's velocity. For higher momenta, it increases logarithmically until the radiative processes occur.

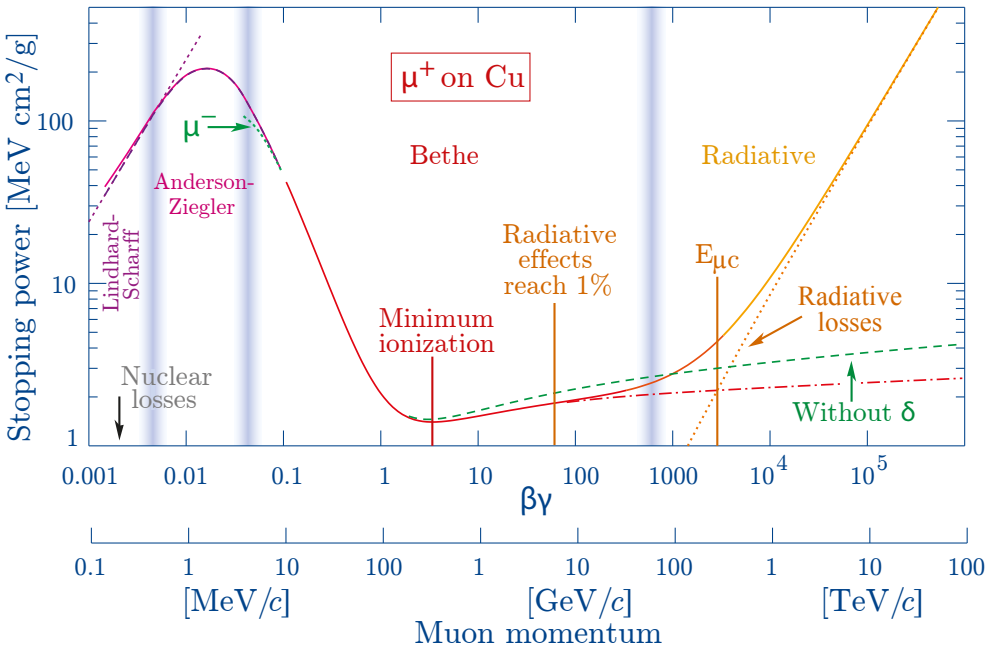


Figure B.5: Stopping power in copper as function of the muon momentum [32].

Minimum Ionizing particle

For a momentum of approximately 3–4 $\beta\gamma$, the incident particle transfers the minimum amount of its kinetic energy. A particle of that momentum is called *minimum ionizing particle (MIP)*. For silicon, this corresponds to the minimum amount of created electron-hole pairs. Thus, a MIP creates the smallest possible signal, which is a convenient benchmark for the characterization of a particle detector. A theoretical approximate value for the MPV (in units of eV) is given as [220]:

$$\text{MPV} = d\,(100.6 + 35.35 \ln d) \tag{B.5.2}$$

$$\overset{d=75}{=} 75\,(100.6 + 35.35 \ln(75))\ \text{eV} = 18992\,\text{eV} \tag{B.5.3}$$

Assuming $\langle E_{eh} \rangle = 3.6\,\text{eV}$ to create an electron-hole pair, approximately 5275 electron-hole pairs are created in the sensitive silicon volume of one PXD sensor, corresponding to $70\,\frac{e^-}{\mu\text{m}}$. According to the particle data group the MPV of created electron-hole pairs for 80 µm thick silicon is [32]:

$$\#e^- = \frac{\left\langle \frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle}{\langle E_{eh} \rangle}\, d = \frac{0.6 \cdot 388\,\frac{\text{eV}}{\mu\text{m}}}{3.6\,\text{eV}}\, 75\,\mu\text{m} = 4850, \tag{B.5.4}$$

where $\langle E_{eh} \rangle$ is the energy to create an electron-hole pair and d is the thickness of the sensitive DEPFET bulk. This corresponds to approximately $65\,\frac{e^-}{\mu\text{m}}$.

Appendix C

Hardware and Measurements

C.1 Clocks

The PXD and the DAQ uses a variety of different clock rates. This section should give an overview about the clocks for the PXD starting from the SuperKEKB accelerator, illustrated in Fig. C.1.

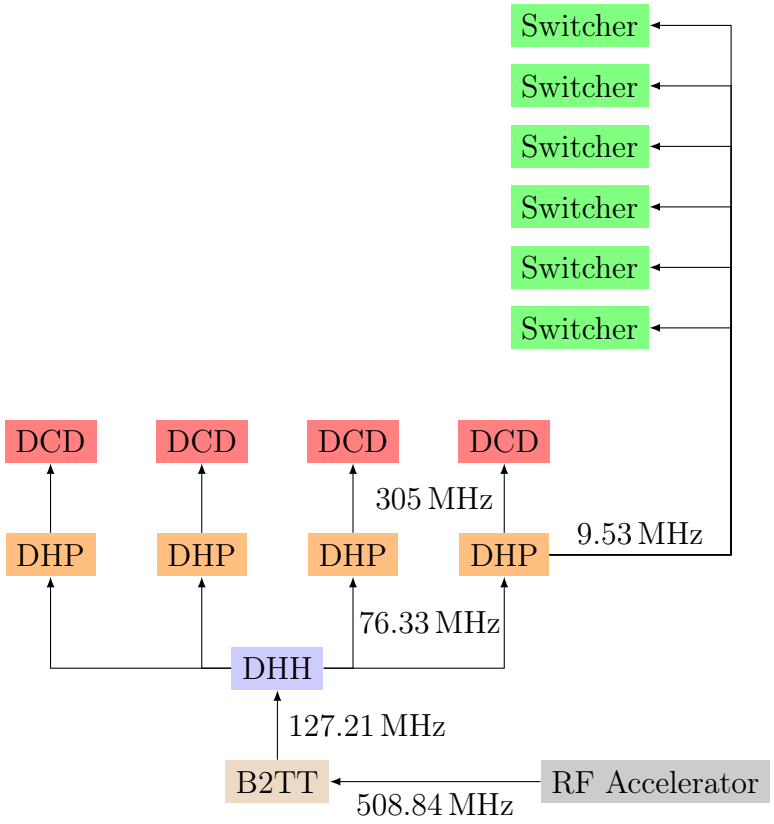


Figure C.1: Sketch of the clocks from the accelerator to the ASICs via B2TT and the DHH.

The system-wide clock of 127.21 MHz (broadcast by the B2TT) is generated from the RF clock of the accelerator, which is 508.84 MHz and is synchronized to the beam-revolution cycle of 10 µs [164, 221]. The DHH lowers the clock by a factor of 3/5 to 76.326 MHz.
The DHH sends the GCK that is provided in parallel to the four DHPs. A phase-locked loop (PLL) integrated in each DHP multiplies the clock frequency by a

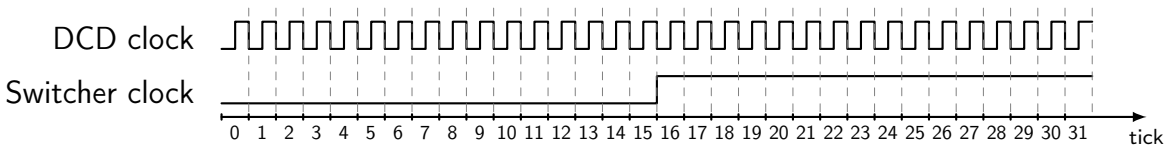


Figure C.2: The DCD clock is 32 times faster than the Switcher clock. The Switcher outputs are controlled by 32 ticks, which have the same frequency as the DCD clock (3.27 ns for GCK=76.33 MHz. The output sequence can be programmed by the operator.

Table C.1: Different GCK clocks and their corresponding DCD and Switcher clocks. The row time (readout time of one row_{gate}) and readout time of a full frame are given.

DHE clock	DCD clock	Switcher clock	row time	readout time (frame)
62.50 MHz	250 MHz	7.81 MHz	128 ns	24.58 µs
65.00 MHz	260 MHz	8.13 MHz	123 ns	23.63 µs
67.84 MHz	271 MHz	8.48 MHz	118 ns	22.64 µs
71.20 MHz	285 MHz	8.90 MHz	112 ns	21.57 µs
76.33 MHz	305 MHz	9.53 MHz	105 ns	20.14 µs

factor of four. Hence, a 305 MHz clock is generated. This clock is used for the DCD and for the Switcher sequence. The Switcher sequence consists of 32 ticks (see Sect. 4.8.1), which control a single DEPFET row (Gate and Clear output drivers of the Switcher). Each tick is applied for 3.28 ns = 1/305 MHz. The Switcher clock is applied once within those 32 ticks, resulting in a Switcher clock of $\frac{305\,\text{MHz}}{32} = 9.53\,\text{MHz}$ (see Fig. C.2).
For lab measurements different GCKs can be generated by the DHE directly. The resulting clock rates for the DCD, for the Switcher and the corresponding readout times are listed in Tab. C.1.

C.2 Important DHP settings

In this section the most important settings for the DHP is briefly described, based on [197, 222, 223].

- **frame_sync_proc_dly**: This setting allows to shift the memory pointer of the DHP in clock cycles of the GCK (13.11 ns, at GCK=76.33 MHz), i.e., at which memory address the DCD data is written into the internal memory of the DHP. As explained in Sect. 4.8.6 the DCD needs 191 clock cycles to send the first data after releasing the `SyncReset` signal (from 1 to 0). Measurements for different settings of `frame_sync_proc_dly` are presented in Sect. 6.3.3. Recommended settings for different GCKs are:

GCK	`frame_sync_proc_dly`
62.5 MHz	65
76.33 MHz	57

- **offset_frame_sync_dly**: The offset values $(0, 1, 2, 3)$ for all pixels are stored in the internal memory of the DHP. As explained in detail in Sect. 4.8.8, the DCD requires 22 clock cycles after releasing the `SyncReset` signal in order to apply the received offset values. Taking this (and the delay of 191 clock cycles to send data from the DCD to the DHP) into account, a delay setting needs to be adjusted for sending the offset values at the correct timing. The `offset_frame_sync_dly` allows to shift the memory pointer for the stored offset values in clock cycles of the global reference clock. For GCK=62.5 MHz the `offset_frame_sync_dly` should be set to 1536. Measurements are shown in Sect. 6.9.1.

- **dcd_clk_sdly** (global delay): This setting allows to add a delay to the DCD clock. which corresponds to a global delay of the transmitted data, sent from the DCD and received by the DHP.

- **dcd_rx_sdly_*i*** (local delay DEPFET data $i = 0, 1, \ldots, 64$): There are 64 settings in order to set the delay for each of the 64 transfer lines between DCD and DHP. The delay shifts the sampling point of the digital waveform, sent from the DCD and received by the DHP as shown in Fig. 4.35. Measurements are presented in Sect. 5.4 and Sect. 6.3.3.

- **offset_dcd_dly_*i*** (local delay offsets): The offset data for the pedestal compression (see Sect. 4.8.7) is sent by the DHP and received by the DCD. To sample the digital waveform reliable (by the DCD), the DHP allows to adjust sending the data as a function of time. This can be set for each of the 16 transfer line individually. Measurements are presented in Sect. 6.9.1.

- **idac_cml_tx_bias** (`bias`): This setting allows the adjustment of the amplitude of the signal, which is transmitted from the DHP to the DHE. The parameter is shown in Fig. 4.29.

- **idac_cml_tx_biasd** (`biasd`): This setting allows the adjustment of the amplitude of the pre-emphasis of the signal, which is transmitted from the DHP to the DHE. The parameter is shown in Fig. 4.29.

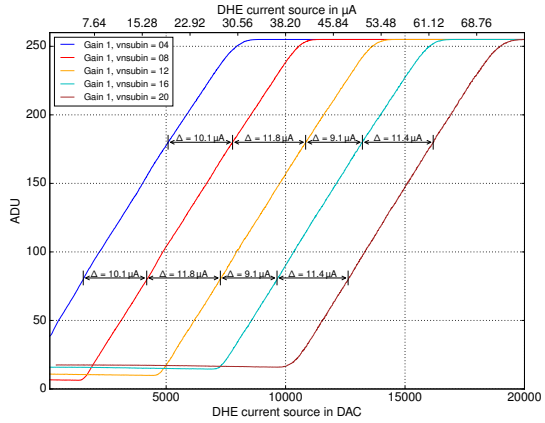
- **pll_cml_dly_sel** (`dly`): This setting allows the adjustment of the width of the pre-emphasis of the signal, which is transmitted from the DHP to the DHE. The parameter is shown in Fig. 4.29.

C.3 ADC Transfer Curve

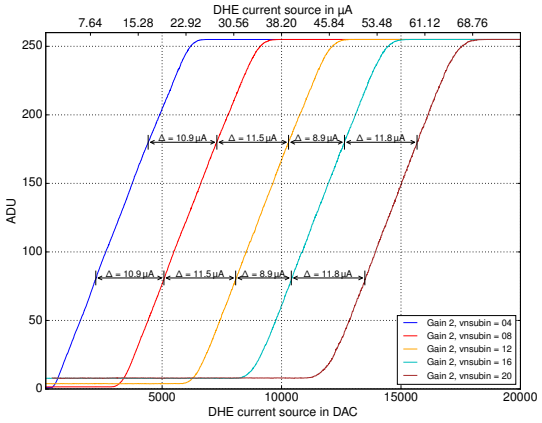
This section explains the characterizations of the DCDs of W30-OB1 in more details compared to Sect. 6.4.
The `VnSubin` setting changes the amount of current, which is subtracted from the input node of the trans-impedance amplifier (see Fig. 4.23). Thus, by increasing the `VnSubin` settings more input current is subtracted. As a result, more current is required to record the characteristic ADC transfer curves (see Fig. C.3).
For DCD 1 the transfer curves for all four gains are plotted using different settings of `VnSubin`. The dynamic ranges and the slopes are calculated for each individual curve. The procedure is repeated for every single DCD and listed in Tab. C.2. The mean value for each gain and each DCD is calculated.
In addition to this, the current, which is subtracted by one DAC setting of `VnSubin`, is roughly estimated by comparing the transfer curves for the same gain but different `VnSubin` settings. The difference in current for the same ADU value is calculated (see Fig. C.3). However, due to the large inhomogeneity in the current spread the calculated value can be seen only as a rough benchmark. The curves for all four DCDs with the same gain (gain 1) and different settings for `VnSubin` are plotted in Fig. C.4.

Table C.2: Gains in nA/ADU for all four DCDs. Different `VnSubin` (vs) settings are applied and the resulting gain is averaged. The calibration was performed for all four possible gains.

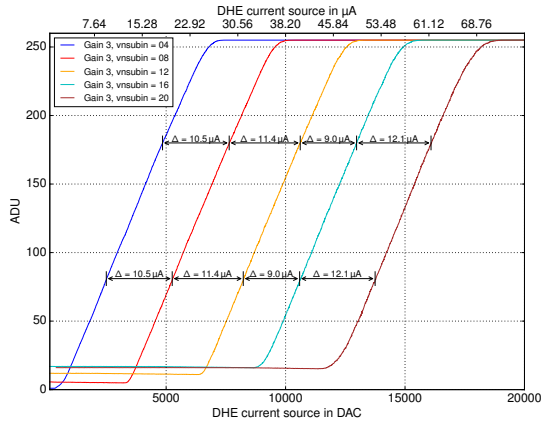
		vs=4	vs=8	vs=12	vs=16	vs=20	Mean
DCD 1	Gain 1	139.4	138.9	138.6	138.2	137.0	138.4 ± 0.8
	Gain 2	85.1	85.7	85.6	85.5	84.5	85.3 ± 0.4
	Gain $\tilde{2}$	91.2	92.4	92.1	91.3	91.3	91.7 ± 0.5
	Gain 4	56.6	57.7	57.1	56.7	58.1	57.2 ± 0.6
DCD 2	Gain 1	136.2	129.7	130.7	130.7	127.7	131.0 ± 2.8
	Gain 2	84.0	80.1	81.0	80.5	79.4	81.0 ± 1.6
	Gain $\tilde{2}$	92.3	86.6	87.1	89.3	85.1	88.1 ± 2.5
	Gain 4	58.5	54.1	54.2	55.0	57.4	55.8 ± 1.8
DCD 3	Gain 1	136.0	136.2	136.0	134.6	134.1	135.4 ± 0.9
	Gain 2	85.0	84.3	84.1	83.5	83.4	84.1 ± 0.6
	Gain $\tilde{2}$	89.7	90.5	90.1	89.6	89.5	89.9 ± 0.4
	Gain 4	55.7	56.0	56.2	56.6	56.2	56.1 ± 0.3
DCD 4	Gain 1	141.0	140.4	140.4	139.8	137.9	139.9 ± 1.1
	Gain 2	86.2	86.5	86.6	86.6	85.4	86.3 ± 0.5
	Gain $\tilde{2}$	91.3	93.9	93.4	91.5	91.7	92.4 ± 1.1
	Gain 4	56.3	58.0	57.8	57.1	57.4	57.3 ± 0.6



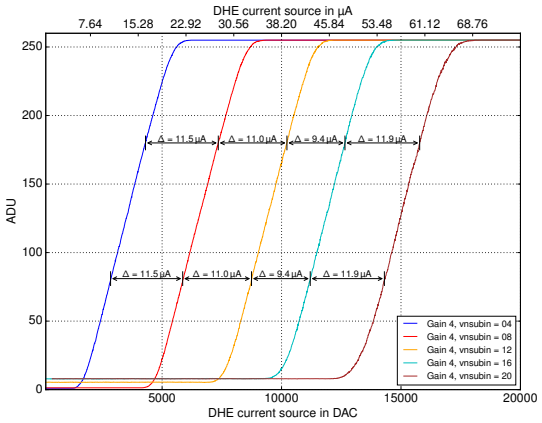
(a) DCD 1: ADC transfer curves with different `VnSubin` settings and gain 1.



(b) DCD 1: ADC transfer curves with different `VnSubin` settings and gain 2.

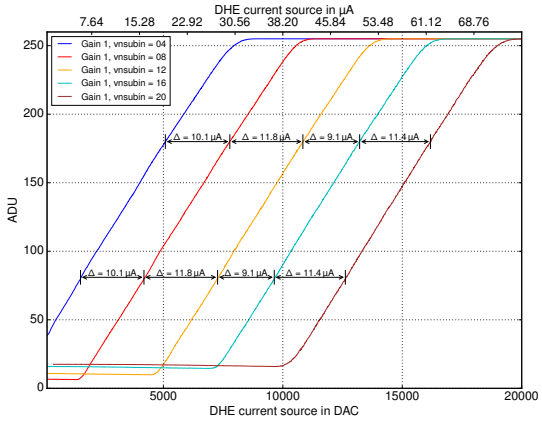


(c) DCD 1: ADC transfer curves with different `VnSubin` settings and gain $\tilde{2}$ (3).

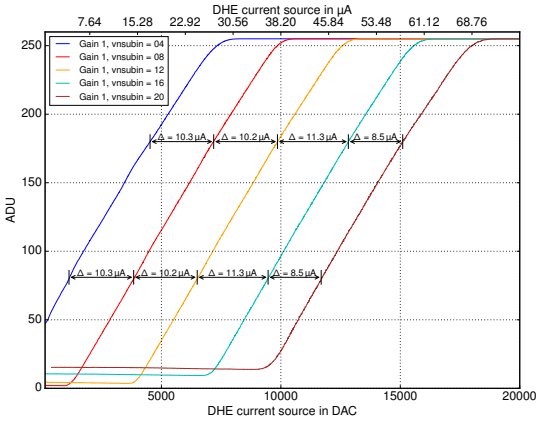


(d) DCD 1: ADC transfer curves with different `VnSubin` settings and gain 4.

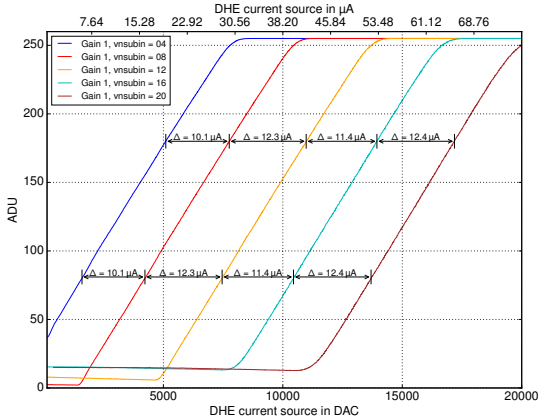
Figure C.3: DCD transfer curves of DCD 1 for different `VnSubin` settings and different gains.



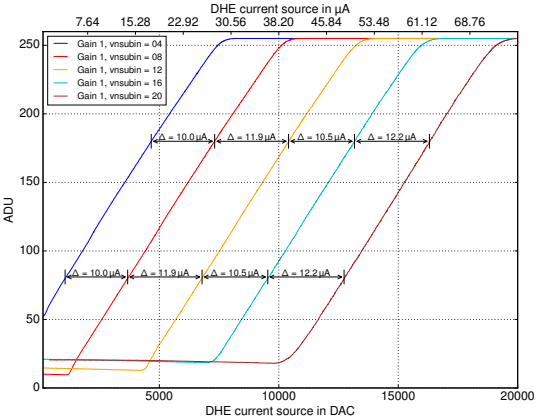
(a) DCD 1: ADC transfer curves with different `VnSubin` settings and gain 1.



(b) DCD 2: ADC transfer curves with different `VnSubin` settings and gain 1.



(c) DCD 3: ADC transfer curves with different `VnSubin` settings and gain 1.



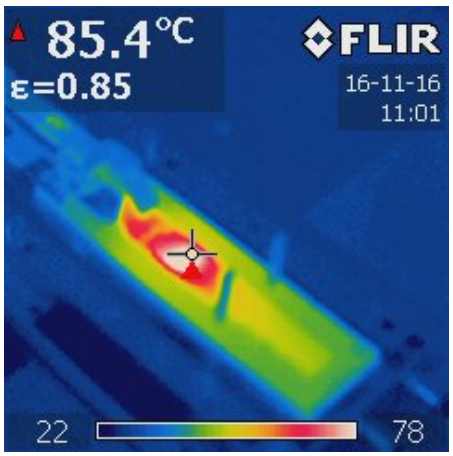
(d) DCD 4: ADC transfer curves with different `VnSubin` settings and gain 1.

Figure C.4: DCD transfer curves of DCD $1, 2, 3, 4$ for different `VnSubin` settings.

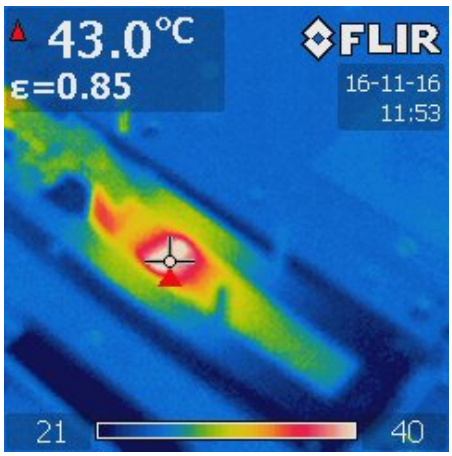
C.4 Cooling Issues

The four DCDs and the four DHPs have a total power of approximately 8 W (see Sect. 4.12). The ASICs are cooled to ensure proper operation. In the lab setup, the module is mounted on a base jig. This jig is mounted on a cooling block. Tap water ($\sim 16^\circ$ C) circulates through the cooling block. An additional vacuum connection could suck the module to the base jig.
An aluminum jig "guides" the Kapton cable to the module (see Fig. 6.3). It is soldered to the module resulting in a stiff mechanical connection. For this reason, the module is tilted (in vertical and horizontal direction) resulting in a small gap between the base jig and the silicon substrate. This gap disappears when the vacuum presses the module to the jig.

To study the thermal behavior a thermal camera is used. Figure C.5a shows the module without a vacuum connection. The temperature of the DCDs is approximately 85° C. Once the vacuum is enabled, the module is sucked to the base jig. The temperature of the DCDs decreases to roughly 43° C as shown in Fig. C.5b. The increased temperature ($\sim 85^\circ$ C) of the DCDs causes transmission errors between the DCDs and the DHPs. In addition, the pedestal values are shifted. This behavior disappears when the module is cooled properly.



(a) The module is put on the base jig without vacuum connection.



(b) Vacuum sucks the module onto the base jig.

Figure C.5: Temperature of the module for disabled and enabled vacuum connection. The highest temperature have the DCDs

C.5 Clear Behavior

In contrast to Sect. 6.10, the analog common mode correction and the offsets are not used for the Clear efficiency measurements in this section. The Clear efficiency is studied for the same pixel as in Sect. 6.10, i.e., $\text{row}_{\text{geo}} = 74$, $\text{col}_{\text{geo}} = 215$. The same sequence, as shown in Fig. 6.42 and explained in Sect. 6.10 is used.

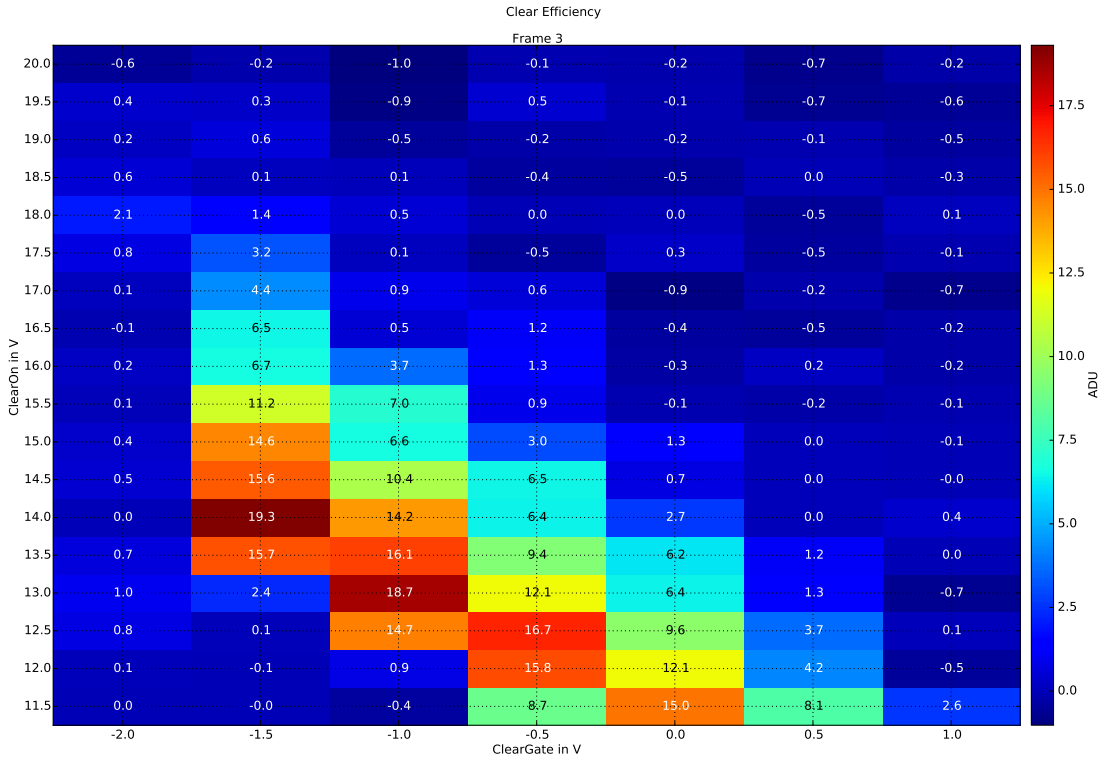


Figure C.6: Pixel: row_{geo}=74, col_{geo}=215. Signal of pixels after having cleared once, corresponding to frame 2.

The charge (in units of ADU) remaining in the *internal Gate* after applying the Clear pulse once (as function of the ClearGate and ClearOn voltages) is shown in Fig. C.6. The remaining charge after having applied the Clear pulse twice is shown in Fig. C.7.

For negative ClearGate=−2 V the potential barrier between the *internal Gate* and the *Clear region* is large. Consequently, the electrons can overcome this barrier during the Clear process only partially and the *internal Gate* is not emptied completely. Furthermore, the negative ClearGate voltages let the polysilicon structure of the *ClearGate* act like an additional transistor, i.e., *Source–ClearGate–Drain*[1]. As a result, the pedestal values are above the upper boundary of the dynamic DCD range for any ClearOn voltage. For this reason, the signal in frame 3 and frame 4 does not vary compared to the pedestals. Therefore, the measurements of the signal charge cannot be performed. The uncertainty of 0 ± 2 ADU is due to small variations in the saturation region of the ADCs in the DCD. Using the analog common mode correction (ACMC) the pedestals are lowered and shifted into the dynamic range, since more current is subtracted at the input node. However, without the ACMC the dynamic range can be shifted by setting `VnSubin` appropriately. The dynamic range of the DCD is not large enough to cover all signals for different ClearGate voltages.

[1]The Source current also increased from $\sim 100\,\mu$A to $\sim 140\,\mu$A pro DEPFET pixel.

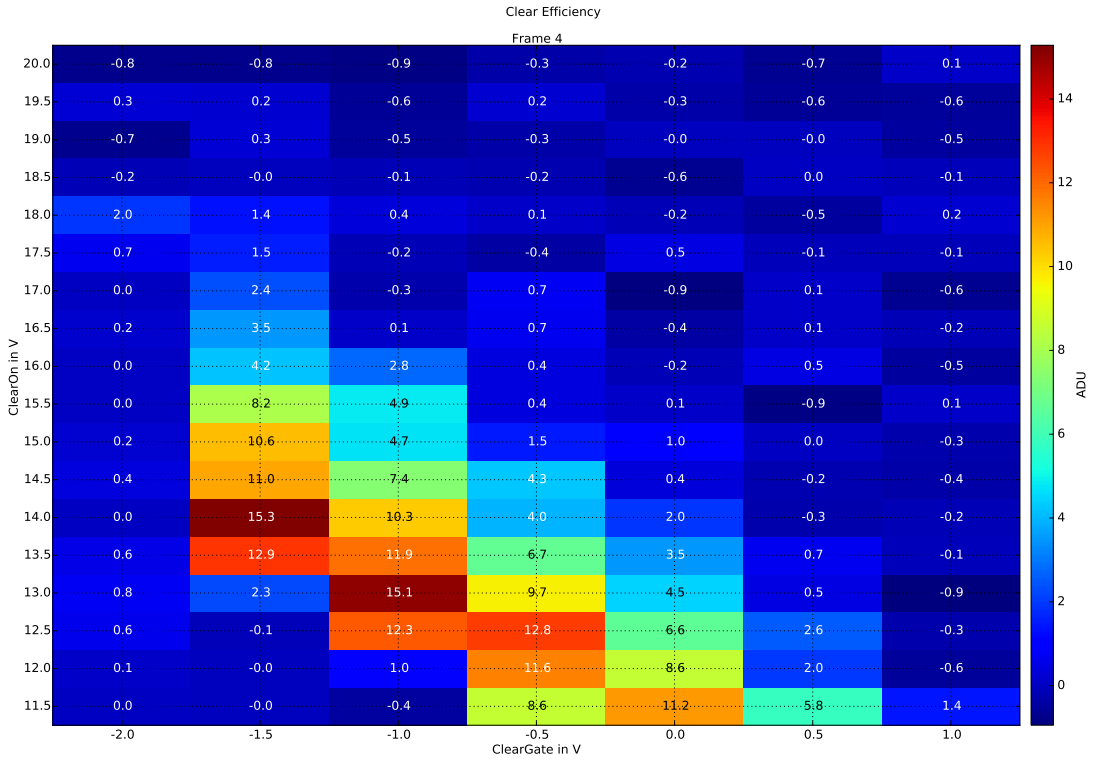


Figure C.7: Pixel: row_{geo}=74, col_{geo}=215. Signal of pixels after having cleared twice, corresponding to frame 3.

For (ClearGate= −1.5 V, ClearOn< 13 V) and (ClearGate= −1 V, ClearOn< 12 V) the same behavior is visible, i.e., the pedestals are too high. No variations in terms of signal between the frames are observed.

For (ClearGate=−1.5 V, ClearOn=13 V), (ClearGate=−1.5 V, ClearOn=13.5 V), (ClearGate=−1.0 V, ClearOn=12.5 V) (ClearGate=−0.5 V, ClearOn=11.5 V) the pedestal values lower. However, the signal in frame 3 still reaches the upper boundary of the dynamic range of the DCD. The pedestals are only approximately 8 − 15 ADU below the upper boundary of the dynamic range. Therefore, the remaining charge (> 15 ADU), measured in frame 3, corresponds only to a small fraction of the real charge, which is still accumulated in the *internal Gate*.

Increasing the ClearOn voltage, the pedestals lower (since electrons can drift easier to the *Clear region*). The remaining charge after applying the Clear pulse (in frame 3) can be measured quantitatively. The measurements, which represent the Clear behavior are for ClearGate voltages above −1.5 V and above the line between the values (ClearGate=−1.5 V, ClearOn=14 V) and (ClearGate=0 V, ClearOn=11.5 V).

The operating voltages, which ensure a proper Clear behavior, are above ClearGate of −2.0 V and above the line between the points (ClearGate=−1.5 V, ClearOn=18.5 V) and (ClearGate=1 V, ClearOn=12 V) for this region. The measurements are consistent with the Clear behavior using the analog common mode correction in

Sect. 6.10.

Figure C.7 shows that approximately one fourth of the remaining charge (of frame 3) is removed by applying the Clear pulse twice. However, for the Belle II experiment, the entire charge must be removed after having applied the Clear pulse once.

C.6 Inhomogeneity of the DCD current sink

The inhomogeneity of the 2-bit offset compensation for the pedestal compression is studied. An EMCM is more suited for this study since one can decouple the effects from the DEPFET matrix and the DCD (no matrix is connected to any input channel of the DCD 1–DCD 3[2]). Moreover, current cannot flow out of the DCD along the Drain lines to the DEPFETs.

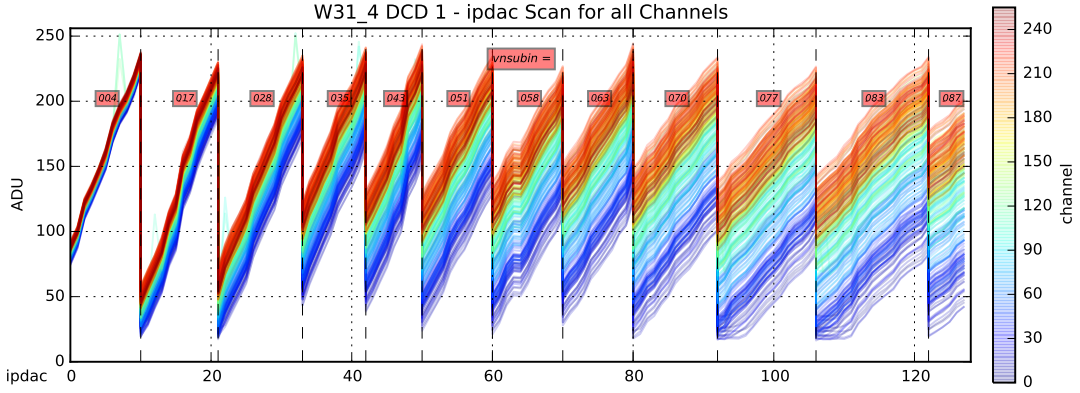


Figure C.8: DCD 1: Current signal as function of `IPDAC` for different `VnSubin`.

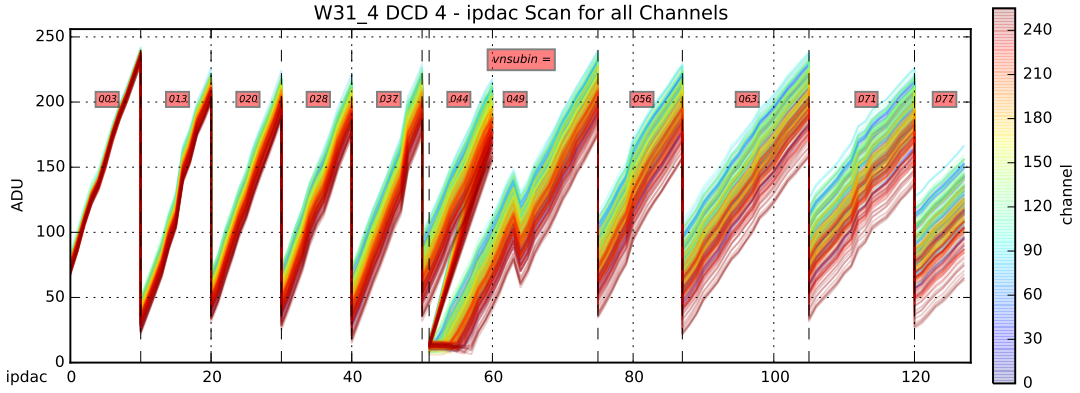


Figure C.9: DCD 4: current signal as function of `IPDAC` for different `VnSubin`.

The measurement is performed in the following procedure.
Offsets of value 3 are uploaded into the DHP offset memory. Consequently, the

[2]A small matrix is even not assembled on the EMCM W31-4.

current $3 \times I_{\text{DAC–glo}}$ is added to the input current of the DCD. The $I_{\text{DAC–glo}}$ current value is increased successively by varying the DCD setting `IPDAC` (see [153] for the naming scheme of the settings). When the upper boundary of the dynamic range is almost reached (around 230 ADU), more current is subtracted by the current sink `VnSubin`. This results in a shift of the signals to the direction of the lower boundary of the dynamic range. This procedure is repeated until the `IPDAC` setting has reached its maximum value of 127. The signals as function of `IPDAC` are shown for DCD 1 and DCD 4 in Fig. C.8 and Fig. C.9. The spread of the input current increases with increasing values for `IPDAC`. In addition, the pinmap of the DCDs, i.e., the measured signals by the DCD arranged in the ASIC footprint, for different `IPDAC` values are plotted in Fig. C.10 and Fig. C.11.

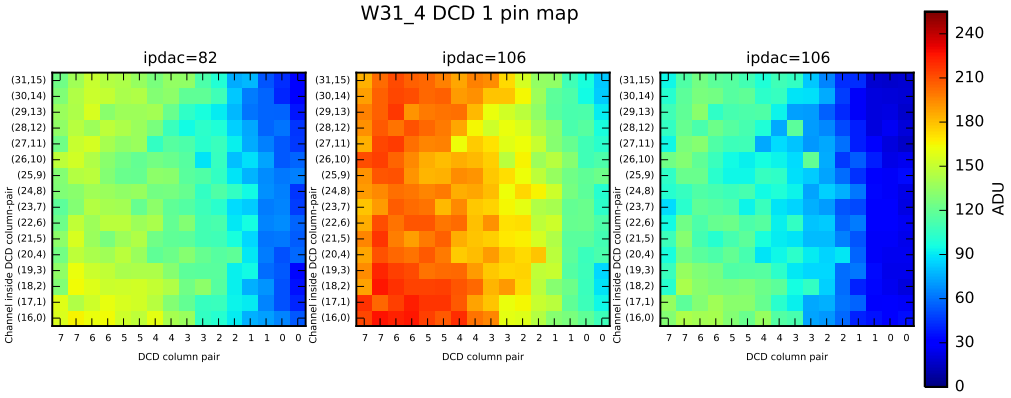


Figure C.10: DCD 1: Pinmap of DCD signals for `IPDAC`=82, 106. For `IPDAC`=106 two different `VnSubin` values are set.

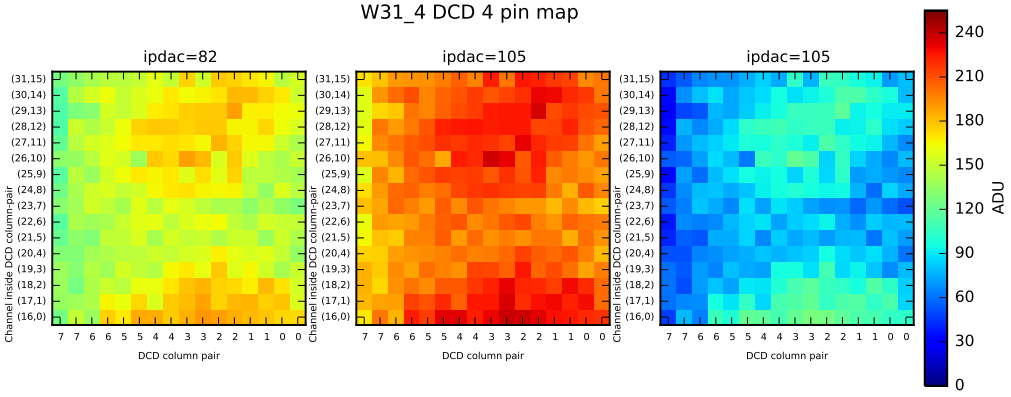


Figure C.11: DCD 4: Pinmap of DCD signals for `IPDAC`=82, 105. For `IPDAC`=105 two different `VnSubin` values are set.

Since the current source $I_{\text{DAC–glo}}$ exceeds the dynamic input range of the DCD at any gain, the resulting current for large $I_{\text{DAC–glo}}$ must be shifted into the dynamic range. This is done by subtracting a certain amount of the current by setting an appropriate value for `VnSubin`.

The spread in DCD 1 is from left to right along the ASIC in contrast to DCD 4. For the latter one the spread is from top to bottom. This is due to cooling issues and a voltage drop across the module which should be fixed by the new version of the DCD, DCDB4.2. In contrast to the pilot run modules, the EMCM cannot be sucked by a vacuum connection to the cooling jig. The same behavior has been observed on various EMCMs.

C.7 Radioactive Source Scans of W30-OB1

The parameters and results of GateOn voltage scan (see Sect. 6.11) and the measured distributions (see Fig. C.12) are listed in Tab. C.3.

Table C.3: Parameters and results of the GateOn scan (see Fig. C.12 and Fig. 6.46). The mean value and the standard deviation of the Gaussian fit are abbreviated by μ and σ. SNR is the signal-to-noise ratio and g_q is the internal amplification. A peak could not be detected for DCD 3 and DCD 4 for GateOn of $-0.5\,\mathrm{V}$ due to missing statistics.

	GateOn voltage	-2.50 V	-2.00 V	-1.50 V	-1.00 V	-0.50 V
DCD 1	μ [ADU]	21.89	21.23	18.74	15.93	11.98
	σ [ADU]	2.96	2.37	2.08	1.95	1.51
	SNR	43.01	41.31	35.91	30.50	23.93
	g_q [pA/e^-]	481	467	412	350	263
DCD 2	μ [ADU]	23.59	22.07	18.58	15.78	11.31
	σ [ADU]	2.64	2.46	2.36	2.24	1.78
	SNR	43.24	40.62	33.85	28.43	20.30
	g_q [pA/e^-]	491	459	387	328	235
DCD 3	μ [ADU]	20.96	18.77	15.78	13.11	N/A
	σ [ADU]	2.60	2.40	2.10	1.96	
	SNR	37.77	34.07	28.25	23.46	
	g_q [pA/e^-]	451	404	339	282	
DCD 4	μ [ADU]	19.71	17.21	14.26	11.45	N/A
	σ [ADU]	2.45	2.24	1.94	1.79	
	SNR	37.03	32.41	26.57	21.42	
	g_q [pA/e^-]	438	382	317	254	

Table C.4 lists the parameters of the ClearOff voltage scan shown in Fig. 6.48. Table C.5 summarizes the parameters and results of the Drift voltage scan shown in Fig. 6.50.

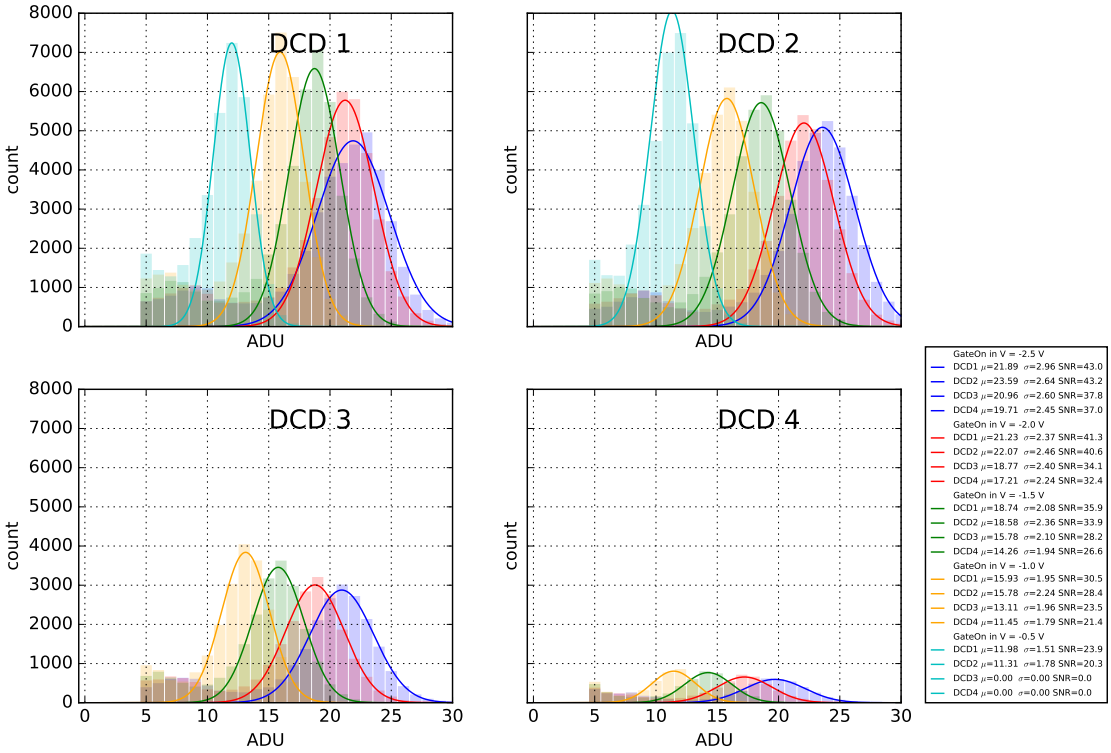


Figure C.12: The signal distribution as function of the GateOn voltage of the four DCDs. DCD 4 has a lot of transmission errors resulting in low statistics. The source is centered between DCD 1 and DCD 2. The parameters are summarized in Tab. C.3.

Table C.4: Parameters of the ClearOff voltage scan. The distributions are plotted in Fig. 6.48. μ and σ are the mean value and the standard deviation of the Gaussian fit. SNR is the signal-to-noise ratio and g_q the internal amplification of the DEPFET matrix.

	ClearOff voltage	1.00 V	1.50 V	2.00 V	2.50 V	3.00 V	3.50 V	4.00 V	4.50 V	5.00 V	5.50 V
DCD 1	μ [ADU]	19.84	20.19	20.19	20.20	20.07	19.93	19.73	19.66	19.49	19.23
	σ [ADU]	3.04	2.98	2.94	2.90	2.92	2.96	2.97	3.12	3.10	3.12
	SNR	35.68	36.40	36.53	36.54	36.06	36.06	35.83	35.58	35.46	34.89
	g_q [pA/e]	436	444	444	444	441	438	434	432	428	423
DCD 2	μ [ADU]	24.66	25.25	25.16	25.16	25.10	24.82	24.72	24.72	24.46	24.31
	σ [ADU]	2.67	2.48	2.43	2.45	2.46	2.47	2.57	2.65	2.68	2.70
	SNR	44.56	46.02	45.84	45.88	45.90	45.27	45.23	45.26	44.82	44.65
	g_q [pA/e]	513	525	523	523	522	516	514	514	509	506
DCD 3	μ [ADU]	24.84	25.06	24.91	24.91	24.82	24.70	24.44	24.52	24.37	24.30
	σ [ADU]	2.32	2.22	2.20	2.19	2.24	2.24	2.32	2.25	2.26	2.25
	SNR	45.82	46.55	46.35	46.45	46.13	46.01	45.46	45.83	45.56	45.06
	g_q [pA/e]	534	539	536	536	534	531	525	527	524	522
DCD 4	μ [ADU]	20.80	21.03	20.94	20.99	20.90	20.70	20.70	20.69	20.59	20.43
	σ [ADU]	2.58	2.58	2.48	2.49	2.55	2.50	2.43	2.47	2.48	2.42
	SNR	38.70	39.38	39.27	39.31	38.99	38.86	38.88	38.92	38.87	38.47
	g_q [pA/e]	462	467	465	466	464	460	460	460	458	454

Table C.5: Parameters of the Drift voltage scan. The distributions are plotted in Fig. 6.50. μ and σ are the mean value and the standard deviation of the Gaussian fit. SNR is the signal-to-noise ratio and g_q the internal amplification of the DEPFET matrix.

	Drift voltage	-7.00 V	-6.50 V	-6.00 V	-5.50 V	-5.00 V	-4.50 V	-4.00 V	-3.50 V	-3.00 V
DCD 1	μ [ADU]	19.62	19.04	19.54	19.47	19.42	19.38	19.27	19.09	18.74
	σ [ADU]	2.91	2.97	2.93	3.04	3.12	3.25	3.16	3.13	3.35
	SNR	35.71	34.18	35.51	35.27	35.35	35.24	35.02	34.63	34.20
	g_q [pA/e]	431	419	430	428	427	426	424	420	412
DCD 2	μ [ADU]	24.53	23.86	24.35	24.43	24.43	24.40	24.40	24.24	23.83
	σ [ADU]	2.47	2.55	2.50	2.55	2.66	2.59	2.59	2.73	2.95
	SNR	44.90	43.35	44.74	44.81	44.83	44.77	44.72	44.52	43.84
	g_q [pA/e]	510	496	507	508	508	508	508	504	496
DCD 3	μ [ADU]	24.42	23.64	23.93	24.26	24.39	24.36	24.14	24.03	23.78
	σ [ADU]	2.23	2.31	2.28	2.30	2.29	2.22	2.28	2.41	2.64
	SNR	45.62	43.61	44.62	45.19	45.35	45.44	45.16	44.84	44.40
	g_q [pA/e]	525	508	514	522	524	524	519	517	511
DCD 4	μ [ADU]	20.48	19.89	20.49	20.48	20.45	20.52	20.29	20.19	19.73
	σ [ADU]	2.39	2.51	2.41	2.43	2.43	2.45	2.47	2.47	2.89
	SNR	38.74	37.26	38.53	38.50	38.43	38.66	38.10	38.11	37.19
	g_q [pA/e]	455	442	455	455	454	456	451	449	438

C.8 Gated Mode - Signal Charge Preservation

The frames 0–2 from the sequence introduced in Sect. 6.12.10 are shown and explained.

Frame 0 – Fig. C.13

In the area marked by the black dashes, for ClearOn voltages of 14–18 V some electrons (up to 49 % of the created electron-hole pairs by a laser pulse) remain in the *internal Gate* although the Clear pulse was applied multiple times (> 1000). The real pedestal values (i.e., for an empty *internal Gate*) are visible for more positive ClearOn voltages (18–20 V) marked by the purple dotted line, which are approximately 88–90 ADU.

The more negative the ClearGate voltage the larger the potential barrier is between the *internal Gate* and the *Clear region* (see Sect. 4.4.2). The remaining electrons in the *internal Gate* (after applying the Clear pulses multiple times) correspond to the difference of the shown signal and the real pedestal value (e.g., for ClearGate=−1.5 V, ClearOn=14 V the value is 50 ADU, which roughly corresponds to 13,000 electrons).

Furthermore, these results prove that the GateOn voltage (of −2.5 V) is reached (independent from the GateOff voltage) at the *external Gate* contacts of the DEPFET. In contrast, if the GateOn voltage was not reached, i.e., GateOn>−2.5 V (for instance due to the large parasitic Gate capacitances), the signals would diminish (since the Drain current and thus the signal depends quadratically on the GateOn voltage).

Frame 1-0 – Fig. C.14

Figure C.14 shows the laser signal (with subtracted pedestal values, i.e., frame 1-frame 0). The amount of charge created by the laser pulse is the same for all voltage combinations. The detected signal in Fig. C.14 varies due to the different pedestal values. For ClearOn voltages (14–18 V) electrons remain in the *internal Gate* after applying the Clear pulse marked by the blue and black regions. For the black marked region, the pedestal value and the created signal by the laser reach the upper limit of the dynamic range of the DCD[3]. Thus, the detected signal (frame 1-frame 0) is lowered. In contrast to this behavior, the signals for ClearGate=0 V with pedestals between 88–110 ADU show the same laser signal for all GateOff and ClearOn voltage combinations (area marked by the red dotted line). All electrons from the *internal Gate*, which have been created by this laser signal are removed. Furthermore, for the brown area, at a ClearGate voltage of −1.5, −2 V the signal is larger compared to more positive voltages. In this case the polysilicon structure acts as an additional transistor (*Source - ClearGate - Drain*). The Source current is increased by roughly 40 % from 100 µA to 140 µA. The optimal voltage combinations are marked by the rosa area.

Frame 2-0 – Fig. C.15

Figure C.15 shows frame 2 (with subtracted pedestal values, i.e., frame 2-frame 0). This corresponds to the Clear efficiency of a single Clear cycle. The signal is measured after having applied the Clear pulse once. The remaining charge, stored in

[3] At the upper boudary the DCD shows a non-linear behavior. This was shown in Sect. 6.4.

the *internal Gate*, is shown. The black area in Fig. C.15 corresponds for voltage combinations with a Clear efficiency less than 100 %. For some voltage combinations, marked by the green area, all electrons from the laser pulse created in frame 1 can be removed within a single Clear cycle. However, for the region marked by the red dotted line, multiple Clear cycles are required to remove all electrons from the *internal Gate*; however, one Clear cycle is not sufficient. The purple area marks the voltage combinations for which a Clear efficiency with 100 % is reached.

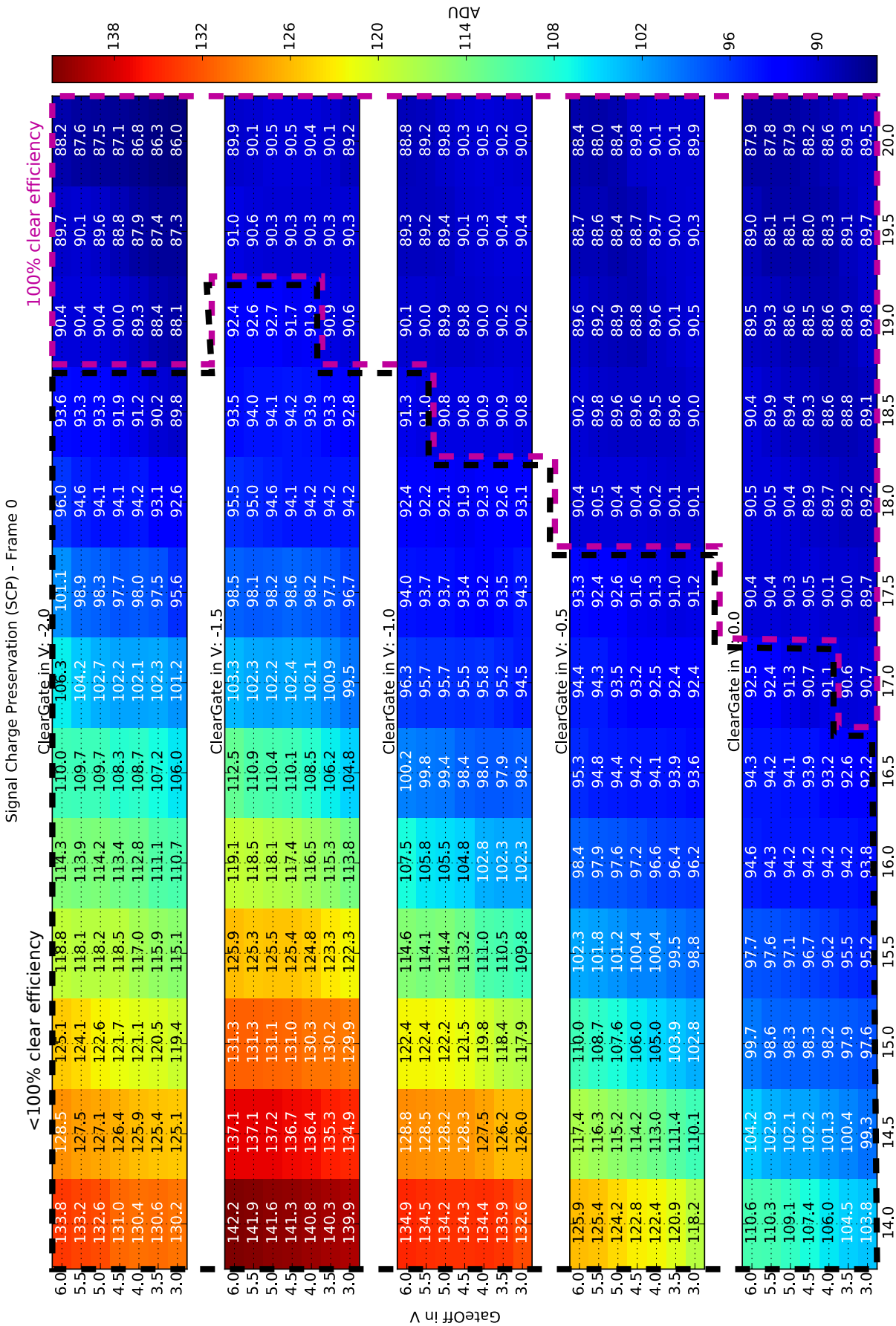


Figure C.13: Pedestals, i.e., frame 0, of the SCP sweep for different voltage combinations.

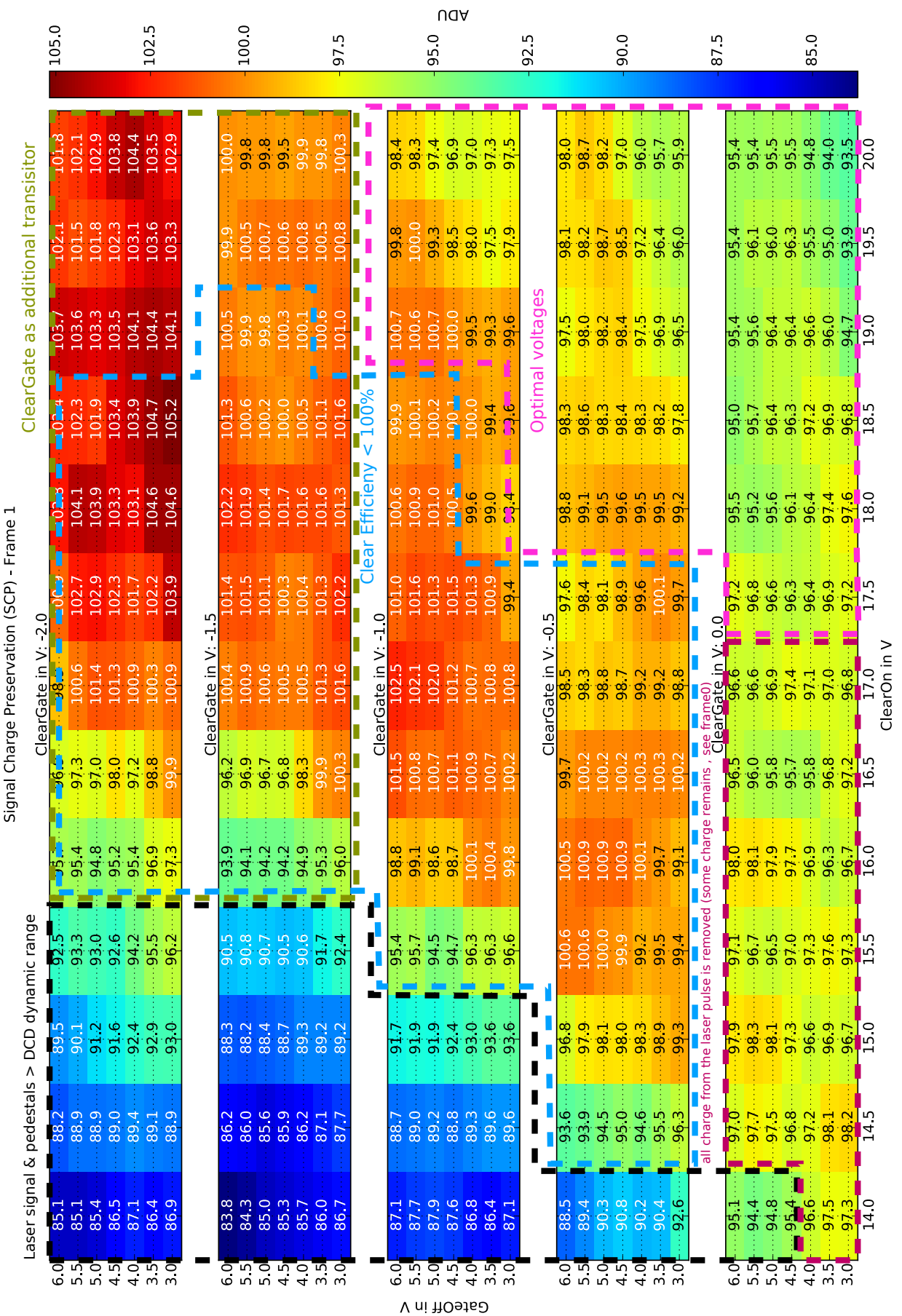


Figure C.14: Laser signal (with subtracted pedestal) for different voltage combinations (frame 1-frame 0).

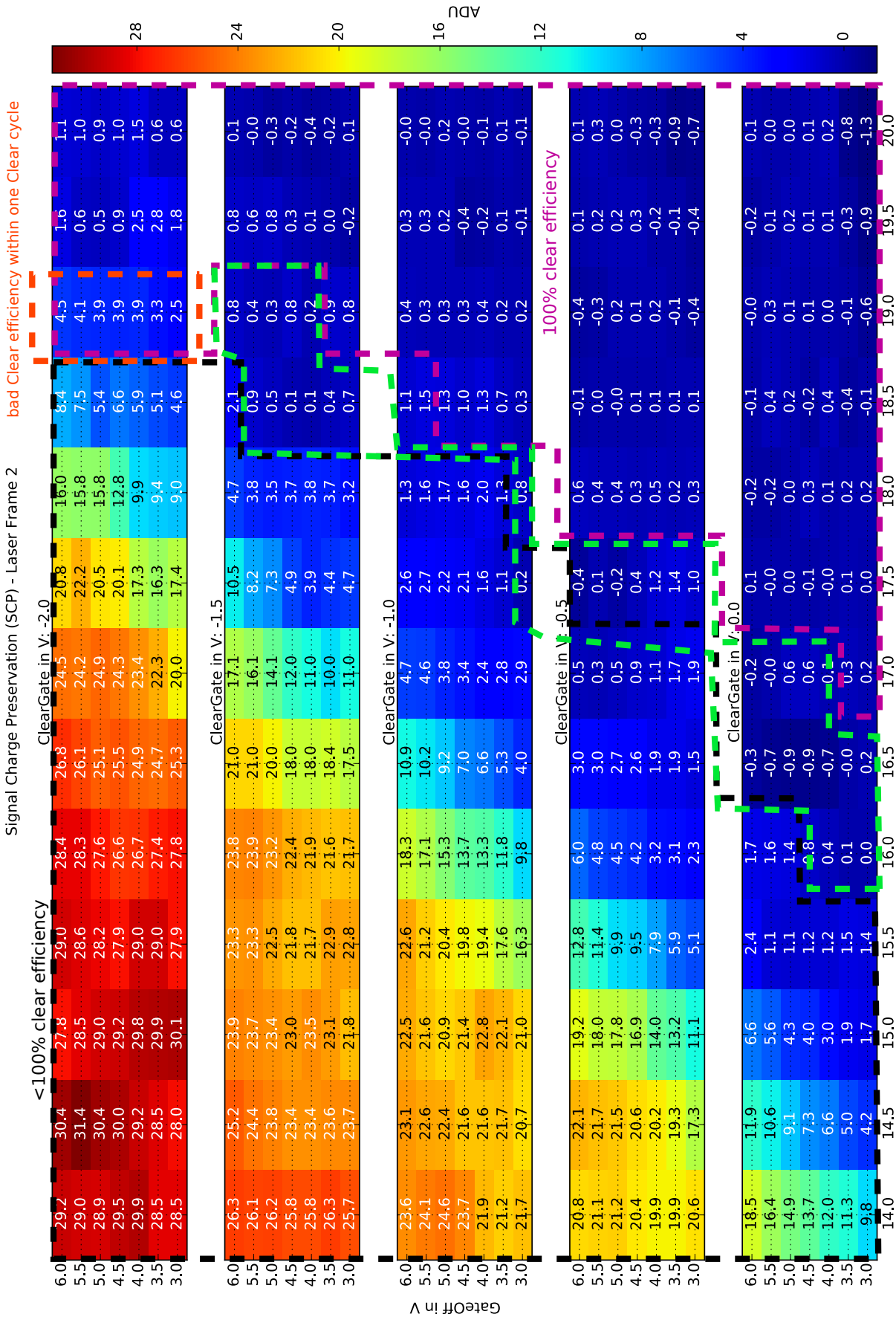
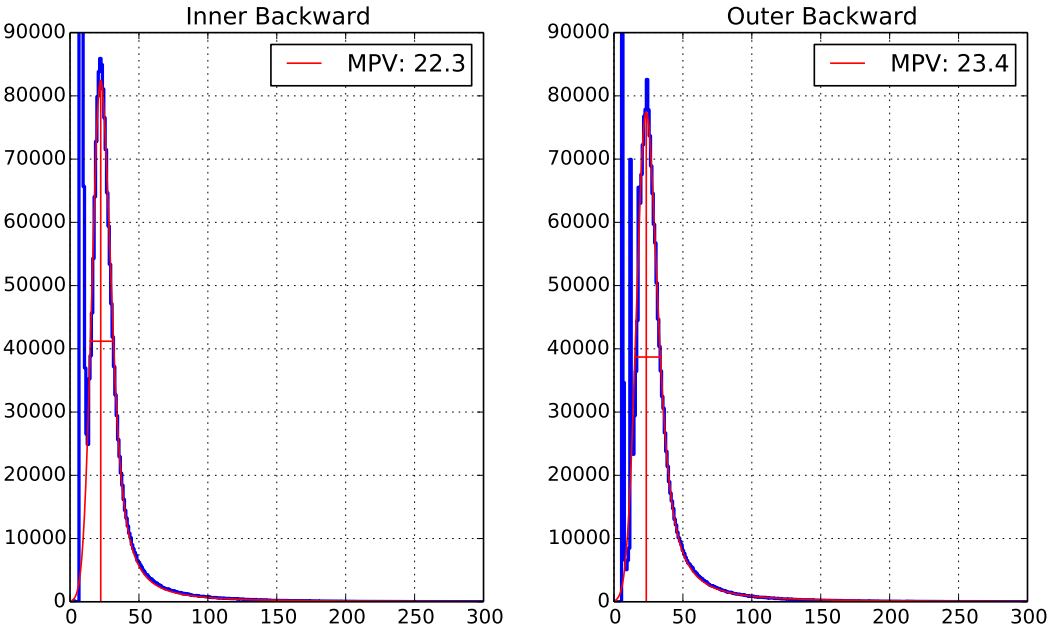


Figure C.15: Signal after having applied the Clear mechanism once for different voltage combinations (frame 2-frame 0).

C.9 Beam Test Results

The cluster charge distribution is calculated with the lab framework. The amount of data that is written to disk by the BonnDAQ is much more compared to the events, which are written to disk by the scaled-down Belle II DAQ. This is due to missing data reduction (HLT, DATCON, ONSEN). The results for the entire sensors OB and IB, i.e., all 24 regions combined (six Switchers and four DCDs), are shown in Fig. C.16. The MPVs for for the 24 areas (six Switcher and four DCDs) of each module are shown in Fig. C.17. The charge distributions are the corresponding fits for the IB and OB modules, for the 24 areas are shown in Figs. C.18 to C.21.



(a) Inner backward. (b) Outer backward.

Figure C.16: Cluster charges of the inner backward and outer backward modules. A convolution between a Landau and a Gaussian distribution is used as fit function.

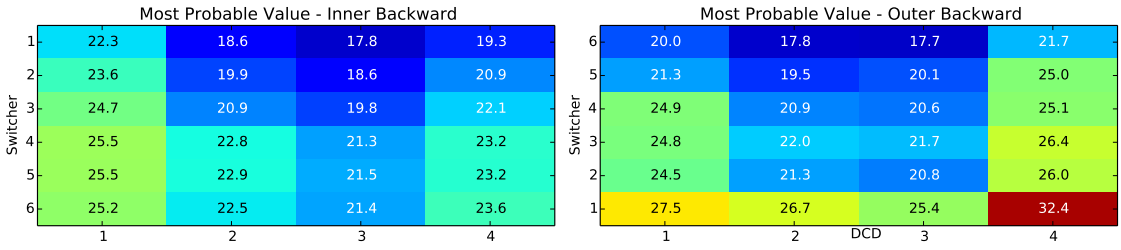


Figure C.17: Most probable values for the Switcher and DCD regions using the lab framework.

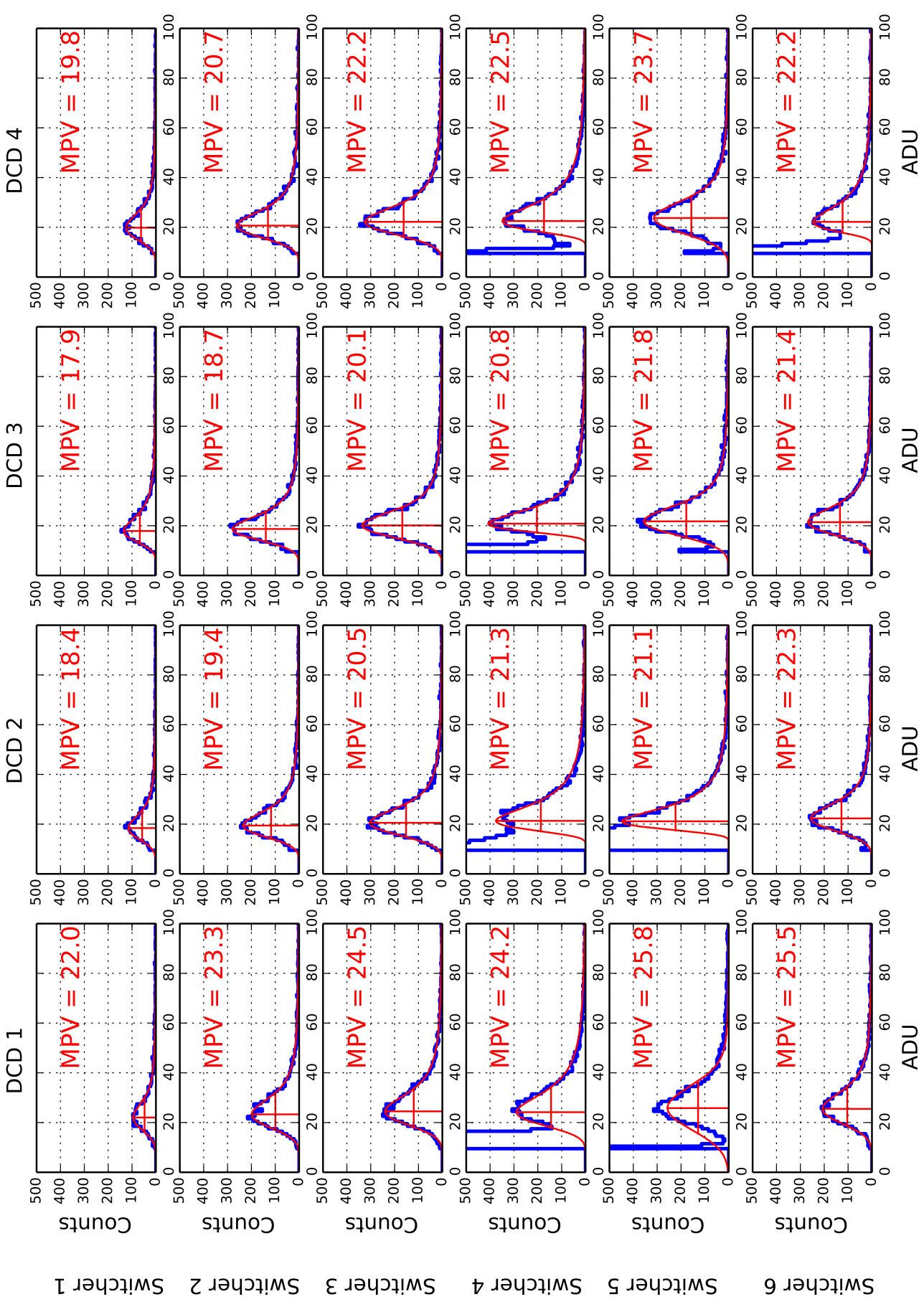


Figure C.18: BASF2, inner backward: Charge distribution, split into 24 regions. Each is controlled and is read out by a different combination of Switcher and DCD.

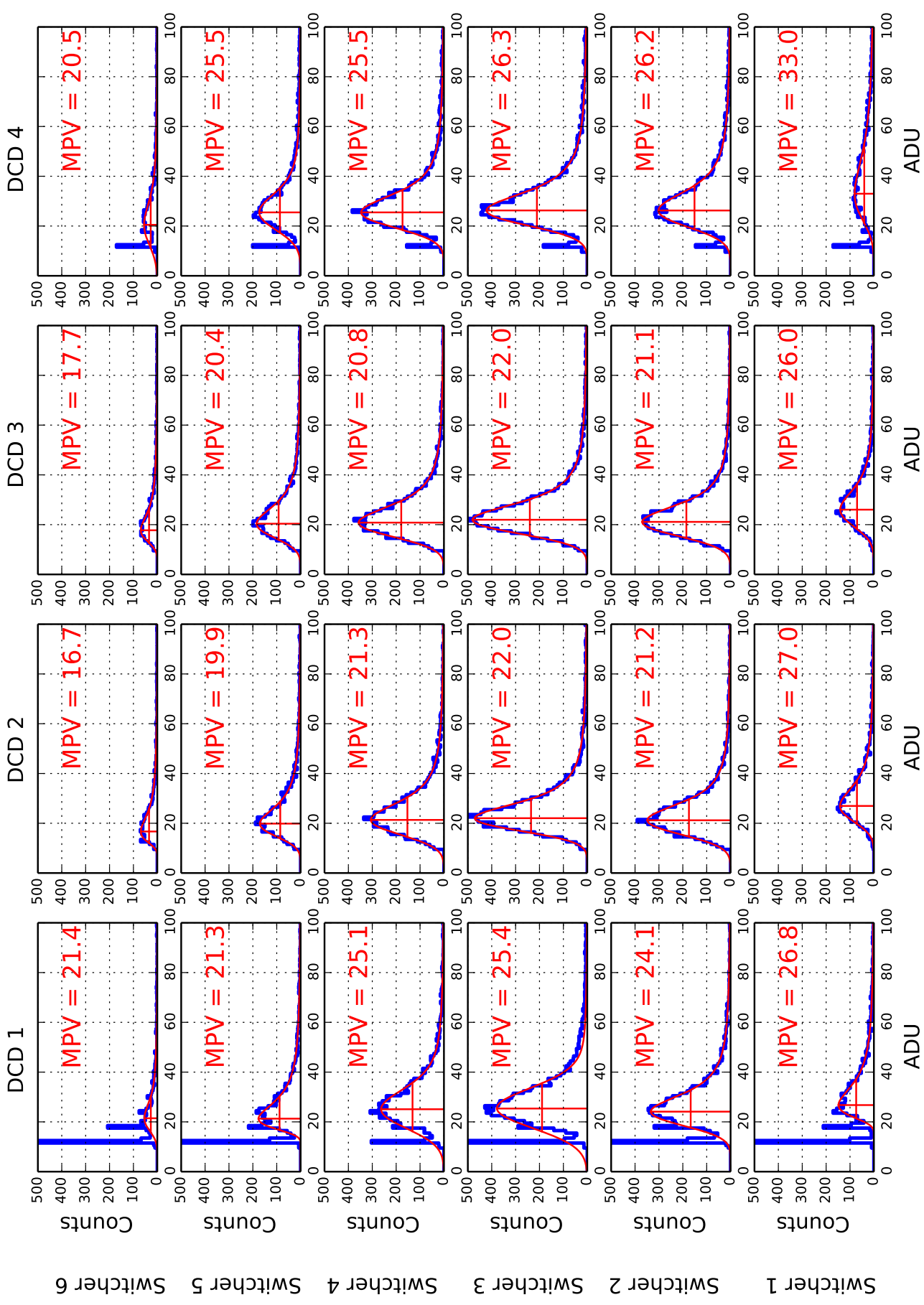


Figure C.19: BASF2, outer backward: Charge distribution, split into 24 regions. Each is controlled and is read out by a different combination of Switcher and DCD.

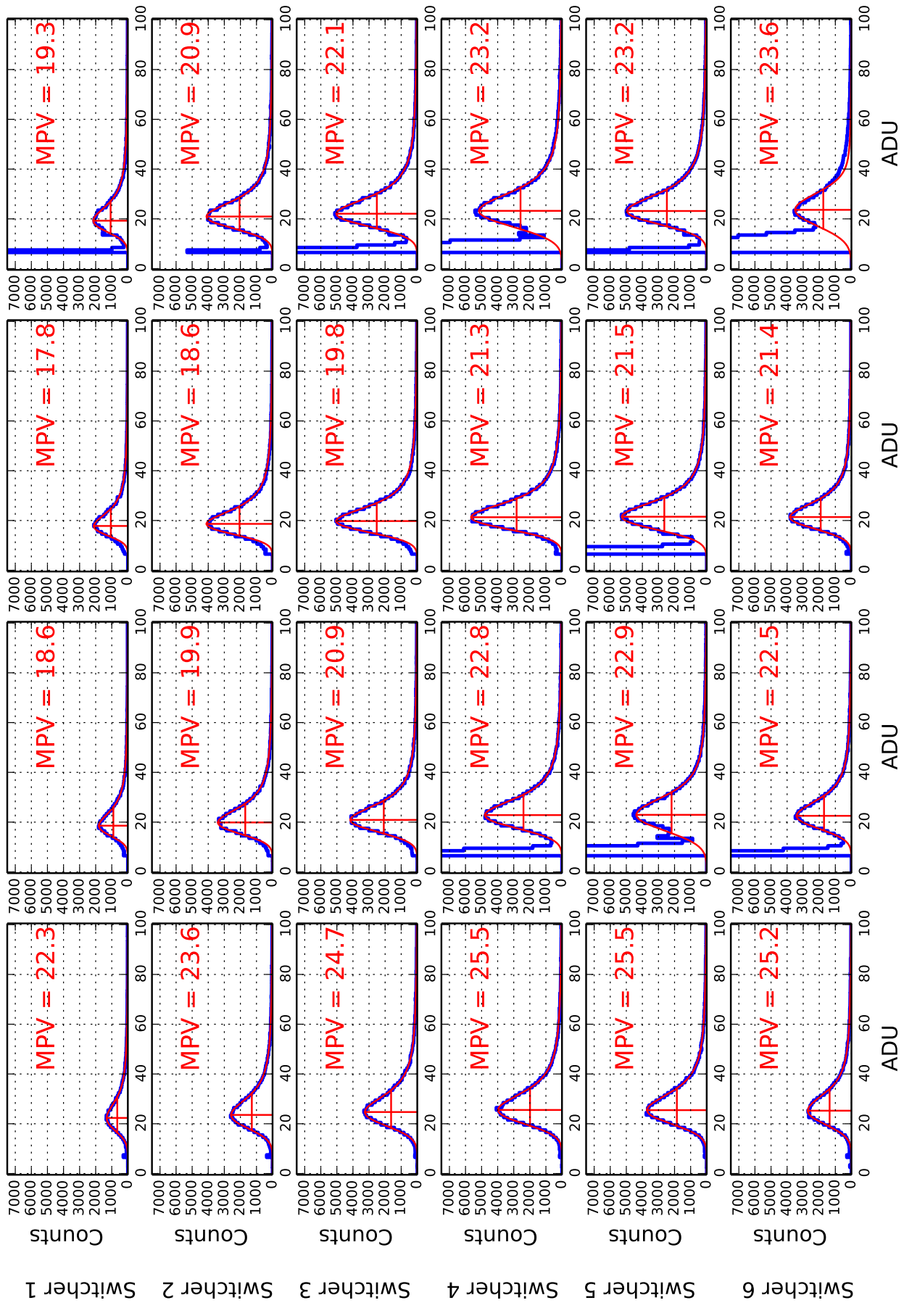


Figure C.20: Lab framework, inner backward: Charge distribution, split into 24 regions. Each is controlled and is read out by a different combination of Switcher and DCD.

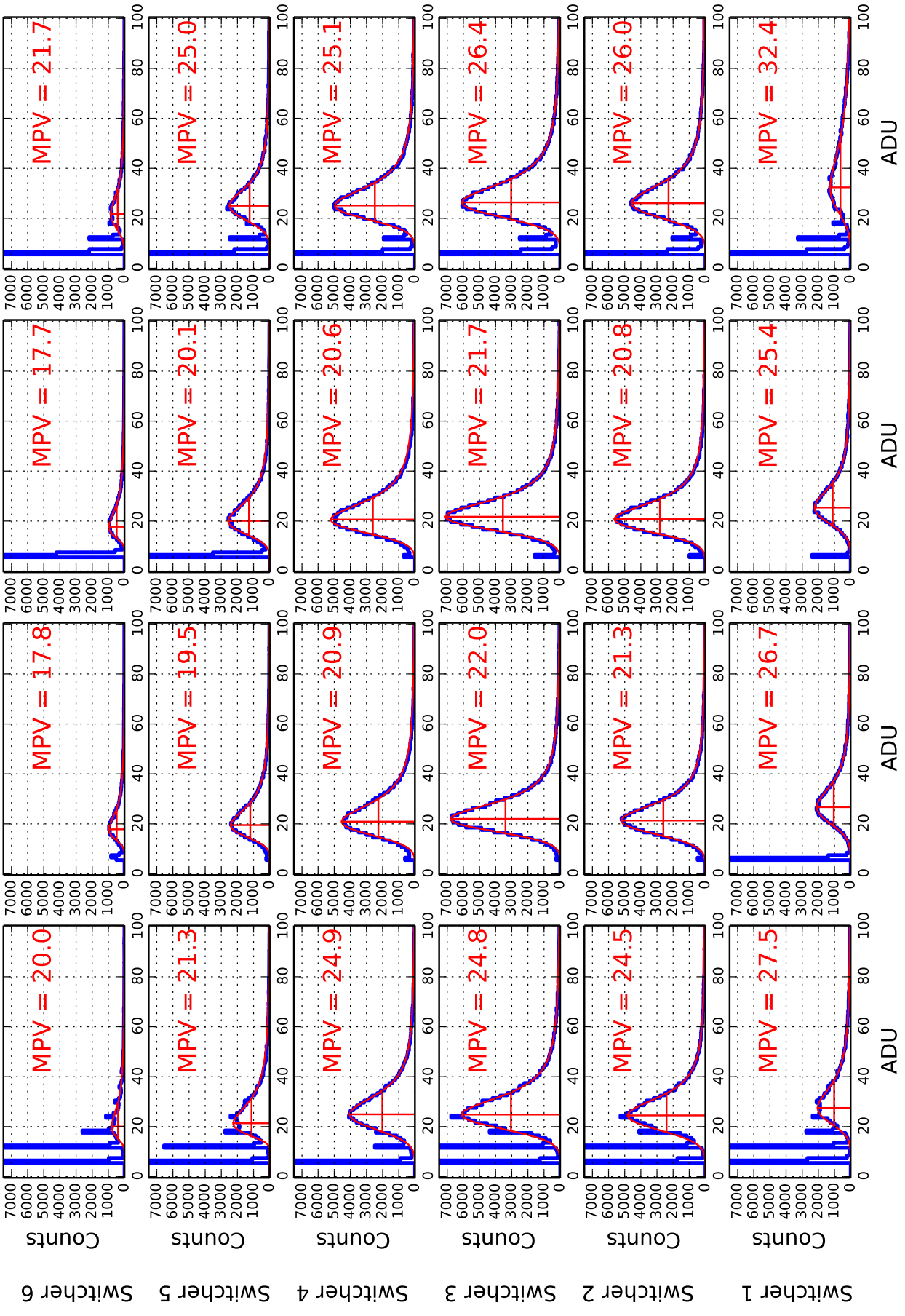


Figure C.21: Lab framework, outer backward: Charge distribution, split into 24 regions. Each is controlled and is read out by a different combination of Switcher and DCD.

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Abbreviations

2PACL 2-phase accumulator controlled loop

ACMC analog common mode correction

ADC analog-to-digital converter

ADU analog-to-digital unit

AMS semiconductor manufacturer, formerly known as Austria Micro Systems

ARES Accelerator Resonantly coupled with Energy Storage

ARICH aerogel ring-imaging cherenkov detector

ASIC application-specific integrated circuit

ATCA advanced telecommunications computing architecture

ATHENA Advanced Telescope for High ENergy Astrophysics

ATLAS a toroidal LHC Apparatus

B2TT Belle II trigger and time distribution system

BaBar B factory

BASF2 Belle Analysis Software Framework 2

BEAST beam exorcisms for a stable belle experiment

Belle Predecessor experiment of Belle II

Belle II Upgrade of the Belle detector

BGO bismuth germanium oxide / bismuth germanate ($Bi_4Ge_3O_{12}$)

BPM beam position monitor

CAD computer-aided design

CAT7 category 7

CC charged current

CCD charge coupled device

CDC central drift chamber

CERN Conseil Européen pour la Recherche Nucléaire

CKM Cabibbo-Kobayashi-Maskawa

CLAWS scintillation light and waveform sensors

CMC common mode correction

CML Current Mode Logic

CMOS complementary metal-oxide-semiconductor

CMS compact muon solenoid

CN computer node

CoG center-of-gravity

CSA charge sensitive amplifier

CsI cesium iodide

CsI(Tl) thallium-doped cesium iodide

DAC digital-to-analog converter

DAQ data acquisition

DATCON data acquisition tracking and concentrator online node

DCD Drain current digitizer

DEPFET DEPleted p-channel Field Effect Transistor

DESY Deutsches Elektronen-Synchrotron

DHC data handling concentrator

DHE data handling engine

DHH data handling hub

DHP data handling processor

DHPT data handling processor from TSMC

DNL differential non-linearity

DPP data patch panel

DR damping ring

DSSD double-sided silicon detector

DUT device under test

ECL electromagnetic calorimeter

EM electromagnetic

EMCM electrical multi-chip module

ENC equivalent noise charge

EOS end-of-stave

EPICS Experimental Physics and Industrial Control System

EUDET Detector-project supported by the European Union

EWT electroweak theory

FANGS FE-I4 ATLAS Near Gamma Sensors

FCNC flavor-changing neutral current

FE-I4 Front-End I4

FPGA field programmable gate array

FTSW front-end timing switch

GCK global reference clock

GD global delay

GEANT4 geometry and tracking

GIM Glashow-Iliopoulos-Maiani

GM Gated Mode

GR general relativity

GUT grand unified theory

HAPD Hybrid Avalanche Photo-Detector

HER high energy ring

HLT high-level trigger

hybrid 5 Prototype for the assembly of 1 Switcher, 1 DCD, 1 DHP and one small (32×64 pixel) matrix.

IB inner backward

IF inner forward

INL integral non-linearity

IR interaction region

I-V current-voltage

JCP junk charge prevention

JTAG Joint Test Action Group

KEKB KEK B factory

KLM detector to identify K_L^0 and muons

laser light amplification by stimulated emission of radiation

LD local delay

LER low energy ring

LHC large hadron collider

LHCb large hadron collider beauty

PS power supply

LSB least significant bit

LVDS low-voltage differential signaling

LySo cerium-doped lutetium yttrium orthosilicate

MAPS monolithic active pixel sensor

MC Monte Carlo

MicroTCA micro telecommunications computing architecture

MIMOSA minimum ionizing particle metal oxide semiconductor active pixel sensor

MIP minimum ionizing particle

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

MPV most probable value

NIM nuclear instrumentation module

NP New Physics

OB outer backward

OF outer forward

ONSEN online selection node

PBB power breakout board

PCB printed circuit board

PEP-II Positron-Electron Project IIs

PERSY permanent setup at DESY

PID particle identification

PIN positive intrinsic negative

PLL phase-locked loop

PLUME pixelated ladder with ultra-low material embedding

PP patch panel

PPP power patch panel

PXD pixel detector

PXD5 prototype production of DEPFET sensor, 450 µm thick

PXD6 prototype production of DEPFET sensor, 50 µm thick

PXD9 final Belle II sensor layout, 75 µm thick

QCD quantum chromodynamics

QCS superconducting final focus quadruple magnet system

QED quantum electrodynamics

QFD quantum flavordynamics

RAM random-access memory

RMS root mean square

ROI region of interest

RPC resistive plate chamber

SCC Single-Cell superconducting Cavities

SCP signal charge preservation

SiPM silicon photomultiplier

SLAC National Accelerator Laboratory

SM Standard Model

SMD surface-mount device

SMU Source Measure Unit

SNR signal-to-noise ratio

SOI silicon on insulator

SR synchrotron radiation

SSB spontaneous symmetry breaking

SuperKEKB Super KEK B factory, the upgrade of KEKB

SVD silicon vertex detector

TLU trigger logic unit

TOP time of propagation

TPC time projection chamber

TSMC Taiwan Semiconductor Manufacturing Company

TTL transistor-transistor logic

UDP User Datagram Protocol

UMC United Microelectronics Corporation

VXD vertex detector

WLS wave-length shifting

WMAP Wilkinson Microwave Anisotropy Probe

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